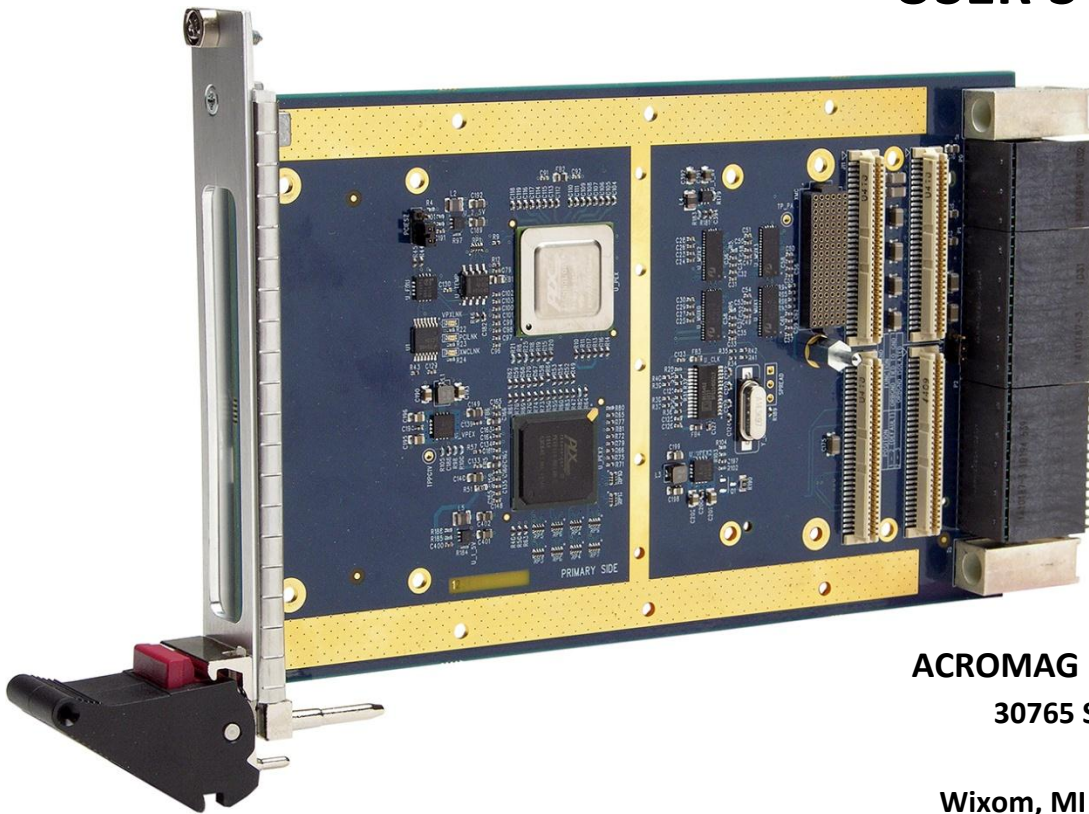




VPX4810 / VPX4810CC / VPX4810REDI

VPX PCIe PMC/XMC 3U Carrier

USER'S MANUAL



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You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

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GENERAL INFORMATION

The VPX4810 series is a 3U VPX Non-Intelligent XMC/PMC carrier board designed for 4x/8x PCIe bus connection. The carrier card uses a PLX Technology® PCIe Switch Chip (PEX 8624) and PLX Technology® PCIe to PCI Bridge Chip (PEX 8114) to interface between the VPX bus and one XMC/PMC mezzanine I/O module card.

Model VPX4810 is an air-cooled product which can be used for front and rear I/O XMC/PMC mezzanine I/O modules.

Model VPX4810CC is an extended temperature conduction-cooled product which supports all Acromag FPGA modules. It only supports Rear I/O.

Model VPX4810REDI is a VITA 48 Ruggedized Enhanced Design Implementation (REDI) model that does not support Front I/O and will only fit in REDI chassis.

The following hardware kits are required when ordering the VPX4810 series for

Key Features

- **PCIe x4 or x8 lane VITA 46.4 Backplane Compliance:** The VPX4810 supports either a 4 or 8 lane PCIe 2.0 connection to the backplane. Lane selection is jumper selectable.
- **Supports either 1 PMC or XMC module** – The VPX4810 supports 1 PMC module compliant to PCI 3.0 -- 32 or 64 bits at 33 or 66MHz or PCI-X 1.0b 64 bits at 66MHz, 100MHz, or 133MHz. Alternatively it supports one XMC module compliant with PCI Express 2.0 up to 8 lanes.
- **ESD Strip** - The VPX4810 board has been designed to provide electrostatic discharge (ESD) capability by using an ESD strip on the board.
- **Injector/Ejector Handle** - The VPX4810 uses a modern injector/ejector handle, which pushes the board into the rack during installation and has a positive self-locking mechanism so it cannot be unlocked accidentally. This handle is fully IEEE 1101.10 compliant and is needed to give leverage to install and remove the board.
- **EMC Front Panel** - The VPX4810 uses the preferred EMC front panel per IEEE 1101.10 specification.
- **Conduction Cooled Frame** - The VPX4810CC board has a custom conduction cooled assembly consisting of a conduction cooled frame, thermo bars, ejector/injectors and wedge-locks designed to thermally conduct heat away from the Conduction Cooled XMC/PMC modules.
- **REDI Frame** - The VPX4810REDI board has a custom conduction cooled and full shield assembly compliant to VITA 48.0. The assembly consists of a conduction cooled frame, thermo bars, ejector/injectors, wedge-locks, and a full bottom and top face plate designed to thermally conduct heat from and to protect from ESD the XMC/PMC modules.
- **Compatible with OPEN VPX VITA 65.0**

Software Support

The VPX4810 family of modules is intended to be used as a non-intelligent bridge between the system PCIe bus and the XMC/PMC module. No software is required to operate the board. However all XMC/PMC modules will require support drivers specific to your operating system. Refer to your XMC/PMC modules manufacturer for information on PCIe drivers.

References

The following two whitepapers related to VPX are available for download on Acromag's website or by contacting your sales representative.

Introduction to VPX: VITA 46, 48, and 65.

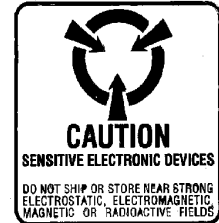
Will Acromag's VPX4810 work in my system?

PREPARATION FOR USE

Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped. **WARNING:** *This board utilizes static sensitive components and should only be handled at a static-safe workstation.*



This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

Card Cage Considerations

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

Each of Acromag's VPX carriers are in a different pitch as determined by the cooling technique. The VPX4180 is a 0.8" pitch board, the VPX4810CC is 0.85" pitch, and the VPX4810REDI is a 1.00" pitch board. Verify your chassis compliance to accommodate the various board pitches.

In an air cooled assembly, adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

IMPORTANT: *Adequate air circulation of 100 LFM. must be provided to prevent a temperature rise above the maximum operating temperature in the VPX4810.*

In a conduction cooled assembly, adequate thermo conduction must be provided to prevent a temperature rise above the maximum operating temperature.

IMPORTANT: *If the VPX4810CC is not installed in a conduction cooled chassis, air circulation of 200 LFM must be provided to prevent a temperature rise above the maximum operating temperature in the VPX4810CC.*

A REDI assembly must be installed in a REDI complaint chassis since conduction is the only method for cooling the board.

IMPORTANT: *The VPX4810REDI should not be operated under air cooled conditions.*

Backplane

This board is design to work with a Backplane profile of BKP3-DIS06-15.2.7-n. Failure to use a compatible backplane could result in damage to this product or others in the chassis. For more information on backplane compatible please refer to the Acromag VPX4810 Compatibility Whitepaper.

WARNING: THE VPX4810 CAN ONLY BE USED ON A 3U BACKPLANE. PLUGGING THIS MODULE INTO A 6U BACKPLANE WILL RESULT IN DAMAGE TO THIS BOARD DUE INCOMPATIBLE POWER SUPPLIES.

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the VPX bus and PMC module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

The model VPX4810 carrier field I/O connections are made through the rear via J4 for a single PMC mezzanine I/O module card.

Jumper Settings

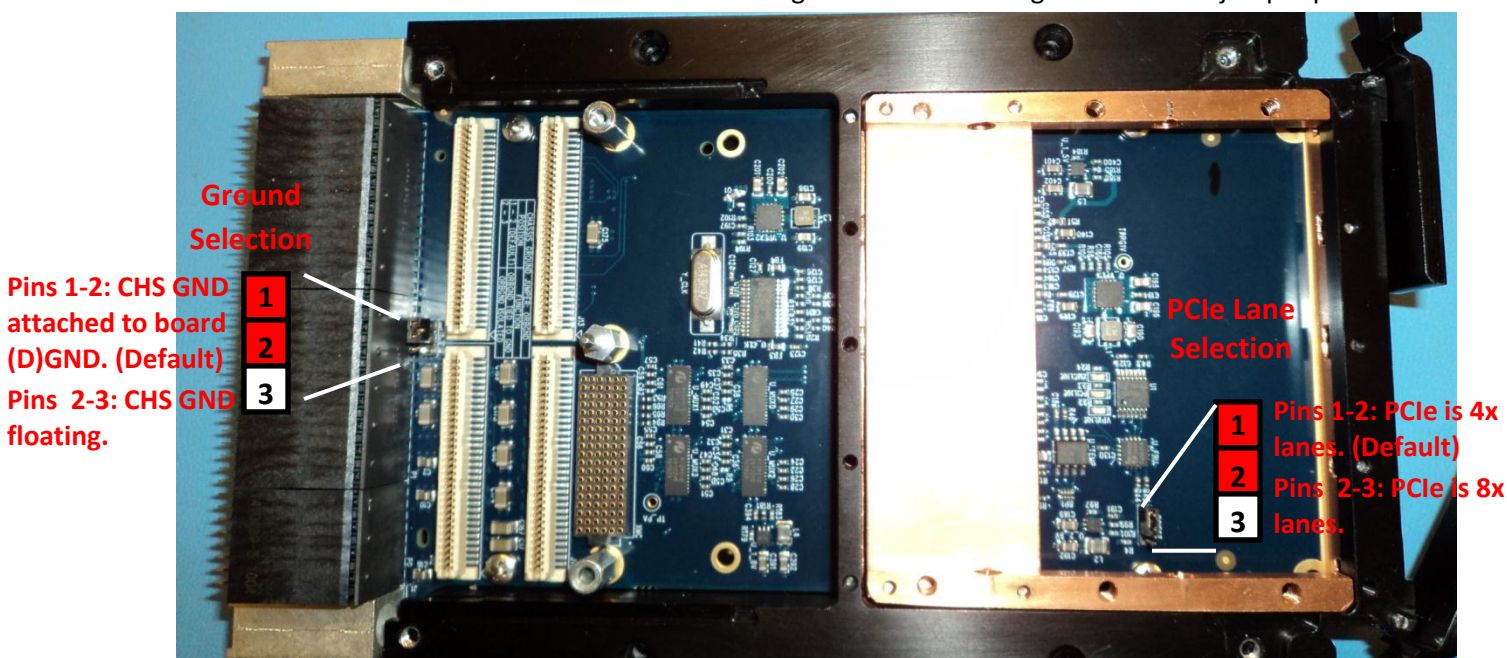
The VPX4810 has two jumpers for selecting the number of PCIe lanes used from the backplane and another to control how the chassis ground is connected. Note that the jumpers are in the same location on each model regardless of metalwork.

PCIe Lane Selection

This jumper sets the VPX4810 to use either the first 4 lanes (fat pipe) or the first 8 lanes (double fat pipe) from the backplane. Users should take care that these lanes are routed directory to the host card and are not shared by another other module. The default selection is 4 lanes. Refer to diagram below for jumper position.

Ground Selection

This jumper allows the user to attach the board metalwork (chassis ground) to either the DC ground or let remain isolated. The default selection is to attach it to ground. Refer to diagram below for jumper position.



PMC Connector Pinout

The following tables list all the board connections to the 4 PMC connectors J1 to J4.

PMC Site Connector J1

This connector contains PCI bus signals and power for PMC modules.

PIN	Signal	PIN	Signal
1	TCK	2	-12V
3	Ground	4	INTA*
5	INTB*	6	INTC*
7	BUSMODE1*	8	+5V
9	INTD*	10	PCI-RSVD*
11	Ground	12	PCI-RSVD*
13	CLK	14	Ground
15	Ground	16	GNT*
17	REQ*	18	+5V
19	V(I/O)	20	AD(31)
21	AD(28)	22	AD(27)
23	AD(25)	24	Ground
25	Ground	26	C/BE(3)*
27	AD(22)	28	AD(21)
29	AD(19)	30	+5V
31	V(I/O)	32	AD(17)
33	FRAME*	34	Ground
35	Ground	36	IRDY*
37	DEVSEL*	38	+5V
39	Ground	40	LOCK*
41	SDONE*	42	SBO*
43	PAR	44	Ground
45	V(I/O)	46	AD(15)
47	AD(12)	48	AD(11)
49	AD(09)	50	+5V
51	Ground	52	C/BE(0)*
53	AD(06)	54	AD(05)
55	AD(04)	56	Ground
57	V(I/O)	58	AD(03)
59	AD(02)	60	AD(01)
61	AD(00)	62	+5V
63	Ground	64	REQ64*

* Indicates that the signal is active low.

PMC Site Connector J2

This connector contains PCI bus signals and power for PMC modules.

PIN	Signal	PIN	Signal
1	+12V	2	TRST*
3	TMS	4	TDO
5	TDI	6	Ground
7	Ground	8	PCI-RSVD*
9	PCI-RSVD*	10	PCI-RSVD*
11	BUSMODE2*	12	+3.3V
13	RST*	14	BUSMODE3*
15	+3.3V	16	BUSMODE4*
17	PCI-RSVD*	18	Ground
19	AD(30)	20	AD(29)
21	Ground	22	AD(26)
23	AD(24)	24	+3.3V
25	IDSEL	26	AD(23)
27	+3.3V	28	AD(20)
29	AD(18)	30	Ground
31	AD(16)	32	C/BE(2)*
33	Ground	34	PMC-RSVD
35	TRDY*	36	+3.3V
37	Ground	38	STOP*
39	PERR*	40	Ground
41	+3.3V	42	SERR*
43	C/BE(1)*	44	Ground
45	AD(14)	46	AD(13)
47	M66EN	48	AD(10)
49	AD(08)	50	+3.3V
51	AD(07)	52	PMC-RSVD
53	+3.3V	54	PMC-RSVD
55	PMC-RSVD	56	Ground
57	PMC-RSVD	58	PMC-RSVD
59	Ground	60	PMC-RSVD
61	ACK64*	62	+3.3V
63	Ground	64	PMC-RSVD

* Indicates that the signal is active low.

PMC Site Connector J3

This connector contains the additional PCI bus signals required for 64-bit transactions.

PIN	Signal	PIN	Signal
1	PCI-RSVD	2	Ground
3	Ground	4	C/BE(7)*
5	C/BE(6)*	6	C/BE(5)*
7	C/BE(4)*	8	Ground
9	V(I/O)	10	PAR64
11	AD(63)	12	AD(62)
13	AD(61)	14	Ground
15	Ground	16	AD(60)
17	AD(59)	18	AD(58)
19	AD(57)	20	Ground
21	V(I/O)	22	AD(56)
23	AD(55)	24	AD(54)
25	AD(53)	26	Ground
27	Ground	28	AD(52)
29	AD(51)	30	AD(50)
31	AD(49)	32	Ground
33	Ground	34	AD(48)
35	AD(47)	36	AD(46)
37	AD(45)	38	Ground
39	V(I/O)	40	AD(44)
41	AD(43)	42	AD(42)
43	AD(41)	44	Ground
45	Ground	46	AD(40)
47	AD(39)	48	AD(38)
49	AD(37)	50	Ground
51	Ground	52	AD(36)
53	AD(35)	54	AD(34)
55	AD(33)	56	Ground
57	V(I/O)	58	AD(32)
59	PCI-RSVD	60	PCI_RSVD
61	PCI-RSVD	62	Ground
63	Ground	64	PCI-

* Indicates that the signal is active low.

PMC Site Connector J4

This connector contains the PMC Rear I/O Signals. These signals are routed to the VPX backplane.

PIN	Signal	PIN	Signal
1	Rear Jn4-1/P2-E1	2	Rear Jn4-2/P2-B1
3	Rear Jn4-3/P2-D1	4	Rear Jn4-4/P2-A1
5	Rear Jn4-5/P2-F2	6	Rear Jn4-6/P2-C2
7	Rear Jn4-7/P2-E2	8	Rear Jn4-8/P2-B2
9	Rear Jn4-9/P2-E3	10	Rear Jn4-10/P2-B3
11	Rear Jn4-11/P2-D3	12	Rear Jn4-12/P2-A3
13	Rear Jn4-13/P2-F4	14	Rear Jn4-14/P2-C4
15	Rear Jn4-15/P2-E4	16	Rear Jn4-16/P2-B4
17	Rear Jn4-17/P2-E5	18	Rear Jn4-18/P2-B5
19	Rear Jn4-19/P2-D5	20	Rear Jn4-20/P2-A5
21	Rear Jn4-21/P2-F6	22	Rear Jn4-22/P2-C6
23	Rear Jn4-23/P2-E6	24	Rear Jn4-24/P2-B6
25	Rear Jn4-25/P2-E7	26	Rear Jn4-26/P2-B7
27	Rear Jn4-27/P2-D7	28	Rear Jn4-28/P2-A7
29	Rear Jn4-29/P2-F8	30	Rear Jn4-30/P2-C8
31	Rear Jn4-31/P2-E8	32	Rear Jn4-32/P2-B8
33	Rear Jn4-33/P2-E9	34	Rear Jn4-34/P2-B9
35	Rear Jn4-35/P2-D9	36	Rear Jn4-36/P2-A9
37	Rear Jn4-37/P2-F10	38	Rear Jn4-38/P2-C10
39	Rear Jn4-39/P2-E10	40	Rear Jn4-40/P2-B10
41	Rear Jn4-41/P2-E11	42	Rear Jn4-42/P2-B11
43	Rear Jn4-43/P2-D11	44	Rear Jn4-44/P2-A11
45	Rear Jn4-45/P2-F12	46	Rear Jn4-46/P2-C12
47	Rear Jn4-47/P2-E12	48	Rear Jn4-48/P2-B12
49	Rear Jn4-49/P2-E13	50	Rear Jn4-50/P2-B13
51	Rear Jn4-51/P2-D13	52	Rear Jn4-52/P2-A13
53	Rear Jn4-53/P2-F14	54	Rear Jn4-54/P2-C14
55	Rear Jn4-55/P2-E14	56	Rear Jn4-56/P2-B14
57	Rear Jn4-57/P2-E15	58	Rear Jn4-58/P2-B15
59	Rear Jn4-59/P2-D15	60	Rear Jn4-60/P2-A15
61	Rear Jn4-61/P2-F16	62	Rear Jn4-62/P2-C16
63	Rear Jn4-63/P2-E16	64	Rear Jn4-64/P2-B16

XMC Connector Pinout

XMC Connector P5

This connector contains eight PCIe lanes as well as all XMC power and control signals. Note that VPRW is 5V on the VPX4810 carrier. The carrier does not support processor XMC modules (PCI enumeration capabilities).

Pin	A	B	C	D	E	F
1	PCIeT0p	PCIeT0n	+3.3V	PCIeT1p	PCIeT1n	+5.0V
2	GND	GND	TRST#	GND	GND	
3	PCIeT2p	PCIeT2n	+3.3V	PCIeT3p	PCIeT3n	+5.0V
4	GND	GND	TCK	GND	GND	
5	PCIeT4p	PCIeT4n	+3.3V	PCIeT5p	PCIeT5n	+5.0V
6	GND	GND	TMS	GND	GND	+12.0V
7	PCIeT6p	PCIeT6n	+3.3V	PCIeT7p	PCIeT7n	+5.0V
8	GND	GND	TDI	GND	GND	-12.0V
9	RFU	RFU	RFU	RFU	RFU	+5.0V
10	GND	GND	TDO	GND	GND	GA0
11	PCIeR0p	PCIeR0n	MBIST#	PCIeR1p	PCIeR1n	+5.0V
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PCIeR2p	PCIeR2n	+3.3V AUX	PCIeR3p	PCIeR3n	+5.0V
14	GND	GND	GA2	GND	GND	MSDA
15	PCIeR4p	PCIeR4n	RFU	PCIeR5p	PCIeR5n	+5.0V
16	GND	GND	MVMRO	GND	GND	MSCL
17	PCIeR6p	PCIeR6n	RFU	PCIeR7p	PCIeR7n	RFU
18	GND	GND	RFU	GND	GND	RFU
19	REFCLK+	REFCLK-	RFU	Wake#	Root#	RFU

VPX Backplane Connector Pinouts

VPX P0 Connector-Power and System Controls

Table 2.2 indicates the pin assignments for the VPX 3U assignments at the P0 connector. The connector consists of 8 wafers with up to 7 signals on each. The system management bus signals SM0, SM1, SM2, and SM3 use I²C to implement the Intelligent Platform Management Bus (IPMB) per VITA 46.11. **The VPX4610 CAN NOT BE PLUGGED INTO A 6U VPX SYSTEM DUE TO POWER INCOMPATIBILITIES BETWEEN THE 3U AND 6U FORM FACTORS. PLUGGING THE VPX4610 INTO A 6U SYSTEM WILL DAMAGE THE BOARD!**

Refer to the VPX specifications for additional information on these signals.

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	+12V	+12V	+12V		+3.3V	+3.3V	+3.3V
2	+12V	+12V	+12V		+3.3V	+3.3V	+3.3V
3	+5V	+5V	+5V		+5V	+5V	+5V
4	SM2	SM3	GND	12V_AUX	GND	SYSRST	NVMRO
5	GAP	GA4	GND	3.3V_AUX	GND	SM0	SM1
6	GA3	GA2	GND	+12V_AU	GND	GA1	GA0
7	TCK	GND	TDO	TDI	GND	TMS	TRST
8	GND	REF_CLK-	REF_CLK+	GND	RES	RES	GND

Note: **BOLD ITALIC** signals are NOT USED by this carrier board.

VPX P1 Connector – PCIe

The VPX 3U P1 connector contains the high speed PCIe signals. The VPX4610 is compliant to VITA 46.4 with up to 8 lanes and PCIe. The board is jumper selectable to select either the bottom 4 lanes (L0-L3) or the full eight lanes (L0-L7). When only the bottom 4 lanes are used the upper four are fully discounted from the backplane via a switch so they will not interfere with any other cards using those signals on the backplane.

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	RES	GND	L0-TX-	L0-TX+	GND	L0-RX-	L0-RX+
2	GND	L1-TX-	L1-TX+	GND	L1-RX-	L1-RX+	GND
3	VBAT	GND	L2-TX-	L2-TX+	GND	L2-RX-	L2-RX+
4	GND	L3-TX-	L3-TX+	GND	L3-RX-	L3-RX+	GND
5	SYS_CON	GND	L4-TX-	L4-TX+	GND	L4-RX-	L4-RX+
6	GND	L5-TX-	L5-TX+	GND	L5-RX-	L5-RX+	GND
7	REG_CLK_SE	GND	L6-TX-	L6-TX+	GND	L6-RX-	L6-RX+
8	GND	L7-TX-	L7-TX+	GND	L7-RX-	L7-RX+	GND
9	P1-SE4	GND	L8-TX-	L8-TX+	GND	L8-RX-	L8-RX+
10	GND	L9-TX-	L9-TX+	GND	L9-RX-	L9-RX+	GND
11	P1-SE5	GND	L10-TX-	L10-TX+	GND	L10-RX-	L10-RX+

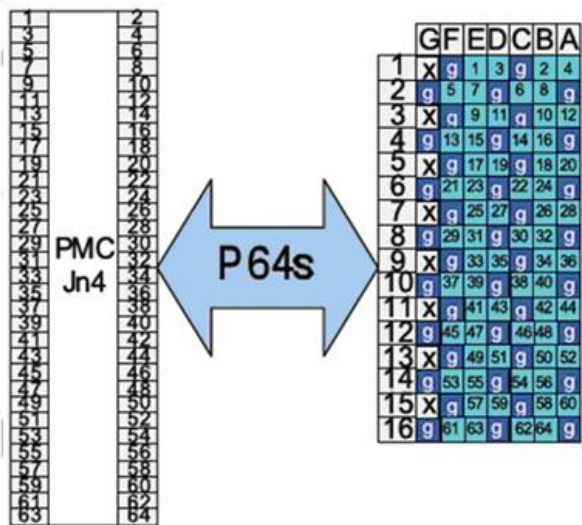
Note: **BOLD ITALIC** signals are NOT USED by this carrier board.

VPX P2 Connector –Rear I/O

The VPX P2 connector contains all of the Rear I/O routing from the PMC J4 connector. This connector consists of 16 differential wafers with 7 signals each. This pin out is compliant with VITA 46.9 P2w1-P64s. Note that the backplane connected to the VPX4610 should be VITA 46.9 P2w1-P64s compliant to avoid any possible signal contentions.

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	NC	GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4
2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND
3	NC	GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12
4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND
5	NC	GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20
6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND
7	NC	GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28
8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND
9	NC	GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36
10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND
11	NC	GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44
12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND
13	NC	GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52
14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND
15	NC	GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60
16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND

Note: **BOLD ITALIC** signals are NOT USED by this carrier board.



Rear I/O pin mapping diagram as defined in VITA 46.9. This product is complaint to rear I/O routing P2w1-P64s.

Installing and Removing PMC/XMC Modules

The procedure for installing and XMC/PMC module into the VPX4810 series carrier varies depending on the carrier type.

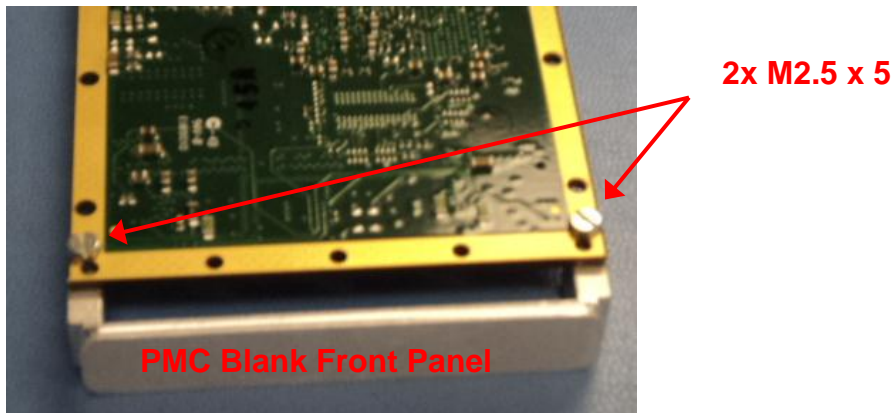
Please note that if you purchase the VPX4810 and one of Acromag's PMC or XMC modules separately you may require one of the following additional hardware kits to complete mounting.

AXM-KIT: This kit contains a blank front panel and 4 screws. It is required for proper installation of any Acromag Virtex 4, Virtex 5, or Spartan 6 board *without an AXM module attached* in an air cooled carrier.

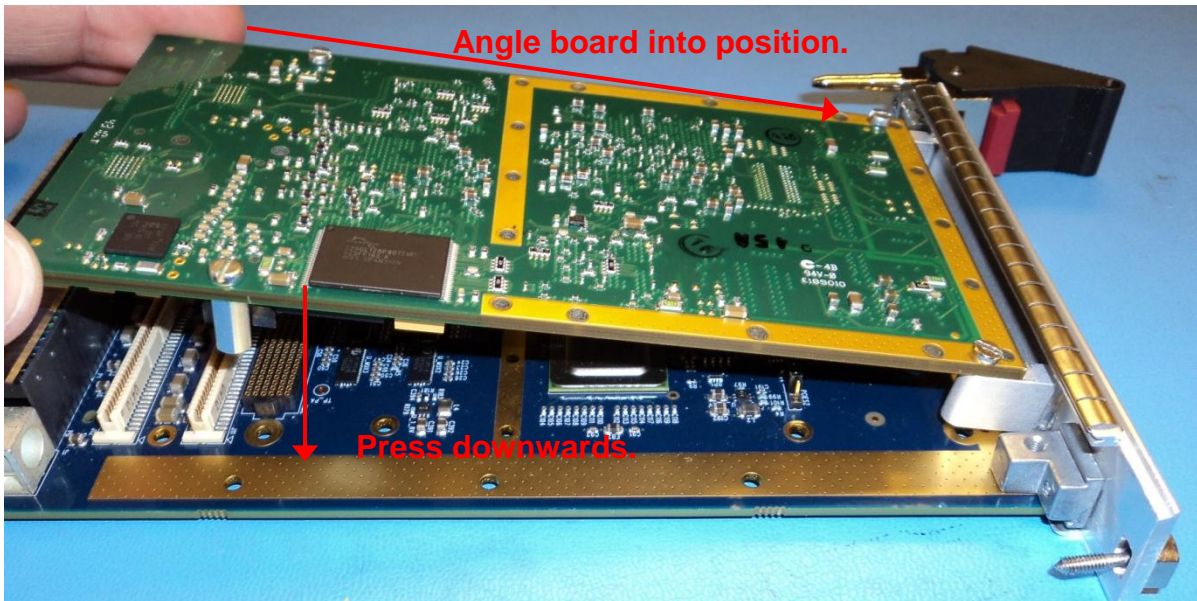
PMC-KIT-CC: This kit contains the necessary screws to attach an Acromag PMC/XMC module to the VPX4810CC or the VPX4810REDI.

VPX4810 Air-Cooled

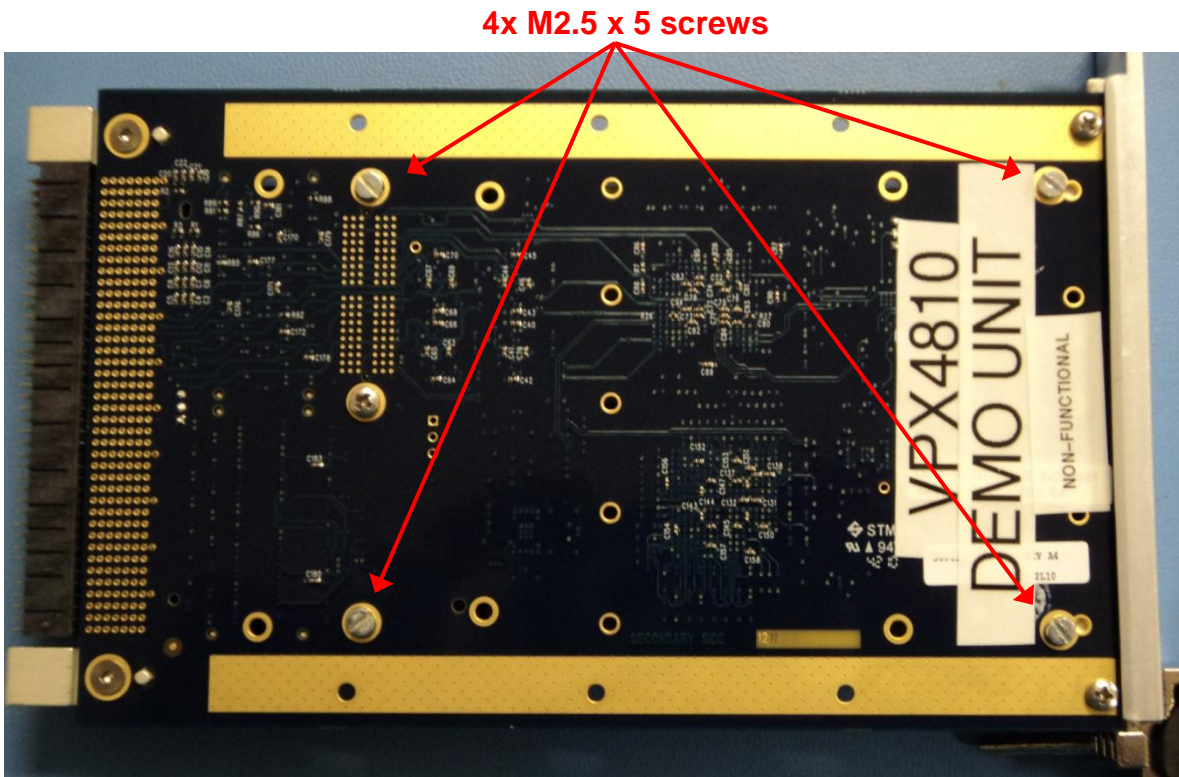
Step 1: Take your XMC/PMC module and verify that it has a front panel attached and properly screwed into the XMC/PMC module. If not then install a blank front panel that is available in the AXM- KIT. Set the jumpers on the VPX 4810 now.



Step 2: Install the PMC/XMC module into the VPX4810 carrier by carefully angling the board so that the front panel slips through the gap in the metalwork. Once set align the connectors and gently push down until the connectors are fully inserted.



Step 3: Flip the VPX4810 over and install 4x M2.5 x 5 screws into the locations noted in the picture below. These correspond to the standoffs and the front PMC panel on the attached module.

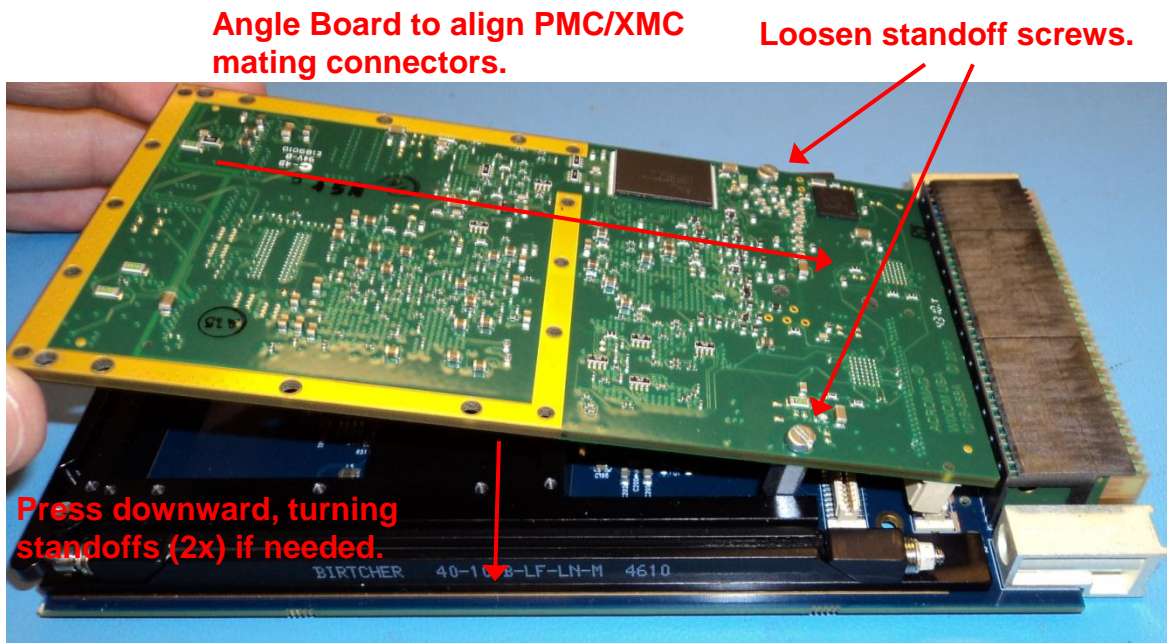


VPX4810CC Conduction Cooled

Step 1: Take your XMC/PMC module and verify that it has the front panel has been removed. Note that you will need the PMC-KIT-CC to complete mounting. Set the jumpers now.

Step 2: Loosen the two screws on the standoff of the PMC/XMC module by about 1 turn. This will allow you to easily move the position of the hex standoffs.

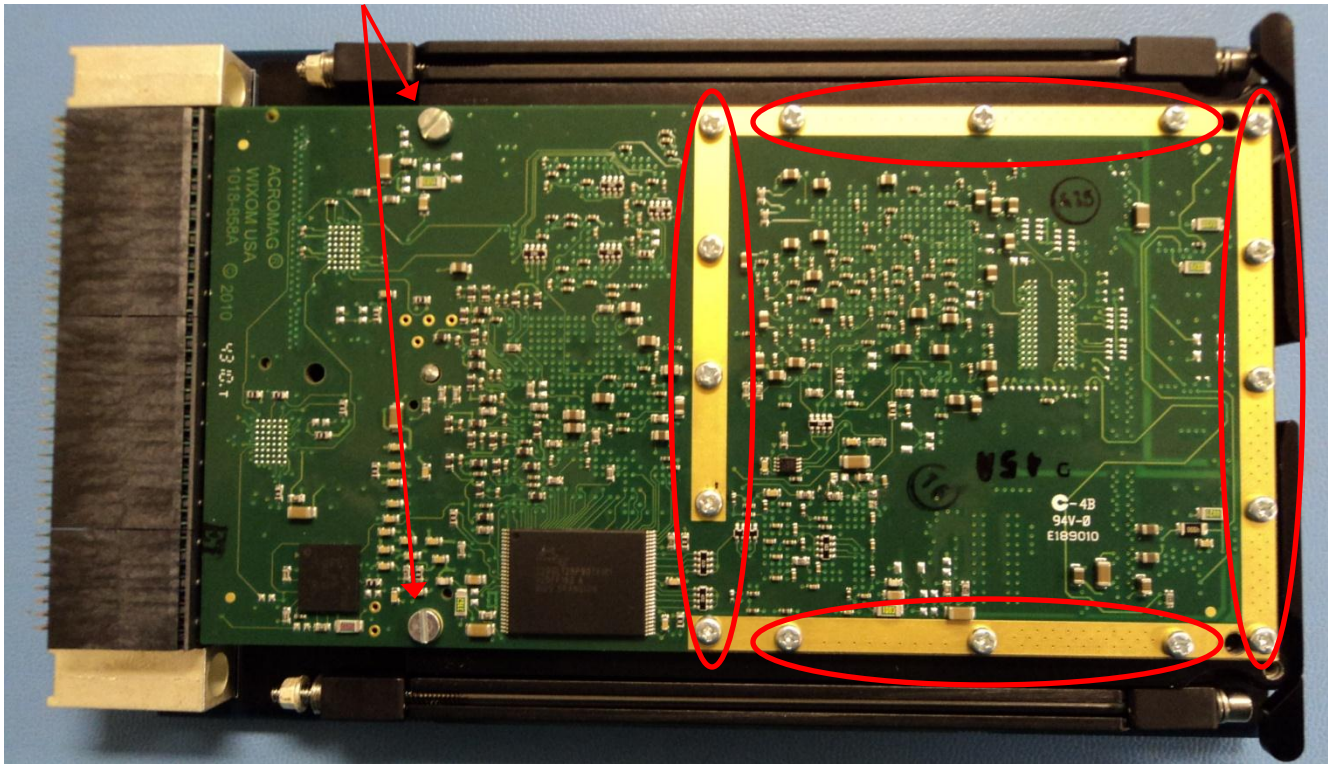
Step 3 Install the PMC/XMC module into the VPX4810CC carrier by carefully angling the board so that the board to board connectors align and then pressing downward. If the hex standoffs prevent the insertion of the board, rotate them slightly until the module will fit.



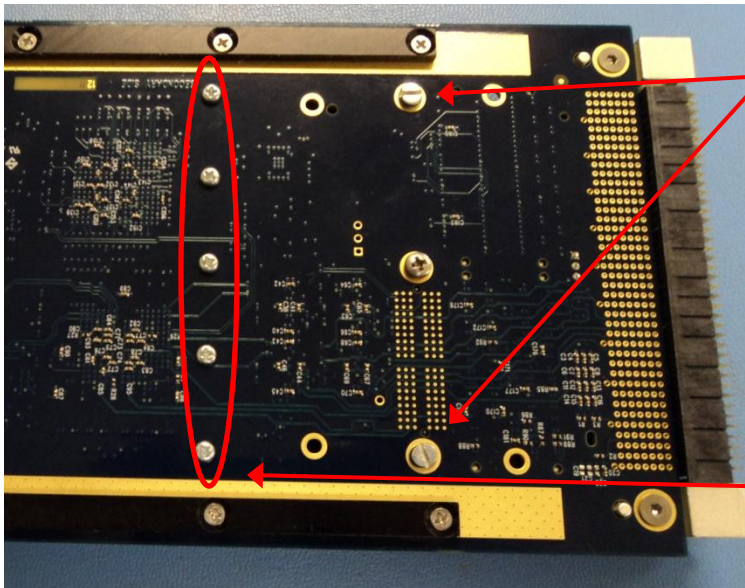
Step 4: Install the 16x M2 x 6 screws on this side of the board and tighten the 2 standoff screws.

Tighten standoff screws

Install 16x M2 x 6 screws



Step 5: Flip the VPX4810CC over and install 2x M2.5 x 5 screws for the standoffs into the locations noted in the picture below. Optionally users can install another 10x M2 x 6 screws into the bottom to further secure the VPX carrier to the metalwork.



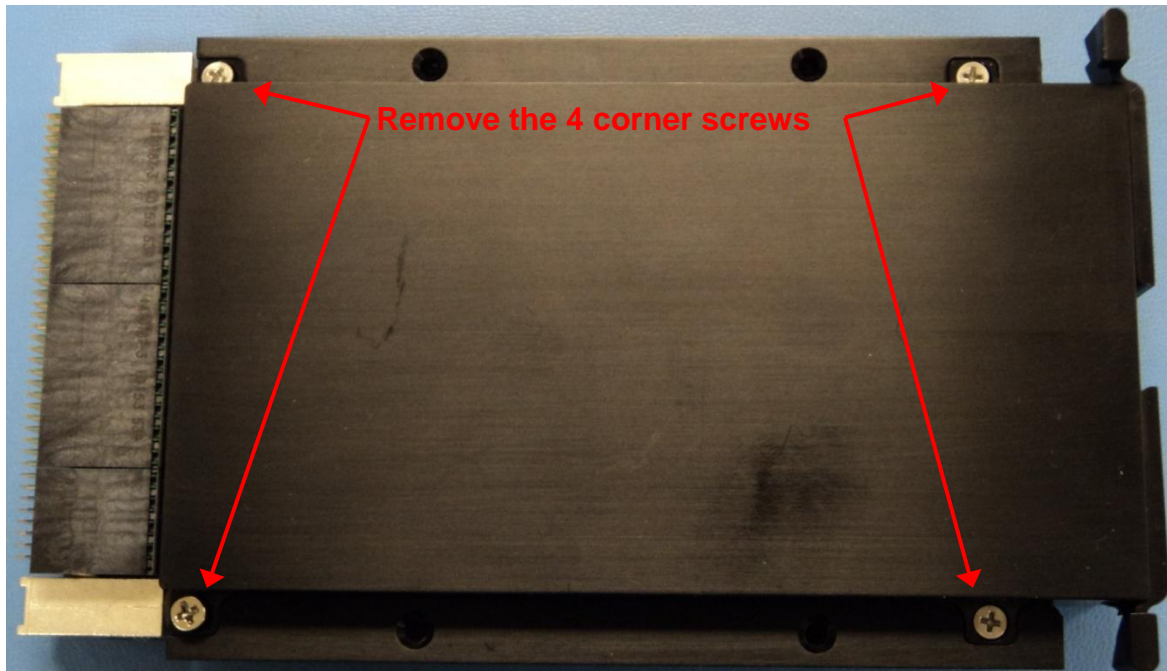
Install 2x M2.5 x 5 screws

**Optional 10x M2 x 6 screws.
Note that only five are shown.**

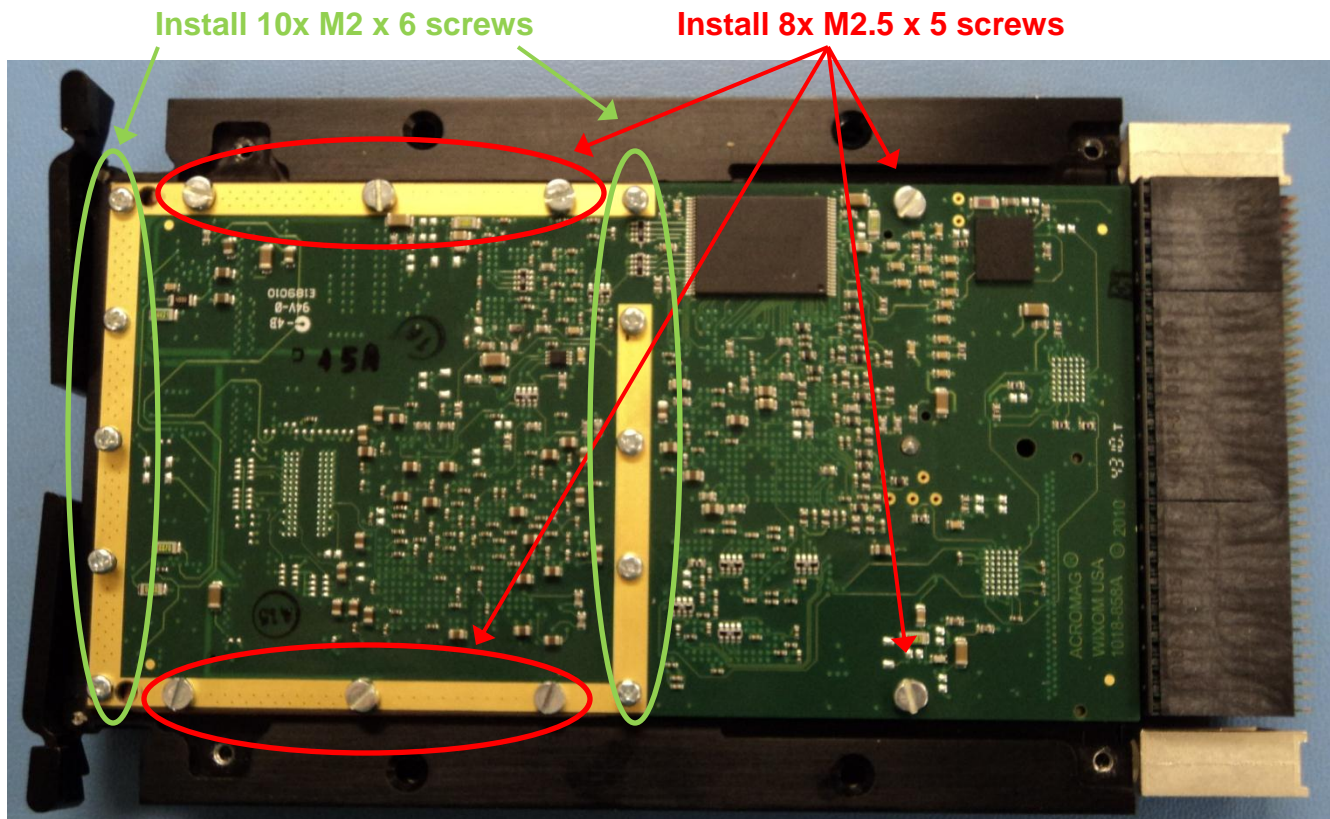
VPX4810REDI VITA 48

Step 1: Take your XMC/PMC module and verify that it has the front panel **and standoffs** have been removed. The standoffs are pre-installed on the VPX4810REDI. Note that you will need the PMC-KIT-CC to complete mounting.

Step 2: Remove the top cover by removing the 4 corner screws. Then, if necessary, change the jumper settings.



Step 3: Insert the PMC/XMC module and press down firmly. Then install 8x M2.5 x 5 screws and 10x M2.0 x 6 screws as shown in the picture below.

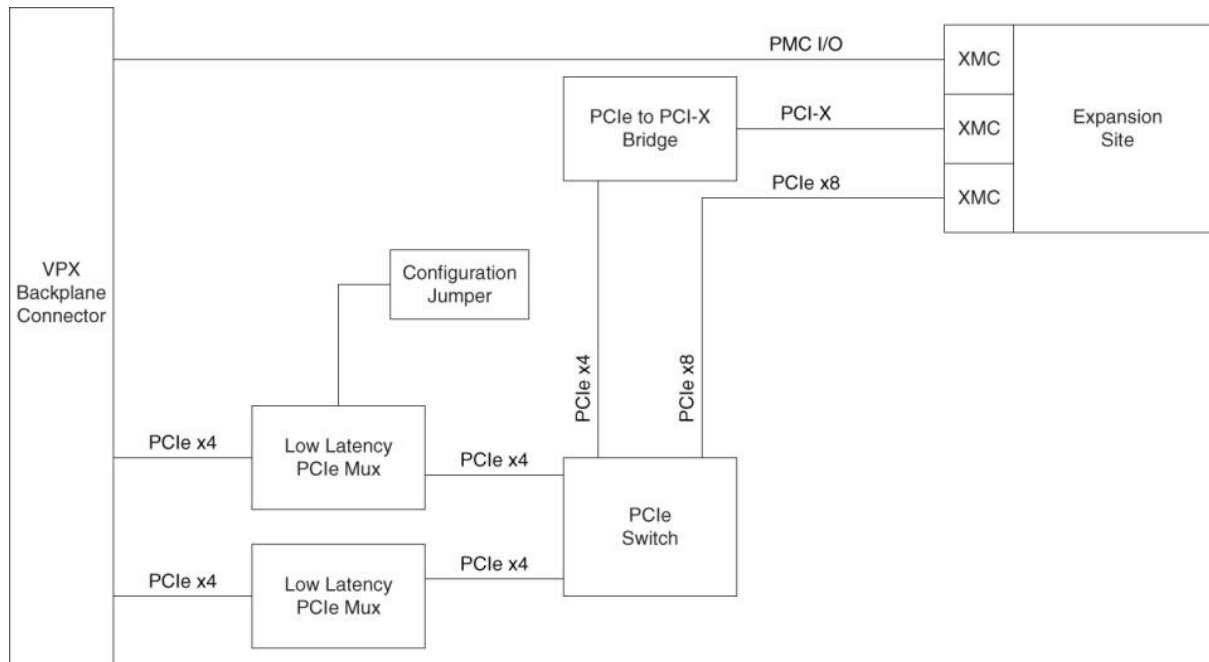


Step 4: Replace the cover and reinstall the 4 corner screws.

THEORY OF OPERATION

Operation of the VPX4810

The VPX4810 carrier can connect to the VPX bus in two ways; either as a Fat Pipe (PCIe x4) device or as a Double Fat Pipe (PCIe x8) device. This is system dependent and controlled by physical jumper. Refer to the jumper settings section for further information. The PCIe bus is then routed to a switch that then automatically connects via 4 or 8 lanes to the XMC module. Alternatively if a PMC module the switch instead uses a connection to a PCIe to PCI-X Bridge that converts the bus signals. The PMC/XMC rear I/O is routed from the J4 connector to the VPX P2 connector.



Due to a BIOS limitation on the XVPX-6300, when used with this CPU module the installed PMC/XMC card may not boot properly when connected to Fat Pipe B. They will function normally from inside an operating system. These devices will boot normally if connected to Fat Pipe A

I2C Bus and Temperature sensor

There is one I2C bus to access the FRU (Field Replaceable Unit). Information such as board module number, part number and revision level can be stored in this location. This device also will report board temperature from a thermocouple on the board. Please contact the factory for further information on the bus operation.

LED's

The VPX4810 uses three LEDs to indicate the status of PCIe link training. The VPXLNK (VPX back plane to the system processor), PCILNK (PCIx link train to the PMC sites) and XMCLNK (XMC link train to the XMC site) will be green during active data cycles. Note that each LED is labeled on the board.

SERVICE AND REPAIR

Preliminary Service Procedure

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation of your PMC module to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board. **WARNING: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS.**

Where to Get Help

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at <http://www.acromag.com>. Our web site contains the most up-to-date product and software information.

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed at the bottom of this page. When needed, complete repair services are also available.

SPECIFICATIONS

PHYSICAL

Physical Configuration	3U VPX Board
Height	3.937 inches (100.0 mm)
Depth	6.299 inches (160.0 mm)
Board Thickness	0.063 inches (1.60 mm)

Pitch (Thickness) includes all metalwork

VPX4810	0.80 inches (20.32 mm)
VPX4810CC	0.85 inches (21.59 mm)
VPX4810REDI	1.00 inch (25.40 mm)

Unit Weight (does not include PMC/XMC modules or shipping material):

Model VPX4610	0.35 pounds (0.16 Kg)
Model VPX4610CC	0.50 pounds (0.23 Kg)
Model VPX4610REDI	0.95 pounds (0.43 Kg)

POWER REQUIREMENTS

3.3 VDC ($\pm 5\%$)*	Typical 900 mA	Max. 3200 mA
5.0 VDC ($\pm 5\%$)*	Typical 900 mA	Max. 3200 mA
+12 VDC ($\pm 5\%$)	Up to 1A for PMC/XMC module	
-12 VDC ($\pm 5\%$)	Up to 1A for PMC/XMC module	

* With no XMC/PMC module installed. Add additional current for PMC/MCX module. VPRW is 5V for the XMC.

ENVIRONMENTAL

Operating Temperature/Airflow Requirements

Model	Op. Temp	Airflow Requirements
VPX4810	0°C to 70°C	100 LFM
VPX4810CC	-40°C to 85°C	200 CFM if not installed in a conduction cooled chassis.
VPX4810REDI	-40°C to 85°C	N/A. Must be installed in REDI complaint chassis.

Relative Humidity: 5-95% Non-Condensing.

Storage Temperature: -55°C to 100°C.

Non-Isolated: PCI/PCIe bus and field commons have a direct electrical connection.

Conduction Cooled PMC/XMC mezzanine card: VPX4810CC and VPX4810REDI models comply with ANSI/VITA 20-2001 (R2005).

Designed to meet the following environmental standards per ANSI/VITA47-2005(R2007)

Model VPX4810

- Environmental Class **EAC4**
- Operating Temperature: AC1 (0 to 70°C)
- Non Operating Class: C3
- Vibration Class: V2
- Shock 20g

Model VPX4810CC and VPX4810REDI

- Environmental Class **ECC3**
- Operating Temperature: CC4 (-40 to 85°C)
- Non Operating Class: C3
- Vibration Class: V3
- Shock 40g

Designed to comply with EMC Directive 2004/108/EC Class B

- **Radiated Field Immunity (RFI):** Complies with IEC 61000-4-3 with no register upsets.
- **Conducted R F Immunity (CRFI):** Complies with IEC 61000-4-6 with no register upsets.
- **Surge Immunity:** Not required for signal I/O per IEC 61000-4-5.
- **Electric Fast Transient (EFT) Immunity:** Complies with IEC 61000-4-4 Level 2 (0.5KV at field I/O terminals).
- **Electrostatic Discharge (ESD) Immunity:** Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) Level 2 (4KV enclosure port contact discharge).
- **Radiated Emissions:** Meets or exceeds European Norm 61000-6-3:2007 for class B equipment. Shielded cable with I/O connections in shielded enclosure is required to meet compliance.

VPX Specifications

Compliant with VITA 46: Base VPX Standard

VITA 46.4 complaint backing signals either 4x (fat pipe) or 8x (double fat pipe) PCIe (jumper selectable).

Rear I/O routed per VITA 46.9 P2w1-P64s.

Front I/O is only available on the VPX4810 (air cooled) model.

Backplane Compatible with the following VITA 65 Profiles:

Module Profile ²	Slot Profile
MOD3-PER-2F-16.3.1-3	SLT3-PER-2F-14.3.1
MOD3-PER-1F-16.3.2-2	SLT3-PER-1F-14.3.2
MOD3-PAY-1D-16.2.6-1 ¹	SLT3-PAY-1D-14.2.6
MOD3-PAY-2F-16.2.7-1 ¹	SLT3-PAY-2F-14.2.7

1. Board is compatible with payload profiles but has no hosting capabilities.
2. This list is not all inclusive. Other profiles may be compatible. Contact the factory with any questions.

PMC Specifications

PMC Compatibility: 32/64 bit, 33/66/133MHz. Complaint to IEEE 1386.1.

Signaling: 3.3V signaling only.

XMC Specifications

PCI Express 2.0: up to 8 lane PCI Express electrical and protocol standards. Performs 5.0 Gbps data rate per lane and per direction.

Supports ANSI/VITA 42.0 and 42.3 Compliant XMC modules.

Reliability Prediction

Mean Time Between Failures: 105,000 hours @ 25°C, Using MIL-HDBK-217F, Notice 2.