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Application Note

Multimedia Processor for Mobile Applications

DDR-SDRAM Interface

EMMA Mobile 1

PREFACE

Purpose   The purpose of this document is to introduce the usage of EMMA Mobile 1 DDR-SDRAM interface.

Organization   This document includes the following:

- Chapter 1. Introduction
- Chapter 2. Usage of DDR-SDRAM Interface
- Chapter 3. Example of DDR-SDRAM Operation
- Chapter 4. Hardware connection of DDR-SDRAM memory
- Appendix DDR-SDRAM API Function

Notation   Here explains the meaning of following words in text:

Note   Explanation of item indicated in the text

Caution   Information to which user should afford special attention

Remark   Supplementary information

Related document   The following tables list related documents.

Reference Document

Document Name	Version/date	Author	Description
S19268EJ1V0UM00_1chip.pdf	1st edition	NECEL	User's Manual
S19265EJ1V0UM00_ASMUGIO.pdf	1st edition	NECEL	User's Manual
S19254EJ1V0UM00_DDR.pdf	1st edition	NECEL	User's Manual
S19255EJ1V0UM00_DMA.PDF	1st edition	NECEL	User's Manual
S19266EJ1V0UM00_TIMER.pdf	1st edition	NECEL	User's Manual
S19907EJ1V0AN00_GD.pdf	1st edition	NECEL	GD Spec
K4X1G323PC.pdf	Sept. 2007	SUMSUNG	Data Sheet

PREFACE

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Chapter 1 Overview

1.1 Introduction

In this document, the below contents of EMMA Mobile 1 mobile DDR-SDRAM interface will be described.

1) the normal process procedure of mobile DDR-SDRAM

2) usage sample of mobile DDR-SDRAM

3) hardware connection method between EMMA Mobile 1 and external mobile DDR-SDRAM memory

As additional, the EMMA Mobile 1 DDR driver interface of EMMA Mobile 1 evaluation program will be explained.

About detail of DDR-SDRAM interface, please refer to "**EMMA Mobile 1 DDR-SDRAM Interface User's Manual**".

1.2 Development Environment

● Hardware environment of this project is listed as below.

Table 1-1 Hardware Environment

Name	Version	Maker
EMMA Mobile 1 evaluation board (PSKCH2Y-S-0016-01)	-	NEC Electronics
PARTNER-Jet ICE ARM	M20	Kyoto Microcomputer Co. Ltd

● Software used in this project is listed as below.

Table 1-2 Software Environment

Name	Version	Maker
GNUARM Toolchain	V4.3.2	GNU
WJETSET-ARM	V5.10a	Kyoto Microcomputer Co. Ltd

Chapter 2 Usage of DDR-SDRAM Interface

2.1 Normal Procedure of DDR-SDRAM Operation

Normal DDR-SDRAM data transfer procedure is shown as below.

Figure 1-1 Normal DDR-SDRAM Process Flow

Note:

1. About the explanation of all the DDR-SDRAM registers mentioned in this document, please refer to "**EMMA Mobile 1 DDR-SDRAM Interface User's Manual**".

2. About the explanation of all the ASMU registers mentioned in this document, please refer to "**EMMA Mobile 1 ASMU/GIO Interface User's Manual**".

3. About the explanation of all the CHG registers mentioned in this document, please refer to "**EMMA Mobile 1 One Chip User's Manual**".

2.2 Detail of Normal DDR-SDRAM Data Transfer Procedure

2.2.1 Configure DDR_CHG and DDR_ASMU Register

It's necessary to configure the EMMA Mobile 1 CHG register before initialize and use DDR-SDRAM.

- Pull-down and enable the input port;
- Set the port driver ability to 12mA (**NOTE**);

Note:

Please set the drive ability according to the DC character of the external DDR-SDRAM chip. In order to supply the higher drive ability, this value is set to the maximum value here.

After CHG register configuration, set ASMU registers for DDR-SDRAM.

Related register:
CHG_PULL0;
CHG_DRIVE0;
RESETREQ0;
RESETREQ0ENA;
CLK_MODE_SEL;
PLL1CTRL0;
PLL3CTRL0;
PLLLOCKTIME;
NORMALA_DIV;
STANDBY_DIV;
POWERON_DIV;
DIVMEMCRCLK;
CLKCTRL;
MEMCCLK270_SEL;
IO_L0_L1_BUZ;
ASMU_MEMC_HS_FAKE;

Explanation:

- In CHG_PULL0, only bit[6:4] need to be set for DDR-SDRAM;

    Bit[6] – DQS_IE;

    Bit[5:4] – DQS_xx;

For DDR-SDRAM, configure CHG_PULL0 as below:

Table 2-1 CHG_PULL0 Register Setting

Signal	Setting	Function
IE	1	Allows input
UPC	0	Pull-Down
POENB	0	Enable Pull-Up/Down

- In CHG_DRIVE0, only bit[19:10] need to be set for DDR-SDRAM;

    Bit[19:18] – DQS

    Bit[17:16] – DQM;

    Bit[15:14] – DQ;

    Bit[13:12] – DDR_CK;

    Bit[11:10] – DDR_A;

For DDR-SDRAM, configure CHG_DRIVE0 as below:

Table 2-2 CHG_DRIVE0 Register Setting

Signal	Setting	Function
DQS	11b	Set the driving capability:
DQM	11b	00b: 2mA
DQ	11b	01b: 4mA (Default value)
DDR_CK	11b	10b: 6mA/8mA
DDR_A	11b	11b: 8mA/12mA

Normally using the default value for drive DDR-SDRAM is enough.

● ASMU Register Setting for DDR

For example, set PLL1 to about 500MHz, set PLL3 to 229.276MHz;

As DDR333 memory chip, set DDR frequency to about 166MHz.

Table 2-3 ASMU Register Setting

Signal	Setting	Function
RESETREQ0ENA	--	Set MEMC_RST_ENA = 1 to enable set register RESETREQ0; Set MEMC_RST_ENA = 0 to disable set register RESETREQ0;
RESETREQ0	--	Set MEMC_RST = 0 to reset DDR-SDRAM
CLK_MODE_SEL	--	After reset, it is Power ON mode; After Initialization, it will be Normal A mode.
PLL1CTRL0	--	Default value: 0x79 → PLL1=499.712MHz
PLL3CTRL0	--	Default value: 0x37 → PLL3=229.376MHz
PLLLOCKTIME	--	PLL1&PLL3 Lock Time enable; And Lock Time=1586us
NORMALA_DIV	2x_xxxxH **(NOTE)**	set MEMCDOMAIN_DIV_A = 2 → MEMC_FREQ = PLL1x1/3 = (499.712/3)MHz = 166.571MHz
STANDBY_DIV	--	Default value. Divisor=16;
POWERON_DIV	--	Default value. Divisor=2;
DIVMEMCRCLK	--	Default value. DIV0xxx[2:0]=100b; DIV1xxx[3:0]=0000b. → MEMC_RCLK = PLL3 / 16 = (229.276 / 16)MHz = 14.336MHz
CLKCTRL	--	Default value.
MEMCCLK270_SEL	--	Default value.
IO_L0_L1_BUZ	--	Default value.
ASMU_MEMC_HS_FAKE	--	Default value.

Note:

Only need set NORMALA_DIV [22:20] for DDR-SDRAM module.

2.2.2 Initialize DDR-SDRAM module

Configure the external memory control register, according to the data sheet of the connected external DDR memory chip.

As reference, the following items need to be set.

- External memory delay setting;
- External memory chip related configuration;
- External memory AC timing setting;
- External memory MRS/EMRS setting;
- External memory command issue control;
- External memory refreshes setting (**NOTE**).

Note:

Please enable self-refresh function of mobile DDR-SDRAM. The explanation about EMMA Mobile 1 MEMC self-refresh mode, please refer "**4.1.2 Refresh control**" of "**EMMA Mobile 1 DDR-SDRAM User's Manual**".

Memory request schedule register "MEMC_REQSCH" also need to configure.

Remark:

MRS = Mode Register Setting

EMRS = Extended Mode Register Setting

Related register:

MEMC_DDR_CONFIGT1;

MEMC_DDR_CONFIGT2;

MEMC_DDR_CONFIGF;

MEMC_DDR_CONFIGA1;

MEMC_DDR_CONFIGA2;

MEMC_DDR_CONFIGC1;

MEMC_DDR_CONFIGC2;

MEMC_DDR_CONFIGR1;

MEMC_DDR_CONFIGR2;

MEMC_DDR_CONFIGR3;

MEMC_REQSCH;

2.2.3 Enable/Disable System Cache

EMMA Mobile 1 supports system cache function to storing data temporarily read from memory. So when the same data is used multiple times, the read cache function is useful. Under this case, enable system cache function can reduce memory access

User can decide use system cache for read/write or not.

Enable or disable system cache function, by configuring register "MEMC_DEGFUN".

Related register:
MEMC_DEGFUN

2.2.4 DDR-SDRAM Data Transfer

Usually, the DDR-SDRAM can be accessed after initialization, without setting system cache.

User can perform basic transfer and with-system-cache transfer. Only when perform the system cache data transfer, it is necessary to set the system cache function.

There are two mode of data transfer: CPU mode and DMA mode. About these two modes, please find its' process flow in "**Chapter 3.7**" and "**Chapter 3.8**".

2.2.5 DDR-SDRAM Power OFF

This step will be performed when system power off.

There are 2 register of ASMU_DDR will be set to stop the clock supply of DDR-SDRAM;

And then reset the DDR_CHG register to disable DDR input port.

Related register:
CHG_PULL0;
RESETREQ0;
RESETREQ0ENA;

Chapter 3 Example of DDR-SDRAM Operation

3.1 Outline of DDR-SDRAM Operation Example

In the EMMA Mobile 1 DDR-SDRAM operation sample, 6 samples are performed, based on the EMMA Mobile 1 evaluation board (PSKCH2Y-S-0016-01).

By these samples, user can know the below usages of EMMA Mobile 1 DDR-SDRAM module.

- How to check the external memory chip area;
- System cache usage;
- How to change clock;
- How to set PLL Full/Half/Quarter mode;
- CPU transfer mode usage;
- DMA transfer mode usage;

3.2 Connection Method of DDR-SDRAM

On the NECEL EMMA Mobile 1 evaluation board (PSKCH2Y-S-0016-01), one 128MB size mobile DDR-SDRAM memory chip (K4X1G323PC-8GC6: DDR333, 32Mwords x 32bit; manufacture: SAMSUNG) is connected.

And the connection method is below:

Figure 3-1 DDR-SDRAM Connection Method of EMMA Mobile 1 Evaluation Board

Table 3-1 Related Register Setting of the External Memory Chip

Register	Setting	Explanation
MEMC_DDR_CONFIGF	0000_000DH	CS0_ENABLE = 1b (CS0 enable)
		CS0_DENSITY = 11b (CS0 memory size: 1Gbit)
		CS0_DOUBLE = 0b (only connect 1x32bit chip)
		CS0_BANK_SPLIT = 00b (4 bank interleave)
		CS1_ENABLE = 0b (CS1 disable)
		CS1_DENSITY = 00b (ignore it when CS1 disable)
		CS1_DOUBLE = 0b (ignore it when CS1 disable)
		CS1_BANK_SPLIT = 00b (ignore it when CS1 disable)
MEMC_DDR_CONFIGC1	8020_0033H	MRS = 0033H
		(Burst Length = 011b: 8 burst;
		BT = 0b: sequential;
		CAS Latency = 011b: 3)
		EMRS = 8020H
		(PASR = 000b: Full Array;
		DS = 01b: 1/2)

Note:

All these registers listed in this table should be set, according to the data sheet of the connected external memory chip.

For MRS and EMRS setting of K4X1G323PC-8GC6, please refer to below figures.

BA1	BA0	A12 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
0	0	RFU[1)	0	0	0	CAS Latency			BT	Burst Length			Mode Register

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Type
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during MRS cycle

Figure 3-2 Mode Register Set of K4X1G323PC-8GC6

BA1	BA0	A12 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
1	0	RFU[1)	0	0	0	DS		RFU[1)		PASR			Mode Register

DS		
A6	A5	Driver Strength
0	0	Full
0	1	1/2
1	0	1/4
1	1	1/8

PASR		
A2	A1	A0	Refreshed Area
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during EMRS cycle

Figure 3-3 Extended Mode Register Set of K4X1G323PC-8GC6

3.3 DDR Sample1 – Check ALL Memory Area

In this sample, all memory area of the external DDR-SDRAM chip is checked.

3.3.1 Operation Flow

Operation flow chart of this sample is shown as below.

Figure 3-4 Flow of Check ALL Memory

Note:

  1. Checking all memory is from 0x3000_0000 to 0x37FF_FFFF, for EMMA Mobile 1 evaluation board (PSKCH2Y-S-0016-01).

3.3.2 Operation Detail

In this part, 3 group operations are performed.

1) write data 0x55555555 and 0xAAAAAAAA to the whole memory area interleaved.

The memory after write data should be as below (ex. Little Endian):

    0x3000_0000: | AA AA AA AA 55 55 55 55 AA AA AA AA 55 55 55 55 |

    0x3000_0010: | AA AA AA AA 55 55 55 55 AA AA AA AA 55 55 55 55 |

    .… ….

    0x37FF FFF0: | AA AA AA AA 55 55 55 55 AA AA AA AA 55 55 55 55 |

2) write data 0x55555555 with 1 word skip to the whole memory area.

The memory after write data should be as below (ex. Little Endian):

    0x3000_0000: | ** ** ** ** 55 55 55 55 ** ** ** ** 55 55 55 55 |

    0x3000_0010: | ** ** ** ** 55 55 55 55 ** ** ** ** 55 55 55 55 |

    .… ….

    0x37FF FFF0: | ** ** ** ** 55 55 55 55 ** ** ** ** 55 55 55 55 |

Caution:

    In this sample, ** ** ** ** means the data is the original data before writing 0x55555555

3) write the address value to the related memory area.

The memory after write data should be as below (ex. Little Endian):

    0x3000_0000: | 30 00 00 0C 30 00 00 08 30 00 00 04 30 00 00 00 |

    0x3000_0010: | 30 00 00 1C 30 00 00 18 30 00 00 14 30 00 00 10 |

    .… ….

    0x37FF FFF0: | 37 FF FF FC 37 FF FF F8 37 FF FF F4 37 FF FF F0 |

Then read out these data and compare with the written data.

If same, it means the Write/Read operation of the whole DDR-SDRAM memory is OK; otherwise, it is abnormally.

3.4 DDR Sample2 – Enable/Disable System Cache

In this sample, data transfer with/without system cache will be evaluated.

3.4.1 Operation Flow

Operation flow chart of this sample is shown as below.

Figure 3-5 Flow of Enable/Disable System Cache

Note:

In this figure, start address of memory area A is 0x30000000;

Start address of memory area B is 0x30010FE0.

3.4.2 Operation Detail

1) Enable or disable system cache function of DDR-SDRAM interface, by call function "em1_ddr_enable_sys_cache".
About function detail of "em1_ddr_enable_sys_cache", please refer to the link.

2) After enable or disable system cache, it is necessary to validate the read/write operation of DDR-SDRAM still can works normally.
By the difference of operation time-consuming between enable system cache mode and disable system cache mode, user can find the effect of system cache.

Data validate procedure of enable/disable system cache mode:
   Write the test data to memory area (A);
   Write the same data to memory area (B);

   Then read out the data from memory area (A);
   Read out the data from memory area (B);

   Then compare the read out data;
   If they are same, it indicates the read/write operation is OK; otherwise, the system cache function is abnormal.

3.5 DDR Sample3 – Change Clock

This sample will show how to change the clock frequency of DDR-SDRAM

3.5.1 Operation Flow

Operation flow chart of this sample is shown as below.

Figure 3-6 Flow of Change Clock Frequency

Note:
    "Operation is OK" in this figure means had change clock frequency successfully.

3.5.2 Operation Detail

1) Change the clock frequency of DDR-SDRAM, by call function "em1_ddr_chg_freq".
About function detail of "em1_ddr_chg_freq", please refer to the link.
It supports 166MHz, 133MHz, and 125MHz.

2) If change the clock frequency successfully, then set delay auto calibration by call function "em1_ddr_delay_auto_cal". Otherwise, return error information.
DDR-SDRAM auto calibration function can set up the initial relationship between clocks automatically. The initial calibration is done only once at system reset after device initialization is complete.
The calibration process can center the resynchronization clock phase into the middle of the captured data valid window to maximize the resynchronization setup and hold margin; center the read data capture valid window instead of the resynchronization window; picks the correct clock edge to align and resynchronize the captured data in the clock domain.
About function detail of "em1_ddr_delay_auto_cal", please refer to the link.

3.6 DDR Sample4 – Set PLL Mode

This sample will show how to set PLL Half mode of DDR-SDRAM.

3.6.1 Operation Flow

Operation flow chart of this sample is shown as below.

Figure 3-7 Flow of Set PLL Half Mode

Note:

"Operation is OK" in this figure means had set PLL divisor successfully.

3.6.2 Operation Detail

1) Set the PLL Half mode of DDR-SDRAM, by call function "em1_ddr_set_PLL_div".
About function detail of "em1_ddr_set_PLL_div", please refer to the link.
It supports Full-mode (1/1), Half-mode (1/2), and Quarter-mode (1/4).

3.7 DDR Sample5 – Transfer with CPU Mode

This sample shows the data transfer procedure of CPU transfer mode.

3.7.1 Operation Flow

Operation flow chart of this sample is shown as below.

Figure 3-8 Flow of CPU Transfer Mode Sample

3.7.2 Operation Detail

1) Set the source data area and the destination data area;
   The source address is set to 0x3000_0000;
   The destination address is set to 0x3080_0000.

2) Start data transfer by CPU mode

Data is transferred from the source address to the destination address by each 32 bits.

Note:

In this sample, 1 LED will light when process the CPU data transfer. GIO5 is used for the output port.

3.8 DDR Sample6 – Transfer with DMA Mode

This sample shows the data transfer procedure of DMA transfer mode with 1 channel and 3 channels.

3.8.1 Operation Flow

Operation flow chart of the sample with 1 DMA channel is shown as below.

Figure 3-9 Flow of 1CH DMA Transfer Mode Sample

Operation flow chart of the sample with 3 DMA channels is shown as below.

Figure 3-10 Flow of 1CH DMA Transfer Mode Sample

Note:

   About detail of the DMA register used in this and the following figures, please refer to "**EMMA Mobile 1 DMA Interface User's Manual**"

3.8.2 Operation Detail

The procedure of 1 channel and 3 channels DMA transfer sample almost are same.

1) Set the DDR DMA interrupt handler

For 1 channel (LCH0) DMA transfer:

The handler will get the INT status and clear the INT source of LCH0.

Then mask the INT source.

For 3 channels (LCH 0/1/2) DMA transfer:

The handler will get the INT status and clear the INT source of LCH0/1/2.

Then mask the INT source.

2) Enable DMA INT

Enable ACPU secure INT;

Enable ACPU INT;

Enable LENG INT of LCH0 – for 1 channel DMA transfer; or

Enable LENG INT of LCH 0/1/2 – for 3 channels DMA transfer.

3) Set DMA channel

For 1 channel (LCH0) DMA transfer:

Operation	Related Register	Setting Value
Set source start address	DMA_ARM_LCH0_AADD	3000_0000H
Set source offset	DMA_ARM_LCH0_AOFF	0H
Set source block count	DMA_ARM_LCH0_ASIZE_COUNT	0H
Set destination start address	DMA_ARM_LCH0_BADD	3080_0000H
Set destination offset	DMA_ARM_LCH0_BOFF	0H
Set destination block count	DMA_ARM_LCH0_BSIZE_COUNT	0H
Set total transfer length	DMA_ARM_LCH0_LENG	60_0000H
Set block size	DMA_ARM_LCH0_SIZE	FFFFH
Set transfer mode	DMA_ARM_LCH0_MODE	E4E4_0000H

For 3 channels DMA transfer (in LCHx, 3x00_0000H, and 3x80_0000H: x= 0, 1, 2)

Operation	Related Register	Setting Value
Set source start address	DMA_ARM_LCHx_AADD	3x00_0000H
Set source offset	DMA_ARM_LCHx_AOFF	0H
Set source block count	DMA_ARM_LCHx_ASIZE_COUNT	0H
Set destination start address	DMA_ARM_LCHx_BADD	3x80_0000H
Set destination offset	DMA_ARM_LCHx_BOFF	0H
Set destination block count	DMA_ARM_LCHx_BSIZE_COUNT	0H
Set total transfer length	DMA_ARM_LCHx_LENG	20_0000H
Set block size	DMA_ARM_LCHx_SIZE	FFFFH
Set transfer mode	DMA_ARM_LCHx_MODE	E4E4_0000H

4) Start DMA transfer by set register "DMA_ARM_CONT".

5) Wait for the transfer complete.

Because only LENG INT is enabled, so the INT only occurs when DMA transfer is finished

Note:

In this sample, 1 LED will light when process the CPU data transfer. GIO5 is used for the output port.

Chapter 4 Hardware Connection of DDR-SDRAM

4.1 Connection Method of DDR-SDRAM

EMMA Mobile 1 DDR-SDRAM interface has 2 CS; each CS can connect Max 1Gbit external memory chip, with 32bits data bus.

In this chapter, 4 connection cases are described.

- 256MB: 32M words x 32 bit x 2 chips;
- 128MB: 16M words x 16 bit x 2 chips;
- 128MB: 32M words x 32 bit x 1 chip;
- 256MB: 32M words x 16 bit x 2 chips;

The connection method of each case is shown in the following figures.

Case 1) 128MB x 2 chips, 32 bit data bus; Use CS0 and CS1

Figure 4-1 32Mwordsx32bitsx2chip DDR-SDRAM Connection Method

Table 4-1 Register Setting of Connection Case 1

Register	Setting	Explanation
MEMC_DDR_CONFIGF	0000_0D0DH	CS0_ENABLE = 1b (CS0 enable)
		CS0_DENSITY = 11b (CS0 memory size: 1Gbit)
		CS0_DOUBLE = 0b (only connect 32bit x 1 chip)
		CS0_BANK_SPLIT = 00b (4 bank interleave)
		CS1_ENABLE = 1b (CS1 enable)
		CS1_DENSITY = 11b (CS1 memory size: 1Gbit)
		CS1_DOUBLE = 0b (only connect 1x32bit chip)
		CS1_BANK_SPLIT = 00b (4 bank interleave)
MEMC_DDR_CONFIGC1	YYYY_XXXXH	MRS = XXXXH[NOTE]
		EMRS = YYYYH[NOTE]

Note:

The value of "MRS" and "EMRS" registers listed in this table should be set according to the data sheet of the connected external memory chip.

Case 2) 64MB x 2 chips, 16 bit data bus; Use CS0 only

EMMA Mobile 1

Chip#1:
16Mwords x 16bit

EMMA Mobile 1	Chip#1
DDR_CSB[0]	CSB
DDR_CKE[0]	CKE
DDR_MCLK	CK
DDR_MCLKB	CKB
DDR_A[12:0]	A[12:0]
DDR_DATA[15:0]	DQ[15:0]
DDR_DQS[3:0]	DQS[3:0]
DDR_DQM[1:0]	DM[1:0]
DDR_BA[1:0]	BA[1:0]
DDR_RASB	RASB
DDR_CASB	CASB
DDR_WEB	WEB

DDR_DATA[31:16]
DDR_DQM[3:2]

DDR_A[13] — N.C
DDR_CSB[1] — N.C
DDR_CKE[1] — N.C

Chip#2:
16Mwords x 16bit

CSB
CKE
CK
CKB
A[12:0]
DQ[15:0]
DQS[3:0]
DM[1:0]
BA[1:0]
RASB
CASB
WEB

$CSB = \overline{CS}$
$CKB = \overline{CK}$
$RASB = \overline{RAS}$
$CASB = \overline{CAS}$
$WEB = \overline{WE}$

Figure 4-2 16Mwordx16bitx2chip DDR-SDRAM Connection Method

Table 4-2 Register Setting of Connection Case 2

Register	Setting	Explanation
MEMC_DDR_CONFIGF	0000_001DH	CS0_ENABLE = 1b (CS0 enable)
		CS0_DENSITY = 11b (CS0 memory size: 1Gbit)
		CS0_DOUBLE = 1b (connect 16bit x 2 chips)
		CS0_BANK_SPLIT = 00b (4 bank interleave)
		CS1_ENABLE = 0b (CS1 disable)
		CS1_DENSITY = 00b (ignore it when CS1 disable)
		CS1_DOUBLE = 0b (ignore it when CS1 disable)
		CS1_BANK_SPLIT = 00b (ignore it when CS1 disable)
MEMC_DDR_CONFIGC1	YYYY_XXXXH	MRS = XXXXH**NOTE**
		EMRS = YYYYH**NOTE**

Note:

　　The value of "MRS" and "EMRS" registers listed in this table should be set according to the data sheet of the connected external memory chip.

Case 3) 128MB x 1 chip, 32 bit data bus; Use CS0 only

Figure 4-3 32Mwordsx32bitx1chip DDR-SDRAM Connection Method

Table 4-3 Register Setting of Connection Case 3

Register	Setting	Explanation
MEMC_DDR_CONFIGF	0000_000DH	CS0_ENABLE = 1b (CS0 enable)
		CS0_DENSITY = 11b (CS0 memory size: 1Gbit)
		CS0_DOUBLE = 0b (only connect 32bit x 1 chip)
		CS0_BANK_SPLIT = 00b (4 bank interleave)
		CS1_ENABLE = 0b (CS1 disable)
		CS1_DENSITY = 00b (ignore it when CS1 disable)
		CS1_DOUBLE = 0b (ignore it when CS1 disable)
		CS1_BANK_SPLIT = 00b (ignore it when CS1 disable)
MEMC_DDR_CONFIGC1	YYYY_XXXXH	MRS = XXXXH**NOTE**
		EMRS = YYYYH**NOTE**

Note:

The value of "MRS" and "EMRS" registers listed in this table should be set according to the data sheet of the connected external memory chip.

Case 4) 128MB x 2 chips, 16 bit data bus; Use CS0 and CS1

EMMA Mobile 1

**Chip#1:
32Mwords x 16bit**

EMMA Mobile 1	Chip#1
DDR_CSB[0]	CSB
DDR_CKE[0]	CKE
DDR_MCLK	CK
DDR_MCLKB	CKB
DDR_A[12:0]	A[12:0]
DDR_DATA[15:0]	DQ[15:0]
DDR_DQS[3:0]	DQS[3:0]
DDR_DQM[1:0]	DM[1:0]
DDR_BA[1:0]	BA[1:0]
DDR_RASB	RASB
DDR_CASB	CASB
DDR_WEB	WEB

**Chip#2:
32Mwords x 16bit**

EMMA Mobile 1	Chip#2
DDR_DATA[31:16]	
DDR_DQM[3:2]	
DDR_CSB[1]	CSB
DDR_CKE[1]	CKE
	CK
DDR_A[13] — N.C	CKB
	A[12:0]
	DQ[15:0]
	DQS[3:0]
	DM[1:0]
	BA[1:0]
	RASB
	CASB
	WEB

CSB = $\overline{CS}$	
CKB = $\overline{CK}$	
RASB = $\overline{RAS}$	
CASB = $\overline{CAS}$	
WEB = $\overline{WE}$	

Figure 4-4 32Mwordsx16bitx2chips DDR-SDRAM Connection Method

Table 4-4 Register Setting of Connection Case 4

Register	Setting	Explanation
MEMC_DDR_CONFIGF	0000_0D0DH	CS0_ENABLE = 1b (CS0 enable)
		CS0_DENSITY = 11b (CS0 memory size: 1Gbit)
		CS0_DOUBLE = 0b (only connect 16bit x 1 chip)
		CS0_BANK_SPLIT = 00b (4 bank interleave)
		CS1_ENABLE = 1b (CS1 enable)
		CS1_DENSITY = 11b (CS1 memory size: 1Gbit)
		CS1_DOUBLE = 0b (only connect 1x16bit chip)
		CS1_BANK_SPLIT = 00b (4 bank interleave)
MEMC_DDR_CONFIGC1	YYYY_XXXXH	MRS = XXXXH[NOTE]
		EMRS = YYYYH[NOTE]

Note:

The value of "MRS" and "EMRS" registers listed in this table should be set according to the data sheet of the connected external memory chip.

Appendix A. DDR-SDRAM Driver Function

A.1 DDR-SDRAM API function list

The following table shows the DDR-SDRAM interface functions:

Table A-1 DDR Driver Function List

Type	Function Name	Function Detail
Driver Function	em1_ddr_preconfig	Set CHG register for DDR-SDRAM
	em1_ddr_reset	Reset DDR-SDRAM interface
	em1_ddr_init	initialize DDR-SDRAM module
	em1_ddr_get_CS_state	Get the state of DDR-SDRAM CS0/CS1
	em1_ddr_set_SelfRefresh	Set to Self-Refresh mode
	em1_ddr_exit_SelfRefresh	Exit from Self-Refresh mode
	em1_ddr_set_DeepPowerDown	Set to Deep Power Down mode
	em1_ddr_chg_freq	Change the clock frequency of DDR-SDRAM
	em1_ddr_set_PLL_div	Set PLL div mode
	em1_ddr_delay_auto_cal	Delay Auto Calibrate function
	em1_ddr_enable_sys_cache	Enable system cache function

A.2 Type Define

A.2.1 Naming rule and coding rule

About naming rule and coding rule, please refer to "**GD_SPEC_EM1_AN&TP.pdf**"

A.2.2 Structure

None

A.3 Function Detail

A.3.1 Preconfig Function

[Function Name]

em1_ddr_preconfig

[Format]

void em1_ddr_preconfig (void);

[Argument]

None

[Function Return]

None

[Function Flow]

Figure A-1 Preconfig for DDR Initialization

[Note]

Set EMMA Mobile 1 CHG register for DDR-SDRAM interface initialization.

1) Set the port to INPUT port and Pull-down;

2) Set the drive ability to 12mA.

About CHG register, please refer to "**EMMA Mobile 1 One Chip User's Manual**".

A.3.2 Reset Function

[Function Name]

　　em1_ddr_reset

[Format]

　　void em1_ddr_reset (void);

[Argument]

　　None

[Function Return]

　　None

[Function Flow]

START

Enable setting MEMC_RST bit
[ASMU_RESETREQ0ENA]

Set MEMC_RST bit
[ASMU_RESETREQ0]

END

Figure A-2 Reset Operation of DDR-SDRAM

[Note]

　　Reset the DDR-SDRAM module

A.3.3 Initialize DDR-SDRAM Interface

[Function Name]

em1_ddr_init

[Format]

DRV_RESULT em1_ddr_init (void);

[Argument]

None

[Function Return]

DRV_OK;
DRV_ERR_ALREADY_INITIALIZED

[Function Flow]

```
                              ┌─────────────┐
                              │    START    │
                              └─────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │      Configure CHG register           │
                  │  [ Call function: em1_ddr_preconfig ] │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │ Set the external memory controller register │
                  │        [ MEMC_DDR_CONFIGT2 ]          │
                  │        [ MEMC_DDR_CONFIGT1 ]          │
                  │        [ MEMC_DDR_CONFIGF ]           │
                  │        [ MEMC_DDR_CONFIGA1 ]          │
                  │        [ MEMC_DDR_CONFIGA2 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │       Command Set: Enable CKE         │
                  │        [ MEMC_DDR_CONFIGC2 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │        Initialize MRS and EMRS        │
                  │        [ MEMC_DDR_CONFIGC1 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │            Command Set:               │
                  │  execute SDRAM initialization sequence│
                  │        [ MEMC_DDR_CONFIGC2 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │ Set memory request schedule mode register │
                  │          [ MEMC_REQSCH ]              │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │            Issue command              │
                  │        [ MEMC_DDR_CONFIGC2 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │         Set the refrence cycle        │
                  │        [ MEMC_DDR_CONFIGR1 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │         Set Auto Self-Refresh         │
                  │        [ MEMC_DDR_CONFIGR2 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                  ┌──────────────────────────────────────┐
                  │          Set Auto Power Down          │
                  │        [ MEMC_DDR_CONFIGR3 ]          │
                  └──────────────────────────────────────┘
                                     │
                                     ▼
                              ┌─────────────┐
                              │     END     │
                              └─────────────┘
```

Figure A-3 Initialization of DDR-SDRAM Interface

[Note]

Initialize the DDR-SDRAM interface.

And this function need to be performed when system power ON.

A.3.4 Get State of DDR-SDRAM

[Function Name]

em1_ddr_get_CS_state

[Format]

DRV_RESULT em1_ddr_get_CS_state (uint ulCsNum, SDR_STATE* pulState);

[Argument]

Parameter	Type	I/O	Detail
ulCsNum	uint	I	CS number. Can be set with: 0 – CS0 or 1 – CS1
pulState	SDR_STATE*	I/O	Return the DDR state.

[Function Return]

DRV_OK;

DRV_ERR_PARAM;

[Function Flow]

None

[Note]

Get the current state of CS0 or CS1 by read register "MEMC_DDR_STATE8".

It should be one of the following states:

    {

    SDR_STATE_IDLE,

    SDR_STATE_EMRS,

    SDR_STATE_INVALID,

    SDR_STATE_SELFREF,

    SDR_STATE_AUTO_PD,

    SDR_STATE_SELFREF_EXIT,

    SDR_STATE_DEEP_PD,

    SDR_STATE_PRECHG,

    SDR_STATE_RDWR,

    SDR_STATE_FRC_CBR,

    SDR_STATE_CBR,

    SDR_STATE_MRS

    }

A.3.5 Switch to Self-Refresh Mode

[Function Name]

em1_ddr_set_SelfRefresh

[Format]

DRV_RESULT em1_ddr_set_SelfRefresh (uint ulCsNum);

[Argument]

Parameter	Type	I/O	Detail
ulCsNum	uint	I	CS number. Can be set with: 0 – CS0 or 1 – CS1

[Function Return]

DRV_OK;

DRV_ERR_STATE;

[Function Flow]

```
                          ┌─────────────┐
                          │    START    │
                          └──────┬──────┘
                                 │
                                 ▼
              ┌──────────────────────────────────────┐
              │ Check the current state of DDR-SDRAM  │
              │ [ call function: em1_ddr_get_CS_state ]│
              └──────────────────┬───────────────────┘
                                 │
                                 ▼
                    ◇──────────────────────◇   YES
                    │ STATE == SDR_STATE_   │────────────┐
                    │ SELFREF ?             │            │
                    ◇──────────┬───────────◇            │
                               │ NO                      │
                               ▼                         │
              ┌──────────────────────────────┐          │
              │ Switch to Self-Refresh mode   │          │
              │ [ MEMC_DDR_CONFIGC2 ]         │          │
              └──────────────┬───────────────┘          │
                             ▼                           │
              ┌──────────────────────────────────────┐  │
              │ Check the current state of DDR-SDRAM  │  │
              │ [ call function: em1_ddr_get_CS_state ]│  │
              └──────────────┬───────────────────────┘  │
                             │                           │
                             ▼                           │
                    ◇──────────────────────◇   YES       │
                    │ STATE == SDR_STATE_   │────────┐   │
                    │ SELFREF ?             │        │   │
                    ◇──────────┬───────────◇        │   │
                               │ NO                  │   │
                               ▼                     ▼   ▼
                 ┌──────────────────────┐   ┌──────────────────┐
                 │ Return DRV_ERR_STATE │   │  Return DRV_OK   │
                 └──────────────────────┘   └──────────────────┘
```

Figure A-4 Switch to Self-Refresh Mode

[Note]

Entry Self-Refresh mode by setting register "MEMC_DDR_CONFIGC2";

A.3.6 Disable Self-Refresh Mode

[Function Name]

    em1_ddr_exit_SelfRefresh

[Format]

    DRV_RESULT em1_ddr_exit_SelfRefresh (uint ulCsNum);

[Argument]

Parameter	Type	I/O	Detail
ulCsNum	uint	I	CS number. Can be set with: 0 – CS0 or 1 – CS1

[Function Return]

    DRV_OK;

    DRV_ERR_STATE;

[Function Flow]

Figure A-5 Exit from Self-Refresh Mode

[Note]

    None

A.3.7 Enter Deep Power Down Mode

[Function Name]

em1_ddr_set_DeepPowerDown

[Format]

DRV_RESULT em1_ddr_set_DeepPowerDown (uint ulCsNum);

[Argument]

Parameter	Type	I/O	Detail
ulCsNum	uint	I	CS number. Can be set with: 　0 – CS0　or 　1 – CS1

[Function Return]

DRV_OK;

DRV_ERR_STATE;

[Function Flow]

Figure A-6 Switch to Deep Power Down Mode

[Note]

None

A.3.8 Set Clock Frequency

[Function Name]

em1_ddr_chg_freq

[Format]

DRV_RESULT em1_ddr_chg_freq (uint ulFreq);

[Argument]

Parameter	Type	I/O	Detail
ulFreq	uint	I	Frequecy value(MHz). Can be set with: 166, 133, or 125

[Function Return]

DRV_OK;

DRV_ERR_ABNORMAL;

[Function Flow]

Figure A-7 Set Clock Frequency

[Note]

EMMA Mobile 1 DDR-SDRAM interface only supports 3 clock frequencies: 166MHz, 133MHz, and 125MHz.

For each frequency, the PLL1 setting value and clock divisor are listed in the below table.

Table A-2 Clock Frequency Setting Table

Target Frequency		166MHz	133MHz	125MHz
PLL1 Value				
1)	target value	499.712MHz	397.312MHz	499.712MHz
2)	Set REG[PLL1CTRL0] =	0x79	0x60	0x79
Clock Divisor				
1)	Set REG[NORMALA_DIV] =	0x00244200	0x00244200	0x00355300
Domain Clock Frequency				
1)	ACPU (divisor)	500MHz (1/1)	400MHz (1/1)	500MHz (1/1)
2)	ADSP (divisor)	500MHz (1/1)	400MHz (1/1)	500MHz (1/1)
3)	HBUS (divisor)	166MHz (1/3)	133MHz (1/3)	125MHz (1/4)
4)	LBUS (divisor)	83.3MHz (1/6)	66.6MHz (1/6)	62.5MHz (1/8)
5)	FLASH (divisor)	83.3MHz (1/6)	66.6MHz (1/6)	62.5MHz (1/8)
6)	MEMC (divisor)	166MHz (1/3)	133MHz (1/3)	125MHz (1/4)

A.3.9 Set PLL Div Mode

[Function Name]

em1_ddr_set_PLL_div

[Format]

DRV_RESULT em1_ddr_ set_PLL_div (SDR_PLL_MODE ulDiv);

[Argument]

Parameter	Type	I/O	Detail
ulDiv	SDR_PLL_MODE	I	PLL Mode. Can be set with: PLL_HALF_OFF, PLL_HALF_DIV2, PLL_HALF_DIV4, PLL_HALF_DIV6, PLL_HALF_DIV8, PLL_HALF_DIV10, PLL_HALF_DIV12, PLL_HALF_DIV14, or PLL_HALF_DIV16

[Function Return]

DRV_OK;

DRV_ERR_ABNORMAL;

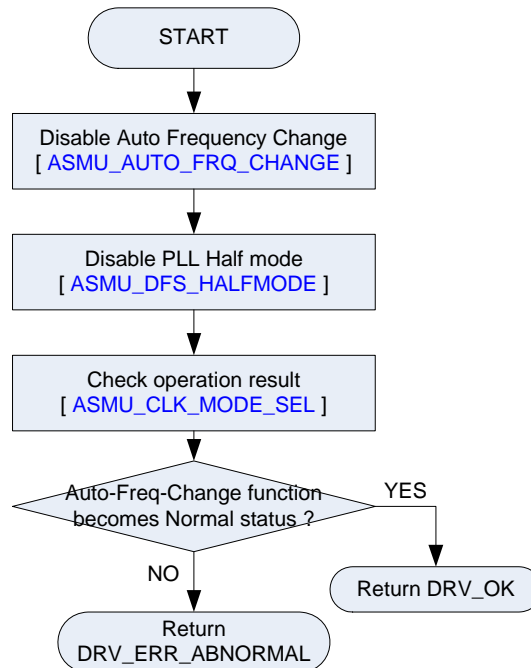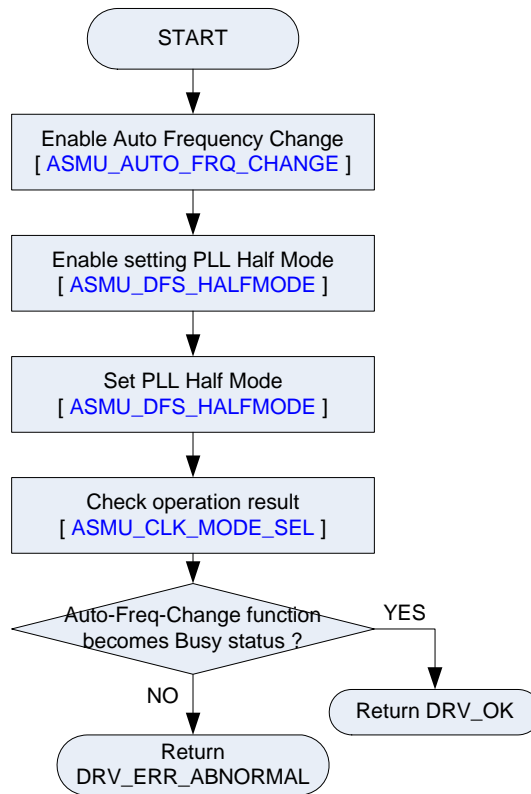**[Function Flow]**

Figure A-8 Disable PLL Half Mode

Figure A-9 Set PLL Half Mode

[Note]

None

A.3.10 Delay Auto Calibrate

[Function Name]

em1_ddr_delay_auto_cal

[Format]

void em1_ddr_delay_auto_cal (void);

[Argument]

None

[Function Return]

None

[Function Flow]

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           ▼
        ┌──────────────────────────────────────┐
        │ Turn OFF MEMC_CLK auto-control mode    │
        │          [ ASMU_AHBCLKCTRL1 ]          │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │ Turn OFF MEMC_CLK270 auto-control mode │
        │            [ ASMU_CLKCTRL ]            │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │     Set MEMC_CLK270 to MEMC_CLK        │
        │         [ ASMU_MEMCCLK270_SEL ]        │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │ Set calibration pattern to 0xAAAA->0x5555 │
        │          [ MEMC_DDR_CONFIGT1 ]         │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │             Set the delay time         │
        │          [ MEMC_DDR_CONFIGT2 ]         │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │ Recovery MEMC_CLK auto-control mode    │
        │          [ ASMU_AHBCLKCTRL1 ]          │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │ Recovery MEMC_CLK270 auto-control mode │
        │            [ ASMU_CLKCTRL ]            │
        └──────────────────┬─────────────────────┘
                           ▼
        ┌──────────────────────────────────────┐
        │          Reset MEMC_CLK270             │
        │         [ ASMU_MEMCCLK270_SEL ]        │
        └──────────────────┬─────────────────────┘
                           ▼
                    ┌─────────────┐
                    │     END     │
                    └─────────────┘
```
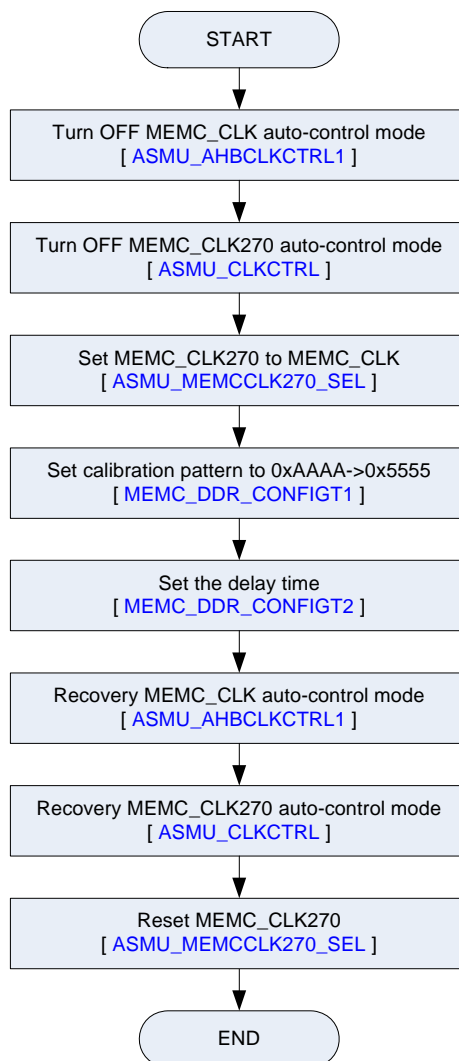
Figure A-10 Set Delay Auto Calibration

[Note]

None

A.3.11 Enable/Disable System Cache

[Function Name]

em1_ddr_enable_sys_cache

[Format]

void em1_ddr_enable_sys_cache (BOOL bEnable);

[Argument]

Parameter	Type	I/O	Detail
bEnable	BOOL	I	Enbale/Disable Flag 　　TRUE – Enable system cache; 　　FALSE – Disable system cache.

[Function Return]

None

[Function Flow]

None

[Note]

Enable/Disable system cache function by set register "MEMC_DEGFUN".

ANNEX Modification History

Number	Modification Contents	Author	Date
V 1.00	New version		Aug, 4, 2009