Generation and Measurement of Burst Digital Audio Signals with Audio Analyzer UPD

Application Note 1GA38_0L

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Subject to change

Product:

Audio Analyzer UPD

ROHDE&SCHWARZ

1. Introduction

Today, digital audio signals are transmitted via standardized interfaces not only in the form of continuous data streams but also increasingly as burst audio signals. This application note shows various ways of generating and analyzing such data bursts with Audio Analyzer UPD. In the applications described, the parameters word clock, bit clock and word length can be set over wide ranges. Single-channel and dual-channel audio data with bit clocks far into the MHz range can be processed.

2. Description of Application

In most audio applications, digital audio data are transmitted as a continuous stream, the frames for one or two audio channels being transmitted without any intervals. The relationship between the parameters word clock, bit clock and word length is as follows:

$$Bit\,clock = word\,clock \times word\,length \times number\,of\,\,channels$$

It is particularly in the field of mobile-radio and telephone applications that recently more and more audio channels have been transmitted on digital lines using time division multiplex. This is done by increasing the clock rate at which the bits are sent. The data words in each channel are thus transmitted more quickly and each "data packet" is followed by an interval, in which data from other channels can be inserted. For measurements on data coders and decoders it is necessary to generate test signals for single channels with a wide variety of burst-to-interval ratios and subsequently analyze these signals. In addition to single-channel test signals, which are used in most cases, burst stereo signals are also needed. The latter are frequently used within a device, for example in multichannel mixing consoles in recording studios for transmitting data streams from one circuit to another.

In the meantime, a wide variety of applications has developed, ranging from 8 to 24-bit data words, sampled at frequencies from 8 to 48 kHz and transmitted at bit clocks up into the MHz range. The intervals between the bursts do not always represent integer multiples of the data words, essential if additional channels are to be inserted. The authors of this text are aware of applications using intervals shorter than a data word.

For the applications described in this note, it is assumed that UPD firmware 3.02 or higher is installed. All of the applications described will also operate with older firmware versions. It should however be noted that the structure and wording of some menu lines in the older versions differ from those described in this note.

3. The Universal Digital Interfaces of Audio Analyzer UPD

The basic version of the Audio Analyzer UPD already incorporates universal serial digital interfaces with user-configurable bit clock, word clock, word length, number of audio bits, bit order and word offset, separately for the generator and the analyzer section. The UPD interfaces are dual-channel; each of the 15-pin DSUB connectors for the generator and analyzer sections has two bit-clock, audio-data and word-sync lines, so that dual-channel audio signals present on different lines can be processed at the same time. Moreover, it is possible to process two multiplexed channels one after the other, which is necessary for stereo signals.

The UPD generator directly supplies the standard 32 kHz, 44.1 kHz and 48 kHz clock rates, and appropriate multiples. With an external clock signal, UPD can generate and analyze data words with sampling frequencies from 100 Hz to 780 kHz, and handle bit clocks up to 32 MHz.

The bit format can be set to "MSB first" or "LSB first", the word length can be set in steps, the maximum length being 32 bits.

The UPD generator is capable of supplying burst signals, provided the timing meets certain criteria. This can be achieved with an additional external synchronization circuit which is described in this application note. The additional circuit can be operated from a -5 V supply available at the DSUB connectors.

4. Basic Settings of UPD Generator

Some of the basic generator settings are valid for all applications discussed in this note. These settings are described in this section. The settings for other parameters may differ considerably from case to case and are therefore described separately for each application.

Selection of generator, *GENERATOR* menu line

Audio Analyzer UPD has three digital generators with different maximum word clock frequencies. The generators are designated *DIG 48kHz*, *DIG 192kHz* and *DIG 768kHz*. If *DIG 768kHz* is selected, multiplexed stereo signals cannot be generated.
Applications for burst data signals seldom use sampling rates above 48 kHz. The ***DIG 48kHz*** setting should therefore be appropriate in most cases.

Setting of *Src Mode* (Source Mode)

UPD can generate signals for a variety of applications. For the application presented in this note, ***AUDIO DATA*** is the right setting.

Selection of audio channels, *Channel(s)* menu line

This menu line determines if only channel 1 or if only channel 2 is to contain audio data (the other channel will contain zero bits in each case), or if both channels are to contain audio data. In the latter case, in-phase (*2 ° 1*) or anti-phase (*2 ° -1*) data generation can be selected.
Normally, only ***channel 1*** is used for burst data words.

Selection of output interface, *Output* menu line

Here, the DSUB connector on the UPD front panel is to be used for serial data output; the setting is ***SERIAL*** for single-channel data streams or ***SERIAL MUX*** for the output of multiplexed stereo signals.

Selection of generator synchronization, *Sync To*

This menu line determines if the internal clock generator is to be used (***GEN CLK***) or if the generated data words are to be synchronized to an external clock (***EXTERN***).

Setting of sampling frequency, *Sample Frq* and *Oversamp* menu lines

The internal clock generator of Audio Analyzer UPD generates the standard clock frequencies 32 kHz, 44.1 kHz and 48 kHz and, with the aid of internal crystal oscillators, twice, four times, eight times and 16 times these frequencies. The word clock is obtained by selecting the fundamental frequency in the *Sample Frq* line and the oversampling factor in the *Oversamp* line. To generate a signal with a clock frequency of 96 kHz, for example, *48 kHz* with an oversampling factor of 2 is to be set.
For other clock rates, the UPD generator can be synchronized to an external clock signal. This requires the application of a clock signal (bit clock) to the serial interface of UPD. In this mode, the three UPD generators have the following frequency limits:

Generator	Max. word clock	Max. bit clock
DIG 48kHz	100 kHz	32 MHz
DIG 192kHz	300 kHz	32 MHz
DIG 768kHz	780 kHz	32 MHz

If UPD is synchronized to an external clock signal, ***EXTERN*** must be selected in the *Sample Frq* line. Moreover, in the next line, the precise sampling frequency (word clock) for calculating the audio data is to be entered. For telephone applications, the sampling frequency will usually be 8 kHz, for other applications, other frequencies may be required.

Definition of word length in data stream, *Wordlength* and *Audio Bits* menu lines

In the *Wordlength* line, the number of bits that make up a data sample is entered. Word lengths of 8 bits, 16 bits, 24 bits and 32 bits can be selected. With 32 bits, however, only 28 bits at most can be used as data bits. The *Audio Bits* setting is closely related to the *Wordlength* setting. The *Audio Bits* line is used to specify how many bits of the data samples to be transmitted are to carry audio data. The remaining bits are set to zero.
The settings made in these two menu lines will be explained in greater detail in the following.

***Wordoffset* menu line**

This line is used to specify the position, relative to the start of the data word, of the sync pulse for the word sync line. The word sync pulse can be shifted over the whole length of a data word.
For the generation of burst audio signals, the word offset must be set according to the type of external circuitry used. More detailed information will be found in the sections describing the various types of external circuitry.

Setting of active clock edge, *Bitclock* menu line

The *Bitclock* line defines the polarity of the clock signal data bits.
Depending on the application, ***RISING*** or ***FALLING*** is to be selected.

***Bit Order* menu line**

This line defines the order of bits in the data stream. For most applications, ***MSB FIRST*** is required.

***Frq Bitclock* display line**

In the "normal operating mode" of the generator, this display indicates the output bit clock. However, this display is not relevant to the applications presented in this note. The displayed value is equal to the set word length multiplied by the sampling clock rate. Since the intervals are not taken into account, this value does not correspond to the system clock used for burst signals.

5. Burst Signals Generated Internally by Audio Analyzer UPD

5.1. Single-Channel Audio Data

The length of data words supplied by the UPD generator is set by means of two parameters. *Wordlength* defines the number of bits per frame, *Audio Bits* defines how many bits in the transmitted frame are to carry audio data. The remaining bits are set to zero. A burst data stream will therefore be obtained only if the number of *Audio Bits* is less than the *Wordlength*. This is illustrated by the Figure below:

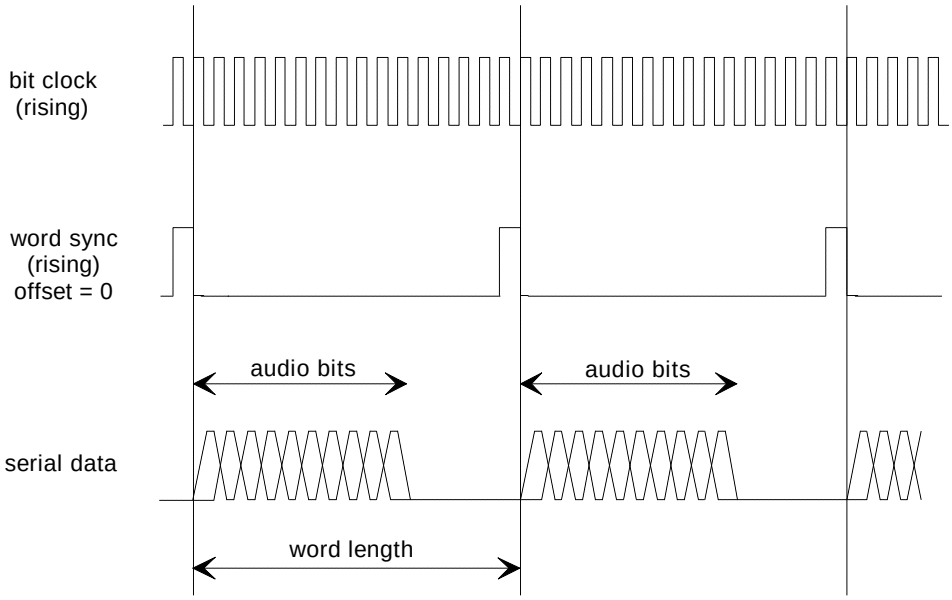

Fig. 1: Burst data stream with *Audio Bits* < *Wordlength*

The settings used in the above example are as follows:

Channel(s)	***1***	*Output*	***SERIAL***
Sync To	***GEN CLK***	*Sample Frq*	***48 kHz***
Wordlength	***16***	*Audio Bits*	***10***
Wordclock	***RISING***	*Bitclock*	***RISING***
Wordoffset	***0***	*Bitorder*	***MSB FIRST***

These settings yield a bit clock of 768 kHz, which is also indicated in the *Frq Bitclock* display line.

However, the data burst to interval ratio in the Figure above cannot be set to any desired value since words can only be 8 bits, 16 bits, 24 bits or 32 bits long and the number of audio bits must be in the range 8 to 28.

Moreover, the word clock and the bit clock must be in the ratios 1:8, 1:16, 1:24 or 1:32 because other ratios cannot be set on the binary dividers in the generator. Initially, this may seem to be unduly restrictive, but a large number of applications use these ratios and so there are, in fact, no real problems.

5.2. Stereo Signals in Time Division Multiplex

Audio Analyzer UPD is able to generate dual-channel signals in basically the same way as the single-channel signals described above. The dual-channel signals are transmitted using time division multiplex (TDM).
To this end, the bit clock is doubled, and the word select line is used instead of the word sync line. The word select line transmits a symmetrical rectangular signal with a frequency equal to the sampling frequency. One audio channel is transmitted during each half-wave. The *WordselCh1* menu item is used to specify which channel is output during which half-wave of the word select signal. This is illustrated by Figure 2.

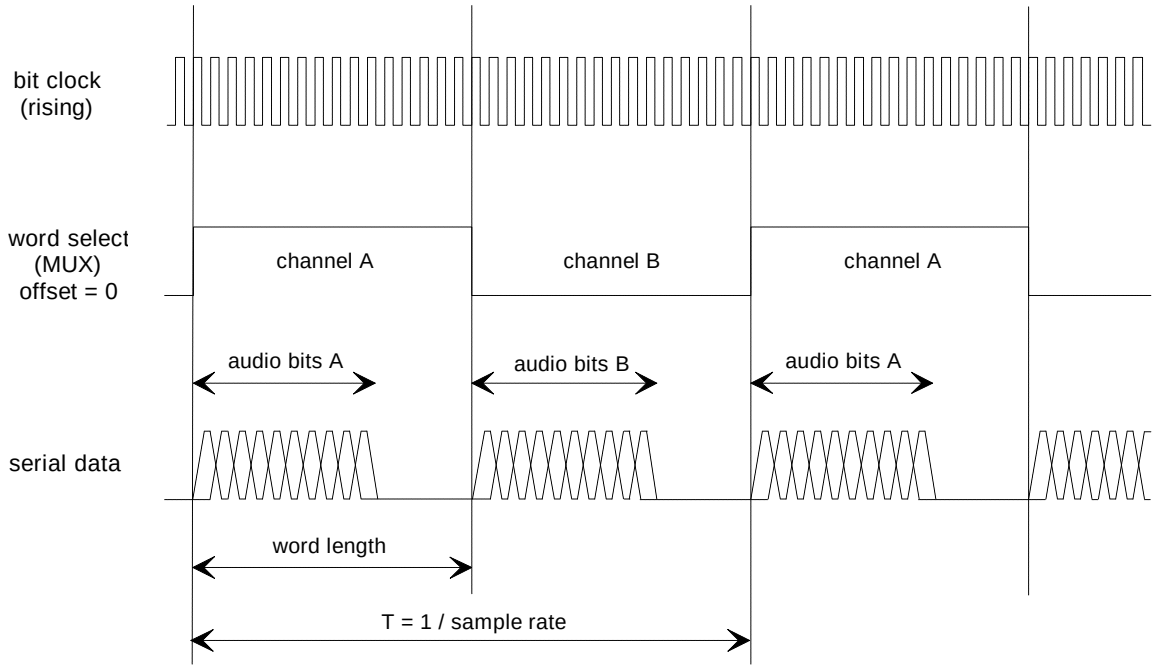

Fig. 2: Burst dual-channel data stream with *Audio Bits* < *Wordlength*

The settings used in the above example are as follows:

Channel(s)	***2 º 1***	*Output*	***SERIAL MUX***
Sync To	***GEN CLK***	*Sample Frq*	***48 kHz***
Wordlength	***16***	*Audio Bits*	***10***
Bitclock	***RISING***	*Wordoffset*	***0***
WordselCh1	***HIGH***	*Bitorder*	***MSB FIRST***

These settings yield a 1536kHz bit clock due to the dual-channel output. The bit clock is also indicated in the *Frq Bitclock* display line.

In this case, too, the data burst to interval ratio cannot be set to any desired value; the restrictions for single-channel signals apply in this case too.

6. Single-Channel Burst Signals with any Burst-to-Interval Ratio

Measurements on data codecs for mobile radio or telephone applications sometimes require digital data streams transmitted in very short bursts. As a rule, these are single-channel audio signals sampled, in most cases, at a rate of 8kHz. Audio Analyzer UPD is able to generate signals of this kind by means of a small external circuit for synchronizing the data generator. The system clock (bit clock) and the word clock must be supplied by the DUT or the test setup; UPD generates the data contents only. Figure 3 shows the setup for this application. The external circuit generates a burst clock signal from the two input signals. While this clock signal is applied, UPD outputs data bits; the number of bits per data word is defined in the generator panel. The word sync signal generated by UPD is fed back to the synchronization circuit and interrupts the clock signal after a complete data word has been sent.

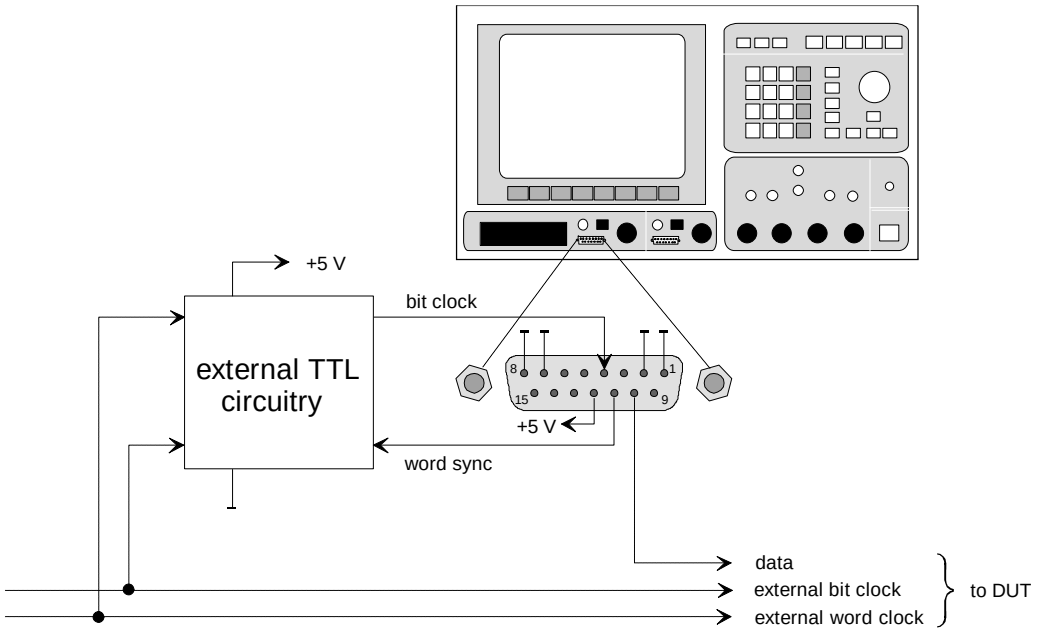

Fig. 3: Test setup for burst signal generation

6.1. Design of External Synchronization Circuit

Figure 4 shows the additional external circuit for generating and synchronizing the external clock signal to supply single-channel data bursts.

Any 5-V TTL logic components may be used for the circuit. In the example shown, a dual D flip-flop 74HCT74, a quad EXOR gate 74HCT86 and a quad NOR gate 74HCT02 are used. The additional logic circuit is powered from UPD via a 5V line brought out at pin 12 of the UPD's serial output connector; up to 50 mA can be drawn. Pins 1, 2, 7 and 8 are grounded (see Figure 3).

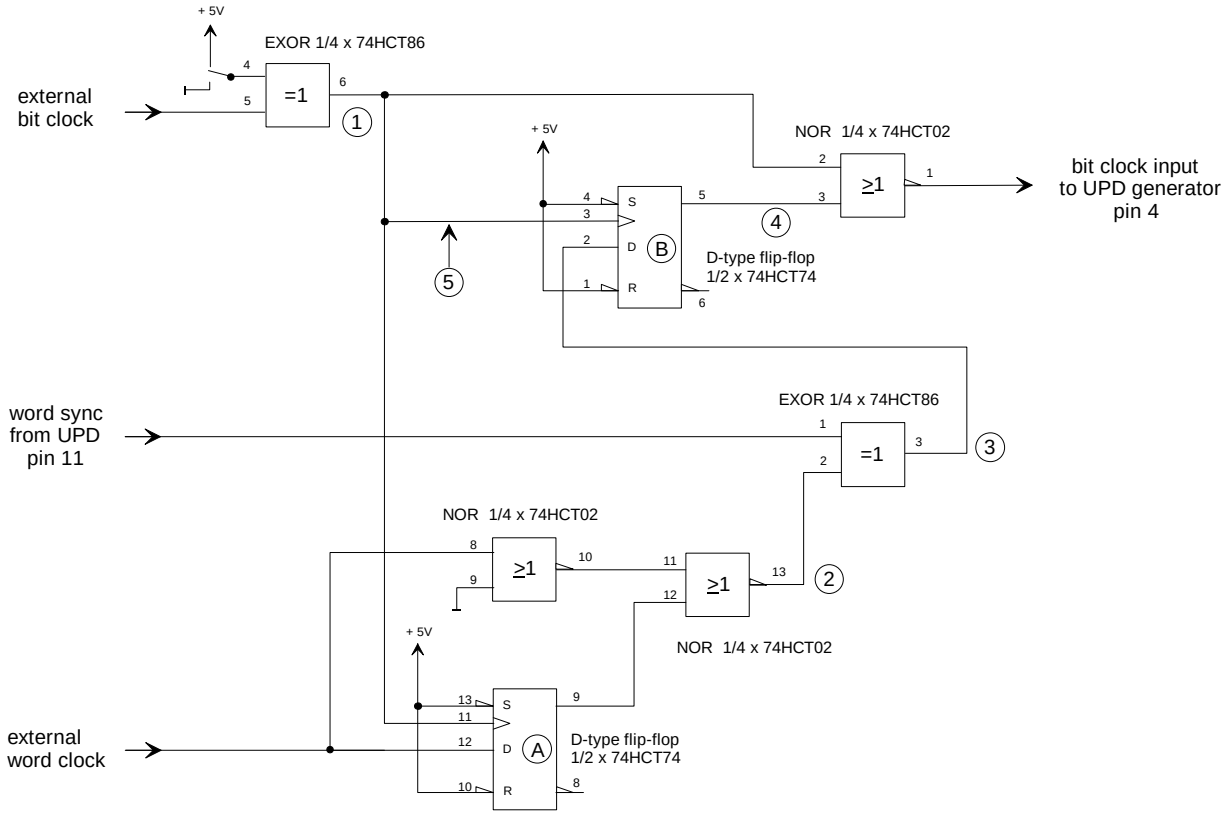

Fig. 4: External circuit connected to UPD for generating any single-channel burst signals

The input signals must meet the following requirements:

- A system clock (bit clock) is required for outputting the data bits. The generator in UPD can handle clock rates up to 32MHz.
- The rising edge of the word clock defines the start of the data words and so the burst-to-interval ratio. The duration of the word clock pulse is irrelevant provided that the signal goes low at least one clock cycle prior to the start of the next data word.
- The bit clock and the word clock must be in sync.

6.2. Operation of External Synchronization Circuit

The easiest way of understanding how the external synchronization circuit operates is to look at the timing diagram shown in Figure 5.
The data stream represented there does not reflect real conditions since UPD can generate only data words with a minimum length of 8 bits. However, to give a more clear-cut representation, a data burst with data words of only 4 bits is shown, followed by intervals of the same length.

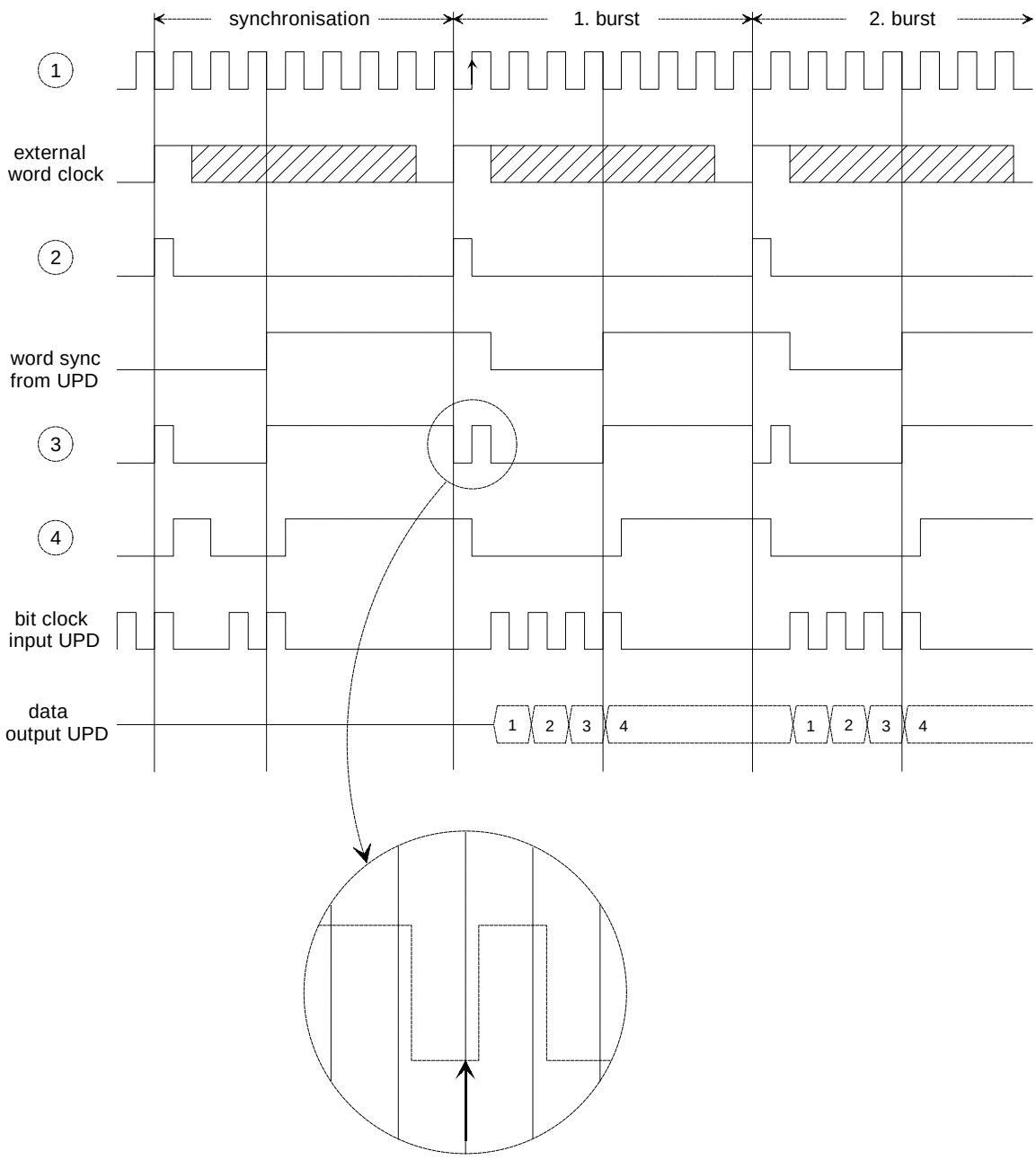

Fig. 5: Timing diagram of external synchronization circuit for UPD data generator

Function of EXOR gate at bit clock input

To ensure well-defined switching states, the rising edge of the word clock must be transmitted on the falling edge of the bit clock. If this is not possible because of the application's circuit design, the bit clock signal can be inverted by means of the EXOR gate by connecting pin 4 to +5 V. If connected differently, the clock signal passes through the gate unchanged, so the gate is actually not needed.

Generation of a narrow word sync pulse from the input word clock

The pulse is generated by means of D flip-flop A and the two NOR gates with output . When the external word clock signal goes high, the output of D flip-flop A first remains low, while pin 13 of the NOR gate goes high. On the rising edge ①, the word clock signal is read into the flip-flop, whose output goes high, and the NOR gate goes low again . This process is not repeated until the next rising edge of the word clock signal, no matter how long the word clock signal remains high.

Synchronization with word sync signal from UPD

The EXOR gate compares signal with the word sync signal from UPD. If the signals are equal, output goes low, if not, output goes high. The pulse on line is thus passed on unchanged. During this time, clock signals are applied to UPD. When the set word length is reached, the UPD's word sync signal goes high. The first part of the timing diagram designated "Synchronization" shows the switching of the UPD word sync line not yet in sync after the next-but-one clock. As a result, output of the EXOR gate goes high. This state is read into the second D flip-flop (B) on the next rising clock edge ①, causing output of the flip-flop to go high, too. Output pin 1 of the subsequent NOR gate is thus held low and the clock signal is no longer passed on to UPD. Due to the absence of the clock signal, the UPD's word sync signal is no longer switched over.

Generation of first data burst

The next external word clock signal produces a new pulse on line ; the EXOR gate goes low for the duration of this pulse. Since the output state of this gate is not changed until the next change in the clock signal ① (the output is delayed, relative to the clock signal, by the propagation times of three gates), the output state is still low when it is read into D flip-flop B. This can be clearly seen from the detail drawing. As a result, line enables the NOR gate, and the UPD generator is clocked again. UPD generates data bits, and its word sync line is reset. Line therefore remains low until the word length set on UPD is attained and the word sync signal is switched to high. Again, no clock signal is received by UPD, and the word sync and the data line remain at the level state last active.
On the next external word clock signal, the procedure is repeated for the second data burst.

6.3. Settings on Audio Analyzer UPD

For the above application, the UPD generator must be set as follows:

Channel(s)	***1***
Output	***SERIAL***
Sync To	***EXTERN***
Sample Frq	The **sampling frequency** for calculating the audio samples is to be entered; the sampling frequency is equal to the external word clock frequency.
Wordlength	The **desired word length** is to be entered.
Audio Bits	The number of **audio bits** usually equals the word length. If the burst length is not divisible by 8, the desired number of bits is to be entered and the word length set to the next higher value.
Wordoffset	The **word offset must always be set to *0*** for this type of circuit since otherwise the start of a word would be shifted into the next or previous burst and the data word would thus be distributed over two bursts.
Wordclock	***RISING***
Bitclock	***RISING*** if a timing as shown in Figure 4 is to be obtained; ***FALLING*** if data words are to be transferred on the falling edge of the clock signal applied to UPD.
Bit Order	***MSB FIRST*** will, as a rule, be the right setting.

6.4. Modification of Circuit

The timing diagram in Figure 5 shows that the external word clock signal is transmitted on the falling edge of the clock signal ①. The first data bit is switched over already on the next falling edge of the clock signal. For some applications, it may be necessary to delay the data bits by one clock cycle. This is very easy to do with the circuit described - simply insert an inverter at . For example, the NOR gate of IC 74HCT02, so far unused, can be connected at this point.
Due to the delay of the clock signal thus caused at the upper flip-flop, line does not enable the clock signal for UPD until one clock cycle later, so that the start of data output is delayed by one clock cycle relative to the external word clock signal.

7. Burst Signals with any Burst-to-Interval Ratio (Stereo Signals)

Burst stereo signals are needed, for example, in multichannel mixing consoles in recording studios for transmitting audio signals between modules.
Audio Analyzer UPD is able to generate multiplexed signals of this type. Same as for the signals described in section 6 ("Single-Channel Burst Signals with any Burst-to-Interval Ratio"), an external circuit must be connected to UPD.

The following input signals are needed:

- System clock (bit clock) for outputting the data bits. The system clock frequency must be twice that for single-channel signal transmission in order to obtain the same data word transmission rate, since the data words for two channels must now be transmitted in the same time available for one channel.
- Word clock, whose rising edge defines the start of the data words.
- The bit clock and the word clock must be in sync.

7.1. Design of External Circuit

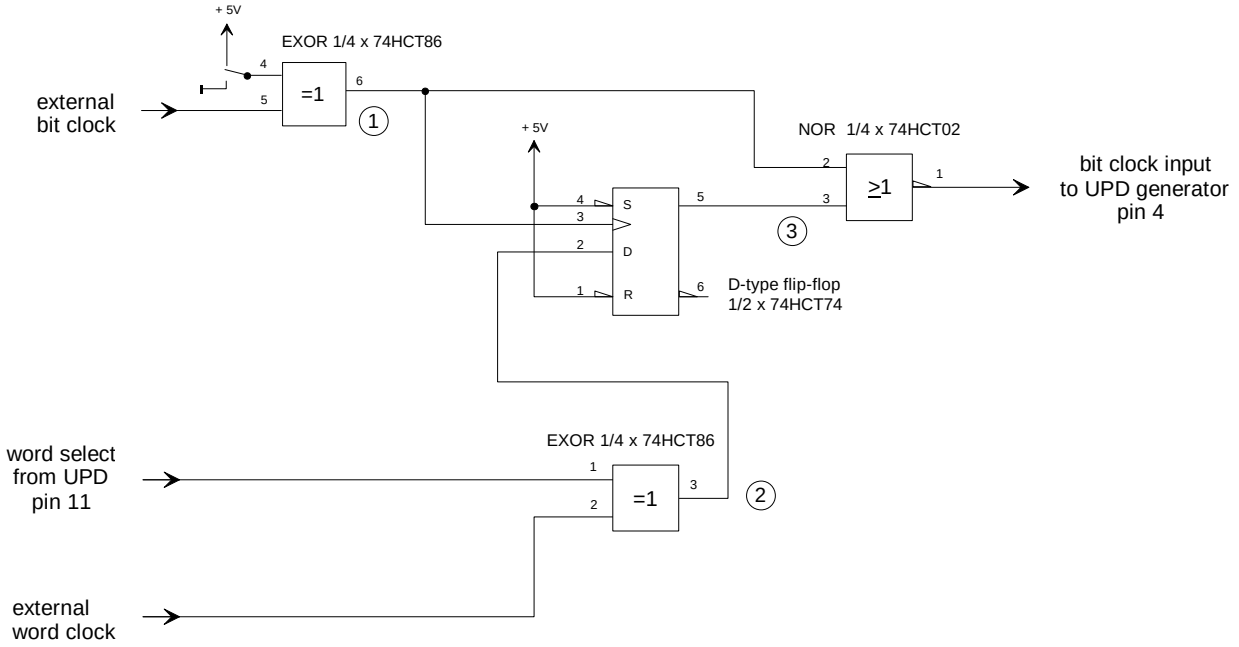

Fig. 6: External circuit connected to UPD for generating dual-channel multiplexed burst signals

In this case, too, any 5V TTL logic components can be used. Components are the same as for the circuit described in section 6. Connection to UPD and to the power supply is also as described in this section.

The word clock for dual-channel multiplexed signals is always a symmetrical rectangular signal transmitting one audio channel during each half-wave. Since this applies both to the external signal and to the word select signal generated by UPD, the external circuit can have a very simple design. The circuit section for synchronizing the external word clock with the UPD word sync required in the circuit described above can be omitted completely here.

7.2. Operation of External Circuit for Synchronization of UPD

Figure 7 shows the timing diagram for the external circuit. For the sake of clarity, data bursts with only 4 bits per data word are shown. These cannot be generated by UPD, but the operating principle of the circuit can be explained just as well using this type of burst.

Function of EXOR gate at bit clock input:

To ensure well-defined switching states, the rising edge of the word clock must be transmitted on the falling edge of the bit clock. If this is not possible because of the application's circuit design, the bit clock signal can be inverted by means of the EXOR gate by connecting pin 4 to +5 V. If connected differently, the clock signal passes through the gate unchanged, so the gate is actually not needed.

Synchronization with word select signal from UPD

The EXOR gate compares the external word clock signal with the word select signal from UPD. If the signals are equal, the output of gate is low, and a clock signal is output to UPD via the NOR gate as shown above in the diagram in Figure 7. When the external word clock signal is switched over, the next rising edge of the external clock signal on line ① causes a high signal to be connected through to the output of flip-flop . The NOR gate is disabled and because there is now no more clock signal output to UPD the state of the output lines does not change anymore. In the example shown, UPD stops after data bit 3 is output.
When the external word clock signal is switched over again, the clock signal for UPD is re-enabled, and data bit 4 in channel B is output. Bit 4 is the last of the data bits set with *Wordlength = 4* in the UPD generator panel, and UPD switches the word select line to high for the subsequent output of channel A. This however interrupts the bit clock signal at the output of the NOR gate again because the channel coding of the external word clock signal does not correspond to that of UPD. There is no further data output.

Output of first synchronized data burst

The external word clock signal switches to channel A. The channel coding of the external word clock signal therefore corresponds to that of UPD. The next rising edge of the external clock signal on line ① switches the output of flip flop to low, the NOR gate outputs the clock signal, and UPD outputs the first data bit for channel A. Three further data bits follow, and when the word length set in the generator panel is reached, the word select signal is switched to channel B. Data output is interrupted until the external word clock signal too goes low. UPD outputs four data bits for channel B, the first burst for the two channels is then completed.

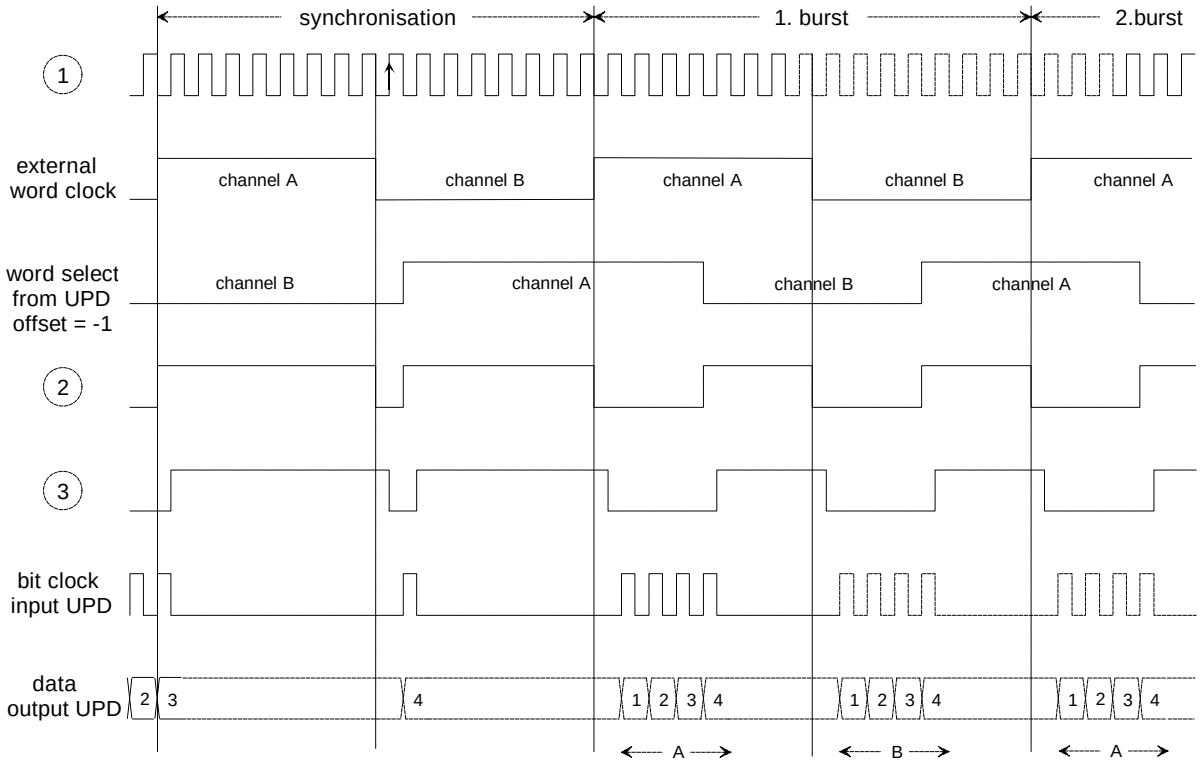

Fig. 7: Timing diagram for the generation of dual-channel multiplexed data bursts

7.3. Settings on Audio Analyzer UPD

To generate stereo signal bursts, the following settings are required for the UPD generator:

Channel(s)	***2 º 1***, for generating in-phase audio signals
Output	***SERIAL MUX***
Sync To	***EXTERN***
Sample Frq	The **sampling frequency** for calculating the audio samples is to be entered; the sampling frequency is equal to the external word clock frequency.
Wordlength	The **desired word length** is to be entered.
Audio Bits	The **number of audio bits** usually equals the word length. If the burst length is not divisible by 8, the desired number of bits is to be entered and *Wordlength* is to be set to the next higher value.
Wordoffset	The **word offset must always be set to *-1*** for this type of circuit since otherwise the start of a word would be shifted into the next or previous burst and the data word would thus be distributed over two bursts. The generated data signal is in this case output with a word offset of 0.
WordselCh1	***HIGH*** if a timing as shown above is to be obtained. If the negative half-wave of the external word clock signal is assigned to channel A, ***LOW*** is to be selected.
Bitclock	***RISING*** if a timing as shown in Fig.7 is to be obtained. ***FALLING*** if the data words are to be output on the falling edge of the clock signal applied to UPD.
Bit Order	***MSB FIRST*** will be appropriate for most applications.

8. Analysis of Burst Digital Audio Signals

To analyze burst digital audio data streams, the DUT is connected to the serial DSUB connector of Audio Analyzer UPD as shown in the figure below.

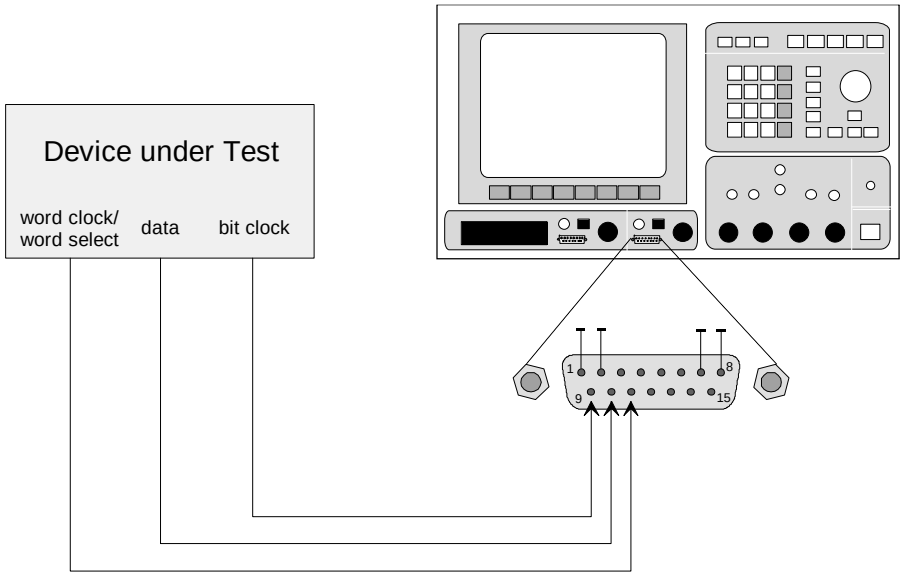

Fig. 8: Connection of DUT to Audio Analyzer UPD

8.1. Settings on Audio Analyzer UPD

The data analyzer of UPD is always operated with the clock signal physically applied. It does not matter if a continuous clock signal or a burst clock signal as described in this application note is applied. UPD therefore does not require any additional circuits in this mode.

The settings required for the analyzer section largely correspond to those of the generator.
The following settings must be made:

Selection of analyzer, *ANALYZER* menu line

The three analyzers of UPD -*DIG 48kHz*, *DIG 192kHz* and *DIG 768kHz* - differ in the maximum word clock frequency they can handle. Analyzer *DIG 768kHz* is not able to process multiplexed signals. Applications for burst audio data seldom use sampling rates above 48 kHz. The setting ***DIG 48kHz*** should therefore be appropriate in most cases.

Setting of *Meas Mode* (measurement mode)

Audio Analyzer UPD can measure various signal parameters. To analyze audio signals, ***AUDIO DATA*** is to be selected.

Setting of lower frequency limit, *Min Freq* menu line

Depending on the analyzer selected, a lower frequency limit of 2 Hz, 10 Hz and 100 Hz can be selected. For the measurement speeds "AUTO" or "AUTOFAST", the speed will increase as the frequency limit is increased.
Usually, ***10 Hz*** will be selected here.

Selection of audio channels, *Channel(s)* menu line

This menu line determines if measurements are to be made on channel 1, channel 2 or on both audio channels. For single-channel signals as described in section 6, ***1*** is to be set; for stereo signals as described in section 7, ***BOTH*** is to be set.

Selection of input interface, *Input* menu line

SERIAL or ***SERIAL MUX*** is to be selected depending on whether single-channel or dual-channel multiplexed data streams are to be analyzed.

Setting of sampling frequency, *Sample Frq* and *Oversamp* menu lines

As to the setting of the sampling frequency and the oversampling factor, the explanations given for the generator apply analogously to the analyzer.
Since the analyzer is always operated with the clock signal physically applied, the sampling rate that was used for calculating the audio data must be entered for the analyzer. If a sampling frequency that differs from the standard clock rates is to be used, this frequency must be entered under *VALUE*. If the entered frequency differs from the frequency of the signal applied, all filters and frequency measurement results will be shifted accordingly!

Definition of word length in data stream, *Wordlength* and *Audio Bits* menu lines

In the *Wordlength* line, the number of bits that make up a data sample is entered. The *Audio Bits* line specifies how many bits of the transmitted data samples are to be used for the analysis. The remaining bits are cut off.
The parameters in these two lines must be adapted to the application in hand; as a rule, they will correspond to the generator settings.

***Wordoffset* menu line**

The explanations given for the generation of data signals apply analogously.
The correct setting is ***Wordoffset*** = ***0***.
Exception: for the circuit described in section 6.4, *Wordoffset* = *1* is to be selected.

Setting of active clock edge, *Bitclock* menu line

The *Bitclock* line defines the polarity of the clock signal on which data bits are accepted. Depending on the application, ***RISING*** or ***FALLING*** is to be selected.

***Wordclock* and *WordselCh1* menu lines**

For single-channel signals, *Wordclock* is to be set to ***RISING***.
For multiplexed signals, *WordselCh1* is to be set to ***LOW*** or ***HIGH*** analogously to signal generation.

***Bit Order* menu line**

Same as for the generator, ***Bit Order*** = ***MSB FIRST*** will be appropriate for most applications.

8.2. Filters

Audio Analyzer UPD incorporates a wide variety of filters for signal analysis. The filters are digital filters, ie they are implemented with DSPs.
All filters implemented internally by UPD, are transformed using the sampling rate valid for the analyzer in question. If the sampling rate used for transformation differs from the actual clock rate (eg because a wrong value was entered), all frequency measurement results will be shifted.

All fixed filters in Audio Analyzer UPD (weighting filters) as well as all user-definable filters in UPD (highpass, lowpass filters, etc) can be used only at sampling rates >32kHz.
Data words with slower word clocks which are used in telephone applications, for example, and can be generated by the UPD data generator by means of an external synchronization circuit cannot be analyzed with the fixed filters of UPD. To analyze data words of this kind, filters for the sampling rates in question must be designed (this can be done with any filter design software) and read into UPD as a file. The procedure is described in detail in the user manual for Audio Analyzer UPD, section 2.7.2.7 "File-defined Filters".
For the 8-kHz sampling frequency, a number of filters are available. Please contact your local Rohde & Schwarz representative.

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