USB5935
User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

USB5935 data acquisition board is compatible with USB bus, may access the computer via USB cable, which constitutes the laboratory, product quality testing center, field monitoring and control, medical equipment and other fields' data acquisition, waveform analysis and processing system, it can also constitute the industrial production process control monitoring system. And it has a small size, plug-and-play characteristics, so it is the best choice for portable system.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- USB5935 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

AD analog input

- Input Range: ±10V, ±5V, ±2.5, 0~10V
- 12-bit resolution, the13 bit is the sign bit
- AD Inversion Frequency: 500KS/s
- Number of Channels: 16SE/8DI
- Data Read Mode: software query mode
- Analog Input impedance: 10 MΩ
- Programmable amplifier type: AD8251(default), compatible AD8250, AD8253
- Amplifier Set-up Time: 785nS(0.001%)(max)
- Non-linear error: ±1LSB(Maximum)
- System Measurement Accuracy: 0.1%
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: −20℃~70℃

DI digital input

- Channel No.: 6-channel
- Electric Standard: TTL compatible
- Maximum sink current: <0.5V
- High Level: ≧2V
- Low Level: ≦0.8V

DO digital output

- Channel No.: 6-channel

- Electrical Standard: TTL compatible
- High Level: ≧2.4V
- Low Level: ≦0.5V
- Power-on output: low level

CNT Counter/timer

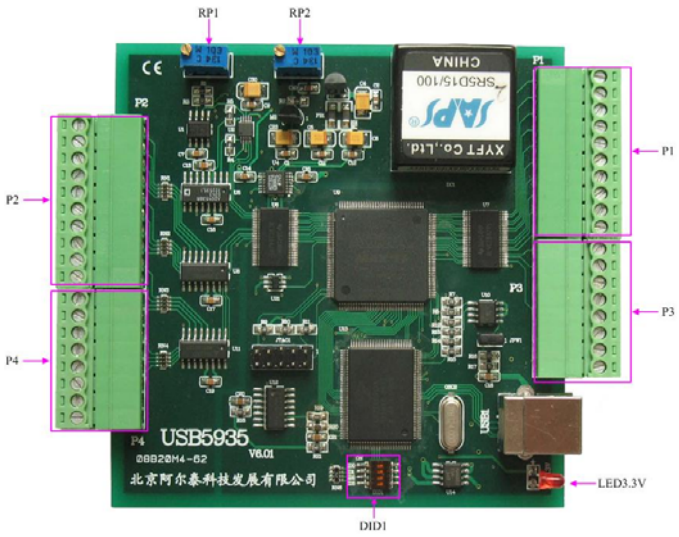
- Tiptop timebase is20 MHz, 24-bit counter/timer
- Function Mode: counter and pulse generator
- Clock Source: local clock (620Hz~20MHz), external clock(maximum count clock frequency 20MHz)
- Gate: rising edge, falling edge, high level, low level
- Pulse generator output: pulse mode and duty cycle set waveform mode

Other features

Board Clock Oscillation: 10MHz

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Components Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

P2, P4: analog signal input connectors
P1, P3: digital signal input/output and counter input/output connectors

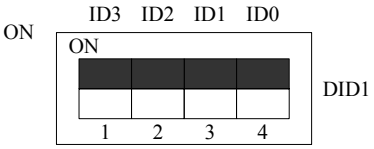
2.2.2 Potentiometer

RP1: Analog signal input zero-point adjustment potentiometer
RP2: Analog signal input full-scale adjustment potentiometer

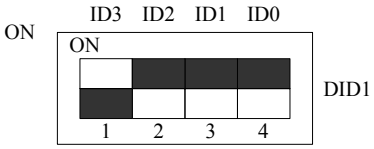
2.2.3 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one USB5935 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-place numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: place "ID3" is the high place."ID0" is the low place, and the black part in the diagram represents the location of the switch. (Test softwares of the company often use the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible. As for the differences between logic ID and physical ID, please refer to the function explanations of "CreateDevice" and

"CreateDeviceEx" of ***The Prototype Explanation of Device Object Management Function*** in ***USB5935S*** software specification).



The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	物理ID（Hex）	物理ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

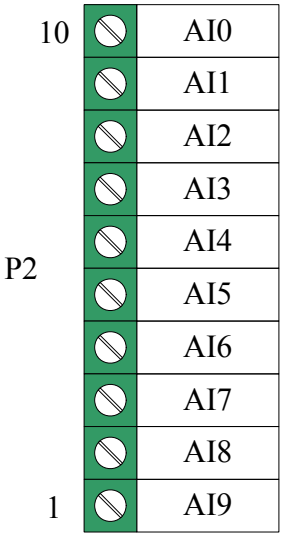
2.2.4 Status indicator

LED3.3V: 3.3V power indicator, on for normal condition.

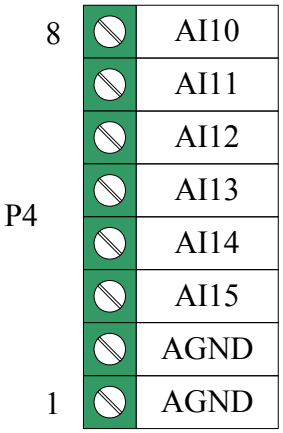
Chapter 3 Signal Connectors

3.1 The Definition of Signal Input Connectors

Pin definition of P2



Pin definition of P4

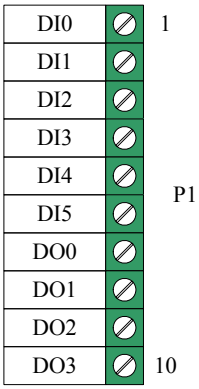


Pin definition about analog inputs

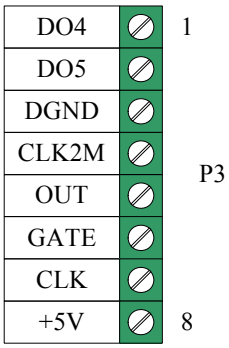
Pin name	Pin feature	Pin function definition
AI0-AI15	Input	Analog input pins
AGAN	GND	Analog signals ground

3.2 The Definition of Digital Signal Connectors

Pin definition of P1



Pin definition of P3



Pin definition

Pin name	Type	Pin function definition
DI0~DI5	Input	Digital input, reference ground is DGND.
DO0～DO5	Output	Digital output.
+5V	Output	Output 5V voltage.
CLK2M	Output	On-board 2.5MHz clock oscillator pulse output, output cycle 0.4 microseconds, provides the clock source signal for CLK
CLK	Input	Timer/counter clock source input, reference ground is DGND. When use external clock as counter clock, the clock frequency not exceeding 20MHz. The default counter clock is internal clock- CLKOUT, frequency range: 620Hz~20MHz.
GATE	Input	Timer/counter gate input, reference ground is DGND.
OUT	Output	Timer/Counter output, only clock output is forbidden, it is counter output, if it is not forbidden, it is AD clock output CLKOUT. The default is counter output, reference ground is DGND.
DGND		Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.

Chapter 4 Connection Ways for Each Signal

4.1 Analog Input Connection Mode

4.1.1 Single-ended Input Connection Mode

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

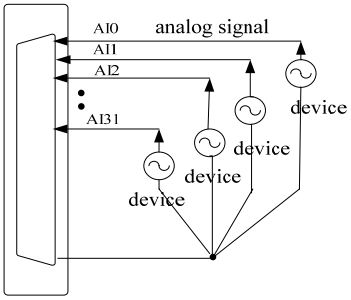


Figure 4.1.1 single-ended input connection

4.1.2 Differential Input Connection Mode

Differential input mode uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB5935 software manual.

According to the diagram below, USB5935 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 16-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with USB5935 board.

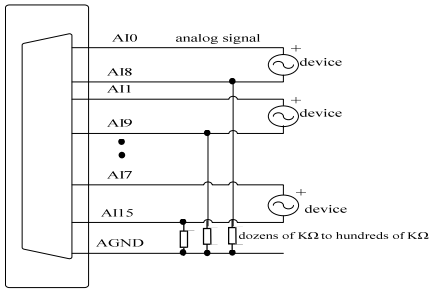
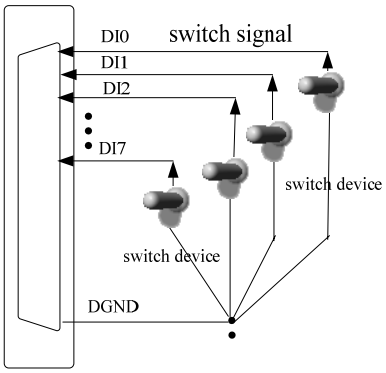
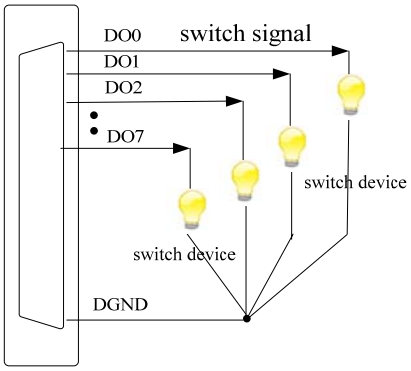


Figure 4.1.2 double-ended input connection

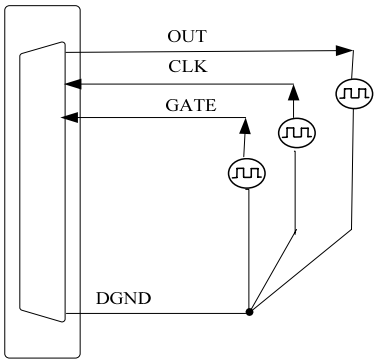
4.2 Digital Input Connection



4.3 Digital Output Connection



4.4 Counter/Timer Connection



Chapter 5 Timer/Counter Function

5.1 Overview

The counter/timer of USB5935 is designed to meet the counting and timing requirements, which has the functions that other common and off-the-shelf counter/timer devices could not reach. Counter/timer devices provide a wide range of solutions for measurement, including measuring a number of time-related variables, event count or the cumulative plus. The counter/timer of USB5935 is a 16-bit counter, which is usually used as the component to perform key timing and synchronization functions in the complicated measurement system. According to work mode, it can be divided into timing pulse generator and counter mode, and the counter mode includes the simple counter and the buffer counter. Under the counter mode, we define the buffer count prohibition as the simple count and the buffer count permission as the buffer count. Each model will have a variety of options for the gate controlling, and they are adapted to the following aspects:

- ✧ Frequency measurement
- ✧ Edge or event count (the cumulative plus)
- ✧ Condition count
- ✧ Pulse width measurement
- ✧ Time tagging of events
- ✧ Frequency generation
- ✧ Pulse sequence generation and pulse width modulation (PWM)

The OUT output of the counter keeps the low level when power is on again. In terms of their needs, users can change "the level direction of counter output" (the software parameter OutputDir) to select that it is the low level or the high level when the counter stops count. The default setting is the low level when the counter stops count.

Please note the CLK, GATE and OUT that mentioned in this chapter which belong to the corresponding pin of the connector CN1, and for the specific definition, please refer to the chapter "Signal Input and Output Connectors".

The gate controlling edge of this counter is captured by an oscillation of 40M.

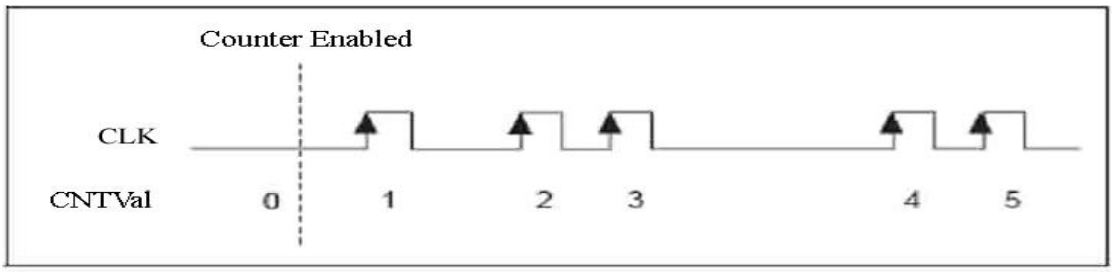
5.2 Count mode

Under the counter function mode, the OUT output in the way of working has the same rule: each time after count, the counter adds "1". When the count value reaches 16777216, the overflow happens, and the overflow symbol is "1". Users can select the "stop count" or the "keep count" after the overflow. When you choose the "stop count", the count value keeps 16777216 after the overflow, and the OUT output of the counter maintains high level; when you choose the "keep count", the counter starts to count from the initial number adding "1" each time after the overflow, and the OUT output is the high level, but for the second overflow, the OUT output is the low level, and so is the following count mode. The default count mode is the "stop count".

The initial count value is controlled by CNTVal parameters, the buffer count number is stored by Width Val under the buffer count, and the setting of this parameter is achieved by the function SetDeviceCNT.

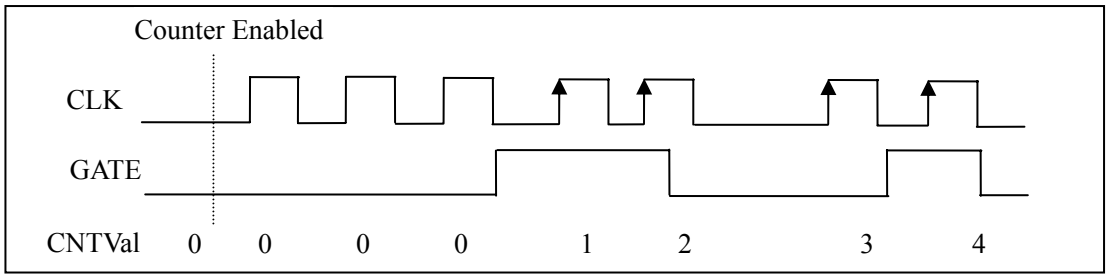
5.2.1 The functions of simple count and time measurement

Mode 0: do not use gate controlling signal



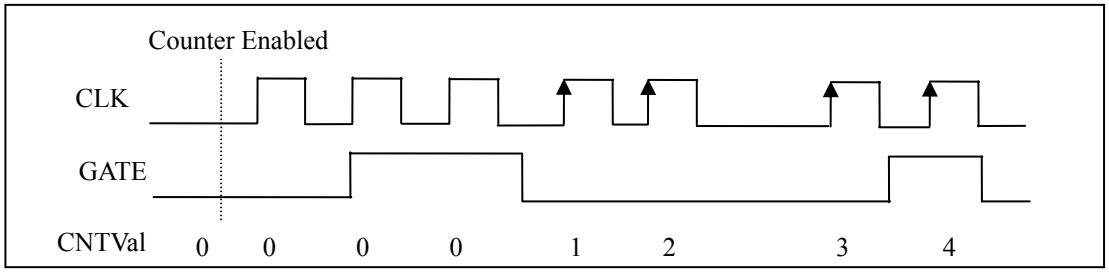
After the user writes the initial number and the count is allowed, the counter starts to increase from the initial number adding "1" each time if CLK generates a rising edge, and so is the following count mode.

Mode 1: The count is triggered on the rising edge of GATE and the following edges are invalid.



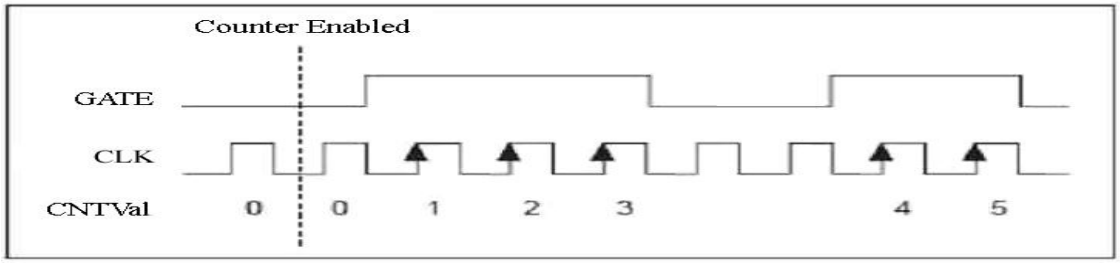
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK only when GATE changes from the low level to the high level and also it means GATE produces a rising edge, and the change of the follow-up GATE is invalid, and so is the following count mode. Under this mode, it is equivalent to use the first rising edge of GATE as the counter's startup signal.

Mode 2: The count is triggered on the falling edge of GATE and the following edges are invalid.



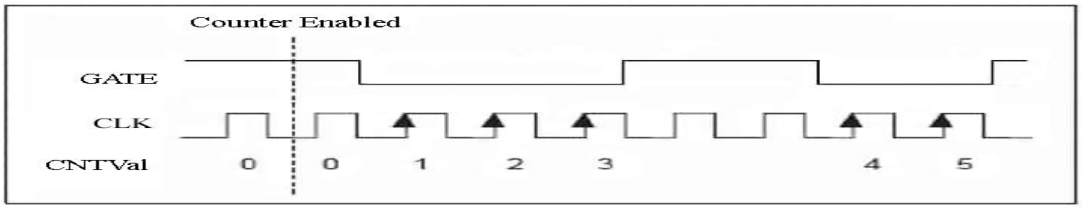
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the falling edge of the CLK only when GATE changes from the high level to the low level and also it means GATE produces a falling edge, and the change of the follow-up GATE is invalid, and so is the following count mode. Under this mode, it is equivalent to use the first falling edge of GATE as the counter's startup signal.

Mode 3: The high level is valid.



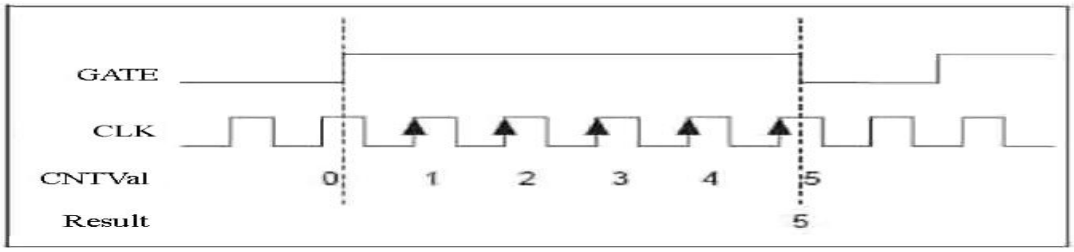
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE is the high level, and when GATE is the low level, the counter stop count and the count value remain unchanged. If GATE turns to be the high level again, the counter starts to count from the former value adding "1" each time, and so is the following count mode. This function is suitable for the unilateral-condition count.

Mode 4: The low level is valid.



After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE is the low level, and when GATE is the high level, the counter stop count and the count value remain unchanged. If GATE turns to be the low level again, the counter starts to count from the former value adding "1" each time, and so is the following count mode. This function is suitable for the unilateral-condition count.

Mode 5: the trigger count on the rising edge and the stop count on the falling edge

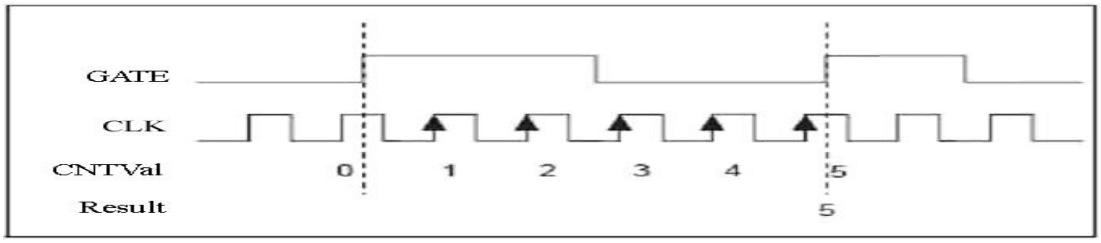


After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the rising edge, and the count stops until the GATE generates the falling edge. The change of the follow-up GATE is invalid. This function is suitable for positive pulse width measurement.

Mode 6: the trigger count on the falling edge and the stop count on the rising edge

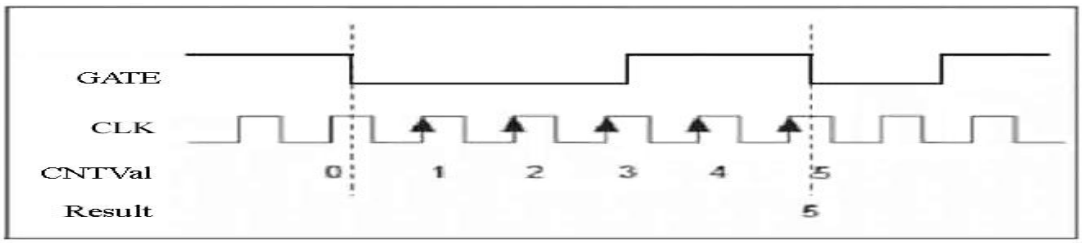
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the falling edge, and the count stops until the GATE generates the rising edge. The change of the follow-up GATE is invalid. This function is suitable for negative pulse width measurement. The measured signal should be connected to the GATE pin of the CN1, and the clock benchmark signal can be input from the CLK pin of the CN1 (You can also choose the LOCAL_CLK). When the counter does not overflow, we suggest that the high clock benchmark should be used as much as possible in order to improve the measurement precision.

Mode 7: the trigger count on the rising edge and the stop count on the next rising edge



After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the rising edge, and the count stops until the GATE generates the next rising edge. The change of the follow-up GATE is invalid. This function is suitable for the whole cycle of the pulse width measurement.

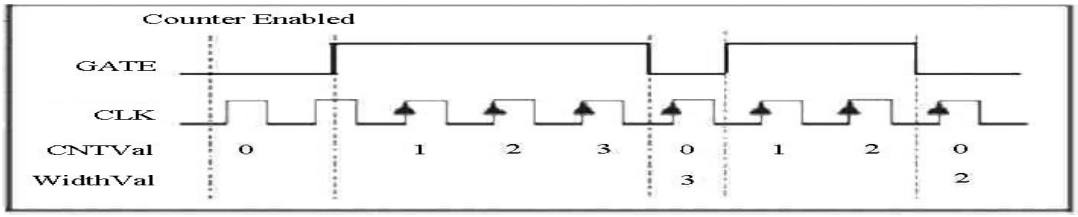
Mode 8: the trigger count on the falling edge and the stop count on the next falling edge



After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the falling edge, and the count stops until the GATE generates the next falling edge. The change of the follow-up GATE is invalid. This function is suitable for the whole cycle of the pulse width measurement.

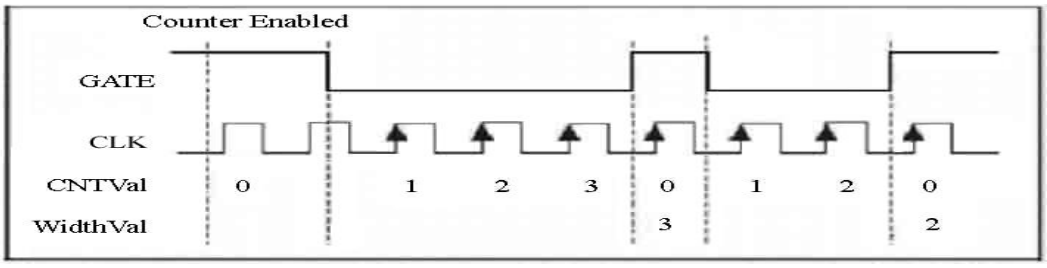
5.2.2 The functions of buffer count and time measurement

Mode 3: The high level is valid.



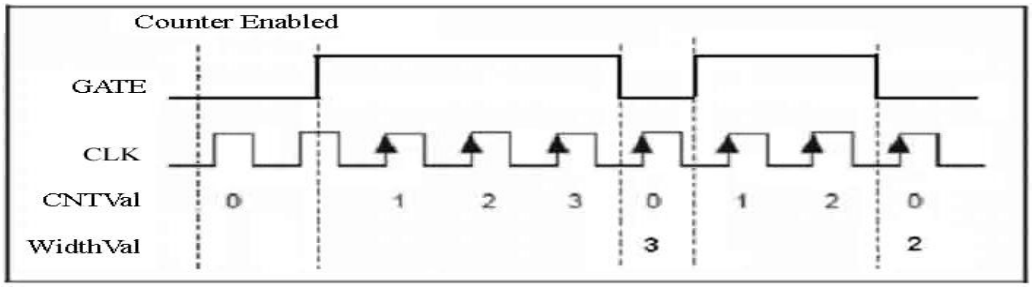
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE is the high level, and when GATE turns to be the low level, the counter latches the count value to the buffer register for the user to read out, and at the same time to clear numerical terms. When GATE turns to be the high level again, the counter starts to count from 0 adding "1" each time, when GATE turns to be the low level, the counter latches the count value to the buffer register, and so is the following count mode.

Mode 4: The low level is valid.



After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE is the low level, and when GATE turns to be the high level, the counter latches the count value to the buffer register for the user to read out, and at the same time to clear numerical terms. When GATE turns to be the low level again, the counter starts to count from 0 adding "1" each time, when GATE turns to be the high level, the counter latches the count value to the buffer register, and so is the following count mode.

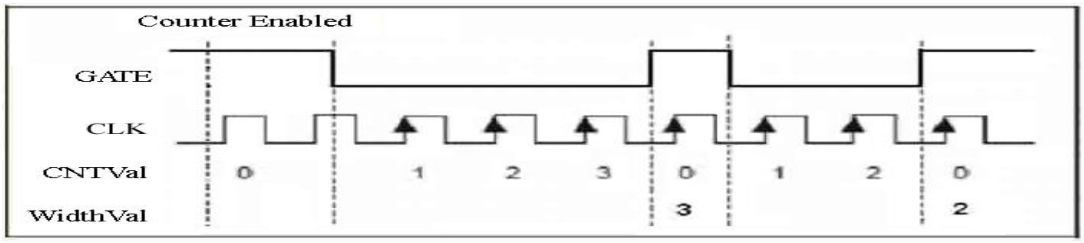
Mode 5: the trigger count on the rising edge and the stop count on the falling edge



After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the rising edge, and the counter generates the falling edge, the counter latches the count value to the buffer register for the user to read out, and at the same time to

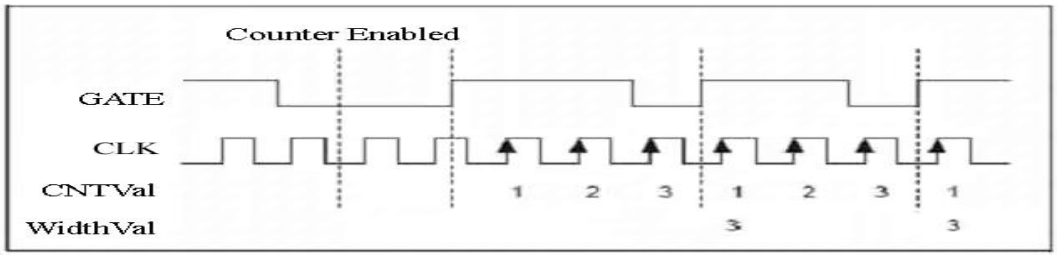
clear numerical terms. When GATE generates the rising edge again, the counter starts to count from 0 adding "1" each time, when GATE turns to generate the falling edge, the counter latches the count value to the buffer register, and so is the following count mode.

Mode 6: the trigger count on the falling edge and the stop count on the rising edge



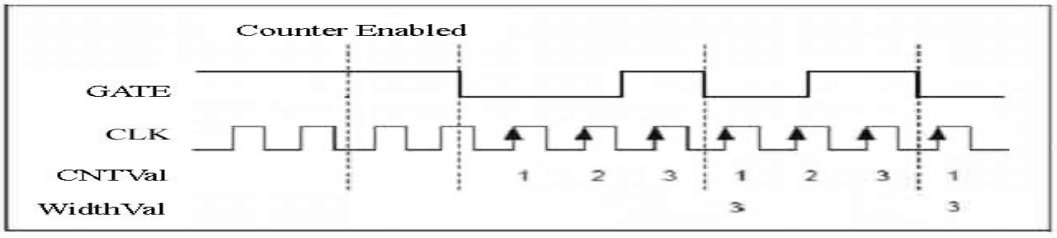
After the user writes the initial number and the count is allowed, the counter starts to count from the initial number adding "1" each time on the rising edge of the CLK when GATE generates the falling edge, and the counter generates the rising edge, the counter latches the count value to the buffer register for the user to read out, and at the same time to clear numerical terms. When GATE generates the falling edge again, the counter starts to count from 0 adding "1" each time, when GATE turns to generate the rising edge, the counter latches the count value to the buffer register, and so is the following count mode.

Mode 7: the trigger count on the rising edge and the stop count on the next rising edge



After the user writes the initial number and the count is allowed, the counter starts to count from 0 adding "1" each time on the rising edge of the CLK when GATE generates the rising edge, and when the counter generates the rising edge again, the counter latches the count value to the buffer register for the user to read out, and at the same time the counter starts to count from 0; When GATE generates the rising edge again, the counter latches the count value to the buffer register again, and at the same time the counter starts to count from 0 again, and so is the following count mode.

Mode 8: the trigger count on the falling edge and the stop count on the next falling edge



After the user writes the initial number and the count is allowed, the counter starts to count from 0 adding "1" each time on the rising edge of the CLK when GATE generates the falling edge, and when the counter generates the falling edge again, the counter latches the count value to the buffer register for the user to read out, and at the same time the counter starts to count from 0; When GATE generates the falling edge again, the counter latches the count value to the buffer

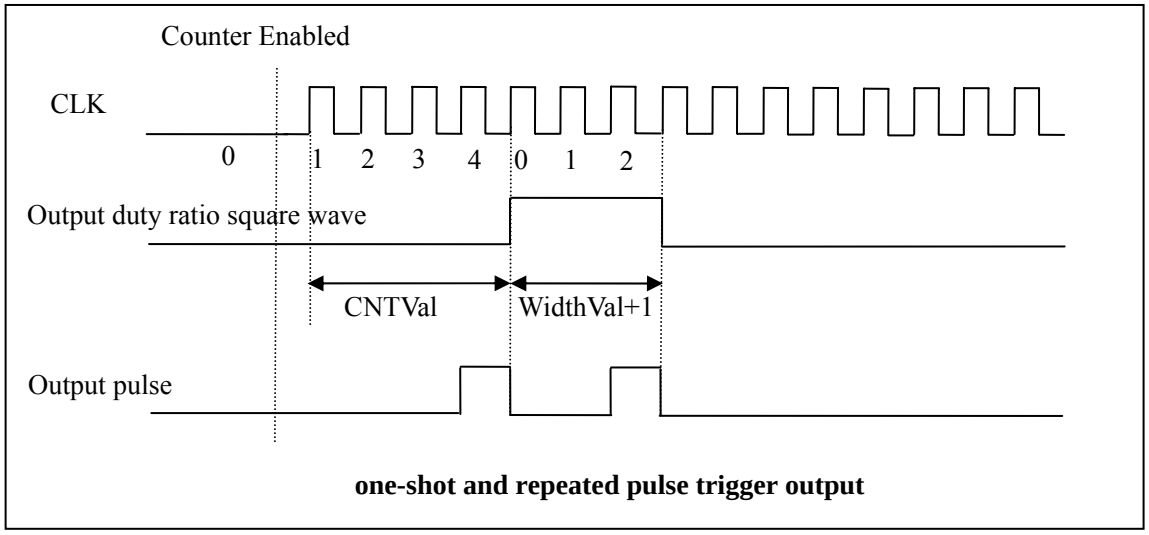
register again, and at the same time the counter starts to count from 0 again, and so is the following count mode.

5.3 Pulse Generator Method

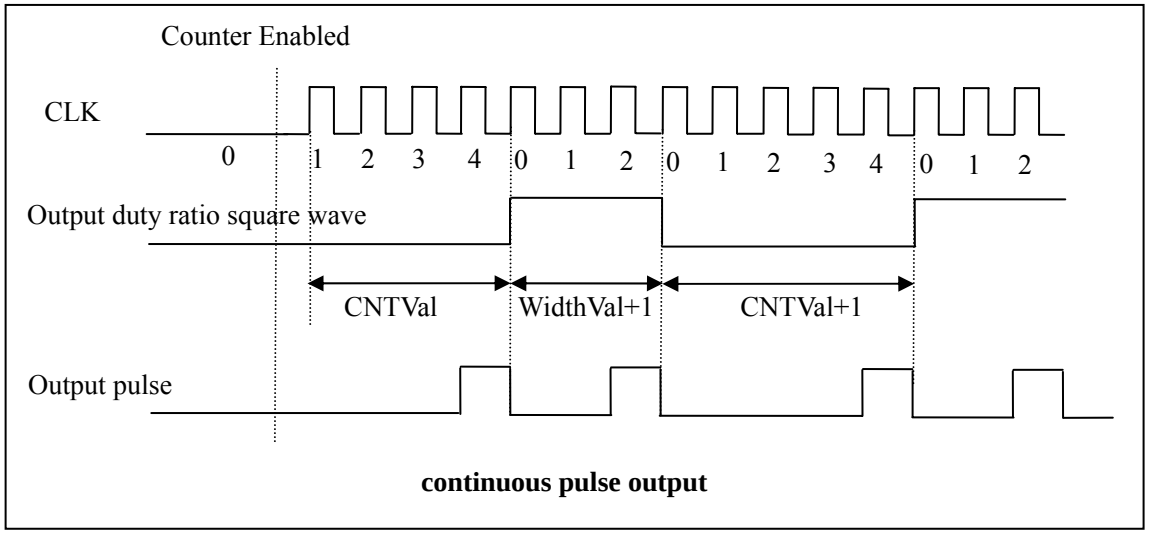
5.3.1The Output Types of the Pulse Generator

Under the pulse generator mode, the output types of OUT can be divided into the duty cycle square wave and the pulse. It needs to set two numerical numbers: initial count value (CNTVal) and pulse width (WidthVal). Initial count (CNTVal) can set the duration of low-level output; pulse width (WidthVal) can set the duration of high-level output. Each count time benchmark is decided by the CLK pulse cycle. The two parameters are set by the SetDeviceCNT in the software. The pulse generator outputs can be divided into one-shot trigger pulse output (mode 0 ~ 2), repeated trigger pulse output (mode 3 ~ 4) and continuous pulse train output (mode 5 ~ 8).

The designed initial count value (CNTVal) = 4, the designed pulse width (WidthVal) = 2



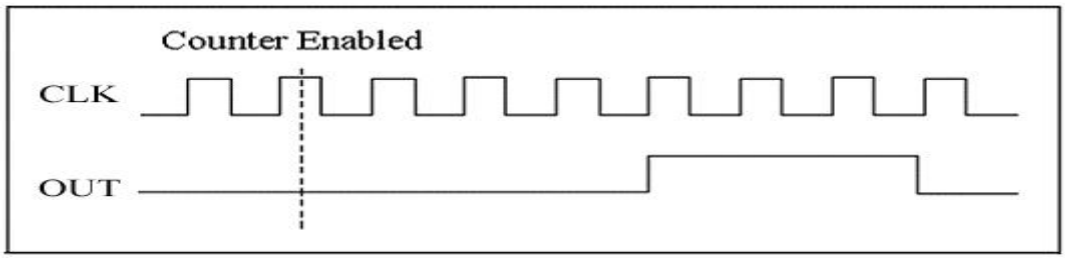
one-shot and repeated pulse trigger output



continuous pulse output

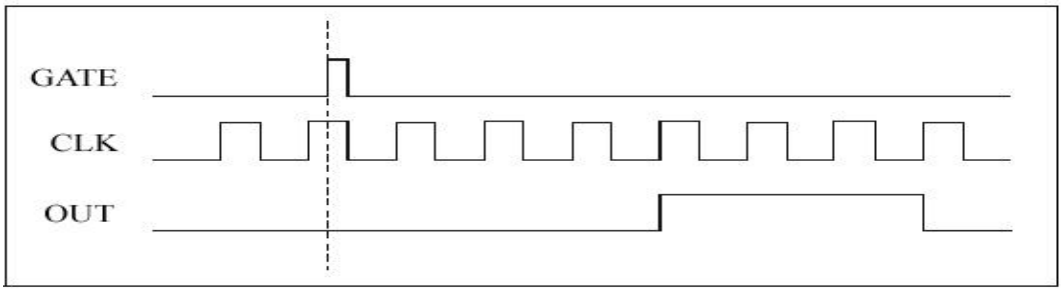
5.3.2 Functions of the Pulse Generator

Mode 0: Do not use the one-shot pulse generation of the GATE.



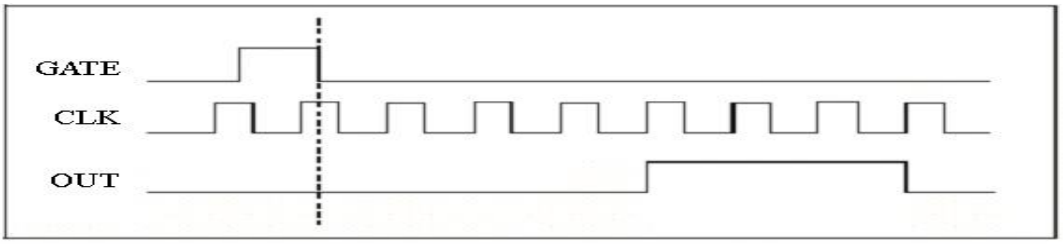
After the user writes the appointed initial count value and pulse width, and the count is allowed, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, the output keeps the low level. The mode is equivalent to start the occurrence of one pulse, which is started by users' software.

Mode 1: the one-shot pulse generation of the rising edge of GATE



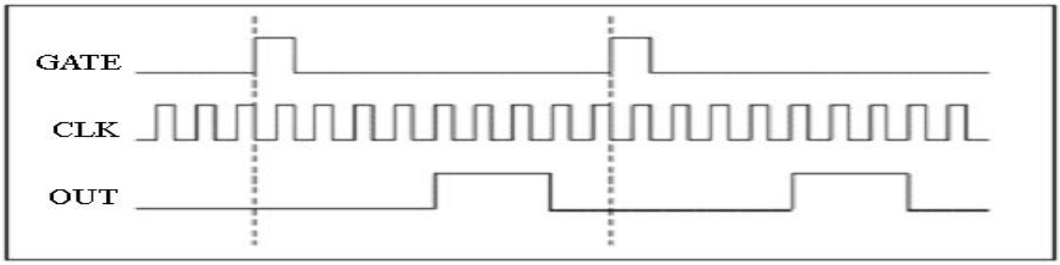
After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a rising edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, the output keeps the low level. In this process, other edges of GATE are invalid, so are the following edges. The mode is equivalent to start the occurrence of one pulse, which is started by the rising edge of an external hardware.

Mode 2：the one-shot trigger pulse generation of the falling edge of GATE



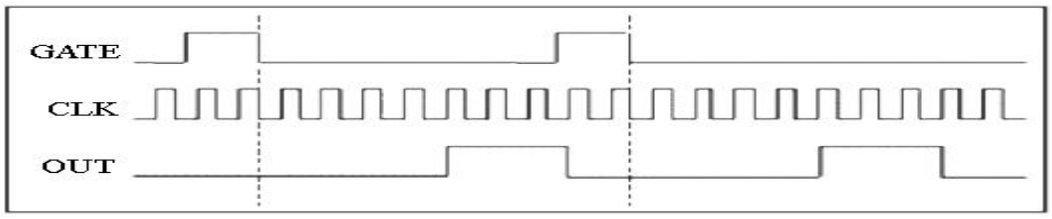
After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a falling edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, the output keeps the low level. In this process, other edges of GATE are invalid, so are the following edges. The mode is equivalent to start the occurrence of one pulse, which is started by the falling edge of an external hardware.

Mode 3：the repeated trigger pulse generation of the rising edge of GATE



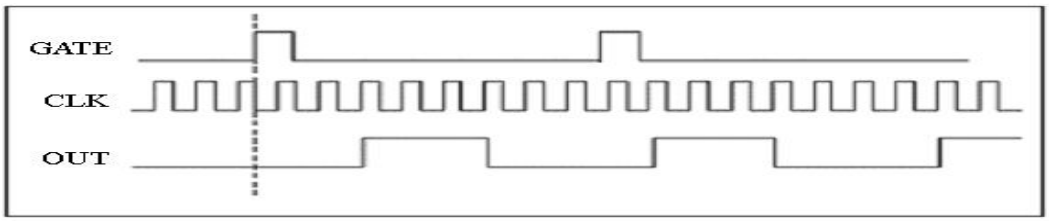
This mode is similar to Mode 1, but the process is repeatedly controlled by GATE. After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a rising edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, the output keeps the low level. In this process, other edges of GATE are invalid, so are the following edges. The mode is equivalent to start the occurrence of one pulse, which is repeatedly started by the rising edge of an external hardware.

Mode 4：the repeated trigger pulse generation of the falling edge of GATE



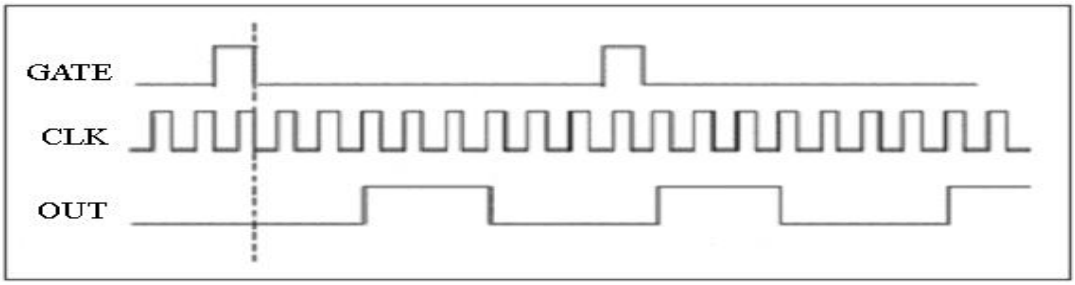
This mode is similar to Mode 4, but the process is repeatedly controlled by GATE. After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a falling edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, the output keeps the low level. In this process, other edges of GATE are invalid, so are the following edges. The mode is equivalent to start the occurrence of one pulse, which is repeatedly started by the falling edge of an external hardware.

Mode 5: the one-shot trigger continuous pulse train generator of the rising edge of GATE



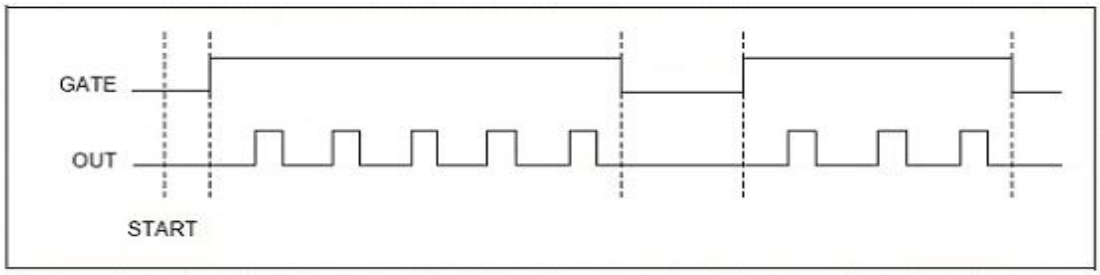
After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a rising edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, it turns into a delay progress of the low level, and then generates a continuous designated frequency and duty ratiopulse train. The mode is equivalent to start the following continuous pulse generation, which is started by the first rising edge of an external hardware.

Mode 6: the one-shot trigger continuous pulse train generator of the falling edge of GATE.



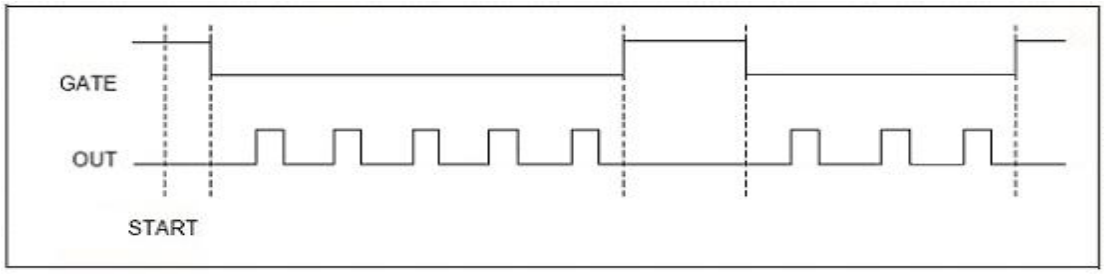
After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE has a falling edge, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, it turns into a delay progress of the low level, and then generates a continuous designated frequency and duty ratiopulse train. The mode is equivalent to start the following continuous pulse generation, which is started by the first falling edge of an external hardware.

Mode 7: GATE high level permitted continuous pulse train generator



After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE is a high level, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, it turns into a delay progress of the low level, and then generates a continuous designated frequency and duty ratiopulse train. When GATE is low level, then the OUT output immediately resets to the initial state. If GATE turns into high level again, then OUT continues to output. The mode is equivalent to start the continuous pulse output which is started by the rising edge of an external hardware and also unilateral high level keeps the pulse output state.

Mode 8: GATE low level permitted continuous pulse train generator



After the user writes the appointed initial count value and pulse width, and the count is allowed, when GATE is a low level, the OUT output of the generator will turn into a delay progress of the low level. The delay time is decided by the initial count value parameter written by the users. After the delay finishes, it will output a high level. The high level delay time is decided by the pulse width written by the users. Later, it turns into a delay progress of the low level, and then generates a continuous designated frequency and duty ratiopulse train. When GATE is high level, then the OUT output immediately resets to the initial state. If GATE turns into low level again, then OUT continues to output. The mode is equivalent to start the continuous pulse output which is started by the rising edge of an external hardware and also unilateral low level keeps the pulse output state.

Chapter 6 Notes, Calibration and Warranty Policy

6.1 Notes

In our products' packing, user can find a user manual, a USB5935 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB5935, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB5935 module.

6.2 Analog Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. USB5935 default input range: ±10V, in the manual, we introduce how to calibrate USB5935 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB5935 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9999.69mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 9999.69mV or about 9999.69mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

6.3 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:
- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.