XEM6310MT User's Manual

A compact (60mm x 75mm) integration board featuring the transceiver-capable Xilinx Spartan-6 LXT FPGA, SuperSpeed USB 3.0, on-board DDR2 memory, and two 16 MiB Flash memories.

The XEM6310MT is a compact USB 3.0 (SuperSpeed) FPGA integration module featuring the Xilinx Spartan-6 LXT FPGA, 1 Gib (64 Mx16-bit) DDR2 SDRAM, two 128 Mib SPI Flash devices, high-efficiency switching power supplies, and three high-density 0.5-mm expansion connectors. The USB 3.0 SuperSpeed interface provides fast configuration downloads and PC-FPGA communication as well as easy access with our popular FrontPanel application and SDK. Two low-jitter 100 MHz crystal oscillators are attached to the FPGA for fabric and transceiver clocking.

Revision History:

Date	Description
20130620	Initial release.
20130906	Update Quick Reference with V_{BATT} and R_{FUSE} connections and fixed incorrect mappings for JP2 pins 73 and 75.
20131204	Add power distribution diagram.
20140402	Added remarks about Pins reference.
20141216	Fixed FBx markings in the power distribution block diagram.
20150303	Added additional information about Pins.

Contents

Introducing the XEM6310MT

The XEM6310MT is a compact FPGA board featuring the Xilinx Spartan-6 FPGA and Super-Speed USB 3.0 connectivity via a USB 3.0 Micro-B receptacle. Designed as a full-featured integration system, the XEM6310MT provides access to over 120 I/O pins on its 484-pin Spartan-6 device, in addition to two dual transceiver tiles, and has a 128-MiByte DDR2 SDRAM available to the FPGA. Two SPI Flash devices provide a total of 32 MiB of non-volatile memory, one attached to the USB microcontroller and one attached to the FPGA. Available with LX45T and LX150T FPGA densities, the XEM6310 is designed for medium- to large-sized FPGA designs with a wide variety of external interface requirements.

PCB Footprint

A mechanical drawing of the XEM6310MT is shown at the end of this manual. The PCB is 60mm x 75mm with four mounting holes (M2 metric screws) spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the XEM6310MT. The USB connector overhangs the PCB by approximately 1mm in order to accommodate mounting within an enclosure.

The XEM6310MT has two high-density 80-pin connectors and one high-density 40-pin connector on the bottom side which provide access to many FPGA pins, transceivers, power, and JTAG.

BRK6310MT Breakout Board

A simple breakout board (the BRK6310MT) is provided as an optional accessory to the XEM-6310MT. This breakout board provides DC power, JTAG connector, and easy access to the high-density connectors on the XEM6310MT by routing them to lower-density 2mm-spaced thru-holes. Additionally, 22 SMA connectors provide access ot the FPGA transceiver tiles. The

breakout board also provides a convenient reference for building boards that will mate to the XEM6310MT.

Opal Kelly reserves the right to change the form-factor and possibly pinout of the BRK6310. Therefore, unlike the XEM6310MT, it is not intended or recommended for production integration.

Full schematics and Gerber artwork files for the BRK6310MT are provided free of charge. If your application depends on the existing form-factor, you may reproduce this board from these documents.

A mechanical drawing of the BRK6310MT is also shown at the end of this document.

Functional Block Diagram
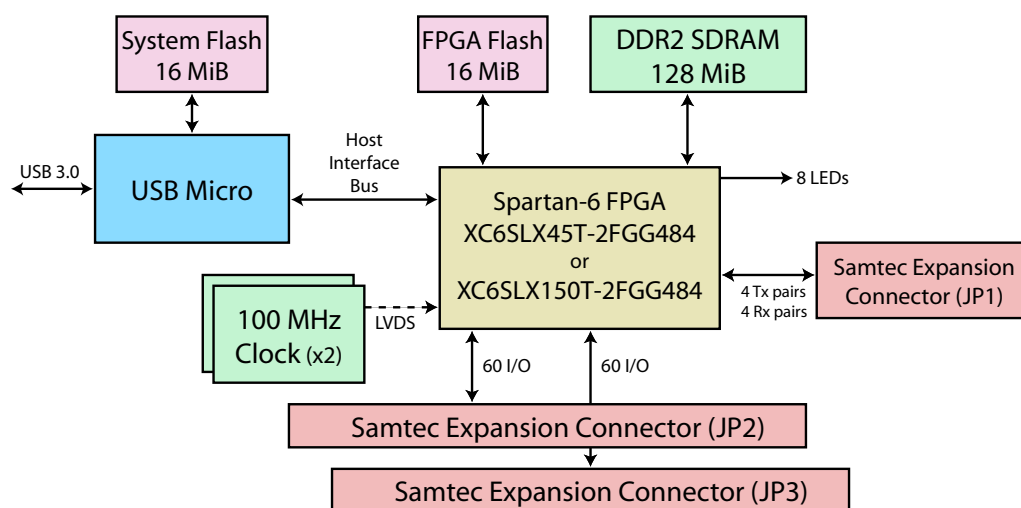
FPGA

The XEM6310MT is available in two variants. These two variants are identical except for the FPGA provided. The table below lists some of the differences between the two devices. Consult the Xilinx documentation for a more thorough comparison. Note that the -LX150T variant is limited availability and may have minimum order requirements and lead times. Please contact Opal Kelly Sales for more information.

Feature	XEM6310MT-LX45T	XEM6310MT-LX150T
FPGA	XC6SLX45T-2FGG484C	XC6SLX150T-2FGG484C
Slice Count	6,822	23,038
D Flip-Flops	54,576	184,304
Distributed RAM	401 Kib	1,355 Kib
Block RAM	2,088 Kib	4,824 Kib
DSP Slices	58	180
Clock Management Tiles	4	6
GTP Transceiver	4	4 (limited by PCB)

Power Supply

The XEM6310MT is designed to be operated from a 5-volt power source supplied through the DC power points on the device or the expansion connectors on the bottom of the device. This provides power for the three high-efficiency switching regulators on-board to provide 3.3v, 1.8v and 1.2v. Each of the three switching regulators can provide up to 2A of current.

DC Power Points

In most applications, +VDC (+4.5 to +5.5) will be delivered to the module from the expansion connector.   However, DC power points are also provided at the northwest corner of the device (from the perspective shown on the mechanical drawing). These are small vias that can be used to deliver power to the module.

SuperSpeed USB 3.0 Interface

The XEM6310MT uses a Cypress FX3 USB microcontroller to make the XEM a USB 3.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen quickly, virtual instruments under FrontPanel update quickly, and data transfers are blazingly fast.

On-board Peripherals

The XEM6310MT is designed to compactly support a large number of applications with a small number of on-board peripherals. These peripherals are listed below.

Low-Jitter Oscillator (FPGA Fabric)

A fixed-frequency, 100 MHz low-jitter oscillator is included on-board and outputs LVDS to the FPGA. The Spartan-6 FPGA can produce a wide range of clock frequencies using the on-chip DCM and PLL capabilities.

Low-Jitter Oscillator (FPGA GTP Transceivers)

A second, dedicated 100 MHz low-jitter oscillator is also provided and is connected at MGTREF-CLK0_101.

128-MByte Word-Wide DDR2 Synchronous DRAM

The module includes a 128-MiByte DDR2 SDRAM with a full 16-bit word-wide interface to the FPGA. This SDRAM is attached exclusively to the FPGA and does not share any pins with the expansion connector. The maximum clock rate of the SDRAM is 333 MHz. With the -2 speed grade of the Spartan-6, the maximum clock rate is 312.5 MHz for a supported peak memory bandwidth of 10 Gb/s.

The DDR2 SDRAM is a Micron MT47H64M16HR-3:H (or compatible).

FPGA Flash - 16 MiB Serial Flash Memory

A 128 Mib serial flash device (Numonyx N25Q128A11B1240E or equivalent) provides on-board non-volatile storage for the FPGA. This device is attached directly to the FPGA for use in your design.

System Flash - 16 MiB Serial Flash Memory

A 128 Mib serial flash device (Numonyx N25Q128A11B1240E or equivalent) provides on-board non-volatile storage accessible to the USB microcontroller. This device is used to store device firmware and configuration settings as well as other user assets such as FPGA configuration files or calibration data. Erase, read, and write functions are available at all times (with or without a configured FPGA) through the use of FrontPanel API methods.

LEDs

Eight LEDs and are available for general use as indicators.

Expansion Connectors

Two high-density, 80-pin expansion connectors are available on the bottom-side of the XEM-6310MT PCB. These expansion connectors provide user access to several power rails on the XEM6310MT, the JTAG interface on the FPGA, and 122 exclusive I/O pins on the FPGA, including several GCLK inputs.

The general purpose connectors on the XEM6310MT are Samtec part number QSE-040-01-H-D-A. The table below lists the appropriate Samtec mating connectors along with the total mated height.

Samtec Part Number	Mated Height
QTE-040-01-F-D-A	5.00mm (0.198")
QTE-040-02-F-D-A	8.00mm (0.316")

One high-density, 40-pin expansion connector also provides access to the transceiver signals on two GTP DUAL transceiver tiles on the FPGA. This connector is Samtec part number QSE-040-01-H-D-A. The table below lists the appropriate Samtec mating connectors along with the total mated height.

Samtec Part Number	Mated Height
QTE-020-01-F-D-A	5.00mm (0.198")
QTE-020-02-F-D-A	8.00mm (0.316")

FrontPanel Support

The XEM6310MT is fully supported by Opal Kelly's FrontPanel Application. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds tremendous value to the XEM6310MT as an experimentation or prototyping system.

Programmer's Interface

In addition to complete support within FrontPanel, the XEM6310MT is also fully supported by the FrontPanel SDK, a powerful C++ class library available to Windows, Mac OS X, QNX, and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for C#, Java, and Python making the API available under those languages as well. Sample wrappers (unsupported) are also provided for Matlab and LabVIEW.

Complete documentation and several sample programs are installed with FrontPanel.

Applying the XEM6310MT

Powering the XEM6310MT

The XEM6310MT requires that this supply be clean, filtered, and within the range of 4.5v to 5.5v. This supply must be delivered through the +VDC pins on the two device's two expansion connectors or the two pins near the northwest corner of the device.

Power Distribution System

A diagram of the power distribution system on the XEM6310MT is shown below. Details for applying this system follow throughout this document. Note that some system supply outputs are unavailable to the user.
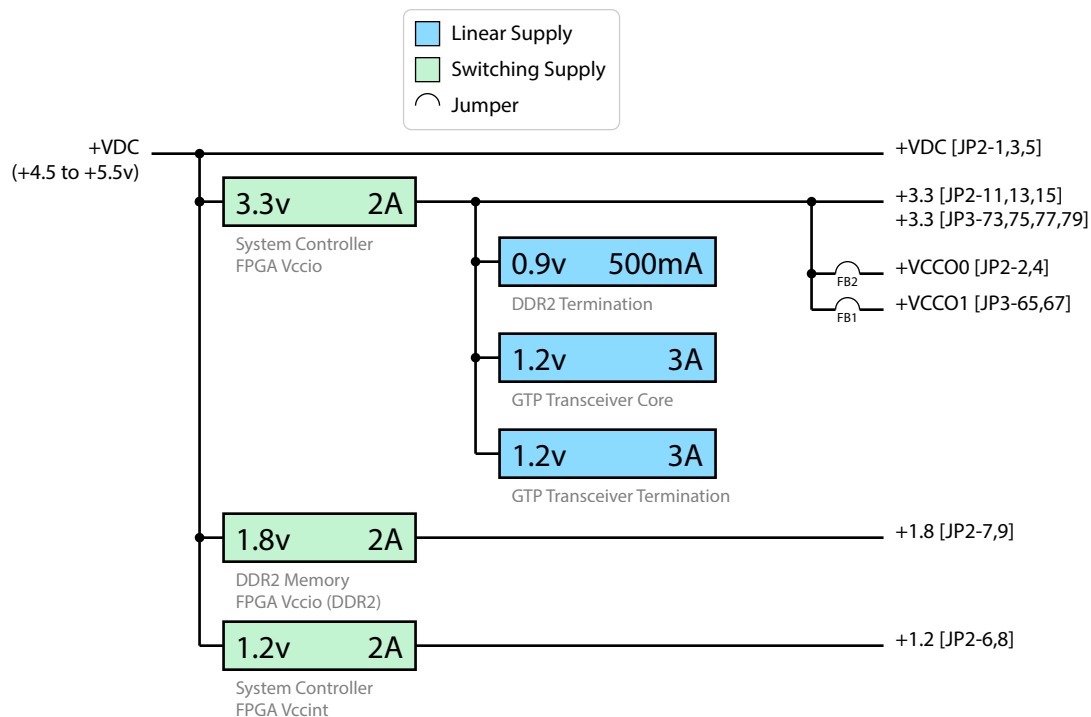
Power Budget

The table below can help you determine your power budget for each supply rail on the XEM-6310MT. All values are highly dependent on the application, speed, usage, and so on. Entries we have made are based on typical values presented in component datasheets or approximations based on Xilinx power estimator results. Shaded boxes represent unconnected rails to a particular component. Empty boxes represent data that the user must provide based on power estimates.

The user may also need to adjust parameters we have already estimated (such as FPGA V$_{CCO}$ values) where appropriate. The values provided below for MGT include four transceivers running at 2.5 Gb/s.

Component(s)	1.2v	1.8v	3.3v
100 MHz			150 mW
DDR2		600 mW	250 mW
FPGA V$_{CCINT}$			
FPGA V$_{CCAUX}$			250 mW
FPGA V$_{CCO3}$ (DDR2), est.		250 mW	
FPGA V$_{CCO2}$ (USB), est.		250 mW	
FPGA V$_{CCO0,1}$			
FPGA MGTA$_{VCC}$			911 mW
FPGA MGTA$_{VTT}$			575 mW
Total:			
Available:	2,400 mW	3,600 mW	6,600 mW

Example FPGA Power Consumption (-LX150T)

XPower Estimator version 12.3 was used to compute the following power estimates for the V$_{CINT}$ supply. These are simply estimates; your design requirements may vary considerably. The numbers below indicate approximately 70% to 80% utilization.

Component	Parameters	V$_{CCINT}$
Clock	150 MHz GCLK - 70,000 fanout	384 mW
Clock	100 MHz GCLK - 50,000 fanout	197 mW
Logic (DFF)	150 MHz, 70,000 DFFs	380 mW
Logic (DFF)	100 MHz, 50,000 DFFs	166 mW
Logic (LUT)	150 MHz, 32,000 Combinatorial, 1,000 SR, 1,000 RAM	287 mW
Logic (LUT)	100 MHz, 32,000 Combinatorial, 1,000 SR, 1,000 RAM	191 mW
BRAM	18-bit, 100 @ 150 MHz, 100 @ 100 MHz	237 mW
DSP	150 MHz, 140 slices	78 mW
MCB	150 MHz	85 mW
GTP	4 channels @ 2.5 Gb/s	188 mW
Misc.	DCM, PLL, etc.	100 mW
	Total:	2,293 mW
	Available:	2,400 mW

Supply Heat Dissipation (IMPORTANT!!)

Due to the limited area available on the small form-factor of the XEM6310MT and the density of logic provided, heat dissipation may be a concern. This depends entirely on the end application and cannot be predicted in advance by Opal Kelly. Heat sinks may be required on any of the devices on the XEM6310MT. Of primary focus should be the FPGA (U6) and SDRAM (U9). Although the switching supplies are high-efficiency, they are very compact and consume a small amount of PCB area for the current they can provide.

If you plan to put the module in an enclosure, be sure to consider heat dissipation in your design.

Host Interface

There are 41 signals that connect the on-board USB microcontroller to the FPGA. These signals comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these signals are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHost module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. Please see the sample projects included with your FrontPanel installation for examples.

Reset Profile RESET

Pin AB14 of the FPGA is an active-high RESET signal from the host interface. This signal is asserted when configuration download begins and is deasserted during the execution of the Reset Profile. For more information on the timing of this deassertion event, see the FrontPanel User's Manual.

System Flash

The Flash memory attached to the USB microcontroller stores device firmware and settings as well as user data that is accessible via the FrontPanel API. The API includes three methods for accessing this memory: `FlashEraseSector`, `FlashWrite`, and `FlashRead`. Please refer to the FrontPanel User's Manual and the FrontPanel API Reference for information about applying these methods.

Layout

The Numonyx N25Q128A11B1240E is a 16 MiB Flash memory arranged into 256 64-kiB sectors. Each sector contains 256 256-byte pages. Sectors 0...15 are reserved for device firmware and settings and are not accessible to user software. The remaining 15 MiB may be erased, written, and read using the FrontPanel API at any time even without a valid FPGA configuration. Full 64 kiB sectors must be erased at a time. However, contents may be read or written on any page address boundary.

Loading a Power-On FPGA Configuration

The user-area in System Flash may be used to store a Xilinx bitfile to configure the FPGA at power-on. Power-on configuration takes approximately 6-10 seconds from when power is applied. A full Reset Profile may also be performed after configuration.

The API is used to erase and program the power-on bitfile and the Flashloader sample is provided to perform these steps from a simple command-line utility. Source code to the Flashloader sample is included with the FrontPanel SDK.

Called with a single argument (the filename for a valid Xilinx bitfile), the Flashloader sample will erase the first sectors in the System Flash user-area, then write the bitfile. It will also setup the Boot Reset Profile to point to this area on power-on.

No Power-On Configuration

Called with no arguments, the Flashloader sample will clear the existing Boot Reset Profile. This has the effect of preventing an FPGA configuration from being loaded at power-on. This functionality may also be accomplished from the API by setting an empty `okTFPGAResetProfile` using the API `SetFPGAResetProfile`. See the *FrontPanel API Reference* for details.

FPGA Flash

The SPI Flash attached to the FPGA is a Numonyx N25Q128A11B1240E or equivalent. It provides non-volatile storage for use by the FPGA. It may not be used for FPGA configuration storage. The System Fash is used to store FPGA "boot" configurations.

The Flash / FPGA pin mappings are shown in the table below.

Flash Pin	FPGA Pin
C	AA1
$\overline{\text{S}}$	AA2
DQ0	Y3
DQ1	V3
DQ2 / $\overline{\text{W}}$	T3
DQ3 / $\overline{\text{HOLD}}$	U4

LEDs

There are eight LEDs on the XEM6310MT in addition to the power LED. Each is wired directly to the FPGA according to the pin mapping tables at the end of this document.

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA on Bank 2 with a bank I/O voltage of 1.8v. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be at logic '1'.

DDR2 SDRAM

The Micron DDR2 SDRAM is connected exclusively to the 1.8-v I/O on Bank 3 of the FPGA. The tables below list these connections.

DDR2 Pin	FPGA Pin
CK	K4
$\overline{CK}$	K3
CKE	F2
$\overline{CS}$	E3
$\overline{RAS}$	M5
$\overline{CAS}$	M4
$\overline{WE}$	H2
LDQS	N3
$\overline{LDQS}$	N1
UDQS	V2
$\overline{UDQS}$	V1
LDM	N4
UDM	P3
ODT	L6
A0	K2
A1	K1
A2	K5
A3	M6
A4	H3
A5	M3
A6	L4
A7	K6
A8	G3
A9	G1

DDR2 Pin	FPGA Pin
A10	J4
A11	E1
A12	F1
A13	J6
BA0	J3
BA1	J1
BA2	H1
D0	R3
D1	R1
D2	P2
D3	P1
D4	L3
D5	L1
D6	M2
D7	M1
D8	T2
D9	T1
D10	U3
D11	U1
D12	W3
D13	W1
D14	Y2
D15	Y1

Clock Configuration (Source Synchronous)

The DDR2 clocking is designed to be source-synchronous from the FPGA. This means that the FPGA sends the clock signal directly to the SDRAM along with control and data signals, allowing very good synchronization between clock and data.

Memory Controller Blocks

Spartan-6 has integrated memory control blocks to communicate with the external DDR2 memory on the XEM6310MT. This is instantiated using the Xilinx Core Generator (memory interface generator, or MIG) to create a suitable memory controller for your design. You should read and become familiar with the DDR2 SDRAM datasheet as well as MIG and the core datasheet. Although MIG can save a tremendous amount of development time, understanding all this information is critical to building a working DDR2 memory interface.

The XEM6310MT provides 1.2v as V_{CCINT}. According to the memory controller block documentation, the Spartan-6, -2 speed grade can operate memory to 312.5 MHz with this internal voltage.

MIG Settings

The following are the settings used to generate the MIG core for our RAMTester sample using Xilinx Core Generator. These settings were used with ISE 12.2 and MIG 2.3. Note that settings may be slightly different for different versions of ISE or MIG.

Frequency	312.5 MHz	
Memory Type	Component	
Memory Part	MT47H64M16XX-3 (1Gb, x16)	
Data Width	16	
Enable DQS Enable	CHECKED	
High-temp self-refresh	DISABLED	
Output drive strength	Reducedstrength	
RTT(nominal)	50 ohms	[default]
DCI for DQ/DQS	CHECKED	
DCI for address/control	CHECKED	
ZIO pin	W4	
RZQ pin	R7	
Calibrated Input Selection	Yes	
Class for address/control	Class II	
Debug signals	Your option	
System clock	Differential	

JTAG

The JTAG connections on the FPGA are wired directly to the expansion connector JP3 on the XEM6310MT to facilitate FPGA configuration and ChipScope usage using a Xilinx JTAG cable. The BRK6310MT has these signals connected to a 2-mm header compatible with the Xilinx JTAG cable.

Key Memory Storage (LX150T only)

The Spartan-6 FPGA supports design security using AES decryption logic and provides two methods for encryption key memory storage. The first is a volatile memory storage supported by an external battery backup supply voltage (V_{BATT}). The second is a one-time programmable eFUSE. The XEM6310MT design supports both types of key storage with user-modification required.

For quantity purchases of 50 or more units, please contact Opal Kelly (sales@opalkelly.com) to discuss factory installation of these components.

Volatile Encryption Key Storage (V$_{BATT}$)

A small lithium rechargeable battery and three support components can be installed to provide V$_{BATT}$ to the FPGA when the XEM is unpowered. This will preserve the contents of the FPGA's volatile key storage so long as V$_{BATT}$ remains over the threshold specified in the Spartan-6 documentation. Please see the Xilinx *Spartan-6 FPGA Configuration User Guide* (UG380) for more details. Alternatively, V$_{BATT}$ may be provided through JP3-80. In this case, BT1 should not be installed.

The applicable schematic section and components required to support this functionality are shown below.

RefDes	Manufacturer	Manufacturer P/N	Comment
BT1	Seiko Instruments	MS412FE-FL26E	3V, 1mAh lithium battery
D10	Micro Commercial	BAS40-04-TP	Schottky Diode, SOT23
C118	Generic	0.1 µF, SM-0402	Decoupling
R5, R6	Generic	4.7 kΩ, 5%, SM-0402	
R17	Generic	0 Ω, SM-0402	Connects V$_{BATT}$ to JP3-80
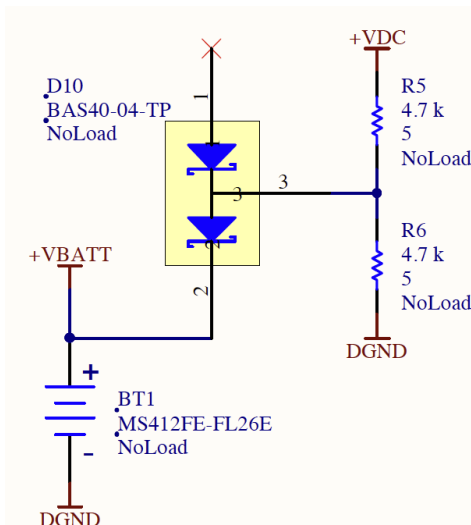
Non-Volatile Encryption Key Storage (eFUSE)

Non-volatile storage of the encryption key is also possible by programming the Spartan-6 eFUSE via JTAG. Please see the Xilinx *Spartan-6 FPGA Configuration User Guide* (UG380) for more details.

To program the eFUSE, you must first install the components listed in the table below. You must also provide an external resistor (R$_{FUSE}$) between JP3-69 and GND. The value of this resistor is specified in the Xilinx *Spartan-6 Datasheet* (DS162) between 1129 Ω and 1151 Ω.

RefDes	Manufacturer	Manufacturer P/N	Comment
C25	Generic	0.1 µF, SM-0402	Decoupling
R9	Generic	0 Ω, SM-0402	Connects FPGA V$_{FS}$ to +3.3v

RefDes	Manufacturer	Manufacturer P/N	Comment
R18	Generic	0 Ω, SM-0402	Connects FPGA R$_{FUSE}$ to JP3-69

Expansion Connectors

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

http://www.opalkelly.com/pins

JP2

JP2 is an 80-pin high-density connector providing access to FPGA Banks 0 and 1. Several pins (45, 47, 53, 55, 58, 60, 77, and 79) of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin mappings for JP2 are available on the XEM6310MT product page on our website. For each pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

JP3

JP3 is an 80-pin high-density connector providing access to FPGA Bank 1. Several pins (2, 4, 21, 23, 25, 27, 42, and 44) of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin JP3-71 is connected to the V$_{REF}$ pins of Bank 1.

Pin mappings for JP2 are available on the XEM6310MT product page on our website. For each pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

JP1 - Transceiver Access

Access to four high-speed serial transceivers pairs (4 Rx and 4 Tx) corresponding to GTP tiles 101 and 123 on the FPGA are available on the JP1. REFCLK0 and REFCLK1 of tile 123 as well as REFCLK1 of tile 101 are also routed to JP1. REFCLK0 of tile 101 is connected to a low-jitter 100 MHz LVDS oscillator.

AC-Coupling

0.1µF AC-coupling capacitors are installed between JP1 and the FPGA for all REFCLK signals.

AC-coupling capacitors are also installed for all GTP receive pairs.

AC-coupling capacitors are not installed for any of the GTP transmit pairs. If AC-coupling is desired or required for the serial application, they should be installed on the expansion side of JP1 (your board).

Setting I/O Voltages

The Spartan-6 FPGA allows users to set I/O bank voltages in order to support several different I/O signalling standards. This functionality is supported by the XEM6310MT by allowing the user to connect independent supplies to the FPGA VCCO pins on two of the FPGA banks.

By default, ferrite beads have been installed that attach each VCCO bank to the +3.3VDD supply. If you intend to supply power to a particular I/O bank, you MUST remove the appropriate ferrite beads. Power can then be supplied through the expansion connectors.

The table below lists details for user-supplied I/O bank voltages

I/O Bank	Expansion Pins	Ferrite Bead
0	JP2-2, 4	FB2
1	JP3-65, 67	FB1

Considerations for Differential Signals

The XEM6310MT PCB layout and routing has been designed with several applications in mind, including applications requiring the use of differential (LVDS) pairs. Please refer to the Xilinx Spartan-6 datasheet for details on using differential I/O standards with the Spartan-6 FPGA.

Note: LVDS output on the Spartan-6 is restricted to banks 0 and 2. LVDS input is available on all banks. For more information, please refer to the *Spartan-6 FPGA SelectIO Resources User Guide* from Xilinx.

FPGA I/O Bank Voltages

In order to use differential I/O standards with the Spartan-6, you must set the VCCO voltages for the appropriate banks to 2.5v according to the Xilinx Spartan-6 datasheet. Please see the section above entitled "Setting I/O Voltages" for details.

Characteristic Impedance

The characteristic impedance of all routes from the FPGA to the expansion connector is approximately 50-Ω.

Differential Pair Lengths

In many cases, it is desirable that the route lengths of a differential pair be matched within some specification. Care has been taken to route differential pairs on the FPGA to adjacent pins on the expansion connectors whenever possible. We have also included the lengths of the board routes for these connections to help you equalize lengths in your final application. Due to space constraints, some pairs are better matched than others.

Reference Voltage Pins (VREF)

The Xilinx Spartan-6 supports externally-applied input voltage thresholds for some input signal standards. The XEM6310MT supports these VREF applications for banks 0 and 1:

For Bank 0, the four V_REF pins are routed to expansion connector JP2 on pins 27, 35, 40, and 52. Note that all four must be connected to the same voltage for proper application of input thresholds. Please see the Xilinx Spartan-6 documentation for more details.

For Bank 1, the four V_REF pins are connected to a single pin on expansion connector JP3, pin 71.

IBERT Configuration

Xilinx provides the IBERT tool to test and experiment with gigabit transceivers. The settings below are compatible with the XEM6310MT and BRK6310MT combination:

Generate Bitstream	Enabled
Add RXRECCLK Probe	Not checked
GTP Dual Naming Style	MGTm n

System Clock
Use External Clock Source	Checked
Frequency	100 MHz
Pin Location	Y11
Pin Input Standard	LVCMOS25

Number of Protocols	1

Line Rate Settings
Name Protocolo	Custom_1
Max Rate (Gbps)	2.5 Gbps
Data Width	20
Refclk	100 MHz
GTP Dual Count	2

MGT_DUAL_123	Custom 1 / 2.5 Gbps
MGT_DUAL_101	Custom 1 / 2.5 Gbps
MGT_DUAL_123	MGTREFCLK0_101
MGT_DUAL_101	MGTREFCLK0_101

BRK6310MT Breakout Board

The BRK6310MT Breakout Board provides convenient access to signals on the XEM6310MT's high-density connectors in prototype situations. The PCB is designed as a 4-layer impedance-controlled board to reduce losses on the transceiver signals which may be accessed via 22 SMA connectors. Please visit the Pins reference for the XEM6310MT for pin mapping details.

Schematics and layout files for the BRK6310MT are available for download from the Opal Kelly website.

Connections

JP2 on the XEM6310MT is pinned out to two 2-mm headers, JP2A and JP2B.

JP3 on the XEM6310MT is pinned out to two 2-mm headers, JP3A and JP3B.

JP1 on the XEM6310MT is the high-frequency transceiver connector. Each transceiver pair connects to two SMA connectors that are appropriately labeled. Connectors marked with a "+" are wired to the P terminal on the transceiver pair. Connectors marked with a "-" are wired to

the N terminal on the trnasceiver pair. Note that termination resistors are not present on the BRK6310MT. Please see the transceiver information earlier in this document for details on the termination resistors on the XEM6310MT.

Pins

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

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Toolbar

The toolbar at the top of a Pins product page has a number of features. Explore a bit; you won't break it.

Click for column selection and filters

Export PDF, CSV, or constraints file

PRODUCT
XEM6310

CHOOSE PRODUCT

Search by typing here

Click for symbol legend

Drop-down for search behaviors

Pin Lists

As the primary reference for Opal Kelly integration module expansion connectors, Pin Lists contain a comprehensive table of the FPGA-to-Connector data including connector pin, FPGA pin, signal description, routed length (when applicable), breakout board pin mapping, FPGA I/O bank, and other properties.

By default, not all data columns are visible. Click on the "Toggle Filters" icon at the top-left to select which columns to show. Depending on the specific module, several additional columns may be shown. The data in these columns is always exported when you export the pin list to CSV.

Filters

You can hide or show the additional information associated with each signal by clicking on the icon at the top left ("Toggle Filters"). Use these filters to limit the visible pin listing to particular subsets of signals you are interested in.

Search

You can search the pin list using the search entry at the top-right. Click on the magnifying glass drop-down to adjust the function of the search to one of:

- Highlight - Highlights search results only.
- Hide Matching - Hides rows where search matches are found.
- Show Only Matching - Shows only rows where a search match is found.

Export (PDF, CSV, Constraints Files)

The export button near the search entry allows you to export the pin list in several formats. PDFs can be viewed or printed. CSV can be loaded into a spreadsheet application or manipulated with scripts. Constraints files can be used as inputs to Xilinx and Altera synthesis and mapping tools.

The constraints files include additional mapping information for other peripherals on the module such as memory, clock oscillators, and LEDs.

Peripherals

A Pins Peripheral is a project definition where you can enter your top-level HDL design nets to have Pins generate a complete constraint file for you.

When you create a Peripheral, you will select a target integration module. The Peripheral is paired to this module so that the design parameters match the features and expansion capabilities of the module.

L38P_0	25.099	0	JP2B-63	SDATA	pix_sdata	| IOSTANDARD=LVCMOS33	
L37P_GCLK13_0	20.996	0	JP2B-64			.VCMOS33	
L38N_VREF_0	22.706	0	JP2B-65			.VCMOS33	
L37N_GCLK12_0	20.055	0	JP2B-66			.VCMOS33	
L51P_0	25.362	0	JP2B-67			.VCMOS33	
L50P_0	21.102	0	JP2B-68			.VCMOS33	
L51N_0	23.293	0	JP2B-69	RESET	pix_reset	| IOSTANDARD=LVCMOS33	
L50N_0	19.964	0	JP2B-70	PIX6	pix_data[6]	| IOSTANDARD=LVCMOS33	

ENTER VALUE FOR DESIGN NET

pix_reset

Specifying Net Names

The Pin List view for a Peripheral includes three additional, editable columns:

- Design Net - The name of the signal as it appears in your top-level HDL.
- Constraints - Text that is inserted into the constraints file for that signal.
- Comment - Additional comment text that is added to the constraints file.

These additional data are merged with the default Pin List constraints file prior to export. The result is a constraints file complete with net names that can be used with your FPGA development flow.

Export Features

Enable the specific module features you would like to appear in the exported constraints file. When a feature is enabled, Pins will export the constraints appropriate to that feature such as pin locations. When a feature is disabled, Pins will skip that portion.

The User Lead In and User Lead Out sections allow you to add custom payloads (your own constraints) that will be added to the exported constraints file. Additional timing constraints or comments can be added here.

Constraint file template   Default

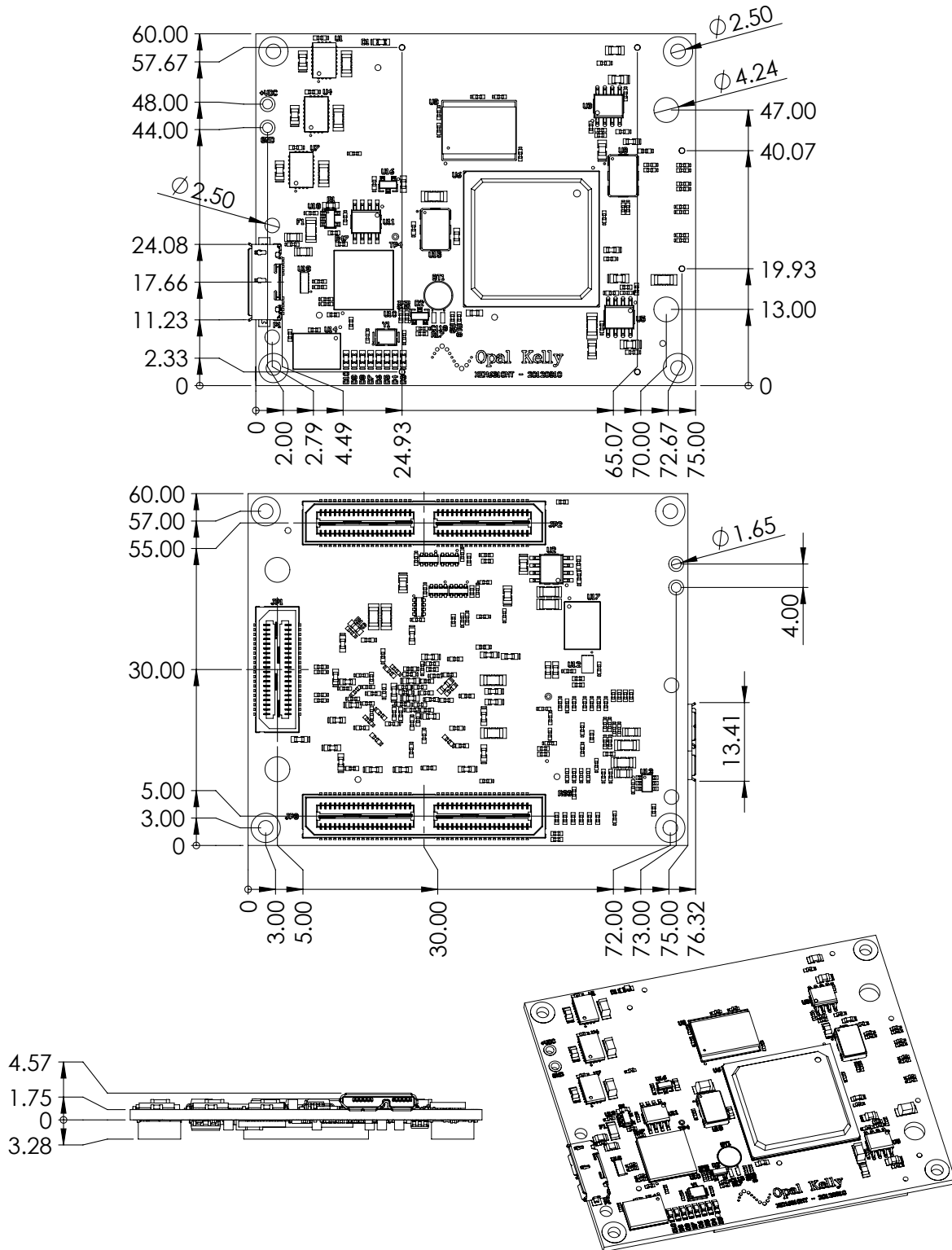**Output filename**   xem6310.ucf

Export features
- ☑ Lead In
- ☑ FrontPanel
- ☑ FrontPanel Timing
- ☐ System Clock
- ☐ Reset
- ☐ User Lead In Add payload
- ☑ LEDs
- ☐ FPGA Flash
- ☑ DDR2
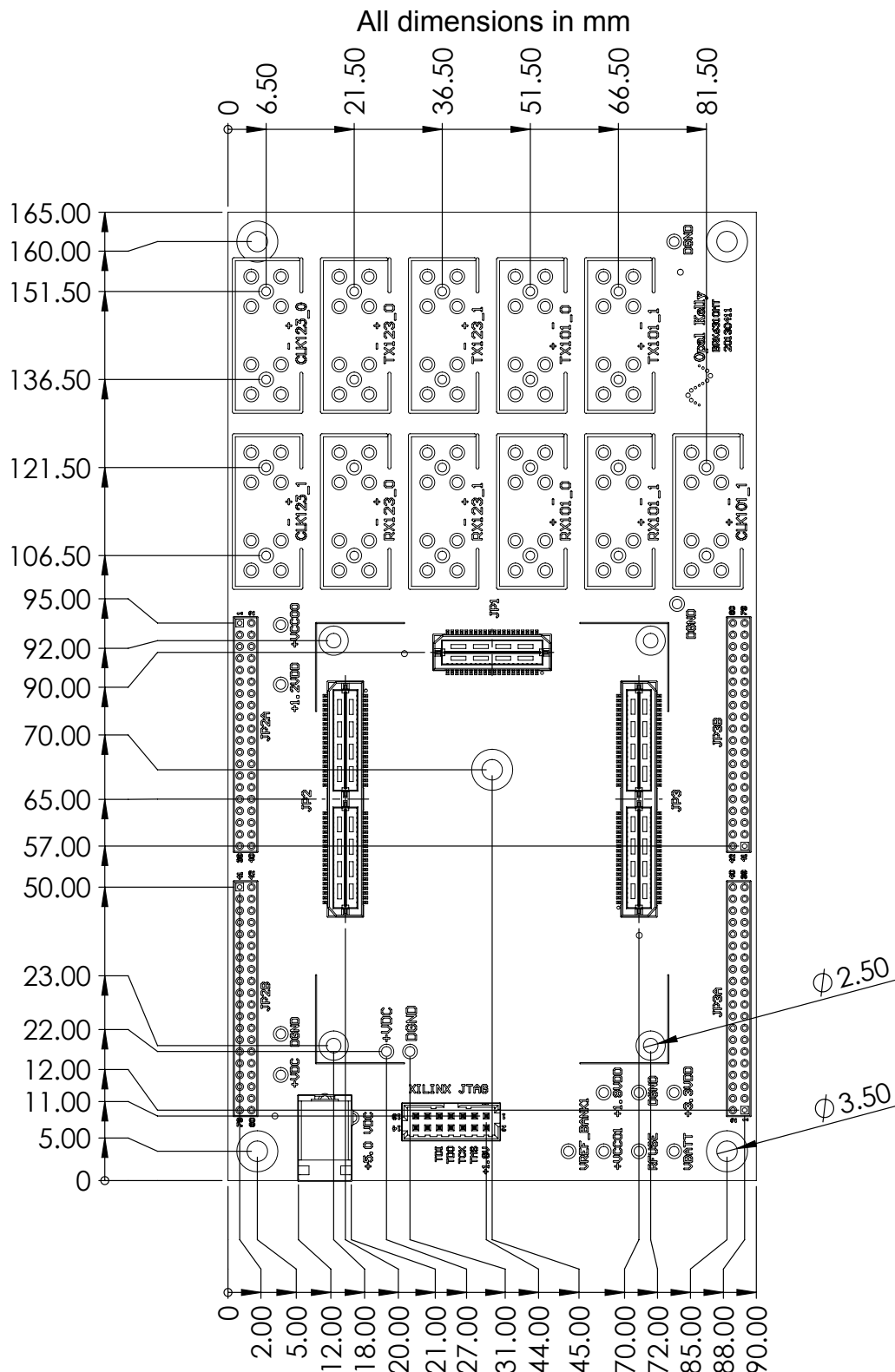- ☐ User Lead Out Add payload

PCB Version History

20130814

First production PCB.

XEM6310MT Mechanical Drawing

All dimensions in mm

BRK6310MT Mechanical Drawing

All dimensions in mm

XEM6310MT Quick Reference

JP3 Pin	Connection	FPGA Pin	Length (mm)
1	DGND		
3	DGND		
5	W22	L51N_1	17.928
7	W20	L51P_1	19.482
9	Y22	L52N_1	12.557
11	Y21	L52P_1	12.671
13	U22	L49N_1	19.512
15	U20	L49P_1	21.769
17	T22	L48N_1	15.054
19	T21	L48P_1	15.147
21	N19	L42N_GCLK6_1	19.989
23	P20	L42P_GCLK7_1	17.420
25	M19	L40N_GCLK10_1	20.064
27	M20	L40P_GCLK11_1	17.873
29	N15	L58N_1	21.033
31	M16	L58P_1	19.757
33	L17	L36N_1	17.747
35	K17	L36P_1	18.324
37	J17	L19N_1	24.503
39	J16	L19P_1	24.090
41	L19	L38N_1	10.451
43	K20	L38P_1	9.368
45	H17	L9N_1	16.585
47	H16	L9P_1	17.270
49	H19	L30N_1	11.495
51	H18	L30P_1	13.003
53	H22	L37N_1	10.485
55	H21	L37P_1	11.776
57	F22	L31N_1	7.441
59	F21	L31P_1	8.530
61	C22	L20N_1	10.151
63	C20	L20P_1	12.394
65	VCCO1		
67	VCCO1		
69	RFUSE	(LX150T only)	
71	VREF Bank 1		
73	+3.3VDD		
75	+3.3VDD		
77	+3.3VDD		
79	+3.3VDD		

JP3 Pin	Connection	FPGA Pin	Length (mm)
2	L22	L43N_GCLK4_1	33.930
4	L20	L43P_GCLK5_1	35.043
6	DGND		
8	DGND		
10	V22	L50N_1	20.673
12	V21	L50P_1	21.939
14	R22	L47N_1	21.910
16	R20	L47P_1	23.003
18	P22	L46N_1	21.951
20	P21	L46P_1	23.216
22	N22	L45N_1	21.175
24	N20	L45P_1	23.443
26	K16	L21N_1	31.702
28	L15	L21P_1	29.176
30	M22	L44N_1	18.876
32	M21	L44P_1	19.112
34	K18	L34N_1	25.923
36	K19	L34P_1	25.432
38	H20	L33N_1	26.532
40	J19	L33P_1	26.538
42	K22	L41N_GCLK8_1	16.338
44	K21	L41P_GCLK9_1	17.433
46	J22	L39N_1	16.816
48	J20	L39P_1	18.961
50	G22	L35N_1	17.509
52	G20	L35P_1	19.602
54	F20	L29N_1	20.494
56	G19	L29P_1	22.882
58	E22	L32N_1	16.990
60	E20	L32P_1	19.093
62	B22	L10N_1	17.311
64	B21	L10P_1	18.609
66	DGND		
68	DGND		
70	R11	L22P_2	35.438
72	JTAG TDI		
74	JTAG TMS		
76	JTAG TCK		
78	JTAG TDO		
80	VBATT	(LX150T only)	

LED	FPGA Pin
D0	U16
D1	W18
D2	Y18
D3	V17
D4	Y17
D5	Y16
D6	W12
D7	V11

XEM6310MT Quick Reference

JP2 Pin	Connection	FPGA Pin	Length (mm)	JP2 Pin	Connection	FPGA Pin	Length (mm)
1	+VDC			2	VCCO0		
3	+VDC			4	VCCO0		
5	+VDC			6	+1.2VDD		
7	+1.8VDD			8	+1.2VDD		
9	+1.8VDD			10	DGND		
11	+3.3VDD			12	R8	L59N_2	48.538
13	+3.3VDD			14	DGND		
15	+3.3VDD			16	DGND		
17	B20	L65P_0	61.552	18	C19	L64P_0	66.977
19	A20	L65N_0	59.892	20	A19	L64N_0	64.444
21	B18	L63P_0	42.809	22	C17	L50P_0	51.818
23	A18	L63N_0	41.106	24	A17	L50N_0	49.117
25	C5	L8P_0	31.274	26	C4	L6P_0	36.002
27	A5	L8N_VREF_0	28.526	28	A4	L6N_0	33.201
29	B3	L5P_0	24.723	30	B2	L3P_0	32.653
31	A3	L5N_0	22.942	32	A2	L3N_0	30.429
33	C3	L1P_HSWAPEN_0	27.741	34	D4	L2P_0	33.384
35	D3	L1N_0	25.163	36	D5	L2N_0	34.984
37	E5	L4P_0	24.654	38	D18	L62P_0	77.825
39	E6	L4N_0	26.471	40	D19	L62N_VREF_0	75.684
41	G8	L32P_0	38.425	42	D17	L66P_0	76.936
43	F9	L32N_0	40.529	44	C18	L66N_0	77.180
45	G9	L34P_GCLK19_0	38.322	46	F7	L7P_0	45.513
47	F10	L34N_GCLK18_0	40.486	48	F8	L7N_0	46.088
49	H10	L33P_0	39.236	50	H13	L38P_0	65.023
51	H11	L33N_0	40.683	52	G13	L38N_VREF_0	64.538
53	F14	L36P_GCLK15_0	54.196	54	H14	L49P_0	58.343
55	F15	L36N_GCLK14_0	54.118	56	G15	L49N_0	59.729
57	G16	L51P_0	62.703	58	E16	L37P_GCLK13_0	67.989
59	F17	L51N_0	63.596	60	F16	L37N_GCLK12_0	67.275
61	P17	L71P_1	51.143	62	M17	L61P_1	55.535
63	P18	L71N_1	53.426	64	M18	L61N_1	56.435
65	R17	L72P_1	51.113	66	N16	L60P_1	61.776
67	T17	L72N_1	50.009	68	P16	L60N_1	60.975
69	T19	L73P_1	51.957	70	R15	L70P_1	53.658
71	T18	L73N_1	50.429	72	R16	L70N_1	57.204
73	DGND			74	U19	L59P_1	62.361
75	DGND			76	T20	L59N_1	62.766
77	H12	L35P_GCLK17_0	52.817	78	DGND		
79	G11	L35N_GCLK16_0	52.575	80	DGND		

XEM6310MT Quick Reference

JP1 Pin	Connection	FPGA Pin	Length (mm)	
1	D7	MGTRXP0_101	5.001	24.858
3	C7	MGTRXN0_101	5.001	24.800
5	DGND			
7	B6	MGTTXP0_101	23.029	
9	A6	MGTTXN0_101	22.953	
11	DGND			
13	D9	MGTRXP1_101	5.001	24.786
15	C9	MGTRXN1_101	4.982	24.762
17	DGND			
19	B8	MGTTXP1_101	23.599	
21	A8	MGTTXN1_101	23.503	
23	DGND			
25	-			
27	-			
29	DGND			
31	-			
33	-			
35	DGND			
37	C11	MGTREFCLK1P_101	2.218	21.829
39	D11	MGTREFCLK1N_101	2.241	22.257

JP1 Pin	Connection	FPGA Pin	Length (mm)	
2	B16	MGTTXP1_123	20.488	
4	A16	MGTTXN1_123	20.563	
6	DGND			
8	D15	MGTRXP1_123	2.658	25.397
10	C15	MGTRXN1_123	2.663	25.425
12	DGND			
14	B14	MGTTXP0_123	22.844	
16	A14	MGTTXN0_123	22.830	
18	DGND			
20	D13	MGTRXP0_123	2.678	25.773
22	C13	MGTRXN0_123	2.664	25.738
24	DGND			
26	DGND			
28	DGND			
30	DGND			
32	A12	MGTREFCLK0P_123	2.969	20.248
34	B12	MGTREFCLK0N_123	2.932	21.379
36	DGND			
38	E12	MGTREFCLK1P_123	2.668	31.120
40	F12	MGTREFCLK1N_123	2.691	31.646