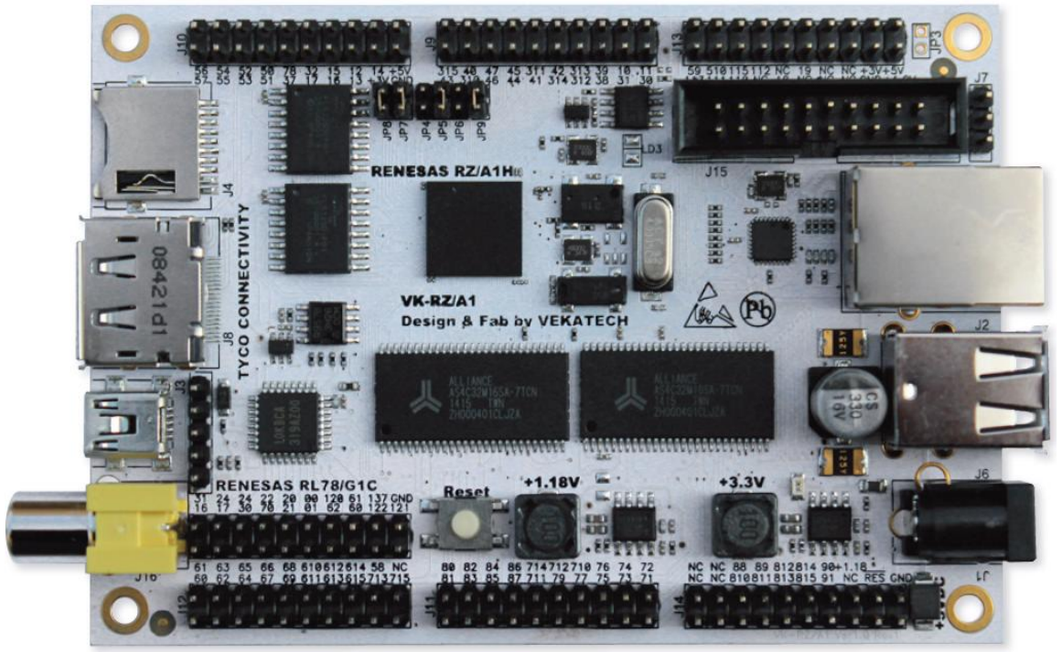
VK-RZ/A1H Development Board

User manual



Rev. 1.0, Dec.10.2014

INTRODUCTION

VK-RZ/A1 is a starter kit which uses MCU R7S721000VCBG from Renesas Electronics. This powerful MCU is actually LSI, single-chip microcontroller that includes an ARM Cortex™-A9 processor along with the integrated peripheral functions required to configure a system. The core includes:

- 32-KB L1 instruction cache
- 32-KB L1 data cache
- 128-KB L2 cache.

Integrated various on-chip peripheral functions and interfaces such as:

- 10-MB large-capacity RAM (128 KB are shared by the data-retention RAM)
- data-retention RAM
- multi-function timer pulse unit 2, OS timer, realtime clock
- motor control PWM timer
- UART, UART with FIFO, I2C, SPI, SPI multi I/O bus controller, CAN, LIN
- serial sound interface, sound generator, CD-ROM decoder
- A/D converter, SCUX
- media local bus, SD host interface, MMC host interface
- NAND flash memory controller
- IEBus™ controller, Renesas SPDIF interface
- Ethernet controller, EthernetAVB
- USB 2.0 host/function
- digital video decoder, video display controller 5
- dynamic range compression, image renderer, image renderer for display
- display out comparison unit
- Renesas graphics processor for OpenVG™
- JPEG codec unit, capture engine unit, pixel format converter
- interrupt controller modules, general I/O ports

The kit supports:

- Ethernet,
- LVDS Port
- up to 128 MB SDRAM
- Mini SD card connector
- Composite video connector
- one USB ↔ UART converter
- two USB communication channels
- 20 pins JTAG programing and debugging interface

All this along with the DC/DC power supply on board and connected to pin headers unused pins of R5F10KBC & R7S721000VCBG allow you to build a diversity of powerful applications to be used in a wide range of embedded tasks.

BOARD FEATURES:

- MCU: RL78/G1C - R5F10KBC
- LSI: RZ/A1H - R7S721000VCBG
- USB Mini B device connector (RL78/G1C)
- 2xUSB Standard A device connectors (RZ/A1H)
- CAN connectors (Infineon TLE 6250)
- LVDS Port connector (RZ/A1H)
- Composite video connector (RZ/A1H)
- Micro SD card connector (RZ/A1H)
- SDRAM 64 MB (2x32MB) (RZ/A1H)
- Ethernet, RJ-45 10/100Mb MAC (RZ/A1H)
- PHY SMSC LAN8710A
- 20 pins Debug/programming connector (JTAG)
- 1 push RESET button
- Power connector for DC/DC 5V
- FR-4, 1.6 mm, Green/White solder mask, component print.
- Dimensions: 105.0mm x 74.0mm

ELECTROSTATIC WARNING

The VK-RZ/A1H - R7S721000VCBG board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

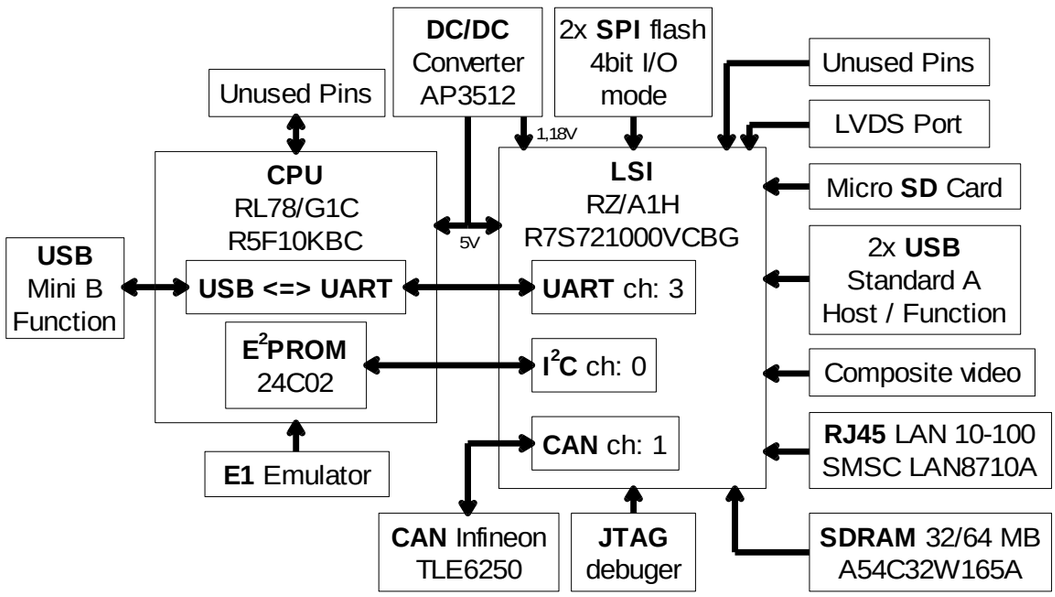
PROCESSOR FEATURES

The VK-RZ/A1H board use MCU R7S721000VCBG from RENESAS ELECTRONICS with these features:

- Power supply voltage: VDD = 3.0 to 3.6 V
- Operating ambient temperature: TA =−40 to +85°C
- Max. CPU clock (Iφ) = 400 MHz)

For more information please visit www.renesas.eu

BLOCK DIAGRAM



EXTERNAL SDRAM BASE ADDRESSES

```
SDRAM CS2:  ORIGIN = 0x08000000,    LENGTH = 64MB
SDRAM CS3:  ORIGIN = 0x0C000000,    LENGTH = 64MB
SDRAM CS2 mirror: ORIGIN = 0x48000000,    LENGTH = 64MB
SDRAM CS3 mirror: ORIGIN = 0x4C000000,    LENGTH = 64MB
```

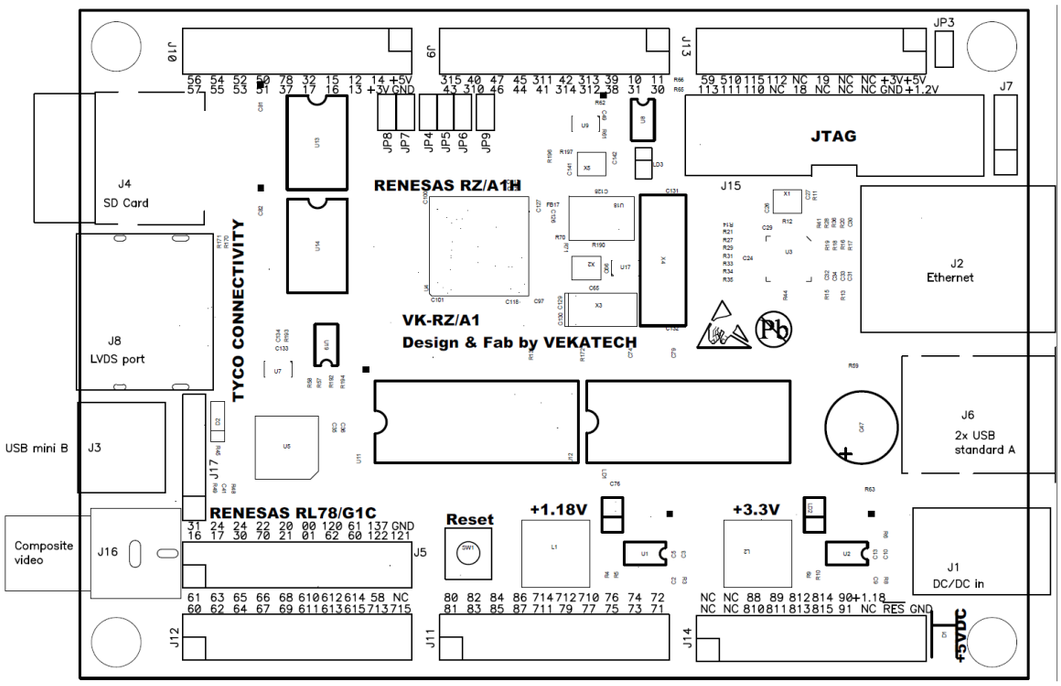
⚠ SDRAM is accessed with 16bit data width

⚠ A14 & A15 are used for bank switching

SCHEMATICS

Please refer to CD for high quality pictures.

BOARD REFERENCE DESIGNATORS



POWER SUPPLY CIRCUIT:

VK-RZ/A1H is powered by (5) VDC applied at the power jack.
VK-RZ/A1H could also be powered by USB Mini B connector.
The consumption of VK-RZ/A1H may vary and the maximum is (@3.3V) 450mA.

CLOCK CIRCUITS:

Quartz Generator 13.3333 MHz is connected to **EXTAL,** pin# **AA14**.
Quartz crystal 32.768KHz is connected to **RTC_X1/RTC_X2,** pins# **AA7/Y7**.
Quartz crystal 4.0000MHz is connected to **RTC_X3/RTC_X4,** pins# **V10/V11**.
Quartz crystal 48.0000MHz is connected to **USB_X1/USB_X2,** pins# **A13/Y13**.
Quartz crystal 27.0000MHz is connected to **VIDEO_X1/VIDEO_X2,** pins# **W21/V20**.
Quartz crystal 25.0000MHz is connected to Ethernet Phy - **SMSC LAN8710A** – (XTAL1/XTAL2 pins# 5/4).

PUSH BUTTONS

Button #	Function	Signal Name	Pin#
SW1	RESET	RESET	U9

JUMPERS CONFIGURATION

■ **Connected** ☐ **Disconnected**

BOOT configuration:

BOOT mode#	JP4, JP5, JP6	Description
0		Boot from **CS0 16 bit** bus width
1		Boot from **CS0 32 bit** bus width
3		Boot from **SPI multi I/O ch0:** [P9_2 - P9_5]
4		Boot from **SD card ch0:** [P4_10 - P4_15]
5		Boot from **MMC card ch0:** [P5_10 - P5_15]

Clock settings:

CLK mode#	JP7, JP8	Description
MD_CLK		CLK source from **EXTAL/crystal resonator**
MD_CLK		CLK source from **USB_X1/crystal resonator**
MD_CLKS		SSCG circuit **OFF**
MD_CLKS		SSCG circuit **ON**

JTAG Debugger settings:

JTAG mode#	JP9	Description
0		Normal operation
1		Boundary scan

CAN Termination:

CAN mode#	JP3	Description
0		CAN line **is** terminated
1		CAN line **is not** terminated

EXTERNAL CONNECTORS DESCRIPTION

PWR J1			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2,3	GND

 The power input should be +(5VDC)

E1 Emulator 5pin connector

E1 J17	
Pin#	Signal Name
1	GND
2	TRESET
3	RESET
4	TOOL
5	+5V

JTAG 20pin connector

JTAG J15			
Pin#	Signal Name	Pin#	Signal Name
1	+3V3	2	+3V3
3	TRST	4	GND
5	TDI/JP0_0	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	-	12	GND
13	TDO/JP0_1	14	GND
15	SRST	16	GND
17	-	18	GND
19	-	20	GND

CAN 3pin connector

CAN J7	
Pin#	Signal Name
1	CAN_L
2	GND
3	CAN_H

CTX1 is connected to **P5_10** pin# **A7** of **R7S721000VCBG**.
CRX1 is connected to **P5_9** pin# **B7** of **R7S721000VCBG**.

 Termination Jumper **JP3**.

Ethernet connector RJ45 type: J2

 Transformer and integrated LEDS are connected/controlled to PHY interface LAN8710A.

 Respective signals from PHY are connected to MII interface of **R7S721000VCBG.**

USB devices

USB mini B J3			
Pin#	Signal Name	Pin#	Signal Name
1	V_USB1	3	D+
2	D-	5	GND

 **Pin#4 ID is disconnected.**
V_USB1 Output USB device power.
D- is connected to **UDM0,** pin#**23** of **R5F10KBC.**
D+ is connected to **UDP0,** pin#**24** of **R5F10KBC.**

USB standard A J6 (lower)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	3	D+
2	D-	4	GND

USB standard A J6 (upper)			
Pin#	Signal Name	Pin#	Signal Name
5	+5V	7	D+
6	D-	8	GND

Both USB are configured as hosts !
lower D- is connected to **DM0,** pin#**AA11** of **R7S721000VCBG**.
lower D+ is connected to **DP0,** pin#**Y11** of **R7S721000VCBG**.
upper D- is connected to **DM1,** pin#**AA9** of **R7S721000VCBG**
upper D+ is connected to **DP1,** pin#**Y9** of **R7S721000VCBG**

Micro SD card slot:

Micro SD J4			
Pin#	Signal Name	MCU PIN#	MCU PORT
1	DAT2	F18	P4_15/SD_D2_0
2	CD/DAT3	F17	P4_14/SD_D3_0
3	CMD	G20	P4_13/SD_CMD_0
4	VDD	-	-
5	CLK	H21	P4_12/SD_CLK_0
6	GND	-	-
7	DAT0	G18	P4_11/SD_D0_0
8	DAT1	H20	P4_10/SD_D1_0
9	NO-b	-	-
10	!CARDEXIST	J21	P4_8/SD_CD_0

DAT0-3 (IN/OUT) - I/O Memory Card Interface Data 0-4.
These are the data lines for the SD connector. They could be both input and output for the MCU depending on the data flow direction.
CMD (OUT) - Output Memory Card Interface Command. This is a command sent form the processor to the memory card and as such it is output from the processor.
CLK (OUT) - Output Memory Card Interface Clock. This signal is output from the MCU and synchronizes the data transfer between the memory card and the MCU.

Composite video

Composite video J16			
Pin#	Signal Name	Pin#	Signal Name
1	V_USB1	2	D+

LVDS port connector: J8

The signals that are coming out from the connector **ARE NOT DISPLAY PORT SIGNALS**, regardless of the fact that the connector is the same.

UNUSED PIN HEADERS

PORT extension

J5 (RL78/G1C)			
Pin#	Signal Name	Pin#	Signal Name
1	P16/TI01/TO01/INTP5	2	P31/TI03/TO03/INTP4/PCLBUZ0
3	P17/TI02/TO02	4	P24/ANI4
5	P30/INTP3/SCK00/SCL00 /(TI03/TO03/PCLBUZ0)	6	P23/ANI3
7	P70/PCLBUZ1	8	P22/ANI2
9	P21/ANI1/AV_{REFM}	10	P20/ANI0/AV_{REFP}
11	P01/ANI16/TO00/INTP9 /SCK01/SCL01/(SCLA0)	12	P00/ANI17/TI00/INTP8/SI01 /SDA01/(SDAA0)
13	P62	14	P120/ANI19/SO01/(PCLBUZ1)
15	P60/SCLA0	16	P61/SDAA0
17	P122/X2/EXCLK	18	P137/INTP0
19	P121/X1	20	GND

LCD extension

J9 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P1_1/RIIC0SDA	2	P3_0/LCD0_CLK
3	P1_0/RIIC0SCL	4	P3_1/LCD0_TCON0 (DE)
5	P3_9/LCD0_DATA1 (B2)	6	P3_8/LCD0_DATA0 (B1)
7	P3_13/LCD0_DATA5 (G0)	8	P3_12/LCD0_DATA4 (B5)
9	P4_2/LCD0_DATA10 (G5)	10	P3_14/LCD0_DATA6 (G1)
11	P3_11/LCD0_DATA3 (B4)	12	P4_1/LCD0_DATA9 (G4)
13	P4_5/LCD0_DATA13 (R3)	14	P4_4/LCD0_DATA12 (R2)
15	P4_7/LCD0_DATA15 (R5)	16	P4_6/LCD0_DATA14 (R4)
17	P4_0/LCD0_DATA8 (G3)	18	P3_10/LCD0_DATA2 (B3)
19	P3_15/LCD0_DATA7 (G2)	20	P4_3/LCD0_DATA11 (R1)

J10 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	GND
3	P1_4/RIIC2SCL	4	+3V3
5	P1_2/RIIC1SCL	6	P1_3/RIIC1SDA
7	P1_5/RIIC2SDA	8	P1_6/RIIC3SCL
9	P3_2/LCD0_TCON1 (ON/OFF)	10	P1_7/RIIC3SDA
11	P7_8/LVDS_HPD	12	P3_7/LCD0_TCON6 (BKL_EN)
13	P5_0/TXCLKOUTP	14	P5_1/TXCLKOUTM
15	P5_2/TXOUT2P	16	P5_3/TXOUT2M
17	P5_4/TXOUT1P	18	P5_5/TXOUT1M
19	P5_6/TXOUT0P	20	P5_7/TXOUT0M

SDRAM extension

J11 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P8_1/A9	2	P8_0/A8
3	P8_3/A11	4	P8_2/A10
5	P8_5/A13	6	P8_4/A12
7	P8_7/A15	8	P8_6/A14
9	P7_11/A3	10	P7_14/A6
11	P7_9/A1	12	P7_12/A4
13	P7_7/WE1/DQMLU	14	P7_10/A2
15	P7_5/RD/WR	16	P7_6/WE0/DQMLL
17	P7_3/CAS	18	P7_4/CKE
19	P7_1/CS3	20	P7_2/RAS

J12 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	P6_1/D1	2	P6_0/D0
3	P6_3/D3	4	P6_2/D2
5	P6_5/D5	6	P6_4/D4
7	P6_7/D7	8	P6_6/D6
9	P6_9/D9	10	P6_8/D8
11	P6_11/D11	12	P6_10/D10
13	P6_13/D13	14	P6_12/D12
15	P6_15/D15	16	P6_14/D14
17	P7_13/A5	18	P5_8/CS2
19	P7_15/A7	20	n.c

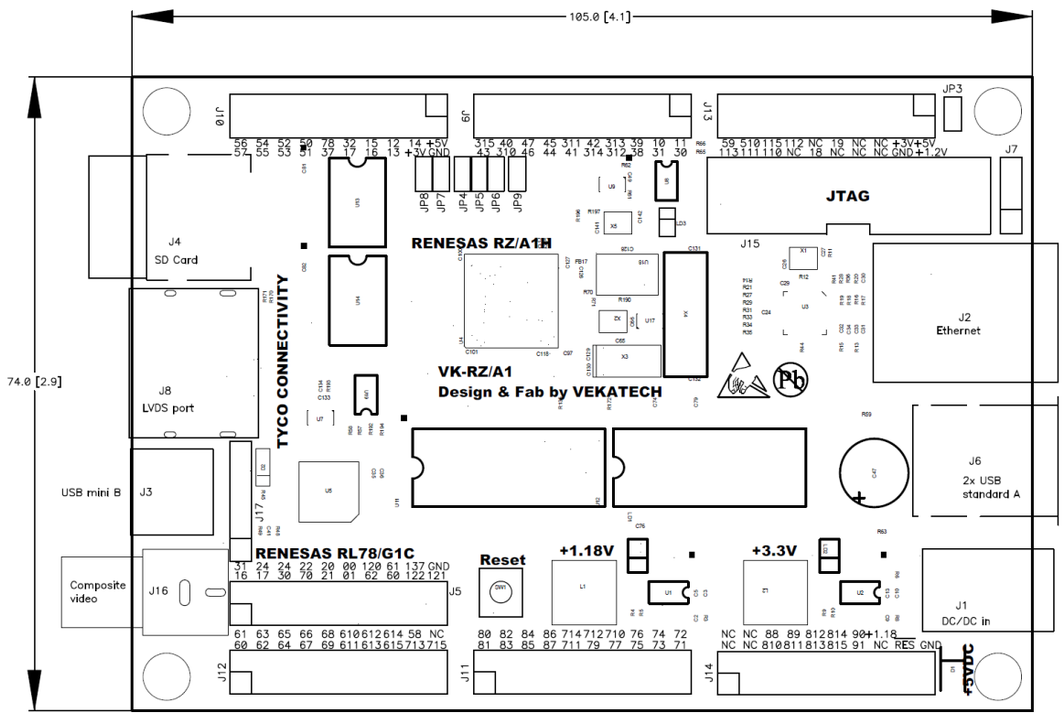
PORT extension

J13 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	+5V	2	+1V18
3	+3V3	4	GND

5	n.c	6	n.c
7	n.c	8	n.c
9	P1_9	10	n.c
11	n.c	12	P1_8
13	P1_12	14	n.c
15	P1_15	16	P1_10
17	P5_10/CAN1TX	18	P1_11
19	P5_9/CAN1RX	20	P1_13

J14 (RZ/A1H)			
Pin#	Signal Name	Pin#	Signal Name
1	n.c	2	n.c
3	n.c	4	n.c
5	P8_10	6	P8_8/TxD3
7	P8_11	8	P8_9/RxD3
9	P8_13	10	P8_12
11	P8_15	12	P8_14
13	P9_1	14	P9_0
15	n.c	16	+1V18
17	RESET	18	+3V3
19	GND	20	+5V

MECHANICAL DIMENSIONS:



Dimensions are in mm [inch].

AVAILABLE DEMO SOFTWARE:

1. FREERTOS(TM) DEMO PROJECT PORTED FOR IAR AND BUILT FOR VK-RZ/A1H development board.
2. CycloneTCP PROJECT PORTED FOR IAR AND BUILT FOR VK-RZ/A1H development board.
3. u-boot, Linux PORTED FOR GCC AND BUILT FOR VK-RZ/A1H development board.