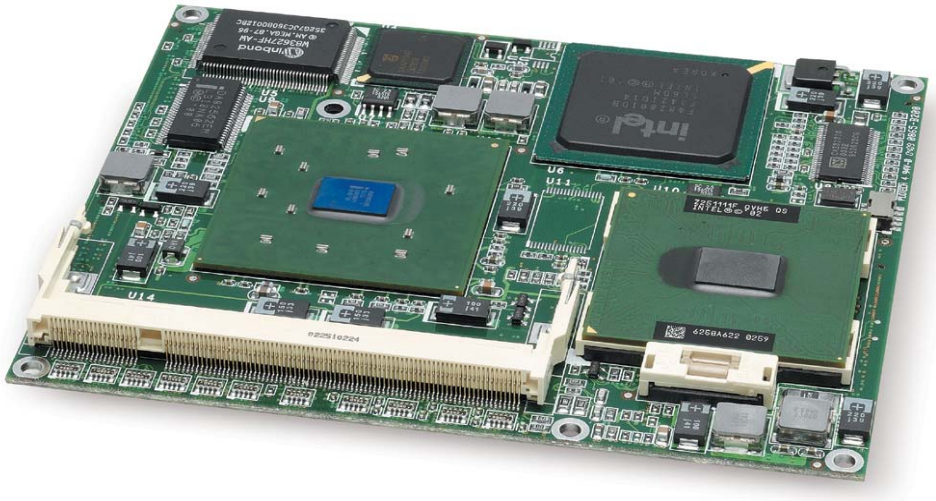
ETX

ETX-IM333

User's Manual
ver. 1.1



ADLINK TECHNOLOGY INC.

Manual Rev. 1.1: March 24, 2005

Trademarks

Revision History

Release	Date	Initials	Change
1.0	01/14/2005	JC	Initial release
1.1	03/23/2005	HB	Correct X3 and X4 pinouts Add Speedstep note to BIOS CPU speed settings page 41

Contents

1 Introduction

1.1 Description

ETX-IM333 is an ETX compatible module specially designed to facilitate speedy development of semi custom designs. ETX is an open standard that targets the market for embedded OEM projects. An ETX core combined with a custom made carrier board represents a value solution that allows OEM customers to get to the market fast. ETX Core modules are also known as COM (Computer on module) or as SOM (System on Module). ETX-IM333 is fully compliant with ETX component SBC™ Specification V2.6.

ETX-IM333 is based on the Intel's embedded 855GME Northbridge and ICH4 Southbridge. It supports Celeron® M and Pentium® M (Banias/Dothan) CPU's in the range of 600MHz to 1.7GHz. The CPU / Chipset combination is ideal for applications that require high performance, reliability, and long product availability.

The Intel® 855GME Chipset graphics memory controller hub (GMCH-M) provides integrated graphics (250MHz) capabilities and power saving features. The 855GME Northbridge incorporates a DDR memory controller and supports DDR333 in addition to DDR266/200 memory for up to 1GB in a single 200-pin SODIMM socket. Graphic support for CRT and single/dual channel LVDS is included. Optionally, the board can support TV 0ut (SDTV and HDTV).

The integrated EIDE controller supports both PIO and UDMA modes, USB ports v2.0, two serial ports, one parallel port (SPP/ECP/EPP), one PS2 keyboard/mouse interface, AC97 audio interface, Fast Ethernet LAN controller, and power management functionality.

2 Specifications

2.1 General

- CPU: Intel® Pentium® M (Banias/Dothan type) or Intel® Celeron® M
  supports soldered LV / ULV uFCBGA packages or uFCPGA socket
- Chipset: Intel® 855GME with 400 FSB and Intel® 82801DB I/O Control Hub 4
- Memory: one SODIMM socket for up to 1GB DDR 200/266/333
- L2 Cache: 512KB (Celeron-M), 1 MB (Pentium-M Banias), 2 MB (Pentium-M Dothan)
- Enhanced IDE: two ports and up to four ATAPI devices,
  supports Ultra DMA transfer rates of up to 33 MB/sec
- BIOS: Phoenix AWARD PnP 4 Mb Flash with console redirection and CMOS EEPROM backup. USB boot/legacy and PXE support
- Hardware Monitor: integrated in Winbond 83627HF
  monitors supply voltages and CPU temperature
- Watchdog: integrated in Winbond 83627HF
  software programmable 1-255 sec or 1-255 min, generates system reset
- Expansion: 32-bit PCI 2.2

2.2 Display

- Chipset: integrated Intel® 855GME Chipset graphics memory controller hub (GMCH-M)
  supports Dual Independent Display on CRT and LVDS channel
- Memory: up to 32 MB UMA Video RAM
- CRT: up to QXGA 2048 x 1536
- Flat Panel: supports single/dual channel LVDS (2x12-bit)
  for display resolutions up to 1600x1200

2.3 TV-out (optional)

- Chipset: Philips SAA-7104/05 Advanced Digital Video Encoder
- Output: PAL or NTSC legacy video output up to 1280 X 1024, HDTV supported

2.4 Audio

- Chipset: integrated in Intel® 82801DB Southbridge
- Audio Codec: VIA VT1616 AC97 ver. 2.0

2.5 LAN

- Chipset: ICH4 integrated Intel® 82562 compatible 32-bit PCI LAN controller
- Interface: 10/100 Mbps with Wake-on-LAN and Alert on LAN support

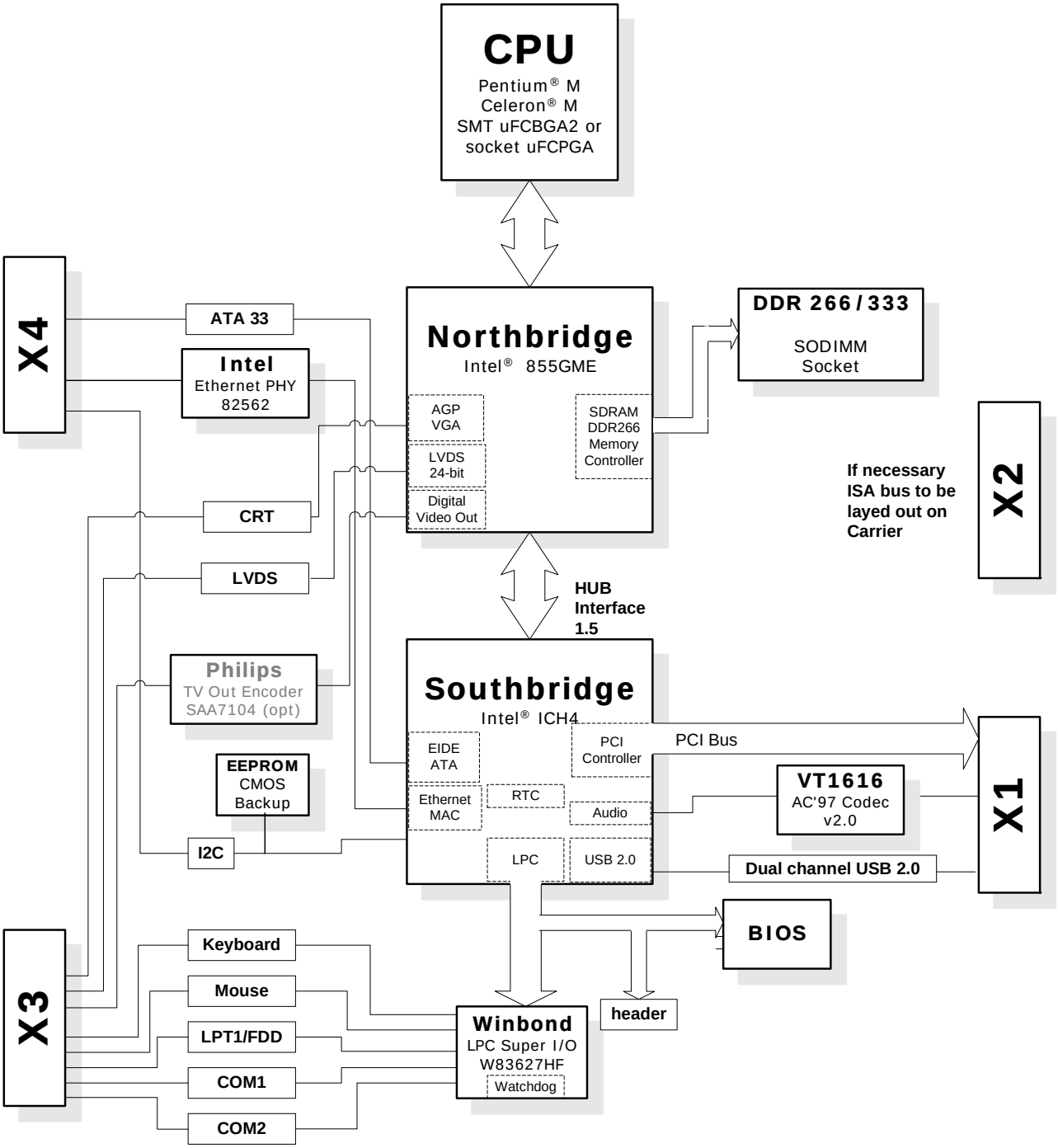
2.6 Multi I/O

- Serial: two high speed RS-232C ports (COM1/COM2)
- Parallel: SPP, EPP, and ECP mode
- FDD: not implemented
- IrDA: supports SIR IrDA 1.1 compliant
- USB: supports up to four ports ver 2.0 (ver 1.1 backward compatible)
- Keyboard & Mouse: one PS/2 keyboard and one PS/2 mouse

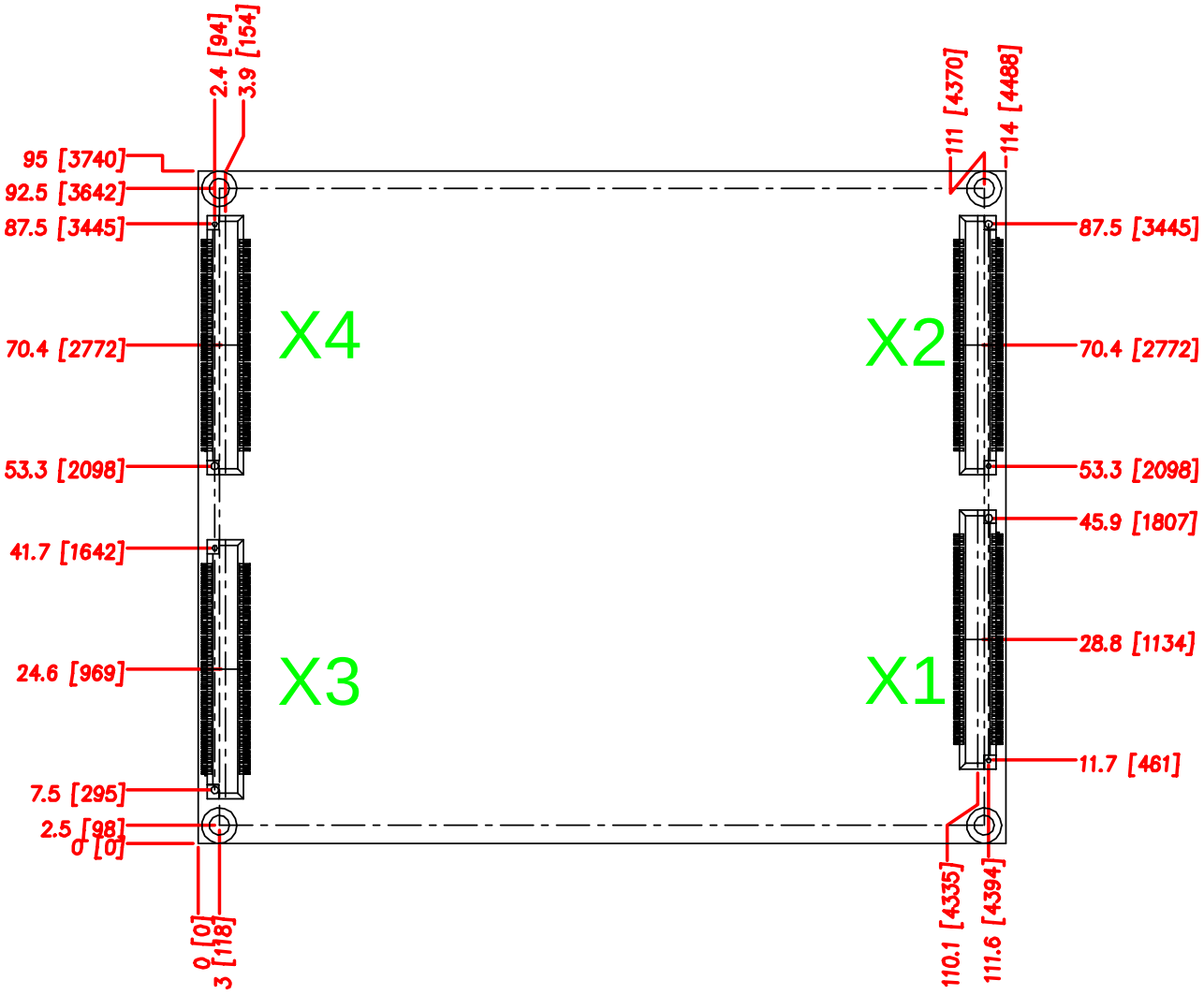
2.7 Mechanical and Environmental

- Power Requirement (+5V only): 18 Watt typical; (uFCBGA Pentium® M 1.1GHz with 512 MB DDR333)
- Operating Temperature: 0 to 55°C (32 to 140°F)
- Relative Humidity: up to 90% @ 55°C
- ETX Board Dimensions: 95 mm x 114 mm (3.7" x 4.5")
- Weight: 87 grams

3 Function diagram



4 Mechanical Dimensions



5 Watchdog Timer

ETX-IM333 implements a watchdog timer embedded in the LPC based Winbond 83627HF Super I/O controller.

The Watchdog timer consists of a one-second/minute resolution down counter (in CRF6 of logical device 8 of 83627HF) and two Watchdog control registers (CRF5 and CRF7 of logical device 8). Once a value is set in the WDT, the timer begins to count down.

Any movement in the keyboard, mouse, or software re-set of the value will cause a reload of the timer value. The Watchdog output is connected to "reset". When the system hangs up without software re-trigger, the system will be reset.

The Watchdog timer that has a 1 second granularity up to 255 seconds or a 1 minute granularity up to 255 minutes. The keyboard and mouse will only reset WDT if Bit 7 and 6 of CRF7 is set, that is values greater than C0h or 192 decimal.

To configure the registers, the following sequence should be followed :

- 1. Writing 87h to location 2Eh twice to enter into the extended function mode.
- 2. Configure the registers to set up WDT.
- 3. Writing 0AAh to location 2Eh to exit the extended function mode.

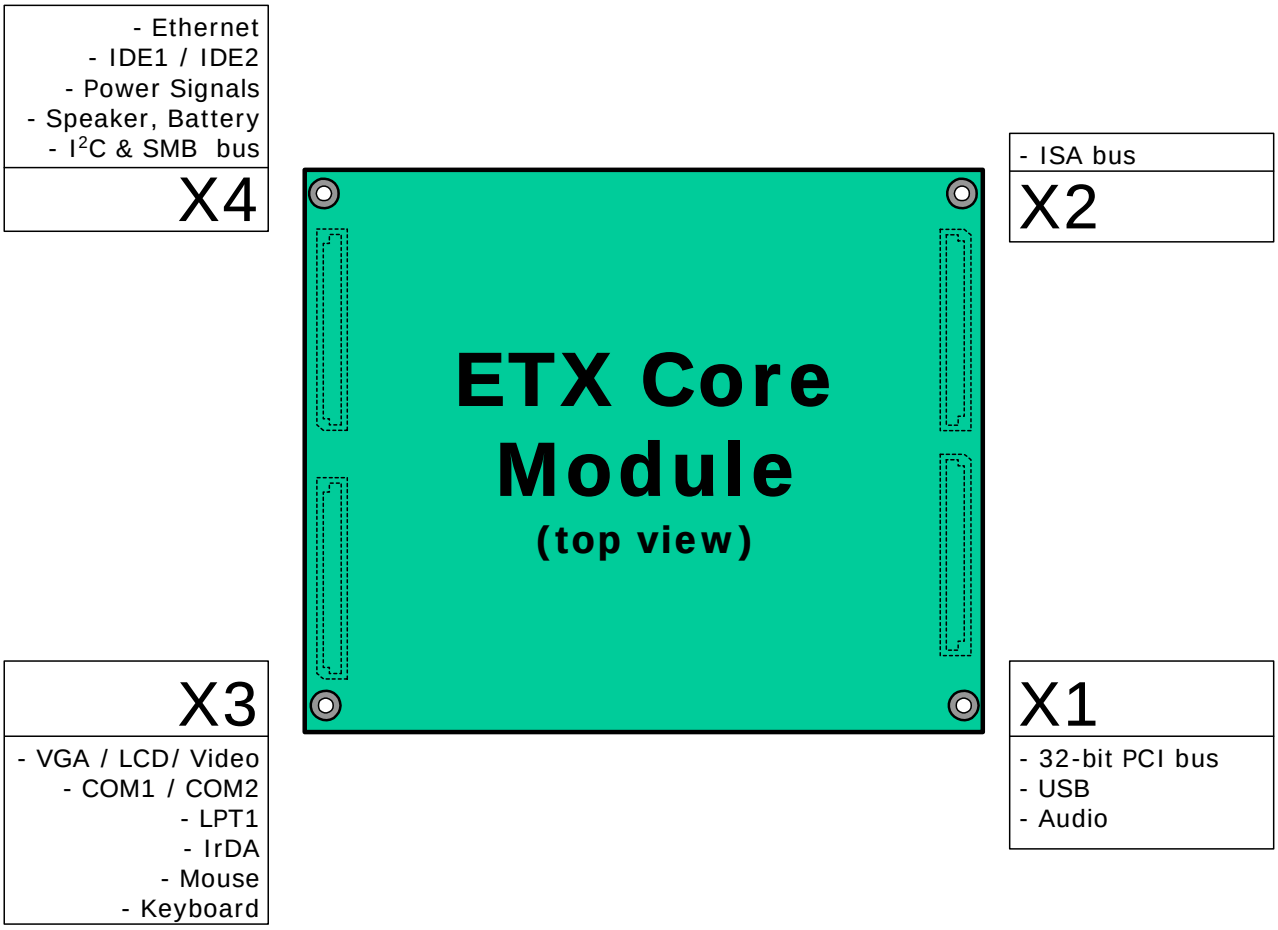
The example shown on the next page will reset the system after 15 seconds. Both keyboard and mouse interrupts will reload WDT from CRF6.

```
begin :

;-----------------------------------------------------;
Enter the extend function mode, interrupt double-write
;-----------------------------------------------------

    mov     dx,2eh
    mov     al,87h
    out     dx,al
    out     dx,al
    mov     dx,2eh
    mov     al,2bh  ; CR2B,   bit4-> 0 = WDTO
                    ; bit4-> 1 = GP24
    out     dx,al
    mov     dx,2fh
    mov     al,0c0h
    out     dx,al

    mov     dx,2eh
    mov     al,07h
    out     dx,al
    mov     dx,2fh
    mov     al,08h              ;device 8
    out     dx,al

    mov     dx,2eh
    mov     al,30h
    out     dx,al
    mov     dx,2fh
    mov     al,01h              ;enable device 8
    out     dx,al

    mov     dx,2eh
    mov     al,07h
    out     dx,al
    mov     dx,2fh
    mov     al,08h              ;device 8
    out     dx,al

    mov     dx,2eh
    mov     al,0f7h
    out     dx,al               ;device 8,CRF7
    mov     dx,2fh
    mov     al,0c0h
    out     dx,al
```

```
    mov     dx,2eh
    mov     al,07h
    out     dx,al
    mov     dx,2fh
    mov     al,08h
    out     dx,al             ;device 8

    mov     dx,2eh
    mov     al,0f5h           ;device 8, CRF5
    out     dx,al
    mov     dx,2fh
    mov     al,00h            ; bit3 -> 0 = second
                              ; bit3 -> 1 = minute
    out     dx,al

    mov     dx,2eh
    mov     al,07h
    out     dx,al
    mov     dx,2fh
    mov     al,08h
    out     dx,al             ;device 8
    mov     dx,2eh
    mov     al,0f6h           ;device 8, CRF6
    out     dx,al
    mov     dx,2fh
    mov     al,0fh
    out     dx,al

;-------------------------------------
; Exit extend function mode
;-------------------------------------

    mov     dx,2eh
    mov     al,0aah
    out     dx,al

.exit

end
```

6 Connectors

6.1 Connector Location

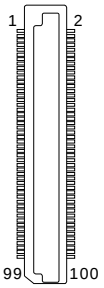


6.2 Pin-Out Compatibillity

All pin-outs on X1, X2, X3, and X4 of the ETX-IM333 comply with pin-out and signal description used in the original : “ETX Specification ver 2.6”. This document contains a description of pin-outs, signal descriptions, and mechanical characteristics of the ETX formfactor.

An additional document, “ETX Design Guide” gives a general introduction to carrier board designs for ETX modules.

6.3 X1 Connector: PCI-bus, USB, and Audio

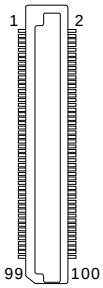


Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V
13	REQ2#	14	GNT1#
15	REQ1#	16	3V
17	GNT0#	18	RSV
19	5VCC	20	5VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SDNL
47	AD15	48	ASSGND
49	CBE1#	50	SNDR

Pin	Signal	Pin	Signal
51	5VCC	52	5VCC
53	PAR	54	SERR#
55	GPERR	56	RSV
57	PME#	58	USB2N
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3N
63	IRDY#	64	STOP#
65	FRAME#	66	USB2P
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3P
73	AD19	74	AD18
75	AD20	76	USB0N
77	AD22	78	AD21
79	AD23	80	USB1N
81	AD24	82	CBE3#
83	5VCC	84	5VCC
85	AD25	86	AD26
87	AD28	88	USB0P
89	AD27	90	AD29
91	AD30	92	USB1P
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

6.4 X2 Connector: ISA Bus

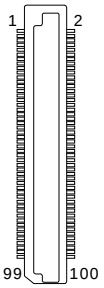


Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	NC	34	NC
35	GND	36	GND
37	NC	38	NC
39	NC	40	NC
41	NC	42	NC
43	NC	44	NC
45	NC	46	NC
47	NC	48	NC
49	NC	50	NC

Pin	Signal	Pin	Signal
51	5VCC	52	5VCC
53	NC	54	NC
55	NC	56	NC
57	NC	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC
65	NC	66	NC
67	GND	68	GND
69	NC	70	NC
71	NC	72	NC
73	NC	74	NC
75	NC	76	NC
77	NC	78	NC
79	NC	80	NC
81	NC	82	NC
83	5VCC	84	5VCC
85	NC	86	NC
87	NC	88	NC
89	NC	90	NC
91	NC	92	NC
93	NC	94	NC
95	NC	96	NC
97	NC	98	NC
99	GND	100	GND

6.5 X3 Connector: CRT, LCD, Video, COM1/2, LPT1, IrDA, Mouse, Keyboard

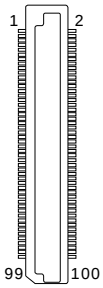


Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	NC	10	DDDA
11	LCD16	12	LCD18
13	LCD17	14	LCD19
15	GND	16	GND
17	LCD13	18	LCD15
19	LCD12	20	LCD14
21	GND	22	GND
23	LCD8	24	LCD11
25	LCD9	26	LCD10
27	GND	28	GND
29	LCD4	30	LCD7
31	LCD5	32	LCD6
33	GND	34	GND
35	LCD1	36	LCD3
37	LCD0	38	LCD2
39	5Vcc	40	5Vcc
41	NC	42	LTGO0
43	NC	44	BLON#
45	NC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

Pin	Signal	Pin	Signal
51	LPT/FDD	52	RSV
53	5Vcc	54	GND
55	STB#	56	AFD#
57	RSV	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DRT2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2	80	PD0
81	5Vcc	82	5Vcc
83	RXD1#	84	PACK#
85	RTS1#	86	BUSY#
87	DRT1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI#	98	KBDAT
99	GND	100	GND

6.6 X4 Connector: IDE1, IDE2, Ethernet, Miscellaneous



Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED
11	RSMRST#	12	ACTLED
13	NC	14	SPDLED
15	NC	16	I2CLK
17	5Vcc	18	5Vcc
19	OVCR#	20	NC
21	EXTSMI#	22	I2DAT
23	SMBCLK	24	SMBDATA
25	S_CS3#	26	SMBALRT#
27	S_CS1#	28	NC
29	S_A2	30	P_CS3#
31	S_A0	32	P_CS1#
33	GND	34	GND
35	PDIAG_S	36	P_A2
37	S_A1	38	P_A0
39	S_INTRQ	40	P_A1
41	NC	42	NC
43	S_AK#	44	P_INTRQ
45	S_RDY	46	P_AK#
47	S_IOR#	48	P_RDY
49	5Vcc	50	5Vcc

Pin	Signal	Pin	Signal
51	S_IOW#	52	P_IOR#
53	S_DRQ	54	P_IOW#
55	S_D15	56	P_DRQ
57	S_D0	58	P_D15
59	S_D14	60	P_D0
61	S_D1	62	P_D14
63	S_D13	64	P_D1
65	GND	66	GND
67	S_D2	68	P_D13
69	S_D12	70	P_D2
71	S_D3	72	P_D12
73	S_D11	74	P_D3
75	S_D4	76	P_D11
77	S_D10	78	P_D4
79	S_D5	80	P_D10
81	5Vccz	82	5Vcc
83	S_D9	84	P_D5
85	S_D6	86	P_D9
87	S_D8	88	P_D6
89	GPE2#	90	CBLID_P#
91	RXD#	92	P_D8
93	RXD	94	S_D7
95	TXD#	96	P_D7
97	TXD	98	HDRST#
99	GND	100	GND

7 System Resources

7.1 Interrupt Assignment

PCI and ISA interrupts supported by the Intel® FW82801DA South Bridge are as follows:

ISA IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
NMI	Edge	High	SERR_L asserted	
IRQ0	Edge	High	Timer0	(1)
IRQ1	Edge	High	Keyboard	
IRQ2	Edge	High	Cascade Interrupt from Slave Interrupt Controller	
IRQ3	Edge	High	COM2	(2)
IRQ4	Edge	High	COM1	(2)
IRQ5	Edge	Low	PCI PnP IRQ	
IRQ6	Edge	High		(2)
IRQ7	Edge	High	LPT1	(2)
IRQ8_L	Edge	Low	Real Time Clock	(2)
IRQ9	Edge	Low	PCI PnP IRQ	
IRQ10	Level	Low	PCI PnP IRQ	
IRQ11	Level	Low	PCI PnP IRQ, USB	(3)
IRQ12	Edge	High	Mouse	(2)
IRQ13	Edge	High	FERR_L asserted	
IRQ14	Edge	High	Primary IDE	(4)
IRQ15	Edge	High	Secondary IDE	(5)

Notes:

1. Internally generated by the FW82801DA.
2. Suggested. These interrupts are plug and play compatible and may be routed to any available interrupt.
3. The USB interrupt is internally routed to the PIRQD# input of the FW82801DA.
4. This interrupt is routed to the IRQ14 input of the FW82801DA.
5. This interrupt is routed to the IRQ15 input of the FW82801DA.

7.2 PCI Bus Arbitration Assignment

PCI Bus Request	PCI Master(s)	IDSEL
Request 0	Routed to ETX connector X1	*
Request 1	Routed to ETX connector X1	*
Request 2	Routed to ETX connector X1	*
Request 3	Routed to ETX connector X1	*

Note: IDSEL routing depends on the design of the carrier board.

7.3 PCI Interrupt Routing

Device	Net PIRQ0_L	Net PIRQ1_L	Net PIRQ2_L	Net PIRQ3_L
ETX Connector X1	PIRQA#	PIRQB#	PIRQC#	PIRQD#

7.4 Memory Map

Address	Size	Description
00000000~0009FFFF	640K	DOS Application Area
000A0000~000BFFFF	128K	Video Buffer Area
000C0000~000DFFFF	128K	Expansion Area
000E0000~000EFFFF	64K	Extended System BIOS Area
000F0000~000FFFFF	64K	System BIOS Area
00100000~DRAM Top	---	System memory area
DRAM Top ~FFFRFFFF	---	Bus area
FFFEFFFF ~ FFFFFFFF	64K	Initialization area

7.5 Direct Memory Access Channels

DMA#	Available	Description
0	Yes	
1	Yes	Unavailable if Sound Blaster is enabled with default configuration
2	Yes	because FDC not impleneted
3	Yes	Unavailable when LPT is in ECP mode
4	No	Used for Cascade
5	Yes	
6	Yes	
7	Yes	

7.6 I/O Address Map

Address	Size	Description
0000 - 001F	32 bytes	Master DMA controller
0020 - 002D	14 bytes	Master Interrupt Controller
0040 - 005F	32 bytes	Timer/Counter
0060 - 006F	32 bytes	Keyboard Controller / NMI Controller
60h	1 byte	KBC data
61h	1 byte	Misc function and Speaker control
64h	1 byte	KBC command / status
0070 - 0077	8 bytes	RTC/CMOS/NMI Controller
0078 - 007F	8 bytes	Available for system use
0080	1 byte	Reserved (Debug port)
0081 - 008F	16 bytes	DMA page registers
0090 - 0091	2 bytes	Available for system use
0092	1 byte	System Control
0093 - 009F	13 bytes	Available for system use
00A0 - 00BF	32 bytes	Slave Interrupt Controller
00C0 - 00DF	32 bytes	Slave DMA Controller
00E0 - 00FF	32 bytes	Available for system use
0100 - 0CF7		Available for system use
0CF8 -0CFB	4 bytes	PCI configuration address
0CFC - 0CFF	4 bytes	PCI configuration data
0D00 - FFFF		Available for system use

7.7 System Management Bus (I²C compatible)

Internally the SMB bus and I2C bus are one and the same. The ICH4 Southbridge support SMBDAT and SMBCLK lines that are I2C compatible.

The X4 connector has pinouts for both I2C and SMB bus. Both are connected to the same internal bus: the SMB bus. It is advisable to always connect external I2C devices to the I2C pins and SMB devices to the SMB pins to stay compatible with other modules that might support two internal busses (separate I2C and SMB bus)

Address	Function	Device
A0h	Identification Info	SODIMM0 EEPROM
AEh	CMOS setting backup	EEPROM
D2h	Timing	Clock generator

8 Phoenix Award BIOS

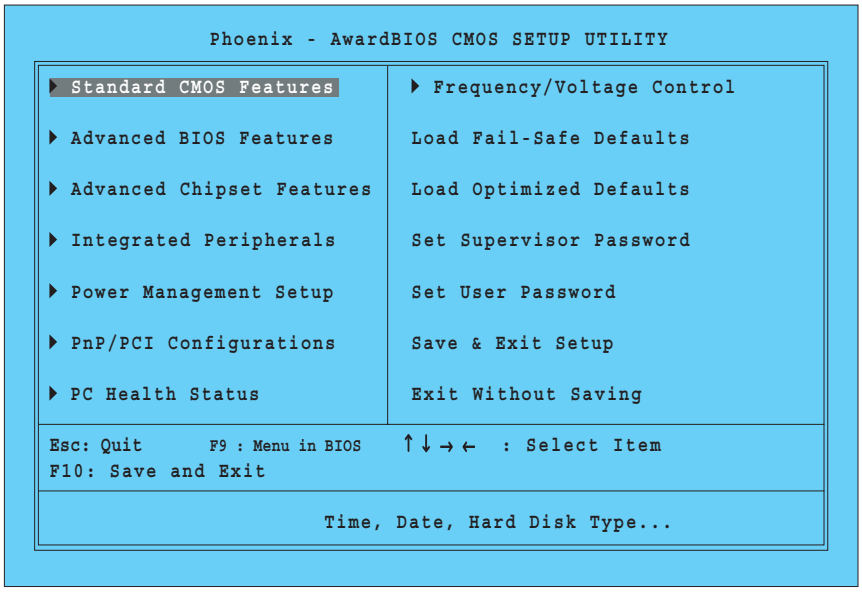
8.1 Description

The module has a Phoenix Award PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access the Phoenix AWARD PCI/ISA BIOS Setup program,

press <Del> key.

The Main Menu will then be displayed.



8.2 Main Menu Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

Standard CMOS Features (see paragraph 9.3)

Use this menu for basic system configuration.

Advanced BIOS Features (see paragraph 9.4)

Use this menu to set the Advanced Features available on your system.

Advanced Chipset Features (see paragraph 9.5)

Change values in the chipset registers and optimize your system's performance.

Integrated Peripherals (see paragraph 9.6)

Use this menu to specify your settings for integrated peripherals.

Power Management Setup (see paragraph 9.7)

Use this menu to specify your settings for power management.

PnP / PCI Configuration (see paragraph 9.8)

This entry appears if your system supports PnP / PCI.

PC Health Status (see paragraph 9.9)

Use this menu to monitor CPU and system temperatures.

Frequency/Voltage Control

Use this menu to specify your settings for frequency/voltage control.

Load Fail-Safe Defaults

Loads the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Loads the BIOS default values that are factory settings for optimal system performance.

Supervisor/User Password

Use this menu to set User and Supervisor Passwords.

Save & Exit Setup

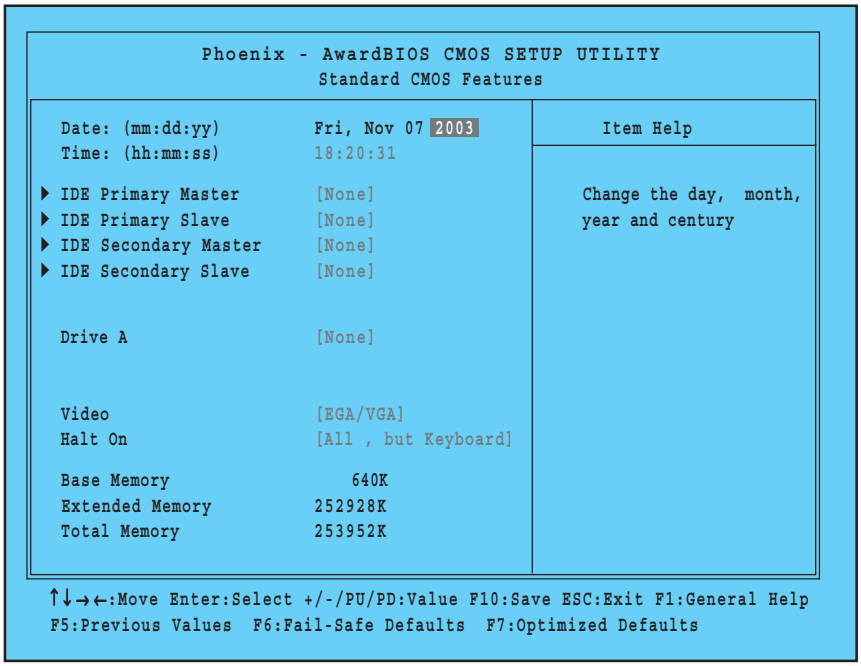
Save CMOS value changes to CMOS and exit setup.

Exit Without Saving

Abandon all CMOS value changes and exit setup.

8.3 Standard CMOS Features

The main menu includes the following main setup categories. Recall that some systems may not include all entries.



Date

The BIOS determines the day of the week from the other date information; this field is for information only.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

IDE Primary and Secondary Master/Slave Items

This selection brings up a configuration menu of the designated Drive (see next page)

Drive A

The ETX-IM333 can support one single FDD drive. Because FDD and LPT1 share the same pins on the X3 connector, only one of them can be used at a time. LPT1 or FDD can be enabled in the following BIOS menu:

▶ Integrated Peripherals ▶ Super I/O Device ▶ LPT1 Setting / FDD

This menu allows setup of LPT1 resources or disabling of LPT1 and setting the mode to FDD. After enabling the FDD, select the correct specifications for the diskette drive:

None: No diskette drive installed

360K: 5.25 inch PC-type standard drive

1.2M: 5.25 inch AT-type high-density drive

720K: 3.5 inch double-sided drive

1.44M: 3.5 inch double-sided drive

2.88M: 3.5 inch double-sided driveIDE Primary and Secondary Master/Slave Items

Video

Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but this is not selected in Setup.

Halt On

During the Power On Self Test (POST), the computer stops if the BIOS detects a hardware error. The BIOS can be instructed to ignore certain errors during POST and continue the boot-up process. The options are as follows:

No errors: POST does not stop for any errors.

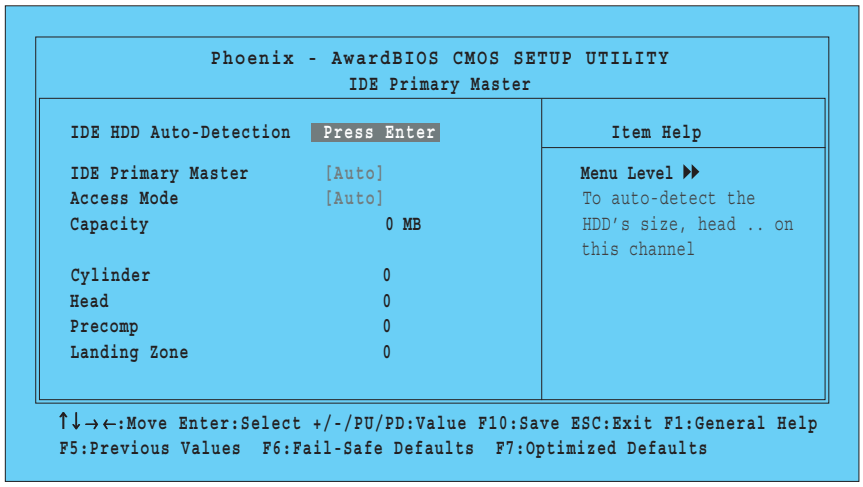
All errors: POST stops for any non-fatal error and will prompt the user to take any corrective measures.

All, But Keyboard: POST does not stop for a keyboard error, but stops for all other errors

All, But Diskette: POST does not stop for diskette drive errors, but stops for all other errors

All, But Disk/Key: POST does not stop for a keyboard or disk errors, but stops for all other errors

IDE Primary and Secondary Master/Slave Items



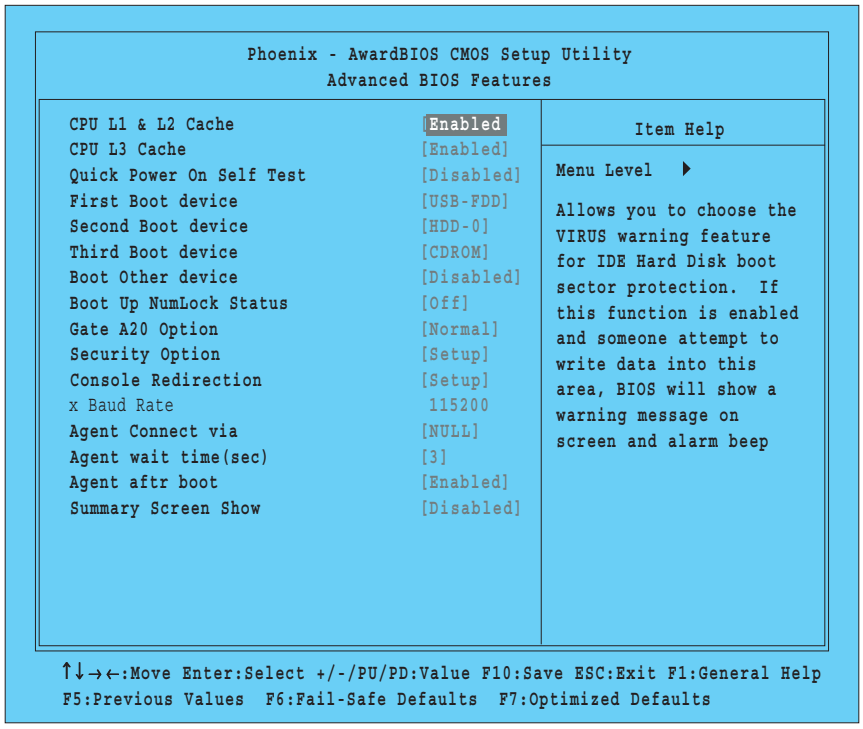
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None/Auto/Manual	Selecting 'manual' allows the user to set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE.
Capacity	Auto Display disk size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	CHS/LBA/Large/Auto	Choose the access mode for this hard disk

The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** Warning: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

8.4 Advanced BIOS Features

This section allows the user to configure the system for basic operation. The following features can be selected here: system default speed, boot-up sequence, keyboard operation, shadowing, security, and CPU Internal Cache/CPU External Cache.



CPU L2 Cache ECC Checking

This function enables/disables CPU L2 Cache ECC checking. Options: Enabled, Disabled.

Quick Power On Self Test

This category speeds up the Power On Self Test (POST). If enabled, BIOS will shorten or skip some check items during POST. Options: Enabled: enables quick POST. Disabled: normal POST.

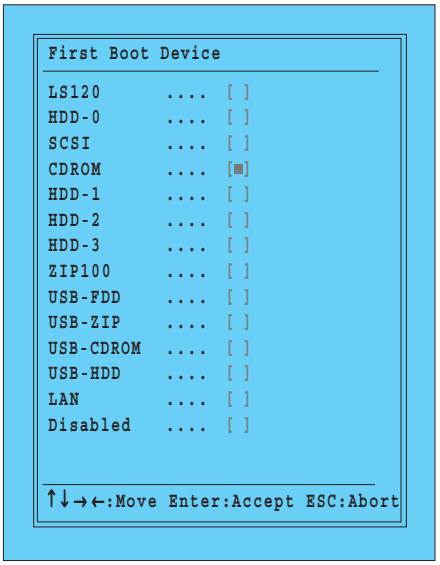
First/Second/Third Boot Device

Pressing Enter brings up the Boot Device Menu. The BIOS attempts to load the operating system from the selected device.

See menu for possible options

Boot Other Device

When enabled, the BIOS will try to boot from second or third option if booting from first device fails. When disabled the BIOS will not use the alternative devices



Boot Up NumLock Status

Select power on state for NumLock. Options: On/Off

Gate A20 Option

Select if chipset or keyboard controller should control GateA20.
Normal: A pin in the keyboard controller controls GateA20
Fast: Lets chipset control GateA20

Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected. Options: Enabled/Disabled.

Typematic Rate (Chars/Sec)

Sets the number of times per second to repeat a key stroke when holding down the key. Options: 6, 8, 10, 12, 15, 20, 24, and 30.

Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. Options: 250, 500, 750, and 1000.

Security Option

Select whether the password is required every time the system boots or only when you enter setup. Chioces :

System: The system will not boot and access to Setup will be denied if an incorrect password is entered at the prompt.

Setup: The system will boot, but access to Setup will be denied if an incorrect password is not entered at the prompt.

To disable security, select PASSWORD SETTING in Main Menu. The user will then be prompted to enter the password. Do not type anything and press <Enter> to disable security. Once security is disabled, the system will boot and Setup can be entered freely.

OS Select For DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system. Options: Non-OS2, OS2.

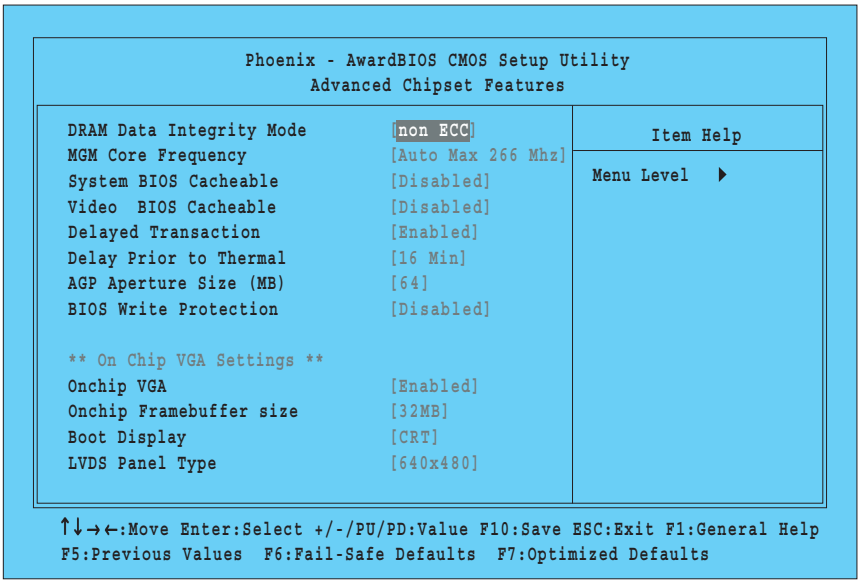
Video BIOS Shadow

Enables copying of Video BIOS to shadow RAM. Improves performance.

Summary Screen Show

Suppress the summary screen. Options: Enable, Disable

8.5 Advanced Chipset Features



DRAM Data Integrity Mode

ECC, which stands for Error Checking and Correction, enables the memory controller to detect and correct single-bit soft memory errors. The memory controller will also be able to detect double-bit errors though it will not be able to correct them. This provides increased data integrity and system stability. However, this feature can only be enabled if you are using special ECC memory modules.

Display may flicker when integrated graphics and ECC support are enabled !

Memory with ECC enabled requires more system memory resources. This will cause the integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer. Display flicker and flashing may occur when ECC is enabled under high-resolution graphics modes.

MGM Core Frequency

This field is to select the FSB Speed / Memory Speed / GFX Low / GFX high core frequency. Default is Automax Max 266.

System BIOS Cacheable

Selecting Enabled allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

Video RAM Cacheable

Select Enabled allows caching of the video RAM, resulting in better system performance. However, if any program writes to this memory area, a system error may result.
Options: Enabled, Disabled, Fast R-W Turn Around.

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.

Delay Prior to Thermal

When the Thermal Monitor is in automatic mode and the thermal sensor detects that the processor has reached its maximum safe operating temperature, it will activate the TCC. The TCC will then modulate the clock cycles by inserting null cycles, typically at a rate of 50-70% of the total number of clock cycles. This results in the processor "resting" 50-70% of the time.

As the die temperature drops, the TCC will gradually reduce the number of null cycles until no more is required to keep the die temperature below the safe point. The thermal sensor then turns the TCC off. This mechanism allows the processor to dynamically adjust its duty cycles to ensure its die temperature remains within safe limits.

The Delay Prior To Thermal BIOS feature controls the activation of the Thermal Monitor's automatic mode. It allows the user to determine when the CPU's Thermal Monitor should be activated in automatic mode after the system boots. For example, with the default value of 16 minutes, the BIOS activates the Thermal Monitor in automatic mode 16 minutes after the system starts booting up.

Generally, the Thermal Monitor should not be activated immediately on booting as the processor will be under a heavy load during the booting process. This causes a sharp rise in die temperature from its cold state. Because it takes time for the thermal output to radiate from the die to the heat sink, the thermal sensor will register the sudden spike in die temperature and prematurely activate the TCC. This unnecessarily reduces the processor's performance during the booting up process.

Therefore, to ensure optimal booting performance, the activation of the Thermal Monitor must be delayed for a set period of time.

It is recommended that this BIOS feature is set to the lowest value (in minutes) that exceeds the time it takes to fully boot up your computer. For example, if it takes 5 minutes to fully boot up your system, you should select 8 minutes.

You should not select a delay value that is unnecessarily long. Without the Thermal Monitor, the processor may heat up to a critical temperature (approximately 135°C), at which point the thermal sensor shuts down the processor by removing the core voltage within 0.5 seconds.

AGP Aperture Size (MB)

Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. Default is 64 MB.
Options: 4M, 8M, 16M, 32M, 65M, 128M, 256M.

BIOS Write Protection

This is a security feature that when enabled prohibits the user to Flash the BIOS. The default setting is Disabled.

Onchip VGA

Can enable or disable the intgrated VGA core. The default setting is Enabled.

Onchip Framebuffer size

The selection lets you configure how much system memory you want to allocate to the integrated GPU. The amount you allocate to the GPU is deducted from the amount of system memory available to your operating system and programs.

Do not assign more memory than absolutely required by the current VGA mode.
For example a resolution of 1600x1200 and colour depth of 32-bit,
amounts to 1600 x 1200 x 32-bits = 61,440,000 bits or 7.68MB.
Set to 8MB in this example.

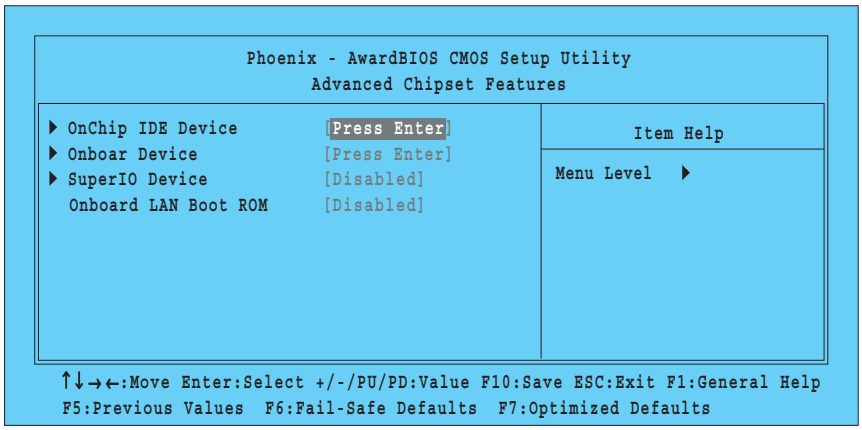
Display Feature

This item allows the user to configure the type of external display used.
Options: CRT, LVDS (displays cannot be used concurrently)

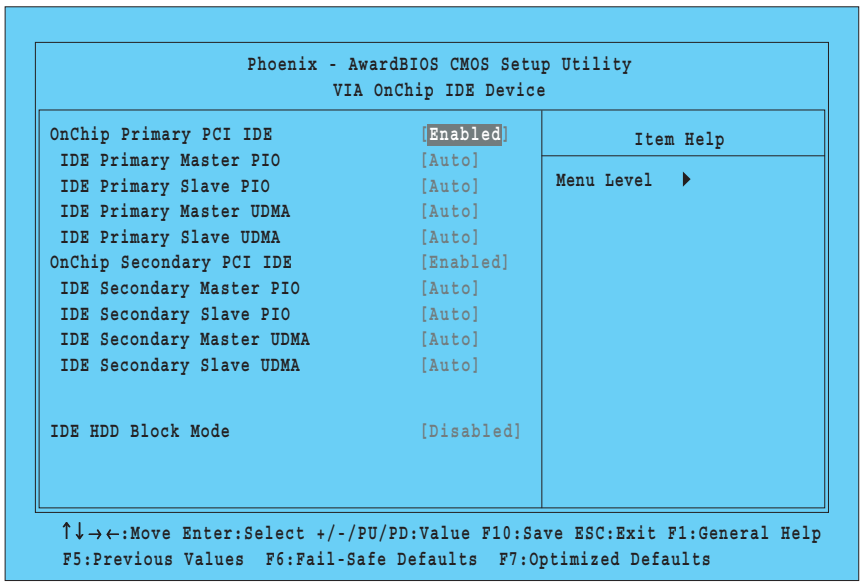
LVDS Panel Type

When LVDS is selected in “Display Feature”, tthe flat panel resolution can be selected.
Options: 640x480 ,800x600, 1024x768, and 1280x1024.

8.6 Integrated Peripherals



OnChip IDE Device *(submenu)*



OnChip Primary/Secondary PCI IDE

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary/secondary IDE interface. Select Disabled to deactivate these interfaces.

Primary & Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields allows the user to set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. Options: Auto, Mode 0, Mode 1, Mode 2, Mode 3, Mode 4.

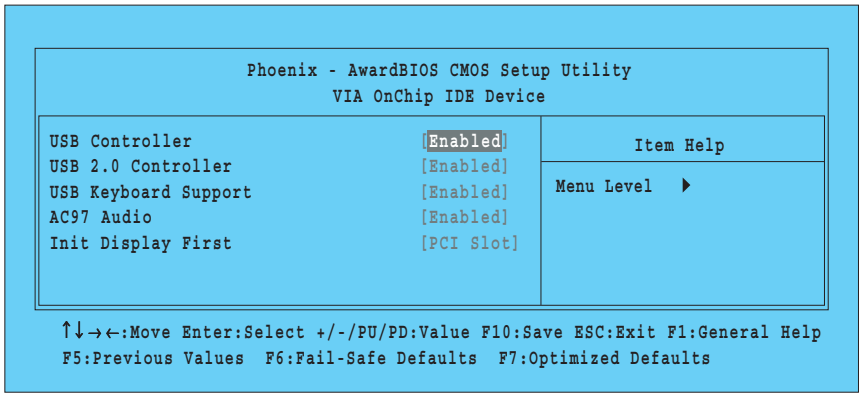
IDE Primary & Secondary Master/Slave UDMA

Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver. If your hard drive and your system software both support Ultra DMA, select Auto to enable BIOS support.

IDE HDD Block Mode

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

OnChip PCI Device (submenu)



USB Controller

This should be enabled to use the internal USB function. Enabling only results in USB 1.1 functionallity. To also obtain USB 2.0 functionallity the “USB 2.0 Controller” setting will also have to be enabled. Options: Enabled, Disabled.

USB 2.0 Controller

This enables USB 2.0 support on the USB controller. Options: Enabled, Disabled.

USB Keyboard Support

Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard. Options: Enabled, Disabled.

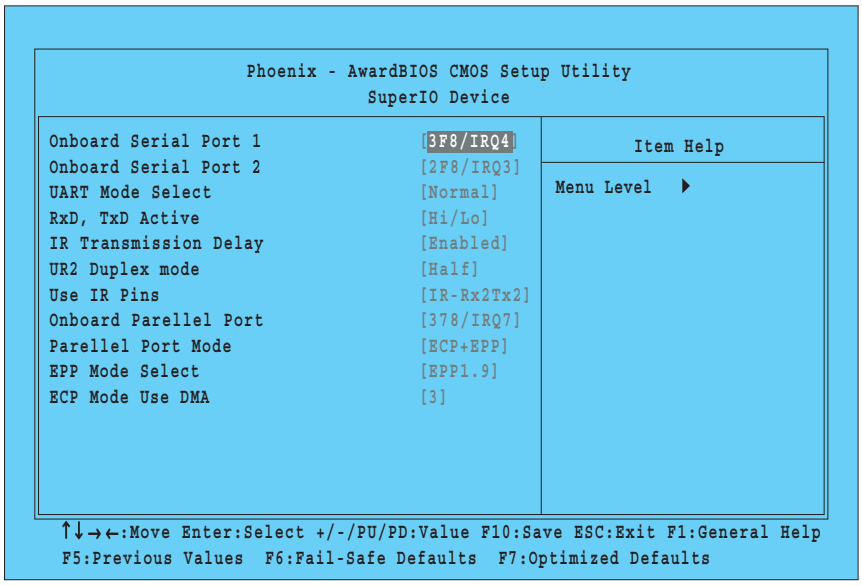
AC ‘97 Audio

This item allows you to control the onboard AC 97 audio. Options: Enable, Disabled.

Init Display First

This BIOS feature allows you to select whether to boot the system using the embedded AGP graphics core or a possible PCI graphics card.

Super I/O Device



Onboard Serial Port 1/2

Select address and interrupt for the serial ports.

UART Mode Select

The serial port 2 on your system offers a varierty of infrared modes. There are two different IR (Infra-Red) modes - IrDA and ASK IR. Select the IR mode that is supported by your external IR device. Choosing the wrong IR mode will prevent your computer from communicating with the external IR device.

RxD, TxD Active

This BIOS feature allows you to set the infra-red reception (RxD) and transmission (TxD) polarity.

IR Transmission Delay

When UART Mode is selected in IrDA or ASKIR mode, it allows the user to enable / disable IR Transmission Delay.

UR2 Duplex Mode

This options controls the operating mode between receiving and transmitting of IrDA or ASKIR. The operating mode will be synchronous bi-directional transmission and reception when Full mode is selected. The operating mode will be asynchronous bi-directional transmission and reception when Half mode is selected. Options: Half; Full

LPT1 Setting / FDD

This setting allows the user to assign resources to LPT1 or disable the function and allow using an FDD drive. Since share LPT1 and FDD share the same pins on the X3 connector, only one of them can be used at a time.

EPP Mode Select

There are two versions of the EPP transfer protocol - EPP 1.7 and EPP 1.9. This BIOS feature allows the user to select the version of EPP that the parallel port should use.

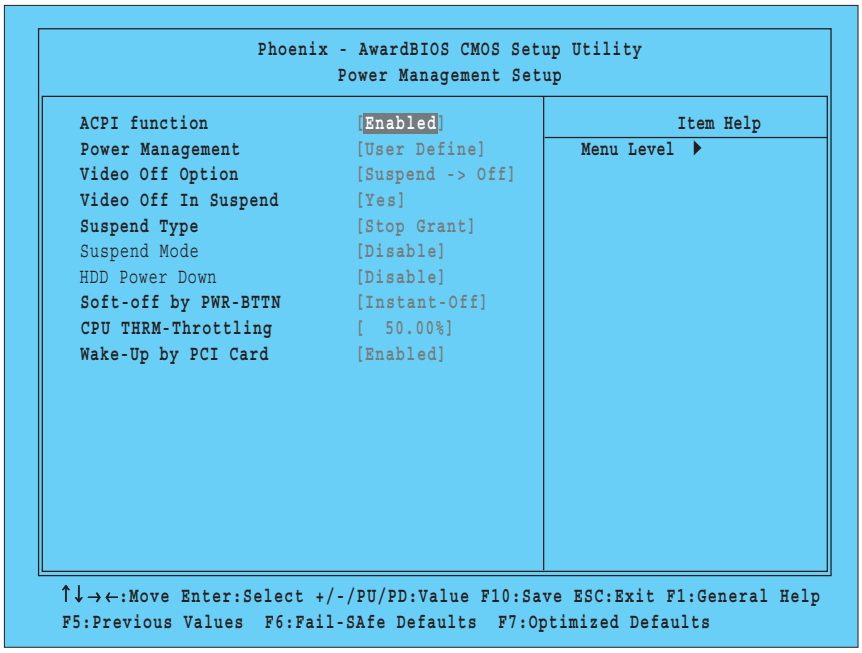
Generally, EPP 1.9 is the preferred setting because it supports the newer EPP 1.9 devices and most EPP 1.7 devices, while offering other advantages such as support for longer cables. However, because certain EPP 1.7 devices cannot work properly with an EPP 1.9 port, this BIOS feature was implemented to allow the user to set the EPP mode to EPP 1.7 when this occurs.

Therefore, it is recommended that you sets this BIOS feature to EPP 1.9. However, if there are problems connecting to the parallel port devices, switch to EPP 1.7.

ECP Mode Use DMA

This BIOS feature determines which DMA channel the parallel port should use when it is in ECP mode. The ECP mode uses the DMA protocol to achieve data transfer rates of up to 2.5 Mbits/s and provides symmetric bidirectional communications. For all this, it requires the use of a DMA channel.

8.7 Power Management Setup



ACPI Function

Select Enabled only if the computer's operating system supports ACPI (Advanced Configuration and Power Interface) specification.

Power Management

User Defined Allows the user to set Suspend Mode manually.

Min. Power Saving: Minimum power management. Suspend Mode = 1 hr

Max. Power Saving: Maximum power management. Suspend Mode = 1 min. (ONLY AVAILABLE FOR SL CPU's)

Video Off Method

This determines the manner in which the monitor is blanked.

Blank Screen: This option only writes blanks to the screen.

V/H SYNC+Blank: Causes the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.

DPMS Support: Display power management signaling.

Video Off in Suspend

When enabled, the video is turned off in suspend mode.

Suspend Mode

Select the Suspend Type. Options: PWRON Suspend, Stop Grant.

Suspend Type

When enabled and after the set time of system inactivity, all devices except CPU are shut off.

HDD Power Down

After the selected period of drive inactivity, the hard disk drive powers down while all other devices remain active.

Soft-Off By PWR-BTTN

The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means the system will be powered off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is held down for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when the power button is held down for less than four seconds. The default is 'Instant-Off'.

State After Power Failure

On: After a power failure, the system will automatically reboot as soon as power is re-stored.

Off: After a power failure, the system will not reboot when power is restored. The system needs to be turned on again manually.

Auto: After a power failure, the system will automatically reboot as soon as power is restored if the PC was turned on when the power failed. If the PC was already turned off when the power failed, the system needs to be turned on again manually.

CPU THRM-Throttling

Thermal Throttling, if enabled (default), is a safety feature against overheating that throttles a processor back as it reaches its maximum operating temperature. Throttling does not change the processor speed but instead reduces the number of available processing cycles, thereby reducing the heat dissipation of the CPU. This cools down the CPU. Once the CPU has once again reached a safe operating temperature, thermal throttling is automatically disabled, and normal full speed processing resumes.
Options: Disabled, 87.5%, 75.0%, 62.5%, 50.0%, 37.5%, 25.0%, 12.5%

Wake-Up by PCI Card

This field should be set to Enabled only if your PCI card (e.g. LAN or modem card) uses the PCI PME (Power Management Event) signal to remotely wake up the system. Accessing the PCI card will cause the system to wake up. Refer to the card's documentation for more information. If set to Disabled, the system will not wake up if the PCI card accessed.

Set CPU Speed/Voltage

This setting is only available for Pentium® M 1.6, 1.8, and 2.0 GHz CPUs (both soldered and socket types).

To reduce overall power consumption or set a hard limit for thermal reasons, this BIOS setting lets you lower the CPU Speed/Voltage. The OS itself cannot override settings in the BIOS, but some Speedstep related software can please read below.

Although the BIOS supports all Pentium® and Celeron® M CPU's, CPU Speed/Voltage switching is only supported for the Pentium® CPUs shown in the table below. Upon bootup, the BIOS auto-detects the CPU type and speed and inserts the correct Speed/Voltage table into the BIOS selection menu.

The default Speed/Voltage settings are shown in **red bold**. These values are used when either "Load Failsafe Defaults" or "Load Optimized Defaults" are applied. Higher Speed/Voltage settings must be set manually.

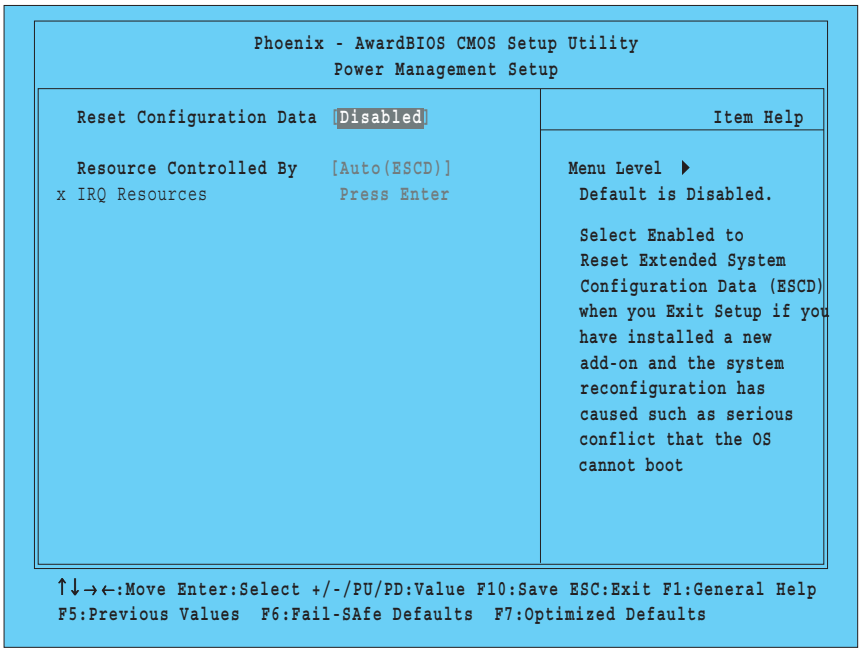
Banias type	Dothan Type	
1.6 GHz	1.8 GHz	2.0 GHz
1.60GHz/1.484V	1.80GHz/1.324V	2.00GHz/1.324V
1.40GHz/1.420V	1.60GHz/1.276V	1.80GHz/1.276V
1.20GHz/1.276V *	**1.40GHz/1.212V** *	1.60GHz/1.228V
1.00GHz/1.164V	1.20GHz/1.164V	**1.40GHz/1.180V** *
800MHz/1.036V	1.00GHz/1.100V	1.20GHz/1.132V
600MHz/0.956V	800MHz/1.052V	1.00GHz/1.084V
	600MHz/0.988V	800MHz/1.036V
		600MHz/0.988V

* Recommended max. speed/voltage when using heatspreader. These values are used when either "Load Failsafe Defaults" or "Load Optimized Defaults" are applied.

WARNING

When certain operating systems are installed, such as Windows XP with Service Pack 2, the above BIOS settings may be automatically overridden by native support for dynamic voltage and frequency switching. This means that the CPU may be switched to a higher frequency and voltage than is specified by the BIOS.

8.8 PnP/PCI Configurations



This section describes the configuring of the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

Reset Configuration Data

Normally, this field is left Disabled. Select Enabled to reset ESCD (Extended System Configuration Date) upon exiting Setup if a new add-on has been installed and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

Resource Controlled By

The Award Plug and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If Auto is selected, all interrupt requests (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

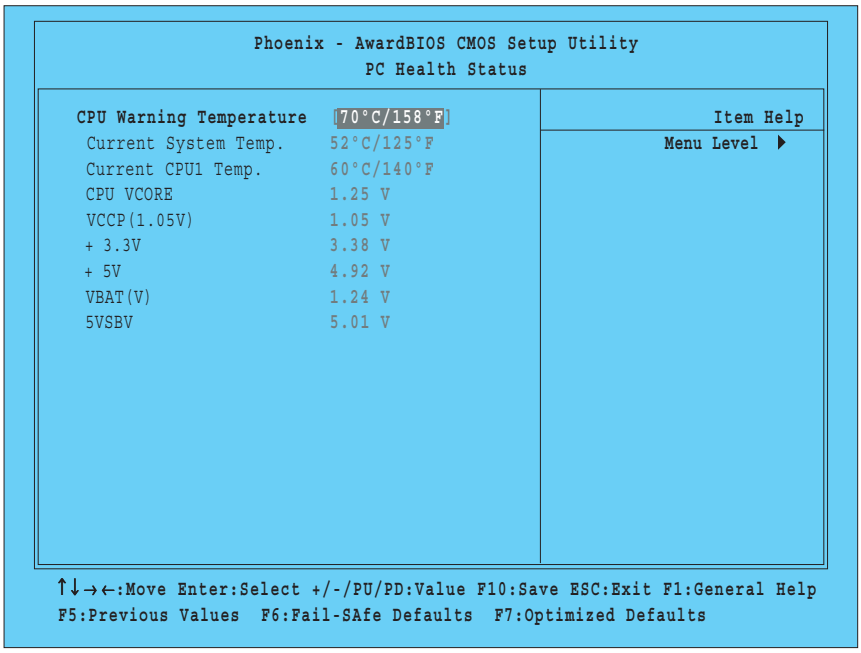
IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

Legacy ISA
Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP
Device complies with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

8.9 PC Health Status



CPU Warning Temperature

Brings up a submenu that lets the user assign a temperature level that is not to be exceeded by the CPU. If the CPU temperature goes over this limit, an audible warning signal sounds.

Current System Temp.

Displays the current system temperature.

Current CPU1 Temp.

Displays the current CPU temperature.

CPU VCORE, VCCP(1.05V), + 3.3V, + 5V, VBAT(V), and 5VSBV

Displays the actual voltage levels on the board.

8.10 BIOS POST Messages

If BIOS detects an error during the Power On Self-Test (POST), it will prompt the user by either sounding a beep code or displaying a message. If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, OR DEL TO ENTER SETUP

POST Beep

Currently there are two kinds of beep codes in BIOS :

- This first beep code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.
- The second beep code indicates that a DRAM error has occurred. This beep code consists of a repeated single long beep.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

- CMOS CHECKSUM ERROR - DEFAULTS LOADED
  Checksum of CMOS is incorrect. This may indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.
- DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER
  No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Reboot the system.
- DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP
  Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.
- DISPLAY SWITCH IS SET INCORRECTLY
  Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

- FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT
  Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

- KEYBOARD ERROR OR NO KEYBOARD PRESENT
  Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

- OFFENDING ADDRESS NOT FOUND
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

- OFFENDING SEGMENT:
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

- PRESS A KEY TO REBOOT
  This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

- PRESS F1 TO DISABLE NMI, F2 TO REBOOT
  When BIOS detects a Non-Maskable Interrupt condition during boot, you can choose to disable the NMI and continue to boot, or you can reboot the system with NMI enabled.

- RAM PARITY ERROR - CHECKING FOR SEGMENT ...
  Indicates a parity error in Random Access Memory.

- SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ..
  Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

- Memory test fail.
  BIOS reports the memory test as failed if the onboard memory test results in an error.

8.11 BIOS POST Codes

Normal POST Codes

POST (hex)	Name	Description
C0	Turn Off Chipset And CPU test	OEM Specific-Cache control cache Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, overflow, The BIOS sets each flag, verifies they are set, then turns each flag off and verifies it is off. Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00. RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory Presence	First block memory detect OEM Specific-Test to size onboard memory. Early chip set initialization Memory presence test OEM chip set routines Clear low 64K of memory Test first 64K memory.
C2	Early Memory Initialization	OEM Specific- Board Initialization
C3	Extend Memory DRAM select	OEM Specific- Turn on extended memory
		Initialization Cyrix CPU Initialization Cache initialization
C4	Special Display Handling	OEM Specific- Display/Video Switch Handling so that Switch Handling display switch errors never occurs
C5	Early Shadow	OEM specific- Early shadow enable for fast boot
C6	Cache presence test	External cache size detection
CF	CMOS Check	CMOS checkup
B0	Spurious	If interrupt occurs in protected mode
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot
BF	Program Chip Set	To program chipset from default values
E1-EF	Setup Pages	E1- Page 1, E2 - Page 2, etc.

POST (hex)	Name	Description
1	Force load Default	Chipset defaults program to chipset
2	Reserved	
3	Early Superio Init	Early Initialized the Super I/O
4	Reserved	
5	Blank video	Reset Video controller
6	Reserved	
7	Init KBC	Keyboard controller init
8	KB test	Test the Keyboard
9	Reserved	
A	Mouse Init	Initialized the mouse
B	Onboard Audio init	Onboard audio controller initialize if exist
C	Reserved	
D	Reserved	
E	CheckSum Check	Check the integrity of the ROM,BIOS and message
F	Reserved	
10	Auto detec EEPROM	Check Flash type and copy flash write/erase routines to 0F000h segments
11	Reserved	
12	Cmos Check	Check Cmos Circuitry and reset CMOS
13	Reserved	
14	Chipset Default load	Program the chipset registers with CMOS values
15	Reserved	
16	Clock Init	Init onboard clock generator
17	Reserved	
18	Identify the CPU	Check the CPU ID and init L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup Interrupt	Initialize first 120 interrupt Vector Table vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM Init	First step initialize if single CPU onboard
1E	Reserved	
1F	Re-initial KB	Re-init KB
20	Reserved	
21	HPM init	If support HPM, HPM get initialized here
22	Reserved	
23	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset
24	Reserved	
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initial KBC and setup BIOS data area
28	Reserved	
29	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.

POST (hex)	Name	Description
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Test video memory, write sign-on message to screen Setup shadow RAM - Enable shadow according to Setup.
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 Mouse setup	Setup PS2 Mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Test DMA channel 0
36	Reserved	
37	Test DMA Controller 1	Test DMA channel 1
38	Reserved	
39	Test DMA Page Registers	Test DMA Page Registers.
3A	Reserved	
3B	Reserved	
3C	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
3D	Reserved	
3E	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
3F	Reserved	
40	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
41	Reserved	
42	Reserved	
43	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no interrupt mask register is on.
	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred.
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests and clear EISA mode flag.
48	Reserved	
49	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.

POST (hex)	Name	Description
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns. NOTE: This test is skipped in EISA mode and can be skipped with ESC key in ISA mode.
4F	Reserved	
50	USB init	Initialize USB controller
51	Reserved	
52	Memory Test	Test all memory of memory above 1MB using Virtual 8086 mode, page mode and clear the memory
53	Reserved	
54	Reserved	
55	CPU display	Detect CPU speed and display CPU vendor specific version string and turn on all necessary CPU features
56	Reserved	
57	PnP Init	Display PnP logo and PnP early init
58	Reserved	
59	Setup Virus Protect	Setup virus protect according to Setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializing onboard Super I/O
5E	Reserved	
5F	Reserved	
60	Setup enable	Display setup message and enable setup functions
61	Reserved	
62	Reserved	
63	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
64	Reserved	
65	PS2 Mouse special	Special treatment to PS2 Mouse port
66	Reserved	
67	ACPI init	ACPI sub-system initializing
68	Reserved	
69	Setup Cache Controller	Initialize cache controller.
6A	Reserved	
6B	Setup Entering	Enter setup check and auto configuration check up
6C	Reserved	
6D	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives.
6E	Reserved	

POST (hex)	Name	Description
6F	FDD install	Install FDD and setup BIOS data area parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialize Hard Drive & Controller	Initialize hard drive controller and any drives.
74	Reserved	
75	Install HDD	IDE device detection and install
76	Reserved	
77	Detect & Initialize Serial/Parallel Ports	Initialize any serial and parallel ports (also game port).
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
7B	Reserved	
7C	HDD Check for Write protection	HDD check out
7D	Reserved	
7E	Reserved	
7F	POST error check	Check POST error and display them and ask for user intervention
80	Reserved	
81	Reserved	
82	Security Check	Ask password security (optional).
83	Write CMOS	Write all CMOS values back to RAM and clear screen.
84	Pre-boot Enable	Enable parity checker Enable NMI, Enable cache before boot.
85	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
86	Reserved	
87	Reserved	
88	Reserved	
89	Reserved	
8A	Reserved	
8B	Reserved	
8C	Reserved	
8D	Reserved	
8E	Reserved	
8F	Reserved	
90	Reserved	
91	Reserved	

POST (hex)	Name	Description
92	Reserved	
93	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
94	Final Init	Final init for last micro details before boot
95	Special KBC patch	Set system speed for boot Setup NumLock status according to Setup
96	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1) Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2) All ADLINK products come with a two-year guarantee:
   - The warranty period starts from the product's shipment date from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.
3) Our repair service is not covered by ADLINK's two-year guarantee in the following situations:
   - Damage caused by not following instructions in the user's manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - Other categories not protected under our warranty.
4) Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5) To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy/. Damaged products with attached RMA forms receive priority.

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