TIP500

Optically Isolated
16 Channel 12 Bit ADC
Version 1.0 Revision A

User Manual

Issue 1.2

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D75500801

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TEWS DATENTECHNIK

TIP500-10
optically isolated
16 channel 12 bit ADC
input voltage range ±10V
gain 1, 2, 5, 10

TIP500-11
optically isolated
16 channel 12 bit ADC
input voltage range ±10V
gain 1, 2, 4, 8

TIP500-20
optically isolated
16 channel 12 bit ADC
input voltage range 0V to +10V
gain 1, 2, 5, 10

TIP500-21
optically isolated
16 channel 12 bit ADC
input voltage range 0V to +10V
gain 1, 2, 4, 8

This manual covers all products

Issue	Description	Date
1.0	First issue	07. Feb. 1996
1.1	Technical Spec.	03. April 1996

This product has been designed to operate with IndustryPack® compatible carriers. Connection to incompatible hardware is likely to cause serious damage.

TEWS DATEN*TECHNIK* GmbH is not liable for any damage arising out of the application or use of the device described herin.

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1. Product Description

The TIP500 is an IndustryPack® compatible module providing a galvanically isolated 16 channel multiplexed 12 bit ADC with on board DC/DC converter.

Data acquisition and conversion time is mode dependent: up to 10 µs without channel / gain change and up to 12.5 µs with channel / gain change.

The 16 input channels of the multiplexer can be configured by software to operate either in single ended mode or in differential mode with eight inputs. The multiplexer of the ADC circuit is over voltage protected up to 70 V_{p-p}. A programmable gain amplifier allows gains of 1, 2, 5, 10 (TIP500-10/-20) or 1, 2, 4, 8 (TIP500-11/-21) . The full scale input range is ±10V for the TIP500-10/-11 and 0V to 10V for the TIP500-20/-21 (for a gain of 1).

Each TIP500 is calibrated at the factory. Calibration information is stored in the Identification PROM unique to each IP.

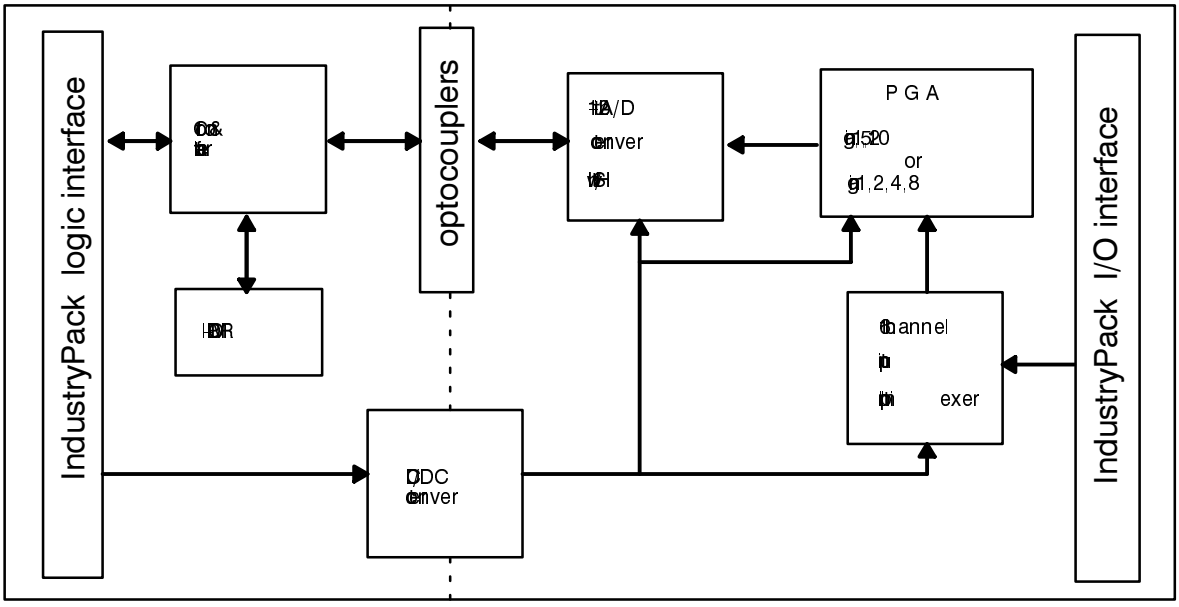


Figure 1: TIP500 Block Diagram

2. Technical Specification

Logic Interface	IndustryPack® Logic Interface
Size	single wide IP
I/O Interface	50-conductor flat cable
Analog Inputs	16 single ended channels or 8 differential channels
Input Isolation	All channels are galvanically isolated from the IP Interface. DC/DC converter on board.
Input Gain Amplifier	Programmable for gain 1, 2, 5, 10 (TIP500-10 and TIP500-20) Programmable for gain 1, 2, 4, 8 (TIP500-11 and TIP500-21)

Input Voltage Range

TIP500-10:	TIP500-20:	
±10V,	0V to 10V	(gain = 1)
±5V ,	0V to 5V	(gain = 2)
±2V ,	0V to 2V	(gain = 5)
±1V ,	0V to 1V	(gain = 10)

TIP500-11:	TIP500-21:	
±10V,	0V to 10V	(gain = 1)
±5V,	0V to 5V	(gain = 2)
±2.5V,	0V to 2.5V	(gain = 4)
±1.25V,	0V to 1.25V	(gain = 8)

Input Over Voltage	Input over voltage protection up to 70V p-p
Input ADC	12 bit ADC; data acquisition and conversion time up to 10µs without channel / gain change and up to 12.5µs with channel / gain change (mode dependent).
Calibration Data	Calibration data for gain and offset correction in ID PROM
Accuracy	± 1LSB, after calibration for all TIP500 Modules.
Linearity	± 1LSB for all TIP500 Modules
Wait States	$\overline{\text{IDSEL}}$ 1 wait state $\overline{\text{IOSEL}}$ 0 wait state $\overline{\text{INTSEL}}$ 0 wait state
Power Requirements	typ. 310 mA @ 5V
Temperature Range	Operating -40°C to 85°C Storage -45°C to 125°C
Humidity	5 - 95% non-condensing

3. Functional Description

3.1. Analog Input

The TIP500 provides 16 single ended or 8 differential multiplexed analog inputs for. The desired input and the mode (single ended or differential) is selected by programming the input multiplexer.

A software programmable gain amplifier with gain settings of 1, 2, 5 and 10 for the TIP500-10, -20 and 1, 2, 4 and 8 for the TIP500-11, -21 allows a direct connection of a wide range of sensors and instrumentation. The maximum analog input voltage range is ±10V at a gain of 1 for the TIP500-10 and TIP500-11. For the TIP500-20 and -21 the maximum analog input voltage range is 0V to 10V at a gain of 1.

The ADC is a 12 bit ADS7808 with a maximum sample and conversion time of 10µs . The 12 bit data are alined in the bits 15-4 of a 16 bit data word, bits 3-0 are always zero.

In multiplexed analog input systems a settling time must expire before the data can be converted after the change of the input channel. This settling time is depended on the programmed gain. At the most analog input solutions it is the responsibility of the user to observe the settling time. The TIP500 module has an Automatic Settling Time Control mode. If this mode is enabled, a write to the ADC Control Register, which is necessary to select a new input channel by the multiplexer, initiates a data conversion automatically after the settling time has expired.

The absolute accuracy of the module is increased by using the possibility to correct the data by software with factory calibration factors, which are stored in the individual ID PROM of the module.

3.2. Data Correction

There are two errors which affect the DC accuracy of the ADC. The first is the zero error (offset). This is the data value when converting with the input connected with its own ground in single ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from all readings.

The second error is the gain error. Gain error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. It is corrected by multiplying the data value by a correction factor.

The data correction values are obtained during factory calibration and are stored in the modules individual version of the ID PROM. The ADC has a pair of offset and gain correction values for each of the programmable gains.

The correction values are stored in the ID PROM as two's complement byte wide values in the range -128 to 127. For higher accuracy they are scaled to ¼ LSB.

3.2.1. ADC Correction Formula

The basic formula for correcting any ADC reading for the **TIP500-10 / -11** (input voltage range +/- 10V) is :

$$\mathbf{Value = Reading * (1 - Gain_{corr} / 8192) - Offset_{corr} * 4}$$

The basic formula for correcting any ADC reading for the **TIP500-20 / -21** (input voltage range 0V to 10V) is:

$$\mathbf{Value = Reading * (1 - Gain_{corr} / 16384) - Offset_{corr} * 4}$$

Value is the corrected result, Reading is the data read from the ADC, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

$Gain_{corr}$ and $Offset_{corr}$ correction factors are stored for each for the possible gain settings.

Note

Floating point arithmetics or scaled integer arithmetics is necessary to avoid rounding error while computing above formula.

4. ID Prom Contents

ADDRESS	FUNCTION	
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 18
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 15
$ 17	C R C	$ variable
$ 19	Version -10	$ 0A
$ 1B	Offset Error at Gain = 1	$ board dependent
$ 1D	Offset Error at Gain = 2	$ board dependent
$ 1F	Offset Error at Gain = 5	$ board dependent
$ 21	Offset Error at Gain = 10	$ board dependent
$ 23	Gain Error at Gain = 1	$ board dependent
$ 25	Gain Error at Gain = 2	$ board dependent
$ 27	Gain Error at Gain = 5	$ board dependent
$ 29	Gain Error at Gain = 10	$ board dependent
$ 2B	Not used	$ 00
.....		.....
$ 3F		$ 00

Figure 2: ID PROM Contents TIP500-10 V1.0

ADDRESS	FUNCTION	
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 18
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 15
$ 17	C R C	$ variable
$ 19	Version -11	$ 0B
$ 1B	Offset Error at Gain = 1	$ board dependent
$ 1D	Offset Error at Gain = 2	$ board dependent
$ 1F	Offset Error at Gain = 4	$ board dependent
$ 21	Offset Error at Gain = 8	$ board dependent
$ 23	Gain Error at Gain = 1	$ board dependent
$ 25	Gain Error at Gain = 2	$ board dependent
$ 27	Gain Error at Gain = 4	$ board dependent
$ 29	Gain Error at Gain = 8	$ board dependent
$ 2B	Not used	$ 00
.....		.....
$ 3F		$ 00

Figure 3: ID PROM Contents TIP500-11 V1.0

ADDRESS	FUNCTION	
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 18
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 15
$ 17	C R C	$ variable
$ 19	Version -20	$ 14
$ 1B	Offset Error at Gain = 1	$ board dependent
$ 1D	Offset Error at Gain = 2	$ board dependent
$ 1F	Offset Error at Gain = 5	$ board dependent
$ 21	Offset Error at Gain = 10	$ board dependent
$ 23	Gain Error at Gain = 1	$ board dependent
$ 25	Gain Error at Gain = 2	$ board dependent
$ 27	Gain Error at Gain = 5	$ board dependent
$ 29	Gain Error at Gain = 10	$ board dependent
$ 2B	Not used	$ 00
.....		.....
$ 3F		$ 00

Figure 4: ID PROM Contents TIP500-20 V1.0

ADDRESS	FUNCTION	
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 18
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 15
$ 17	C R C	$ variable
$ 19	Version -21	$ 15
$ 1B	Offset Error at Gain = 1	$ board dependent
$ 1D	Offset Error at Gain = 2	$ board dependent
$ 1F	Offset Error at Gain = 4	$ board dependent
$ 21	Offset Error at Gain = 8	$ board dependent
$ 23	Gain Error at Gain = 1	$ board dependent
$ 25	Gain Error at Gain = 2	$ board dependent
$ 27	Gain Error at Gain = 4	$ board dependent
$ 29	Gain Error at Gain = 8	$ board dependent
$ 2B	Not used	$ 00
.....		.....
$ 3F		$ 00

Figure 5: ID PROM Contents TIP500-21 V1.0

5. IP Addressing

The TIP500 is controlled by a set of registers, which are directly accessible in the IO address space of the IP.

ADDRESS	NAME	FUNCTION	SIZE	ACCESS
$ 00	CONTREG	ADC Control Register	word	R/W
$ 02	DATAREG	ADC Data Register	word	R/W
$ 05	STATREG	ADC Status Register	byte	RO
$ 07	CONVERT	ADC Convert Start Register	byte	WO
$ 09	INTVEC	Interrupt Vector Register	byte	R/W
$ 0B	IDWRENA	ID-PROM write enable	byte	WO

Note

IDWRENA is for factory use only, do **not** write to this register.

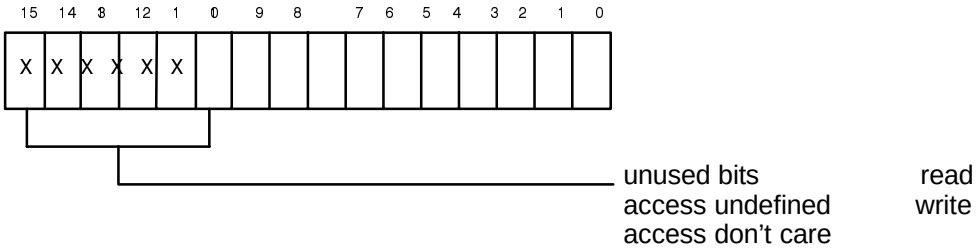
5.1. ADC Register Set

The ADC of the TIP500 is controlled by a set of 4 registers. All registers are cleared by $\overline{\text{IP\_RESET}}$.

ADC Control Register
ADC Data Register
ADC Status Register
ADC Convert Start Register

5.1.1. ADC Control Register Address $00

The ADC Control Register CONTREG is used to select an input channel, the gain and the mode for the next data conversion. This is done by writing the corresponding bit pattern into bit 0 to bit 9.

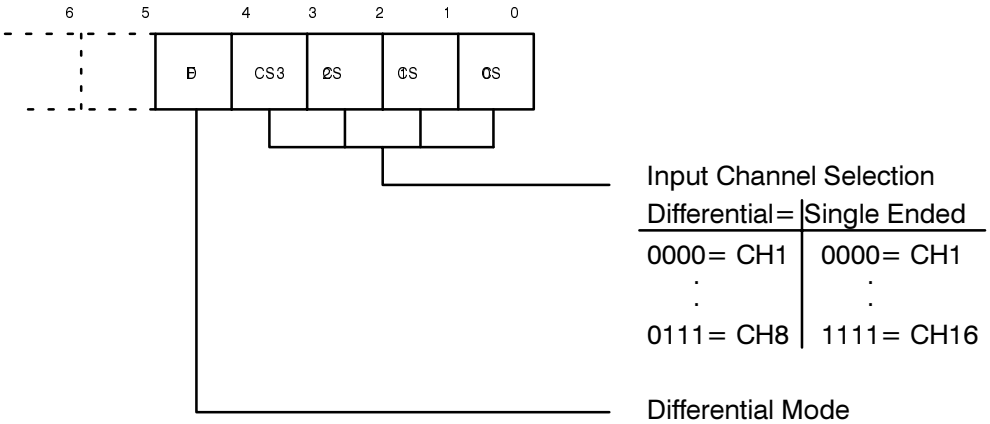


5.1.1.1. ADC Channel Selection

Bit 0 to bit 3 of the ADC Control Register CONTREG are used to select an input channel for the data conversion.

Bit 4 of the ADC Control Register CONTREG is used to control if the module operates in differential or in single ended mode. If this bit is set to '1' differential mode is selected.

Figure 6: CONTREG Input Channel Selection and Mode



Note

In differential mode only channels 1 to 8 may be selected. In this mode channels 9 to 16 are used as - - input for channels 1 to 8.

5.1.1.2. ADC Gain Selection

Bit 5 and bit 6 of the ADC Control Register CONTREG are used to program the gain of the input amplifier.

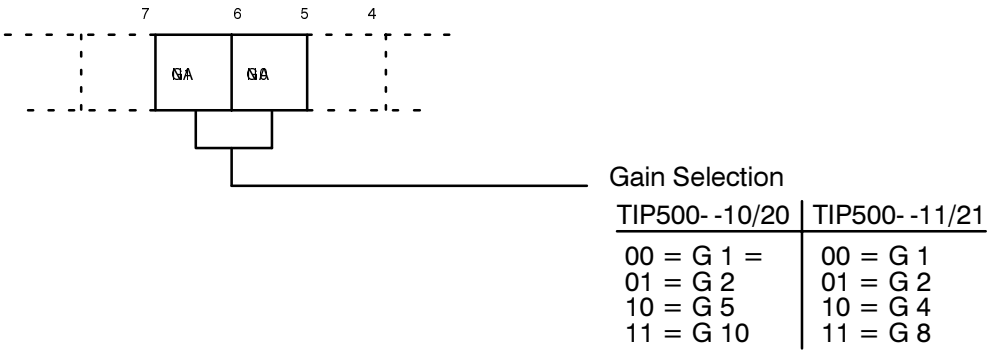


Figure 7: CONTREG Input Gain Selection

5.1.1.3. ADC Automatic Settling Time Control

If bit 7 of the ADC Control Register CONTREG is set to '1', the Automatic Mode for the settling time is enabled. In this mode a data conversion is initiated by writing to the ADC Control Register CONTREG, but however is automatically delayed by hardware until the gain depended settling time has expired.
If bit 7 of the ADC Control Register CONTREG is set to '0', the Normal Mode for the settling time is enabled. In this mode a data conversion is initiated by writing to the ADC Convert Start Register CONVERT after selecting the desired channel and gain by writing to the ADC Control Register CONTREG.

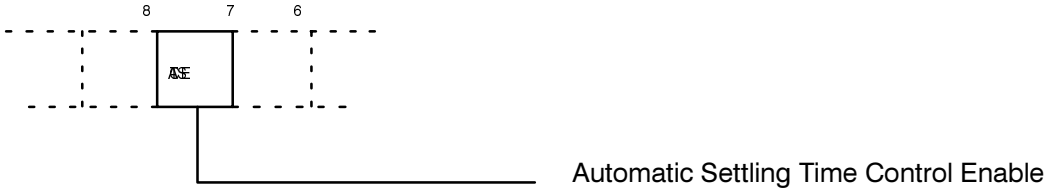


Figure 8: CONTREG Automatic Settling Time Control

Note

The settling time for all TIP500 Modules is 10µs for all gains.

5.1.1.4. ADC Pipeline Mode Control

If bit 8 is set to '1' the pipeline mode is selected. In pipeline mode the result from the conversion (N-1) is shifted into the ADC Data Register DATAREG during the conversion N.

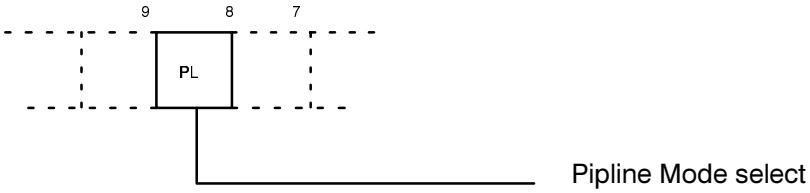


Figure 9: CONTREG Pipeline Mode Control

5.1.1.5. ADC Interrupt Enable

Bit 8 of the ADC Control Register CONTREG is used to enable interrupt generation of the module. If this bit is set to '1' interrupts are always initiated, whenever the settling time is over (on IP_INTREQ1) and data conversion has been completed (on IP_INTREQ0). If the module is in the automatic mode (bit7 set to '1') only one interrupt at the end of data conversion (on IP_INTREQ0) is being generated.

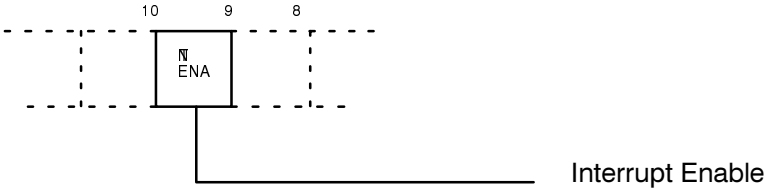


Figure 10: CONTREG Interrupt Enable

5.1.2. ADC Data Register Address $02

The ADC Data Register DATAREG contains the converted data value. The 12 bit ADC value is shifted in the higher bit's of the data register by hardware . This allows direct processing of the data as a 16 bit two's complement integer value for the TIP500-10/11 and 16 bit straight binary for TIP500-20/21.

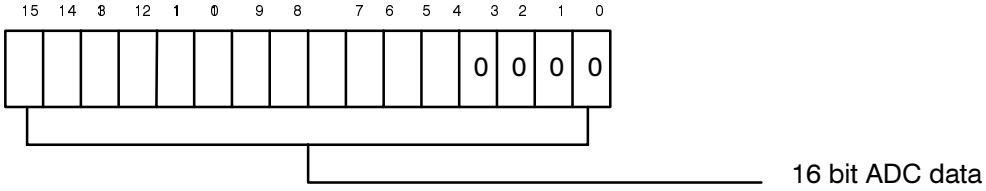


Figure 11: ADC Data Register

Figure 12: Data Register Description

DESCRIPTION	DIGITAL OUTPUT	
	binary two's complement TIP500 - - 10/11=	straight binary TIP500 - - 20/21
+ Full Scale (FS - - 1LSB)	$7FF0	$FFF0
Midscale	$0000	$8000
One LSB Below Midscale	$FFF0	$7FF0
- - Full Scale	$8000	$0000

Note

The contents of ADC Data Register DATAREG is not valid as long as the ADC Busy Flag is read as '1'.

5.1.3. ADC Status Register Address $05

Bit 0 and bit 1 of the ADC Status Register STATREG reflect the status of the ADC converter. As long as bit 0 is read as '1', the settling time did not expire after writing to the ADC Control Register CONTREG. Bit 1 indicates the busy status of the ADC converter itself ('1' = ADC busy). If Automatic Mode is active bit 1 indicates a '1' during the settling time and the conversion time.

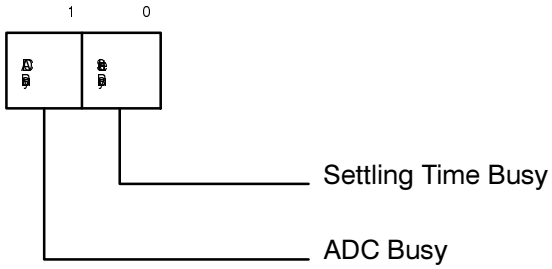


Figure 13: ADC Status Register

Note

Bit 2 - - 7 of the ADC Status Register are undefined.

5.1.4. ADC Convert Start Register Address $07

If the TIP500 is configured in Normal Mode writing any value into the ADC Convert Register CONVERT starts a data conversion immediately.

Note

In normal mode it is in the responsibility of the user to observe the settling time busy flag and the ADC busy flag of the ADC Status Register. Writes to the ADC Convert Start Register CONVERT during ADC busy = '1' are ignored.

5.1.5. Interrupt Vector Register Address $09

The Interrupt Vector Register INTVEC is a byte wide read/write register. The Interrupt Vector Register is shared between both interrupt sources, but both, the settling time ready and the ADC data ready will create an individual interrupt. A read cycle to the INTVEC Register acknowledges and clears the interrupt.

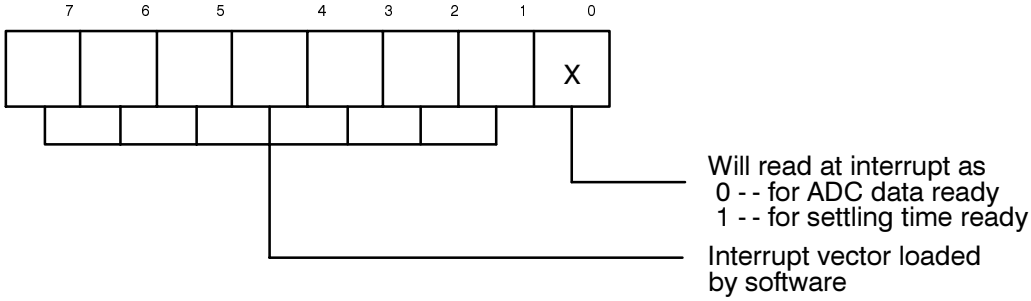


Figure 14: INTVEC Interrupt Vector Register

For an interrupt from settling time ready bit 0 of the interrupt vector will read as '1'. For an interrupt from the ADC data ready bit 0 will read as '0'. If the vector register is for example loaded with '$60', settling time ready will create an interrupt at vector '$61' and ADC data ready will create an interrupt at vector '$60'.

Note

The interrupt settling time ready is created by the falling edge of settling time busy status and uses the $\overline{\text{INTREQ1}}$, the interrupt ADC ready is created by the falling edge of ADC busy status and uses the $\overline{\text{INTREQ0}}$ interrupt line of the IP bus.

5.1.6. ID Write Enable Register Address $0B

This register is for factory use only. Do not write to this register. If bit 0 is set '1' a write access to the ID-PROM is enabled.

6. Operating Modes

The TIP500 supports four operating modes which are selected with bit 7 (Normal / Automatic Mode) and bit 8 (Pipeline / no Pipeline Mode) of the ADC Control Register CONTREG.

6.1. Mode Overview

- Normal Mode / No Pipeline Mode
- Automatic Mode / No Pipeline Mode
- Normal Mode / Pipeline Mode
- Automatic Mode / Pipeline Mode

	CONTREG Bit 7 = 1 Automatic Mode	CONTREG Bit 7 = 0 Normal Mode
CONTREG Bit 8 = 1 Pipline Mode	After the settling time has expired conversion N is started and the result of conversion N-1 is shifted into the ADC Data Register.	A write access to the CONVERT register starts conversion N and shifts the result of conversion N-1 into the ADC Data Register.
CONTREG Bit 8 = 0 No Pipline Mode	After the settling time has expired conversion N is started and the result of conversion N is shifted into the ADC Data Register.	A write access to the CONVERT register starts conversion N and shifts the result of conversion N into the ADC Data Register.

Figure 15: Operating Modes

Note

In Normal Mode the user should observe the settling time by the settle busy flag in the ADC Status Register.

6.2. Automatic Mode

The Automatic Mode is enabled by setting bit 7 of the ADC Control Register CONTREG to '1'. A write access to the ADC Control Register CONTREG with bit 7 set to '1' start a conversion for the programmed channel and gain after the settling time has expired. In Pipeline Mode (bit 8 of the ADC Control Register CONTREG set to '1') the result of the previous conversion is shifted into the ADC Data Register DATAREG during the actual conversion. If the Pipeline Mode is switched off the result of the actual conversion is shifted into the ADC Data Register DATAREG.

6.2.1. State Diagram Automatic Mode

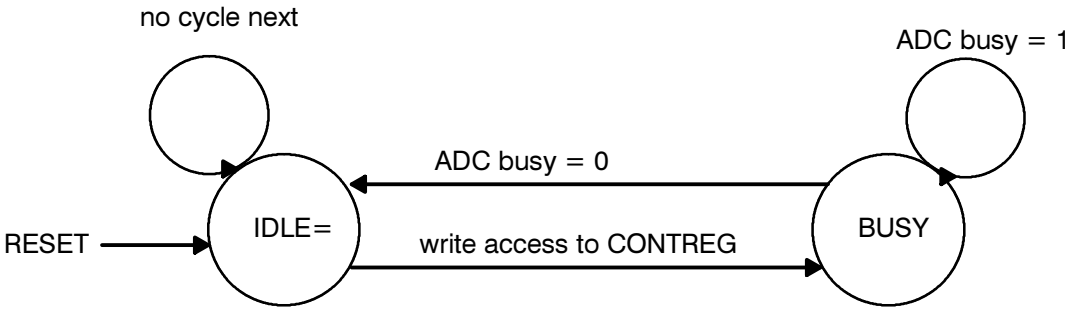


Figure 16: State Diagram Automatic Mode

In Automatic Mode the ADC busy flag is active during the whole cycle of channel/gain select, settling time and data conversion. When the ADC busy flag becomes inactive (= '0') the conversion result is accessible in the ADC Data Register DATAREG and an interrupt will be generated if interrupts are enabled.

6.2.2. Automatic Mode with Data Pipeline

If Automatic Mode with Pipeline is selected during conversion N the result of conversion N-1 is shifted into the ADC Data Register DATAREG. The acquisition and conversion time in this mode is 20µs.

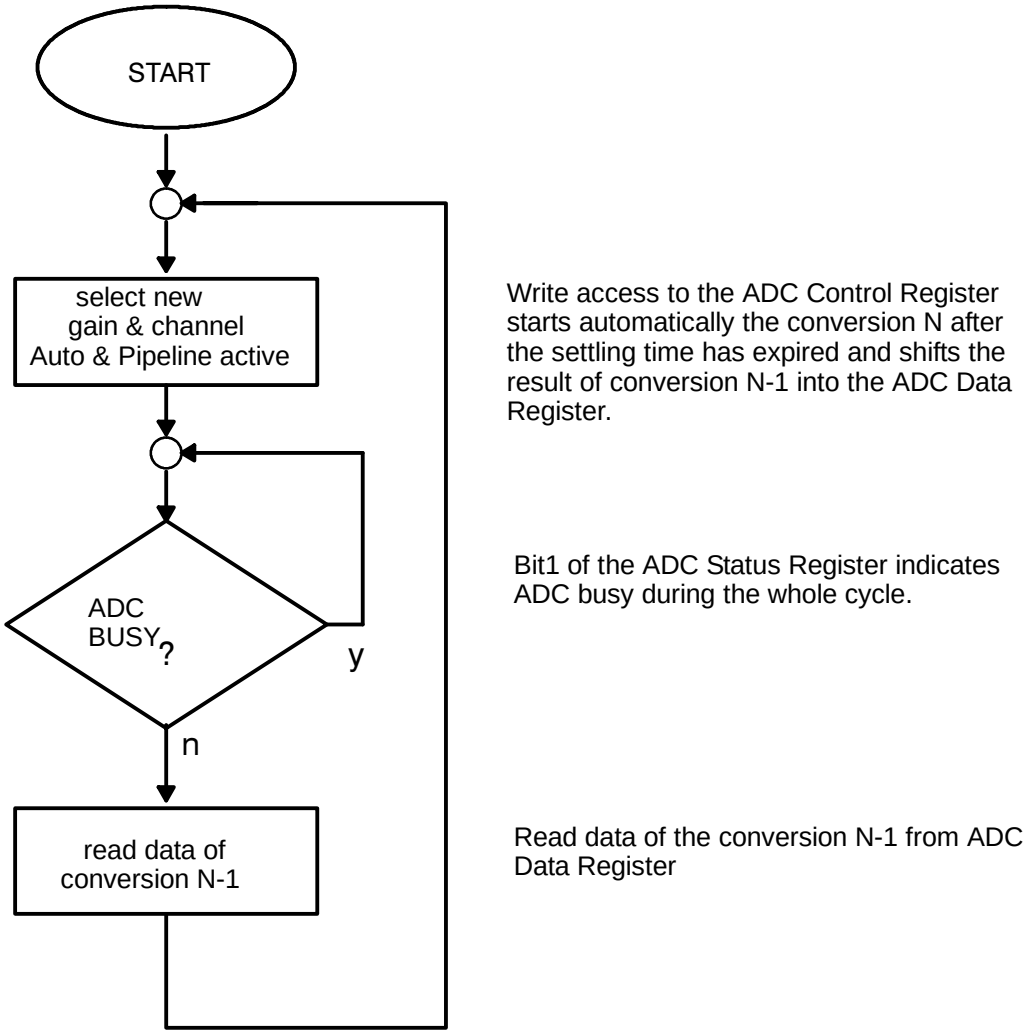
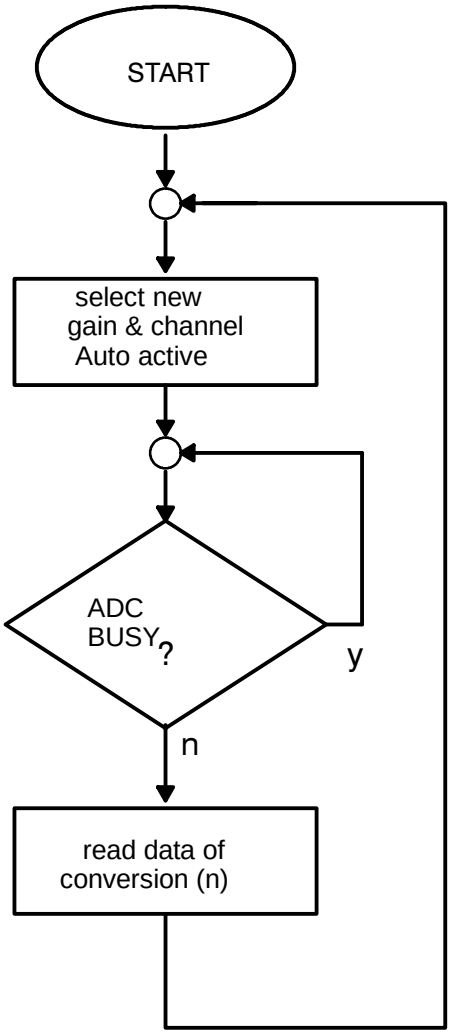


Figure 17: Flowchart Automatic Mode with Data Pipeline

6.2.3. Automatic Mode without Data Pipeline

If Automatic Mode without Pipeline is selected the result of the actual conversion is shifted into the ADC Data Register DATAREG. The acquisition and conversion time in this mode is 30µs.



Write access to the ADC Control Register starts automatically the conversion after the settling time has expired and shifts the result into the ADC Data Register.

Bit1 of the ADC Status Register indicates ADC busy during the whole cycle.

Read data of the actual conversion from the ADC Data Register

Figure 18: Flowchart Automatic Mode without Data Pipeline

6.3. Normal Mode

The Normal Mode is enabled by setting bit 7 of the ADC Control Register CONTREG to ‘0‘. A write access to the ADC Control Register CONTREG with bit 7 set to ’0’ (Normal Mode enabled) selects a new channel and gain for the next conversion. As long as the settling time expires bit 0 of the ADC Status Register STATREG (settle busy flag) reads as ‘1‘. After the settling time has expired a conversion can be started by writing to the ADC Convert Start Register CONVERT. To achieve higher conversion rates it is possible to select a new channel and gain for the next conversion after the previous conversion has been started. In this mode the settling time for the new channel and the conversion time of the actual channel proceed simultaneously. As long as bit 1 of the ADC Status Register STATREG (ADC busy flag) reads as ‘1‘ conversion is in progress. Reading bit 1 of the ADC Status Register as ‘0‘indicates that the conversion result is accessible in the ADC Data Register DATA-REG.

If interrupts are enabled two interrupts will be generated: the first interrupt at the end of the settling time, the second interrupt at the end of conversion.

6.3.1. State Diagram Normal Mode

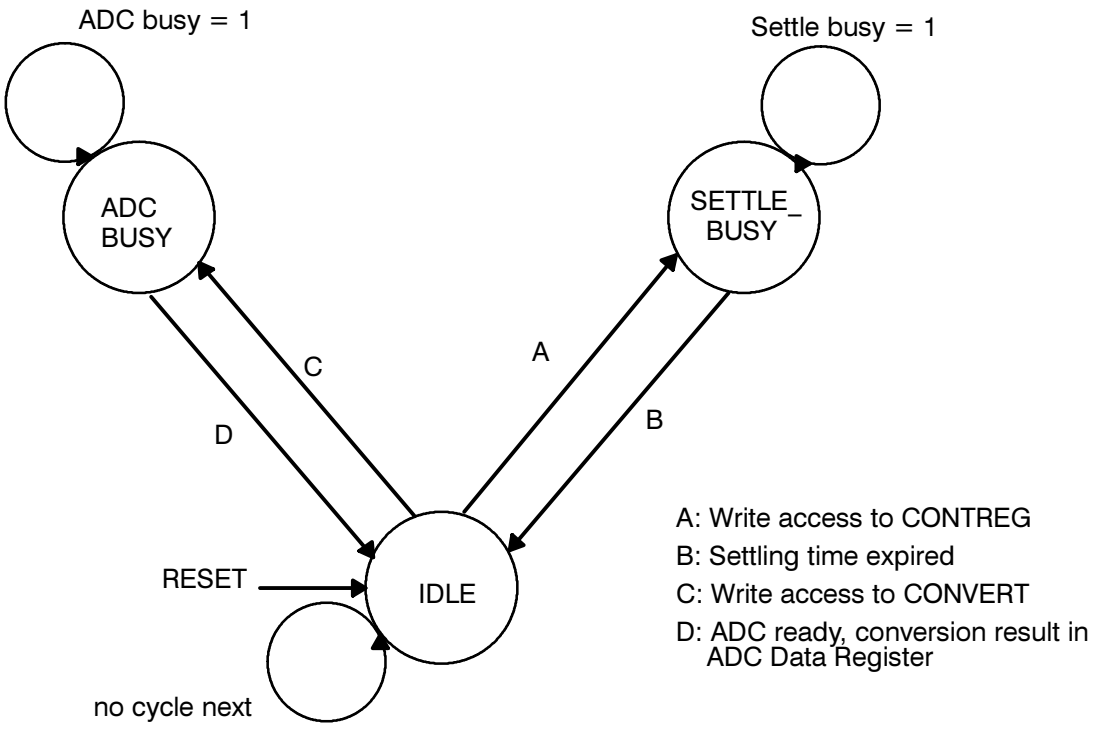


Figure 19: State Diagram Normal Mode

6.3.2. Normal Mode with Data Pipeline

If Normal Mode with Pipeline is selected during conversion N the result of conversion N-1 is shifted into the ADC Data Register DATAREG. In this mode it is possible that the settling time and conversion time simultaneous proceed. The acquisition and conversion time in this mode is 10µs with no change of channel / gain and 12.5µs with change of channel / gain.

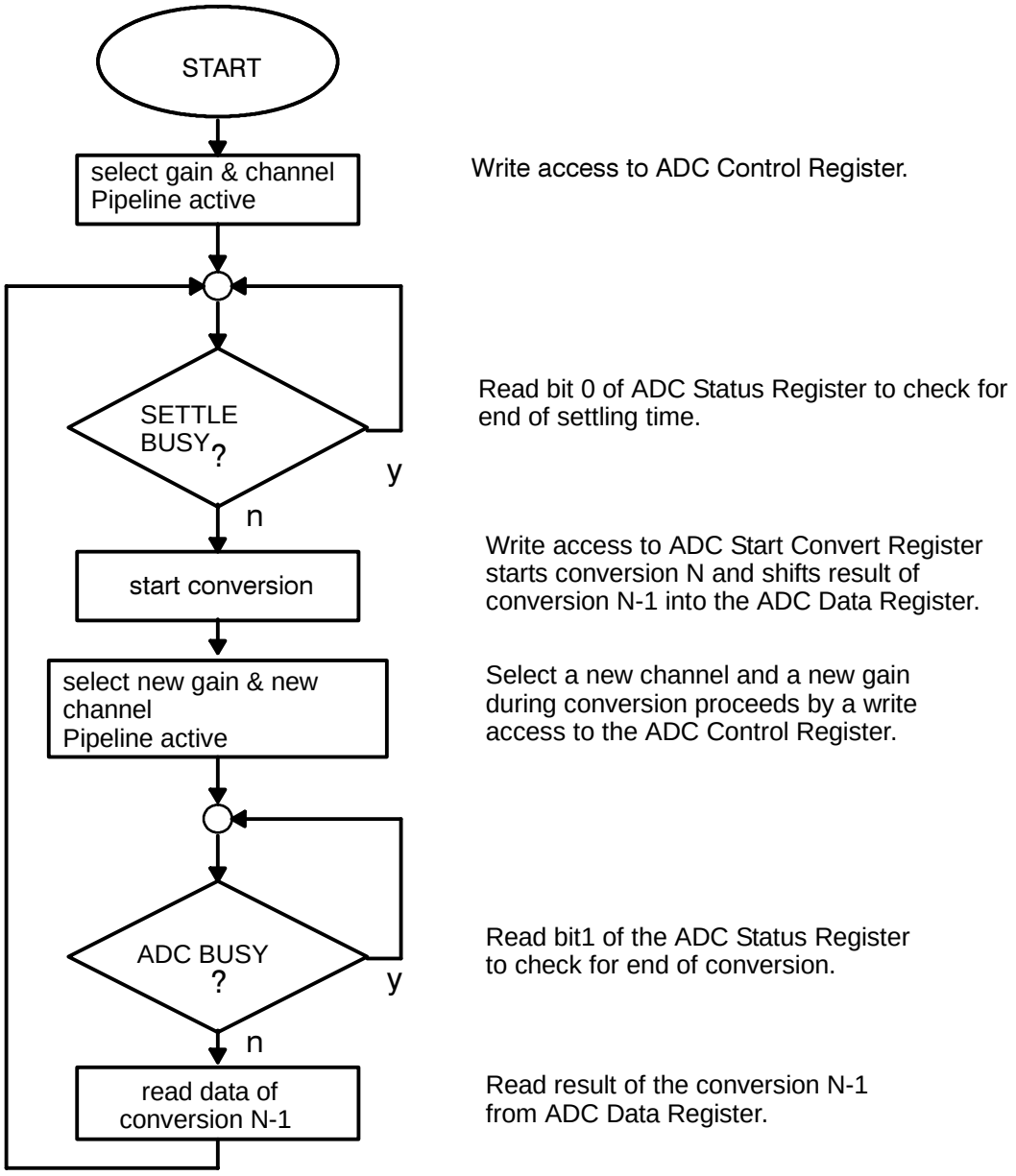


Figure 20: Flowchart Normal Mode with Data Pipeline

Note

For conversions without channel and gain change it is not necessary to observe the settle busy flag of the ADC Status Register.

6.3.3. Normal Mode without Data Pipeline

If Normal Mode without Pipeline is selected the result of the actual conversion is shifted into the ADC Data Register DATAREG. In this mode it is possible that the settling time and conversion time simultaneous proceed. The acquisition and conversion time in this mode is 20µs.

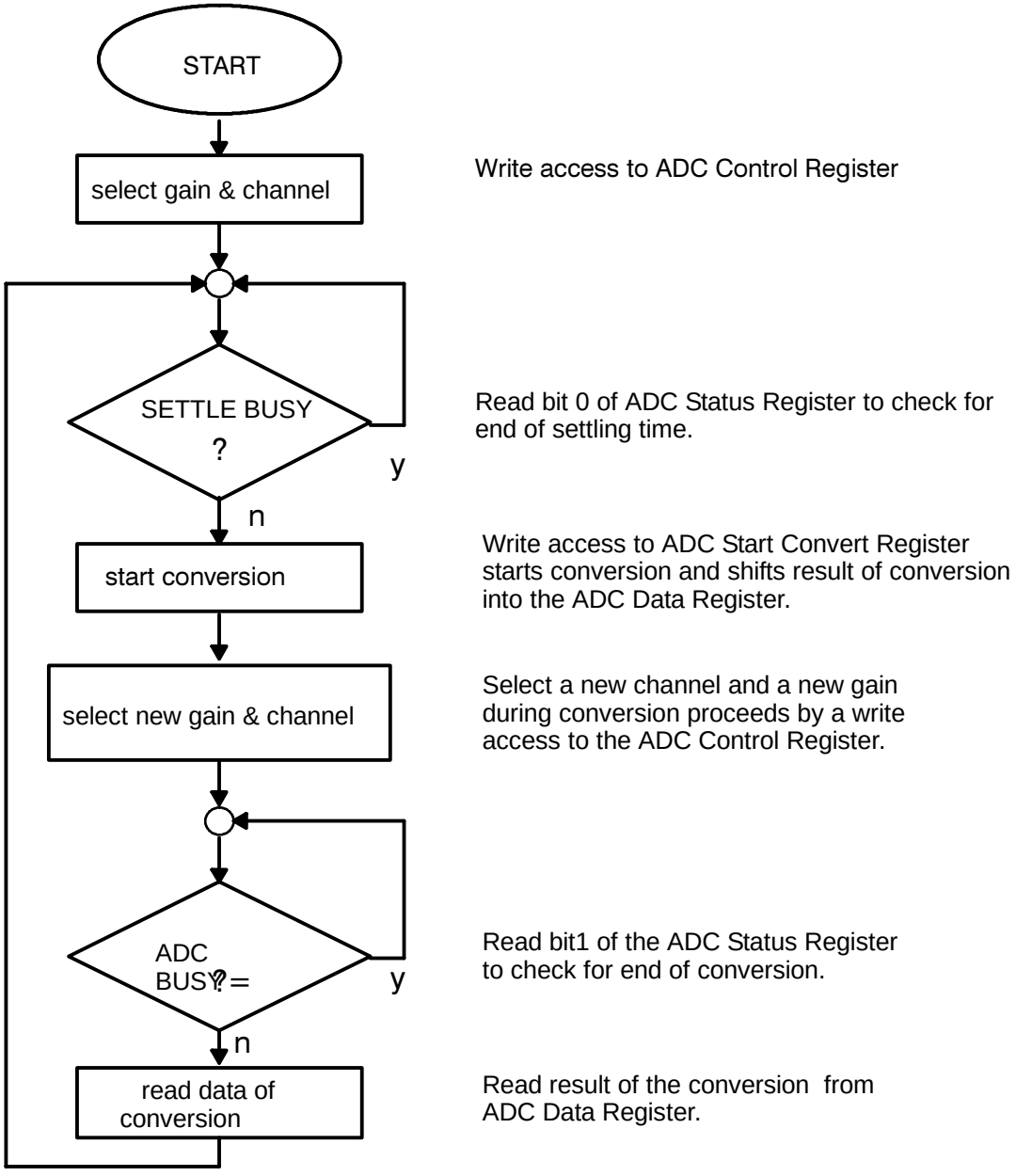


Figure 21: Flowchart Normal Mode without Data Pipeline

Note

For conversions without channel and gain change it is not necessary to observe the settle busy flag of the ADC Status Register.

7. IP I/O connector

7.1. Analog Input Connections

Pin-Number	Mode: Single Ended	Mode: Differential
01	ADC Input 1	ADC Input 1 +
02	ADC Input 9	ADC Input 1 -
03	AGND	AGND
04	ADC Input 10	ADC Input 2 -
05	ADC Input 2	ADC Input 2 +
06	AGND	AGND
07	ADC Input 3	ADC Input 3 +
08	ADC Input 11	ADC Input 3 -
09	AGND	AGND
10	ADC Input 12	ADC Input 4 -
11	ADC Input 4	ADC Input 4 +
12	AGND	AGND
13	ADC Input 5	ADC Input 5 +
14	ADC Input 13	ADC Input 5 -
15	AGND	AGND
16	ADC Input 14	ADC Input 6 -
17	ADC Input 6	ADC Input 6 +
18	AGND	AGND
19	ADC Input 7	ADC Input 7 +
20	ADC Input 15	ADC Input 7 -
21	AGND	AGND
22	ADC Input 16	ADC Input 8 -
23	ADC Input 8	ADC Input 8 +
24	AGND	AGND

Figure 22: TIP500 Analog Input Connections

7.2. Power Input Connections

Pin-Number	Function
44	AGND
45	-15V
46	AGND
47	+15V
48	AGND
49	+5V
50	AGND

Figure 23: TIP500 Power Input Connections

Note

The power input connections are reserved for special versions of the TIP500 without on board DC/DC converter.