Acromag®

Series IP320 Industrial I/O Pack
12-Bit High Density Analog Input Board

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 624-1541
Fax: (248) 624-9234

8500-484-F00J005

Table of Contents **Page**

DRAWINGS **Page**

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP320 module is a 12-bit, high-density, single-size IP analog input board with the capability to monitor 20 differential or 40 single-ended analog input channels. The IP320 utilizes state of the art Surface Mounted Technology (SMT) to achieve its high channel density. It offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

Model	Operating Temperature Range
IP320	0 to 70°C
IP320E	-40 to 85°C

KEY ANALOG INPUT FEATURES

- **High Channel Count -** Monitors up to 20 differential, or 40 single-ended analog inputs (acquisition mode and channels are selected via a programmable control register). Up to four units may be mounted on a carrier board providing up to 80 differential inputs, or 160 single-ended inputs in a single system slot.
- **12-bit Accuracy -** Contains an enhanced, 12-bit, successive approximation Analog to Digital Converter (ADC) with an 8.5uS conversion time.
- **High Speed -** A maximum system throughput rate of 100K samples per second can be obtained using the pipelined mode of operation.
- **Multiple Input Range -** Three hardware jumper-selectable ranges capture both bipolar and unipolar voltage inputs: -5 to +5V, -10 to +10V, and 0 to +10V.
- **Programmable Gain -** Gains of 1, 2, 4, and 8 are programmable via the control register.
- **Software/Hardware Trigger -** Input acquisition can be triggered via software, or by an external hardware input for synchronization to external events.
- **Precision References -** On-board, high-precision voltage references provide the means for accurate and reliable software calibration of the module.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **16-bit I/O** - Control register Read/Write and A/D Conversion/Read are performed through 16-bit data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - (typically 0 to 3 wait states are required for data transfer, see specifications for detailed information).
- **Wait/Hold State Support** - This IP module supports both "wait" states (generated by the IP module) and "Hold" states (generated by the carrier board).

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent carrier boards). Consult the documentation of your carrier board to ensure compatibility with the following interface products (since all connections to field signals are made through the carrier board which passes them to the individual IP modules).

Cables:
Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The shielded cable is recommended for optimum performance with precision analog I/O applications, while the unshielded cable is recommended for digital I/O.

Termination Panel:
Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:
Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to AVME9630/9660 boards via a flat 50-pin ribbon cable within the card cage (cable Model 5025-550-X or 5025-551-X).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO320.TXT" file in the "IP320" subdirectory on the diskette for more details.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All possible jumper settings will be discussed in the following sections. The jumper locations are shown in Drawing 4501-433.

Power should be removed from the board when configuring hardware jumpers, installing IP's, cables, termination panels and field wiring. Refer to Drawing 4501-434 and IP documentation for IP configuration and assembly instructions.

Default Hardware Jumper Configuration

A board shipped from the factory is configured as follows:

- Analog input range is configured for a 10V bipolar input span (i.e. an ADC input range of -5 to +5 Volts).
- Internal ±12 Volt power supplies are used (sourced from P1 connector).
- Programmable software control register bits are undefined at reset. The control register should be programmed to the desired gain, mode, and channel configuration before starting ADC analog input acquisition.

Analog Input Range Hardware Jumper Configuration

The ADC input range is programmed via hardware jumpers J1 and J2. J1 controls the input voltage span. J2 controls the selection of unipolar or bipolar input ranges. The configuration of the jumpers for the different ranges is shown in the following table. "IN" means that the pins are shorted together with a shorting clip. "OUT" means that the clip has been removed.

Table 2.1: Analog Input Range Selections (Pins of J1 and J2)

Desired ADC Input Range (VDC)	Required Input Span (Volts)	J1 Pins 1&2	J1 Pins 2&3	Reqd. Input Type	J2 Pins 1&2	J2 Pins 2&3
-5 to +5	10	In	Out	Bipolar	Out	In
-10 to +10*	20	Out	In	Bipolar	Out	In
0 to +10*	10	In	Out	Unipolar	In	Out

* These ranges can only be achieved with ±15V external power supplies. The input ranges will be clipped if ±12V supplies are used, typically to ±9 V maximum inputs.

Power Supply Hardware Jumper Configuration

The selection of internal or external analog power supplies is accomplished via hardware jumpers J3 and J4. J3 (J4) controls the selection of either the internal +12 (-12) Volt supply sourced from P1 connector, or the external +15 (-15) Volt supply sourced from the P2 connector. The configuration of the jumpers for the different supplies is shown in the following table. "IN" means that the pins are shorted together with a shorting clip. "OUT" means that the clip has been removed.

Table 2.2: Power Supply Selections (Pins of J3 and J4)

Power Supply Selection*	J3 (1&2)	J3 (2&3)	J4 (1&2)	J4 (2&3)
±12 Volt (Internal, P1)	OUT	IN	OUT	IN
±15 Volt (External, P2)	IN	OUT	IN	OUT

* Internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts).

Control Register Configuration

The control register is software configurable. There are no hardware jumpers associated with it. Control register bits are undefined at reset and must be programmed to the desired gain, acquisition mode, and channel configuration, before starting ADC analog input acquisition (refer to Section 3 for details).

Analog Input Data Format

The analog input data will appear as Unipolar Straight Binary (USB) for unipolar input ranges (e.g. 0 to +10V); it will appear as Bipolar Offset Binary (BOB) for bipolar input ranges (e.g. -5 to +5V).

The following tables indicate the relationship between data format and the ideal analog input voltage to the module.

Table 2.3: Unipolar Straight Binary (USB) Analog Data Format*

Analog Input Voltage (Volts)	USB Data (Hex)
9.9976	FFF0
9.9951	FFE0
. .	. .
0.0024	0010
0.0000	0000

* For Table 2.3 it is assumed that the analog input range (unipolar) is 0 to +10 Volts (i.e. with a programmable gain of 1). The 12-bit USB data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are shown as zero in the table. Actually, they are undefined and must be zeroed or ignored in calculations made with the data returned from the IP module.

Table 2.4: Bipolar Offset Binary (BOB) Analog Data Format*

Analog Input Voltage (Volts)	BOB Data (Hex)
4.9976	FFF0
4.9951	FFE0
. .	. .
0.0024	8010
0.0000	8000
-0.0024	7FF0
. .	. .
-4.9976	0010
-5.0000	0000

* For Table 2.4 it is assumed that the analog input range (bipolar) is -5 to +5 Volts (i.e. with a programmable gain of 1). The BOB, 12-bit data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are shown as zero in the table. Actually, they are undefined and must be zeroed or ignored in calculations made with the data returned from the IP.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IP modules to the carrier board. P2 is a 50-pin receptacle female header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly. P2 pin assignments are unique to each IP model (see Table 2.5) and normally correspond to the pin numbers of the front-panel, field I/O interface connector on the carrier board (you should verify this for your carrier board).

In Table 2.5, channel designations are abbreviated to save space. For example, single-ended channel 0 is abbreviated as "SCH00"; the +input for differential channel 0 is abbreviated as "+DCH00". Both of these labels are attached to pin 1, but only one applies according to whether the input is single-ended or differential (i.e. if your inputs are applied differentially, follow the differential channel labeling for each channel's + and - input leads).

Table 2.5: IP320 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
SCH00/+DCH00	1	SCH32/-DCH12	26
SCH20/-DCH00	2	SCH13/+DCH13	27
SCH01/+DCH01	3	SCH33/-DCH13	28
SCH21/-DCH01	4	SCH14/+DCH14	29
SCH02/+DCH02	5	SCH34/-DCH14	30
SCH22/-DCH02	6	SCH15/+DCH15	31
SCH03/+DCH03	7	SCH35/-DCH15	32
SCH23/-DCH03	8	SCH16/+DCH16	33
SCH04/+DCH04	9	SCH36/-DCH16	34
SCH24/-DCH04	10	SCH17/+DCH17	35
SCH05/+DCH05	11	SCH37/-DCH17	36
SCH25/-DCH05	12	SCH18/+DCH18	37
SCH06/+DCH06	13	SCH38/-DCH18	38
SCH26/-DCH06	14	SCH19/+DCH19	39
SCH07/+DCH07	15	SCH39/-DCH19	40
SCH27/-DCH07	16	SENSE	41
SCH08/+DCH08	17	SENSE	42
SCH28/-DCH08	18	COMMON	43
SCH09/+DCH09	19	COMMON	44
SCH29/-DCH09	20	RESERVED	45
SCH10/+DCH10	21	RESERVED	46
SCH30/-DCH10	22	-15V DC	47
SCH11/+DCH11	23	*Ext Trigger	48
SCH31/-DCH11	24	+15V DC	49
SCH12/+DCH12	25	SHIELD	50

* Indicates an Active-Low Signal.

Analog Input Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the IP module and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references. See Drawing 4501-435 for analog input connections for differential and single-ended inputs.

Single-ended inputs only require a single lead (+) per channel, with a shared "sense" (reference) lead for all channels, and can be used when a large number of input channels come from the same location (e.g. printed circuit board). The channel density doubles when using single-ended inputs, and this a powerful incentive for their use. However, caution must be exercised since the single "sense" lead references all channels to the same common which will induce noise and offset if they are different.

The IP320 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP320 input module.

External Trigger Input

The external trigger signal on P2 is an active-low input which may be used for synchronizing the ADC conversion of analog inputs from several IP modules to external events. The external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The conversion is triggered on the falling edge of a normally high signal.

The trigger pulse must be low for a minimum of 250nS to guarantee acquisition. It must not stay low for more than 5uS, or additional, unwanted acquisitions may be triggered. See Section 3 for programming information.

IP Logic Interface Connector (P1)

The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.6). Note that the IP320 does not utilize all of the logic signals defined for the P1 connector. Logic lines NOT USED used by this model are indicated in ***BOLD ITALICS***.

Table 2.6: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	***INTReq0****	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

P1 of the IP module provides the logic interface to the mating connector on the carrier board (see Table 2.6). This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to control the acquistion of analog inputs from the field. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP320 only uses a portion of this space. The I/O space address map for the IP320 is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on a 16-bit word basis (D0..D15).

Table 3.1: IP320 I/O Space Address Memory Map

Base Address + (Hex)	Even Byte D15 D08	Odd Byte D07 D00
00	R/W - Control Register	
02 ↓ 0E	Repeated Control Register[1]	
10	W - ADC Convert Command	
12 ↓ 1E	Repeated ADC Convert Command[1]	
20	R - Read ADC Data	
22 ↓ 2E	Repeated Read ADC Data[1]	
30 ↓ 3E	Not Used[2]	
40 ↓ 4E	Reserved	
50 ↓ 7E	Not Used[2]	

Notes (Table 3.1):
1. Registers appear in multiple locations in the memory map because of simplified address decoding (these locations can be ignored).
2. The IP will not respond to addresses that are "Not Used".

The function of each register noted in Table 3.1 will be discussed in the following sections.

IP Identification PROM - (Read Only, 32 odd-byte addresses)

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP320 ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block. The IP320 ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM. Execution of an ID PROM Read requires 0 wait states.

Table 3.2: IP320 ID Space Identification (ID) PROM

Hex Offset From ID PROM Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		32	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		2E	CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):
1. The IP model number is represented by a two-digit code within the ID PROM (the IP320 model is represented by 32 Hex).

Control Register - (Read/Write, Base + 00H)

The IP320 Control Register reflects and controls analog input channel data acquisition functions. This register must be written/read, one word (D16) at a time. Execution of a Control Register read (write) requires 0 (1) wait states. The function of each bit is described as follows:

EVEN Byte

MSB D15	D14	D13	D12	D11	D10	D09	LSB D08
CTRIG	Not used	Not used	Not used	Not used	Not used	MODE 1	MODE 0

ODD Byte

MSB D07	D06	D05	D04	D03	D02	D01	LSB D00
GSEL 1	GSEL 0	Not used	SEL HIGH	CH3	CH2	CH1	CH0

RESET CONDITION: all bits are undefined. Registers should be programmed to the desired configuration before starting ADC analog input acquisition.

Bit 15: When read, the CTRIG bit indicates whether an ADC conversion has been triggered, either by software command or external trigger input. If the bit reads high, the conversion could be taking place or has been completed. CTRIG is cleared by reading the ADC data. Writing to this bit position will have no effect.

Bits 14-10: Not used - if read will return data written to those bit positions.

Bits 9 & 8: Control the input acquisition mode as described in the following table:

Acquisition Mode	MODE1 Bit (D09)	MODE0 Bit (D08)
Differential Input CH0-19 & CAL0-3	0	0
Single-ended Input CH0-19	0	1
Single-ended Input CH20-39	1	0
Auto Zero Input*	1	1

* Auto Zero input is enabled by the mode bits, overriding all channel selection bits.

Bits 7 & 6: Control the programmable gain setting as described in the following table:

Desired Gain Setting	GSEL1 Bit (D07)	GSEL0 Bit (D06)
1	0	0
2	0	1
4	1	0
8	1	1

Bit 5: Not used - if read will return data written to the bit position.

Bit 4: The SEL HIGH bit acts as the MSB for analog input channel selection. As such, its action is grouped with that of bits 3-0 (see following).

Bits 3-0: Control the selection of analog input channels per the following table. Note that the SEL HIGH bit and MODE bits are also shown to completely define the channel selection. When MODE 1 & MODE 0 are both 0, differential channels 0-19 and calibration voltages 0-3 may be selected; when MODE 1 is 0 and MODE 0 is 1, single-ended channels 0-19 may be selected; when MODE 1 is 1 and MODE 0 is 0, single-ended channels 20-39 may be selected; when both MODE 1 & MODE 0 are 1, the Auto Zero input is selected regardless of any other bit levels.

Desired Chan.	SEL HIGH Bit D04	CH3 Bit D03	CH2 Bit D02	CH1 Bit D01	CH0 Bit D00	Mode 1 Bit D09	Mode 0 Bit D08
0	0	0	0	0	0	0	0/1
1	0	0	0	0	1	0	0/1
2	0	0	0	1	0	0	0/1
3	0	0	0	1	1	0	0/1
4	0	0	1	0	0	0	0/1
5	0	0	1	0	1	0	0/1
6	0	0	1	1	0	0	0/1
7	0	0	1	1	1	0	0/1
8	0	1	0	0	0	0	0/1
9	0	1	0	0	1	0	0/1
10	0	1	0	1	0	0	0/1
11	0	1	0	1	1	0	0/1
12	0	1	1	0	0	0	0/1
13	0	1	1	0	1	0	0/1
14	0	1	1	1	0	0	0/1
15	0	1	1	1	1	0	0/1
16	1	0	0	0	0	0	0/1
17	1	0	0	0	1	0	0/1
18	1	0	0	1	0	0	0/1
19	1	0	0	1	1	0	0/1
CAL0	1	0	1	0	0	0	0
CAL1	1	0	1	0	1	0	0
CAL2	1	0	1	1	0	0	0
CAL3	1	0	1	1	1	0	0
20	0	0	0	0	0	1	0
21	0	0	0	0	1	1	0
22	0	0	0	1	0	1	0
23	0	0	0	1	1	1	0
24	0	0	1	0	0	1	0
25	0	0	1	0	1	1	0
26	0	0	1	1	0	1	0
27	0	0	1	1	1	1	0
28	0	1	0	0	0	1	0
29	0	1	0	0	1	1	0
30	0	1	0	1	0	1	0
31	0	1	0	1	1	1	0
32	0	1	1	0	0	1	0
33	0	1	1	0	1	1	0
34	0	1	1	1	0	1	0
35	0	1	1	1	1	1	0
36	1	0	0	0	0	1	0
37	1	0	0	0	1	1	0
38	1	0	0	1	0	1	0
39	1	0	0	1	1	1	0
Auto Zero	X	X	X	X	X	1	1

ADC Convert Command - (Write, Base + 10H)

The ADC Convert Command is a write only register (will not respond to reads) that is used to trigger a conversion. The data written to this location should be all ones to reduce digital noise, although the write action alone is sufficient to trigger the conversion. Execution of this command requires 0 wait states.

D15...D00
FFFF

NOTE: "FFFF" means that all bits are programmed as ones.

Read ADC Data - (Read, Base + 20H)

Use the Read ADC Data command to read the results of the last ADC conversion. This command should be used following the ADC Convert command or an external trigger input. Bit 15 (CTRIG) in the Control Register can be used to determine if a conversion has been triggered, either by software command or external trigger input. If the Read ADC Data command is executed while the ADC conversion is taking place, then the IP320 will institute wait states until the data is available (up to 8.5 uS.) before providing the ADC data and completing the cycle. Execution of the read command requires 3 wait states, if the ADC conversion completed prior to initiating the read command. The execution of this command will reset the CTRIG bit in the Control Register.

The 12-bits of data are left-justified within the 16-bit word (D16). The four LSB's are not driven by the ADC and are undefined (typically passive pull-ups on the carrier board will cause undriven bits to read high). Data format, is either Bipolar Offset Binary (BOB) or Unipolar Straight Binary (USB); see Section 2 for details.

MSB											LSB				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
←							DATA				→	X	X	X	X

"X" means “Don’t Care” - the bit value does not matter.

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The IP320 provides two different methods of analog input acquisition to give the user maximum flexibility for each application. The following sections describe the features of each and how to best use them.

Using the Separate ADC Convert and Read Commands

Use of the separate convert and read commands is a straighforward and accurate way to acquire data. This method is useful for most applications.

Programming Example (Separate ADC Convert & Read)

NOTE: For this example it is assumed that the external trigger input is NOT being used to trigger conversions.

1. Write to the control register to configure the acquisition mode, gain, and channel selections.
2. Delay to allow for input settling.
3. Execute the ADC Convert command.
4. Write to the control register to configure the acquisition mode, gain, and channel selections for the next acquisition - if they are different. This may be done while the conversion is in progress because the ADC is in the hold mode.
5. The ADC conversion takes several microseconds. This time can be put to use for other purposes (e.g. calibration of ADC channel data).
6. Read ADC Data - if the conversion is still in progress, the read command will generate wait states until it can deliver the data.
7. Repeat steps 3-6. as required to acquire additional analog input samples. Note that the input settling delay does not have to be inserted, since writing to the control register to configure for the next acquisition, immediately after initiating the previous conversion, will allow the input to adequately settle before the next conversion is started. The overlapping of these tasks with the ADC conversion cycle is what gives rise to "pipelined" operation and maximum system throughput.

Using External Conversion Triggers

External hardware triggers are generated by the user via an external TTL compatible input through the field I/O connector (see Section 2) - make sure that all pertinent voltage and pulse width constraints are met. The conversion is initiated on the falling edge of the external trigger signal. This type of conversion triggering is useful for synchronizing the ADC conversion of analog inputs (e.g. several IP320's) to external events. Precise time intervals between conversions can be achieved with an external timing device.

Programming Example (External Conversion Trigger)

NOTE: For this example it is assumed that the external trigger input is being used to trigger conversions.

1. Write to the control register to setup the acquisition mode, gain, and channel selections.
2. Delay to allow for input settling.
3. Poll Bit 15 (CTRIG) in the control register to determine when an ADC conversion has been triggered (this assumes some prior knowledge in the application program that a hardware external trigger will occur for a particular channel's conversion).
4. Read ADC Data - if the conversion is still in progress, the read command will generate wait states until it can deliver the data. The Read ADC Data command will reset the CTRIG bit in the control register to prepare for the next external trigger.
5. Repeat steps 3-4 for acquisition of the same input. Otherwise, repeat steps 1-4 as required.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Software calibration uses some fairly complex equations. Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code. The functions are written in the “C” programming language and can be linked into your application. Refer to the “README.TXT” file in the root directory and the “INFO320.TXT” file in the “IP320” subdirectory on the diskette for details.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Programmable Gain Amplifier (PGA) and the Analog to Digital Converter (ADC). The untrimmed PGA and ADC have the following performance:

PGA203KP @25^{O}C:

Linearity Error is ±0.012% Maximum (i.e. 1/2-LSB).
Offset Error RTI is ±(0.5mV + 5/Gain) Typical;
±(2mV + 24/Gain) Maximum. This is summarized as:

PGA Gain	Max Offset Error RTI (mV)	Max Offset Error RTO (mV)
1	26	26
2	14	28
4	8	32
8	5	40

Gain Error is 0.05% typical, 0.25% maximum for all gains xxxxx.

(ADC) ADS774KE @25^{O}C:

Linearity Error is ± 0.5 LSB Maximum.
Unipolar Offset Error is ± 2 LSB Maximum.
Bipolar Offset Error is ± 4 LSB Maximum.
Full Scale Calibration Error is ± 0.25% of span, Maximum.

Table 3.3 summarizes the maximum uncalibrated error combining the PGA and the ADC errors:

Table 3.3: Maximum Overall Uncalibrated Error

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Offset Error (±LSB)	Max Gain Error (±LSB)
-5 to +5	1	-5 to +5	14.7	15.4
-2.5 to +2.5	2	"	15.5	"
-1.25 to +1.25	4	"	17.1	"
-0.625 to +0.625	8	"	20.4	"
-10 to +10	1	-10 to +10	9.3	"
-5 to +5	2	"	9.7	"
-2.5 to +2.5	4	"	10.6	"
-1.25 to +1.25	8	"	12.2	"
0 to +10	1	0 to +10	12.7	20.5
0 to +5	2	"	13.5	"
0 to +2.5	4	"	15.1	"
0 to +1.25	8	"	18.4	"

Note that the worst case non-linearity error is ±1 LSB (the sum of the 1/2-LSB non-linearities of the PGA and ADC).

Calibrated Performance

Very accurate calibration of the IP320 can be accomplished by using calibration voltages present on the board. The four voltages and the analog ground reference are used to determine the endpoints of a straight line which defines the analog input characteristic. The calibration voltages are precisely adjusted at the factory to provide optimum performance, as detailed in the following table:

Calibration Signal	Ideal Value (Volts)	Maximum Tolerance @25^{O}C (Volts)	Maximum Temperature Drift (ppm/^{O}C)
Auto Zero	0.0000	±0.0002	0
CAL0	4.9000	±0.0005	±15
CAL1	2.4500	±0.0005	±20*
CAL2	1.2250	±0.0004	"
CAL3	0.6125	±0.0002	"

* Worst case temperature drift is the sum of the ±15 ppm/^{O}C drift of the calibration voltage reference plus the ±5 ppm/^{O}C drift of the resistors in the voltage divider.

The calibration voltages are used with the auto zero signal to find two points that determine the straight line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in the following table:

Table 3.4: Recommended Calib. Voltages For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Rec. Low Calib. Voltage "Volt$_{CALLO}$" (Volts)	Rec. High Calib. Voltage "Volt$_{CALHI}$" (Volts)
-5 to +5	1	-5 to +5	0.0000 (A. Z.)	4.9000 (CAL0)
-2.5 to +2.5	2	"	"	2.4500 (CAL1)
-1.25 to +1.25	4	"	"	1.2250 (CAL2)
-0.625 to +0.625	8	"	"	0.6125 (CAL3)
-10 to +10	1	-10 to +10	"	4.9000 (CAL0)
-5 to +5	2	"	"	4.9000 (CAL0)
-2.5 to +2.5	4	"	"	2.4500 (CAL1)
-1.25 to +1.25	8	"	"	1.2250 (CAL2)
0 to +10	1	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +5	2	"	"	4.9000 (CAL0)
0 to +2.5	4	"	"	2.4500 (CAL1)
0 to +1.25	8	"	"	1.2250 (CAL2)

The following equation (1) is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected\_Count} = [(4096 * m) / \text{Ideal\_Volt\_Span}] * [\text{Count\_Actual} + ((\text{Volt}_{CALLO} * \text{Gain}) - \text{Ideal\_Zero}) / m - \text{Count}_{CALLO}] \quad (1)$$

where, "m" represents the actual slope of the transfer characteristic as defined in equation 2:

$m = Gain * (Volt_{CALHI} - Volt_{CALLO}) / (Count_{CALHI} - Count_{CALLO})$ **(2)**

Gain	=	The Programmable Gain Amplifier Setting Used (See Previous Table)
$Volt_{CALHI}$	=	High Calibration Voltage (See Previous Table)
$Volt_{CALLO}$	=	Low Calibration Voltage (See Previous Table)
$Count_{CALHI}$	=	Actual ADC Data Read With High Calibration Voltage Applied
$Count_{CALLO}$	=	Actual ADC Data Read With Low Calibration Voltage Applied
Ideal_Volt_Span	=	Ideal ADC Voltage Span (See Following Table)
Count_Actual	=	Actual Uncorrected ADC Data For Input Being Measured
Ideal_Zero	=	Ideal ADC Input For Zero Count (See Following Table)

Table 3.5: Ideal Voltage Span and Zero For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	"Ideal_Volt_Span" (Volts)	"Ideal_Zero" (Volts)
-5 to +5	1	-5 to +5	10.0000	-5.0000
-2.5 to +2.5	2	"	"	"
-1.25 to +1.25	4	"	"	"
-0.625 to +0.625	8	"	"	"
-10 to +10	1	-10 to +10	20.0000	-10.0000
-5 to +5	2	"	"	"
-2.5 to +2.5	4	"	"	"
-1.25 to +1.25	8	"	"	"
0 to +10	1	0 to +10	10.0000	0.0000
0 to +5	2	"	"	"
0 to +2.5	4	"	"	"
0 to +1.25	8	"	"	"

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) for each active input range should be determined at startup and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 16) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty.

Calibration Programming Example 1

Assume that the input range is -10 to +10 volts. Channel 0 is connected differentially, and corrected input channel data is desired. From Tables 3.4 & 3.5, several calibration parameters can be determined:

Gain = 1 (From Table 3.4)
$Volt_{CALHI}$ = 4.9000 volts (CAL0; From Table 3.4)
$Volt_{CALLO}$ = 0.0000 volts (Auto Zero; From Table 3.4)
Ideal_Volt_Span = 20.0000 volts (From Table 3.5)
Ideal_Zero = -10.0000 volts (From Table 3.5)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

1. To prepare to measure $Count_{CALLO}$, write to the Control Register (@Base + 00H) to setup the auto zero acquisition mode and PGA gain = 1 by writing 0300H. Note that "not used" and "don't care" bits are set to zero.
2. Delay to allow for input settling.
3. Execute ADC Convert Command (@Base + 10H).
4. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
5. Repeat steps 3 and 4 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALLO}$.
6. To prepare to measure $Count_{CALHI}$, write to the Control Register (@Base + 00H) to setup the CAL0 acquisition mode and PGA gain = 1 by writing 0014H. Note that "not used" bits are set to zero.
7. Delay to allow for input settling.
8. Execute ADC Convert Command (@Base + 10H).
9. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
10. Repeat steps 8 and 9 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALHI}$.
11. Calculate m = actual_slope from equation 2, since all parameters are known.

    It is now possible to correct input channel data from any input channel using the same input range (i.e. -10 to +10 volts with a PGA gain = 1). Repeat steps 1-11. periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

12. To prepare to measure channel 0 differentially, write to the Control Register (@Base + 00H) to setup the differential input channel 0 acquisition mode and PGA gain = 1 by writing 0000H. Note that "not used" bits are set to zero.
13. Delay to allow for input settling.
14. Execute ADC Convert Command (@Base + 10H).
15. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word. This data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. Calculate the calibrated value "Corrected_Count". This is the desired, corrected value for input channel 0.
16. Repeat steps 12-15 to re-measure channel zero's data as desired.

Calibration Programming Example 2

Assume that the input range is 0 to +1.25 volts. Channel 39 is connected single-ended, and corrected input channel data is desired. From Tables 3.4 and 3.5, several calibration parameters can be determined:

Gain = 8 (From Table 3.4)
$Volt_{CALHI}$ = 1.2250 volts (CAL2; From Table 3.4)
$Volt_{CALLO}$ = 0.6125 volts (CAL3; From Table 3.4)
Ideal_Volt_Span = 10.0000 volts (From Table 3.5)
Ideal_Zero = 0.0000 volts (From Table 3.5)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

1. To prepare to measure $Count_{CALLO}$, write to the Control Register (@Base + 00H) to setup the CAL3 acquisition mode and PGA gain = 8 by writing 00D7H. Note that "not used" bits are set to zero.
2. Delay to allow for input settling.
3. Execute ADC Convert Command (@Base + 10H).
4. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
5. Repeat steps 3 and 4 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALLO}$.
6. To prepare to measure $Count_{CALHI}$, write to the Control Register (@Base + 00H) to setup the CAL2 acquisition mode and PGA gain = 8 by writing 00D6H. Note that "not used" bits are set to zero.
7. Delay to allow for input settling.
8. Execute ADC Convert Command (@Base + 10H).
9. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
10. Repeat steps 8 and 9 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALHI}$.
11. Calculate m = actual_slope from equation 2, since all parameters are known.

    It is now possible to correct input channel data from any input channel using the same input range (i.e. 0 to +1.25 volts with a PGA gain = 8). Repeat steps 1-11 periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

12. To prepare to measure channel 39 single-ended, write to the Control Register (@Base + 00H) to setup the single-ended input channel 39 acquisition mode and PGA gain = 8 by writing 02D3H. Note that "not used" bits are set to zero.
13. Delay to allow for input settling.
14. Execute ADC Convert Command (@Base + 10H).
15. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word. This data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. Calculate the calibrated value "Corrected_Count". This is the desired, corrected value for input channel 39.
16. Repeat steps 12-15 to re-measure channel 39's data as desired.

Error checking should be performed on the "Corrected_Count" value to make sure that calculated values below 0 or above 4095 are restricted to those end points. Note that the software calibration cannot recover signals near the end points of each range which are clipped off due to the uncalibrated hardware (e.g. PGA and ADC).

The maximum corrected (i.e. calibrated) error is summarized in Table 3.6 as the worst case accuracy possible for each range. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25^{o}C. Typical accuracies are significantly better.

Table 3.6: Maximum Overall Calibrated Error @25ºC

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Error ± LSB(% Span)
-5 to +5	1	-5 to +5	1.8 (0.044)
-2.5 to +2.5	2	"	2.1 (0.051)
-1.25 to +1.25	4	"	2.5 (0.061)
-0625 to +0.625	8	"	2.9 (0.071)
-10 to +10	1	-10 to +10	2.8 (0.069)
-5 to +5	2	"	1.8 (0.044)
-2.5 to +2.5	4	"	2.1 (0.051)
-1.25 to +1.25	8	"	2.5 (0.061)
0 to +10	1	0 to +10	3.2 (0.078)
0 to +5	2	"	2.2 (0.055)
0 to +2.5	4	"	3.1 (0.076)
0 to +1.25	8	"	5.1 (0.125)

4.0 THEORY OF OPERATION

This section describes the functionality of the IP320 circuitry. Refer to the block diagram of Drawing 4501-436 as you study the following paragraphs.

ANALOG INPUTS

The field I/O interface (via the carrier board) is through connector P2. Field analog inputs are non-isolated. This means that the field analog return and logic common have a direct electrical connection. Care must be taken to avoid ground loops and excessive common mode voltage (see Section 2 for connection recommendations). These can cause measurement error, and with extreme abuse, circuit damage.

Analog inputs and calibration voltages are selected via CMOS analog multiplexers (MUX's). A software programmable control register contains gain, acquisition mode (e.g. single-ended or differential) and channel selection information to control the multiplexers. Up to 40 single-ended inputs can be monitored, where each channel's +input is individually selected along with a single sense lead for all channels. Up to 20 differential inputs can be monitored, where each channel's + and - inputs are individually selected. Single-ended and differential channels cannot be mixed (i.e. they must all be single-ended or differentially wired). A Programmable Gain (Instrumentation) Amplifier (PGA) takes as input the selected channel's + and - inputs (or + and sense) and outputs a single-ended voltage proportional to it. The gain can be 1, 2, 4, or 8, and is selected through the control register.

The output of the PGA feeds the Analog to Digital Converter (ADC). The ADC is a state of the art, 12-bit, successive approximation converter with a built-in Sample and Hold (S/H) circuit. The S/H goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then it returns to the sample mode to acquire the next channel. Once a conversion has been started, the control register can be updated for the next channel. This allows the input to settle for the next channel while the previous channel is converting, which gives rise to the pipelined mode of operation (and maximum system throughput).

Hardware jumpers J1 and J2 control the range selection for the ADC (-5 to +5, -10 to +10, or 0 to +10 Volts) as detailed in Section 2. Jumper selection should be made prior to powering the unit. Thus, all channels will use the same ADC range. However, the analog input range can vary on an individual channel basis depending on the programmable gain selection.

The logic interface provides ±12 Volt supplies to the analog circuitry. The -10 to +10 and 0 to +10 Volt ADC ranges will be clipped if these supplies are used, typically to ±9 Volt maximum inputs. The user has the option of providing ±15 Volt external supplies to fully utilize input ranges to ±10 Volts. These supplies are selected via hardware jumpers J3 and J4 as detailed in Section 2. Note that jumper selection should be made prior to powering the unit. Further, internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts).

The board contains four precision voltage references and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for any desired ADC range and gain combination, when compared to fixed hardware potentiometers for offset and gain calibration of the ADC and PGA. The calibration signals are selected (multiplexed into the PGA) like any other input channel.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1. Not all of the IP logic P1 pin functions are used (refer to Table 2.6). P1 also provides +5V and ±12V to power the module.

A programmable logic device installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O and ID spaces and produces the chip selects, control signals, and timing required by the ADC, control register, and ID PROM, as well as, the acknowledgement signal required by the carrier board per the IP specification. The control logic also provides the trigger to start an ADC conversion. This may be initiated by software commands or by a user-generated external trigger input from connector P2 (see Sections 2 and 3 for details).

The ID PROM (read only) installed on the IP module provides the identification for the individual module per the IP specification. The programmable control register is read/write and has been described with the analog input circuitry. The ID PROM, control register, and ADC data are all accessed through the 16-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....0 to +70°C
…….-40 to +85°C (E Version)
Relative Humidity.....5-95% non-condensing
Storage Temperature.....-40 to +100°C
…….-55 to +105°C (E Version)
Physical Configuration.....Single Industrial I/O Pack Module
Length.....3.900 in. (99.0 mm)
Width.....1.800 in. (45.7 mm)
Board Thickness.....0.062 in. (1.59 mm)
Max Component Height.....0.314 in. (7.97 mm)
Connectors:
P1 (IP Logic Interface)... .....50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O).....50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%).....270mA Typical, 350mA Maximum
+12 Volts (±5%) from P1 or....12mA Typical, 20mA Maximum
+15 Volts (±5%) from P2.....(See Note 1)
-12 Volts (±5%) from P1 or.....8mA Typical, 20mA Maximum.
-15 Volts (±5%) from P2.....(See Note 1)
Non-Isolated.....Logic and field commons have a direct electrical connection.

Note:
1. The ±12 volt power supplies are normally supplied through P1 (logic interface connector). Optionally (jumper selectable on the IP), the user may connect external ±15 volt supplies through the field I/O interface connector, P2.

ANALOG INPUTS

Input Channels (Field Access).....40 Single-ended or 20 Differential Ended.
Input Signal Type.....Voltage (Non-isolated).
Input Ranges (jumper selectable):
Bipolar -5 to +5 Volts.....(See Note 2).
Bipolar -10 to +10 Volts.....(See Notes 2 & 3).
Unipolar 0 to +10 Volts.....(See Notes 2 & 3).
Programmable Gains.....x1, x2, x4, x8.

Input Overvoltage Protection.....±32 Volts with power applied, ±20 Volts unpowered.
Input Resistance.....1000 MΩ, Typical.
Input Bias Current.....1nA Typical.
Common Mode Rejection Ratio.....71dB Typical, 60Hz.
CH-to-CH Rejection Ratio.....71 dB Typical, 60Hz.
Resistance to RFI.....Error is less than ±0.25% of FSR with field strengths up to 10V/m at frequencies of 27MHz, 159MHz, 460MHz.
A/D Resolution.....12-bits.
Data Format (left-justified).....Bipolar: Bipolar Offset Binary (BOB); Unipolar: Unipolar Straight Binary (USB).
No Missing Codes.....No Missing Codes Over Temperature, 12-bits.
A/D Integral Linearity Error.....±1/2 LSB Maximum.
System Accuracy (See Note 4)....The maximum corrected (i.e. calibrated) error is summarized in the following table as the worst case accuracy possible for each range. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C. Typical accuracies are significantly better.

Maximum Overall Calibrated Error @ 25°C

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Error ±LSB (% Span)
-5 to +5	1	-5 to +5	1.8 (0.044)
-2.5 to +2.5	2	"	2.1 (0.051)
-1.25 to +1.25	4	"	2.5 (0.061)
-0625 to +0.625	8	"	2.9 (0.071)
-10 to +10	1	-10 to +10	2.8 (0.069)
-5 to +5	2	"	1.8 (0.044)
-2.5 to +2.5	4	"	2.1 (0.051)
-1.25 to +1.25	8	"	2.5 (0.061)
0 to +10	1	0 to +10	3.2 (0.078)
0 to +5	2	"	2.2 (0.055)
0 to +2.5	4	"	3.1 (0.076)
0 to +1.25	8	"	5.1 (0.125)

Settling Time (10V step).....8.5uS to 0.01% of FSR.
A/D Conversion Time.....8.5uS Maximum (includes S/H acquisition).
A/D Triggers.....External and Software.
Maximum Throughput Rate...100K conversions/second Maximum (with 10 uS per conversion/read in pipelined mode).
Input Noise.....0.2 LSB rms, Typical (with PGA Gain = 1).
Temperature Coefficient.....See specification of calibration voltages.

Notes:

2. Range assumes the programmable gain is equal to one. Additional ranges are created with other gains. Divide the listed range by the programmable gain to determine the actual input range. Input signal ranges may actually fall short of reaching the specified endpoints due to hardware limitations. For example, if an input may reach zero volts or less, a bipolar input range should be selected.
3. These ranges can only be achieved with ±15 Volt external power supplies. The input ranges will be clipped if ±12 Volt supplies are used, typically to ±9 Volt maximum inputs.
4. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. For critical applications multiple input samples can be averaged to improve performance. Accuracy is specified for the software conversion command. Use of the external hardware trigger input with software polling may degrade accuracy. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.

   Programmable Calibration Voltages follow:

Calib. Signal	Ideal Value (Volts)	Maximum Tolerance @25°C (Volts)	Max Temperature Drift (ppm/°C)
Auto Zero	0.0000	±0.0002	0
CAL0	4.9000	±0.0005	±15
CAL1	2.4500	±0.0005	±20*
CAL2	1.2250	±0.0004	"
CAL3	0.6125	±0.0002	"

* Worst case temperature drift is the sum of the ±15 ppm/°C drift of the calibration voltage reference, plus the ±5 ppm/°C drift of the resistors in the voltage divider.

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per revision 0.7.1.
Electrical/Mechanical Interface.....Single-Size IP Module.
IP Data Transfer Cycle Types Supported:
  Input/Output (IOSel*).....16-bit word read of 12-bit left-justified ADC data; 16-bit read/write of control register; conversion request (write).
  ID Read (IDSel*).....32 x 8 ID PROM read on D0..D7.
Access Times (8MHz Clock):
  ID PROM Read.....0 wait states (250ns cycle).
  Control Register Read.....0 wait states (250ns cycle).
  Control Register Write.....1 wait state (375ns cycle).
  Conversion Request (Write)...0 wait states (250ns cycle).
  Read ADC Data (Note 5).....3 wait states (625ns cycle).

Note:

5. The 3 wait states specified assumes that the previous conversion has been completed, and that data is available to be read. If a conversion is in progress, the command will institute wait states until the data can be delivered. This could take up to 8.5uS, maximum.

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

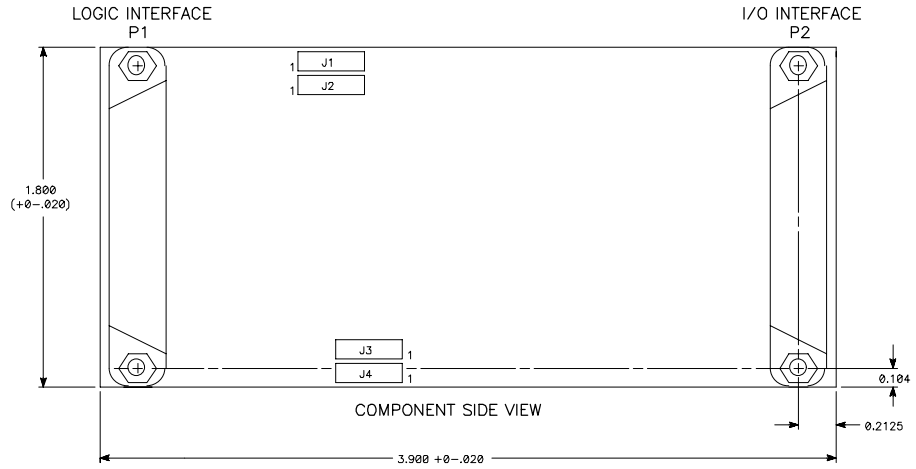
Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board P3-P6 connectors (Both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (P3-P6 connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The P3-P6 connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packed.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 50-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage, or to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.



ANALOG INPUT RANGE SELECTION (PINS J1 AND J2)

DESIRED ADC INPUT RANGE (VOLTS)	REQUIRED INPUT SPAN (VOLTS)	J1 (1 & 2)	J1 (2 & 3)	REQUIRED INPUT TYPE	J2 (1 & 2)	J2 (2 & 3)
−5 TO +5	10	IN	OUT	BIPOLAR	OUT	IN
−10 TO +10*	20	OUT	IN	BIPOLAR	OUT	IN
0 TO +10 *	10	IN	OUT	UNIPOLAR	IN	OUT

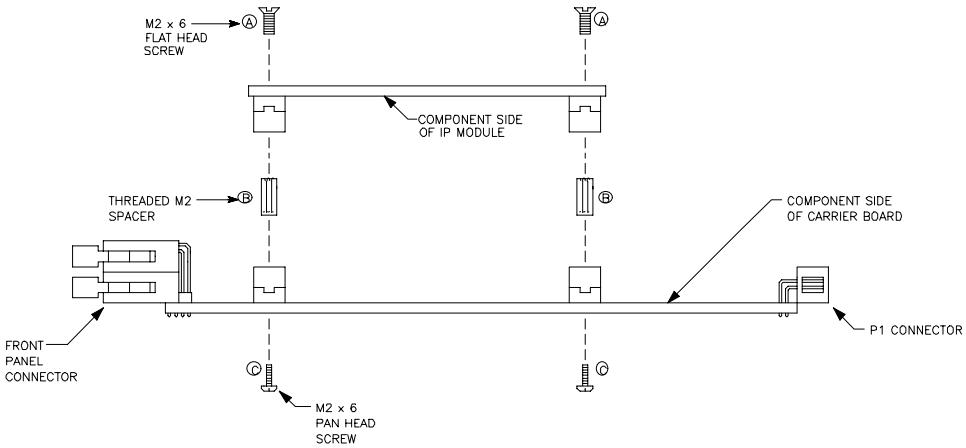
* THESE RANGES CAN ONLY BE ACHIEVED WITH +/−15 VOLT EXTERNAL POWER SUPPLIES. THE INPUT RANGES WILL BE CLIPPED IF +/−12 VOLT SUPPLIES ARE USED, TYPICALLY TO +/−9 VOLT MAXIMUM INPUTS.

POWER SUPPLY SELECTIONS (PINS OF J3 AND J4)

POWER SUPPLY SELECTION *	J3 (1 & 2)	J3 (2 & 3)	J4 (1 & 2)	J4 (2 & 3)
+/−12 VOLT (INTERNAL, P1)	OUT	IN	OUT	IN
+/−15 VOLT (EXTERNAL, P2)	IN	OUT	IN	OUT

* INTERNAL AND EXTERNAL SUPPLIES SHOULD NOT BE MIXED (E.G. DO NOT USE +12 VOLTS WITH −15 VOLTS).

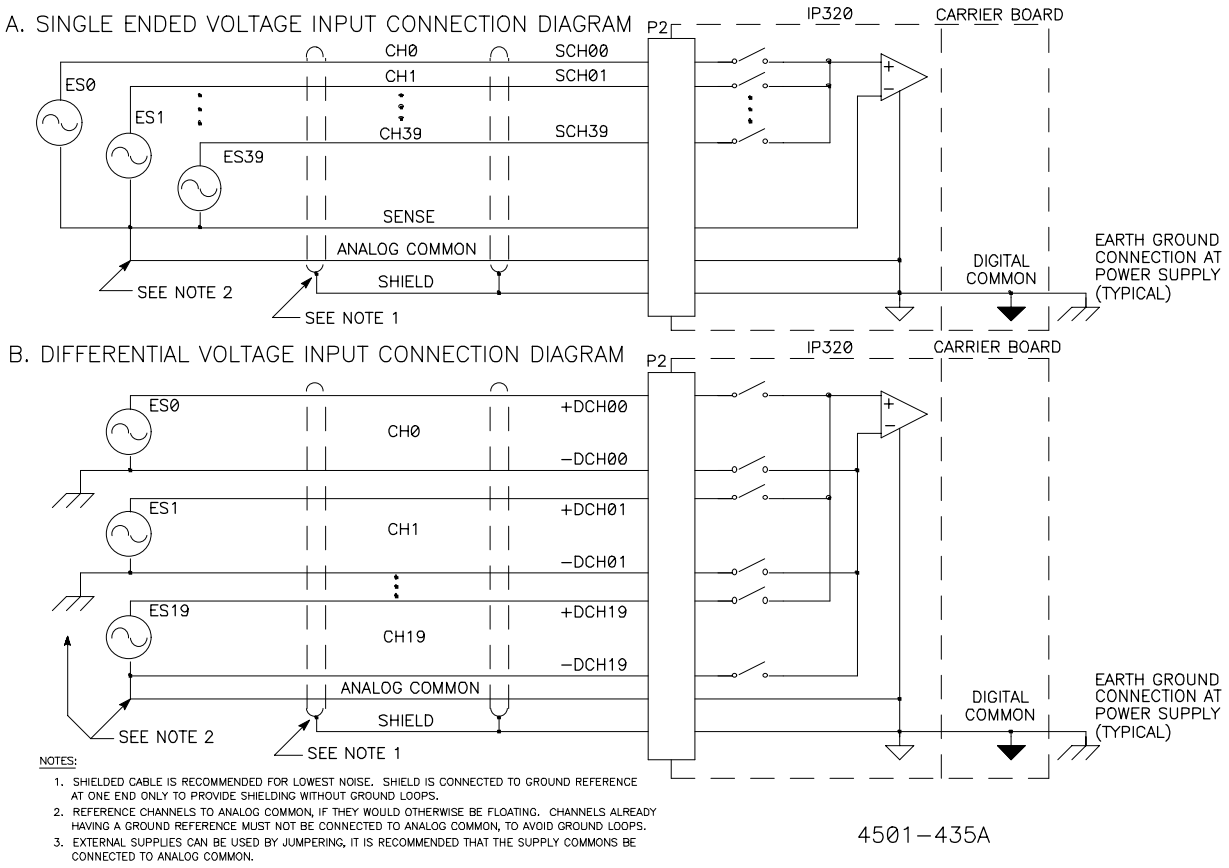
IP320 JUMPER LOCATIONS 4501−433A



ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

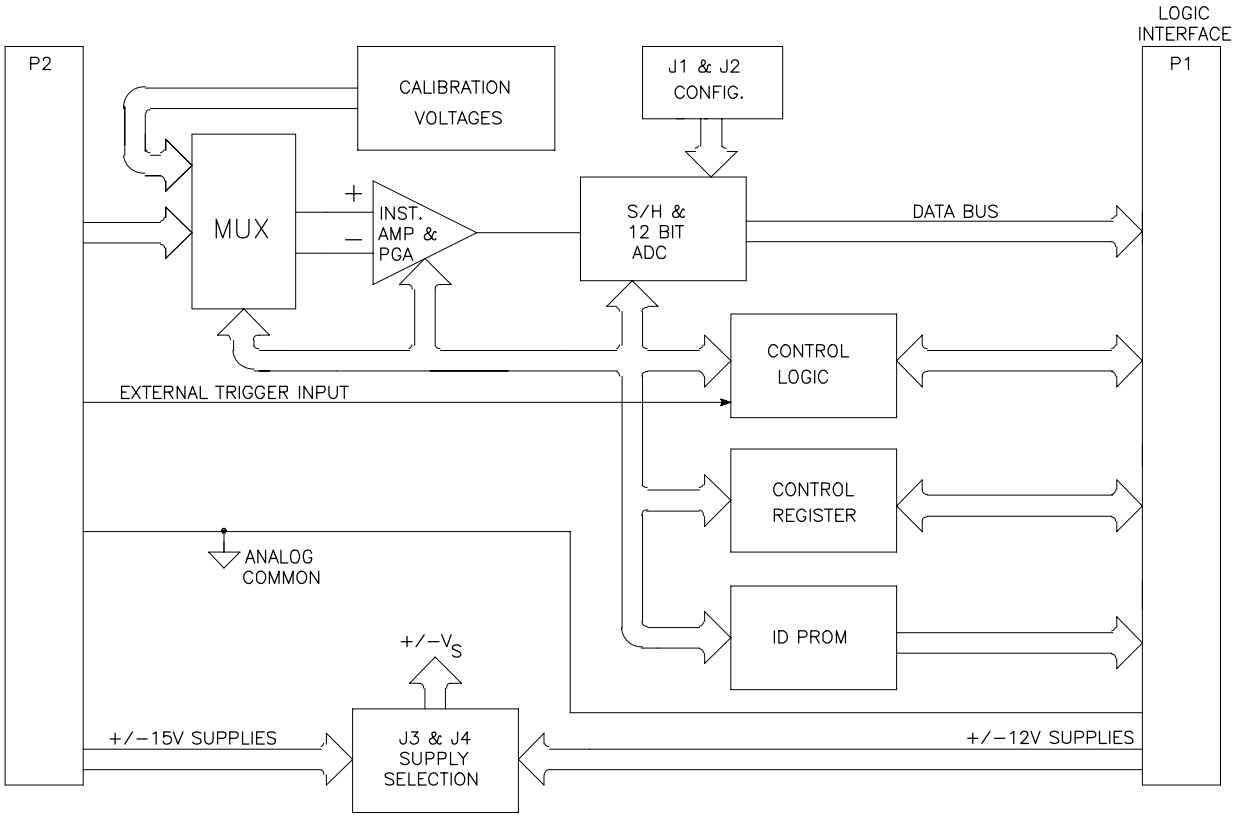
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501−434B



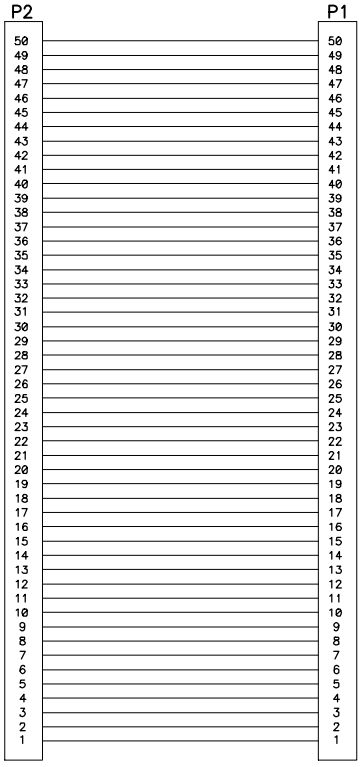
NOTES:

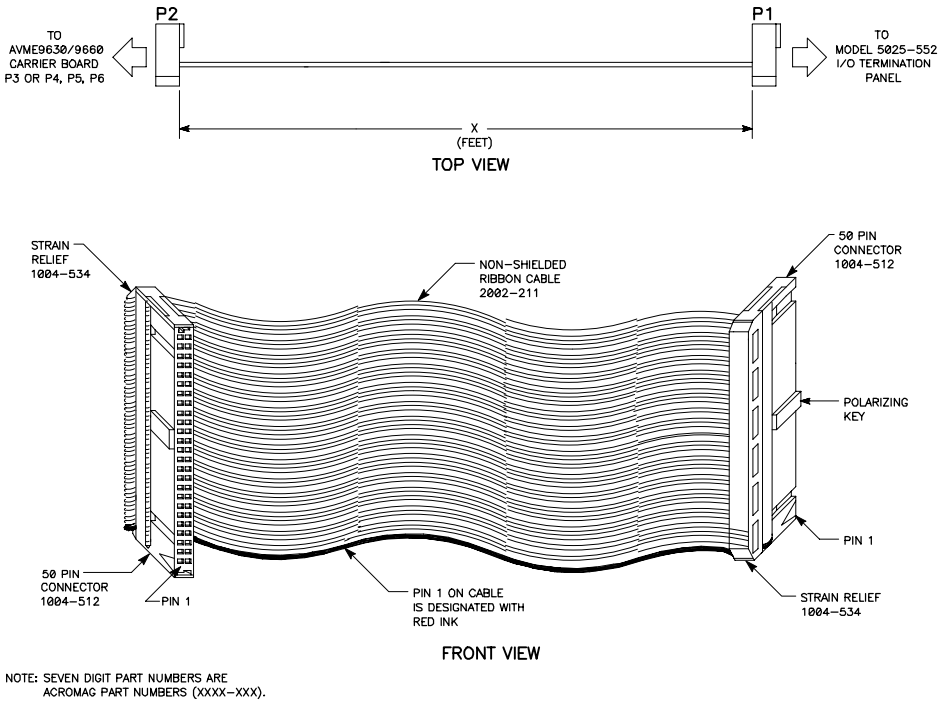
1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.
3. EXTERNAL SUPPLIES CAN BE USED BY JUMPERING, IT IS RECOMMENDED THAT THE SUPPLY COMMONS BE CONNECTED TO ANALOG COMMON.

4501−435A

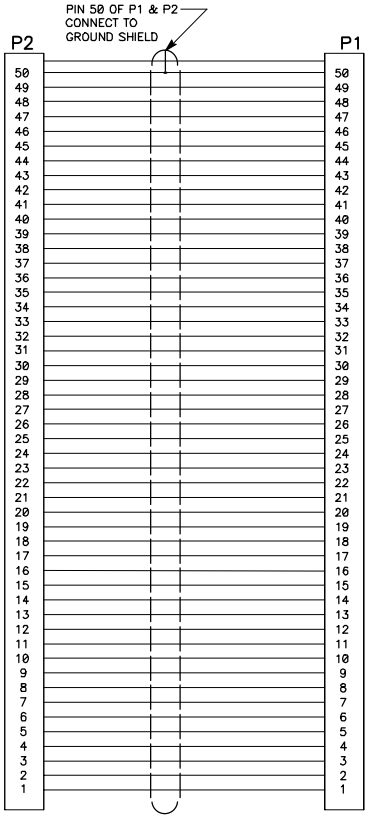


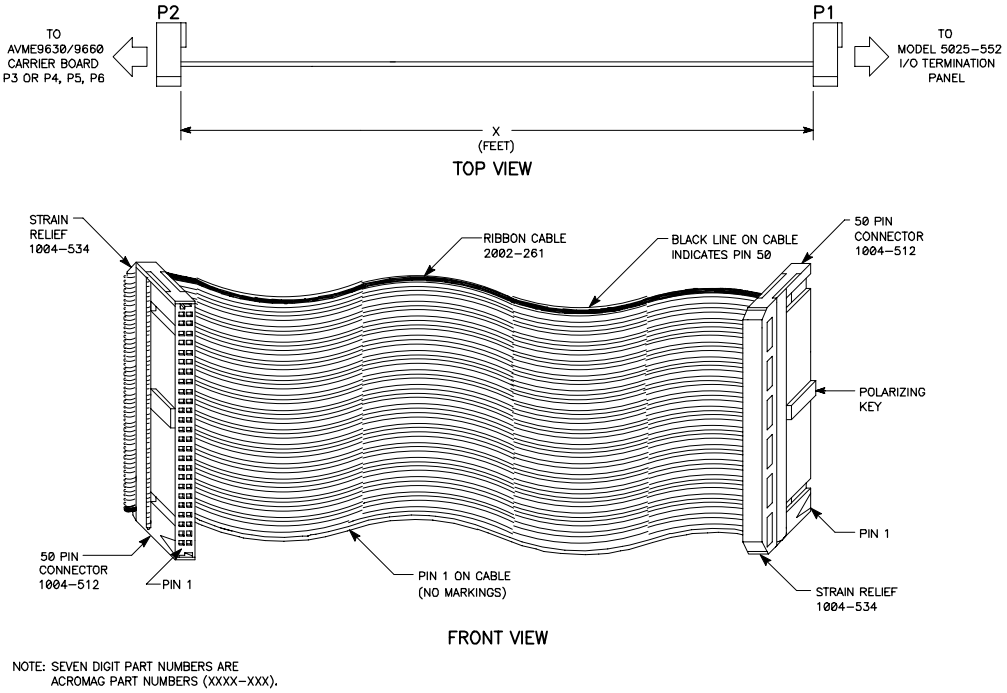
IP320 BLOCK DIAGRAM 4501−436A



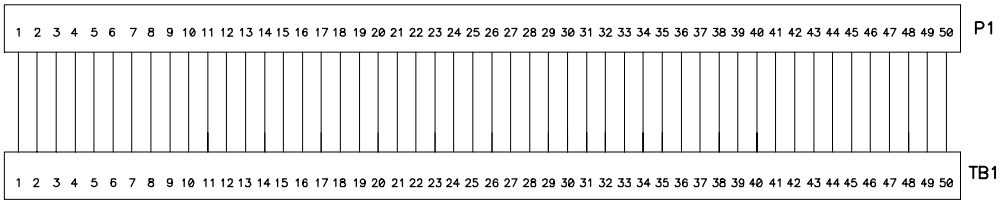


MODEL 5025-550-x SCHEMATIC MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED 4501-462A

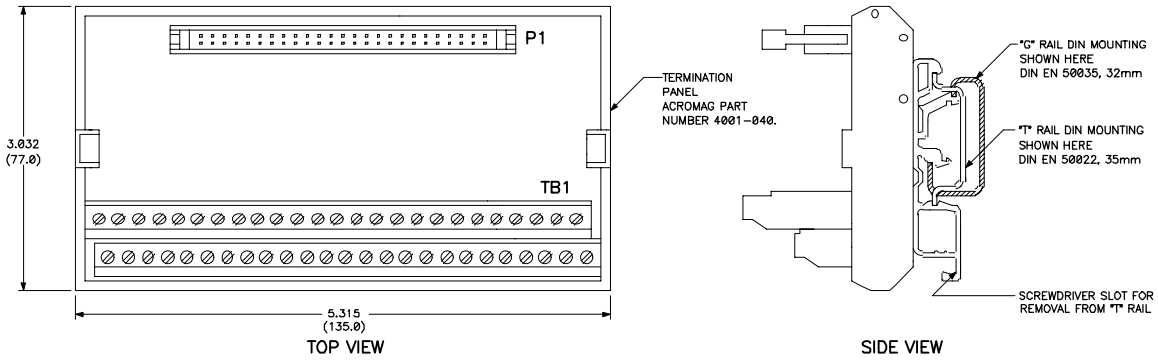




MODEL 5025-551-x SCHEMATIC MODEL 5025-551-x SIGNAL CABLE, SHIELDED 4501-463A



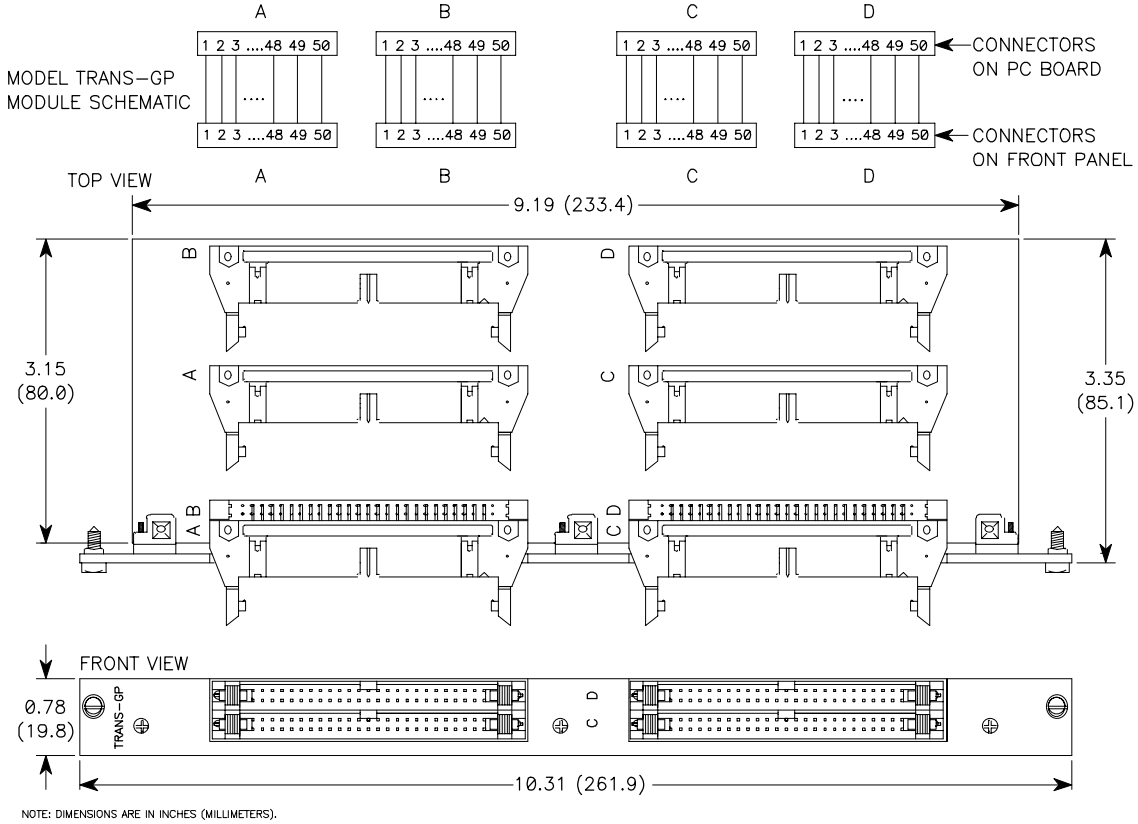
MODEL 5025–552 TERMINATION PANEL SCHEMATIC



NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).

MODEL 5025–552 TERMINATION PANEL

4501–464A



NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).

TRANS–GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC 4501–465A