VME - DPIO32

32 digital Inputs or Outputs

Hardware Manual

N O T E

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Described PCB version	DPI32-5 S/N AB043 and later

Changes in the chapters

The changes in the user's manual listed below affect changes in the **firmware**, as well as changes in the **description** of the facts only.

Chapter	Change
2.	Chapter 'Software' now a separate document.

Further technical changes are subject to change without notice.

User's Manual DPIO32

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1. Hardware

1.1 Overview

1.1.1 Board Description

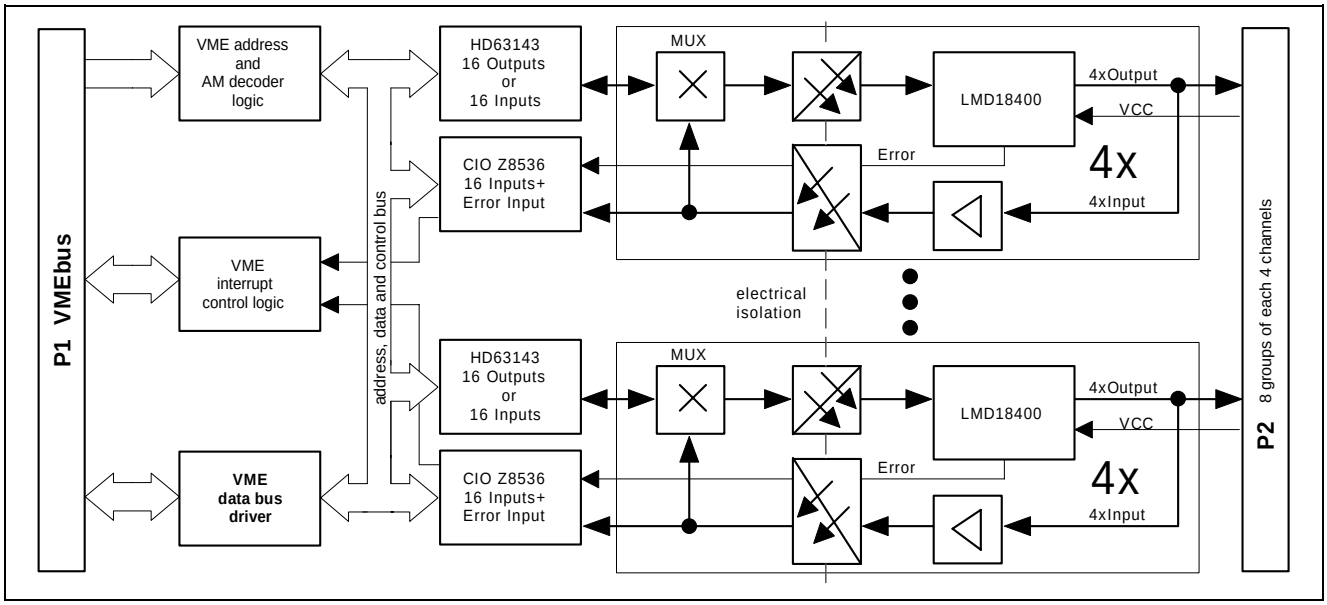


Fig. 1.1.1: Block Diagram of VME-DPIO32

The VME board VME-DPIO32 offers a digital process interface containing 32 optoisolated inputs or outputs. The board is designed in 6 U format and covers one slot.

The 32 digital I/O channels are arranged in 8 electrically isolated groups. Each group of 4 channels has the same reference potential. The user can allocate input or output operation to each group separately.

The input voltage range of the channels is between 5 V(DC) and 30 V(DC). Each input channel can generate an interrupt on the VMEbus on a programmable edge (rising or falling). The inputs are voltage-proof between -3 V(DC) and +36 V(DC).

The digital outputs can be operated at voltages between 6 V and 28 V(DC). The continuous outputs current at 24 V supply voltage is 0.3 A. The component LMD18400 is used as output driver.

The driver protective circuit is activated at short-circuit, over-temperature or overvoltage. An error signal of the drivers will be generated at short-circuit to GND, to VCC, at running without load, overvoltage or overtemperature of the driver component.

In addition to the bit-programmable operating mode of the outputs, it is possible to use the single output channels via the pulse processor components HD63143 for pulse-width modulation (PWM). A total of 2 x 24 programmable 16 bit registers are available for switching period and resolution. The minimum switching period amounts to 10 µs. The outputs can mutually be synchronised.

A total of 20 digital counter inputs of the controllers is available. At this, four of which are connected in parallel to CIO 8536 and to HD63143. The maximum counter frequency for these four CIO counters is 3 MHz. Depending on the operating mode, the HD63143 counters can process frequencies from 100 kHz to 1 MHz. For the counter inputs various operating modes are possible (event counter, pulse-width measurement, frequency measurement, free running with interrupt, incremental encoder inputs etc.).

The actual I/O status of the inputs and outputs is displayed on the front panel of VME-DPIO32 by a two-colored LED for each channel, the error status is displayed group-wise. Additionally there are test sockets for each channel located on the front panel for simulation of the input signals or for disable of the error messages.

1.1.2 Summary of Technical Data

VME specification	
VME interface	IEEE 1014 / D
data transfer mode	SADO24 - slave with A24/D16 access SD16 - slave with A16/D16 access
address modifier (AM)	full evaluation of AM0 to AM5, additionally 'AM2 don't care' circuit possible
basic address	selectable by jumpers over the whole address range of 16 Mbytes
interrupts	I1 to I7 interrupter, level programmable via HD63143

general data	
temperature range	0...70°C ambient temperature
humidity	max. 90%, non-condensing
connector types	P1-DIN 41612-C96 P2-DIN 41612-C64
board size	160 mm x 233 mm
VME dimensions	6 U height / 1 slot width
weight	ca. 470 g
power supply	VMEbus P1: 5V ± 5% (typical values at 20 °C): all outputs OFF: 1.7 A all outputs ON: 2.3 A 16 outputs ON, 16 OFF: 1.7 A all outputs OFF, all inputs ON: 2.3 A

digital outputs	
quantity	32 (less inputs) P-switching: Out = 24 V --> '1' Out = 0 V --> '0'
supply voltage	U*vccmin* = 6 V (DC) U*vccmax* = 28 V (DC) U*vccrated* = 24 V (DC)
load capacity (at 50°C)	rated current/channel (24 V): I*r* = 0.3 A max. current/channel: limited by over-temperature protection (see data sheet of LMD18400) max. current/board: 16 A signal level of outputs at rated current: ≥ U*vcc*-2 V
protective circuits	short-circuit protection and over-temperature protection: electronically with switch-off of output group, overvoltage protection (triggering from U*vcc* > 32 V..35 V)
switching performance (at 20°)	values for U*vccrated* and I*r*: min. pulse time T ≥ 10 µs min. clock periode T*ON* ≥ 10 µs, T*OFF* ≥ 10 µs (With this switching times the signal edges are bad. Additionally the times may become longer due to circuit tolerance and ambient temperature.)
electrical isolation from VMEbus potential	by optocouplers, acc. to VDE 0110b §8, isolation class C: 250 V(AC)/300 V(DC)

digital inputs (part 1)	
quantity	32 (less outputs)
evaluation	all inputs have interrupt capability max. 16 inputs at P2 configurable as counter inputs, all 16 inputs connected to HD63143 and additionally 4 inputs in parallel to CIO Z8536 (higher resolution)
input voltage	permissible input voltage range: -3 V ≤ Uin ≤ 30 V **Attention:** If output driver LMD18400 is supplied by U*vccout*,U*in* may not exceed ***Uin*** ≤ ***Uvccout*** **- 2V** ! (because of parallel connection to outputs) threshold input = '0': U*out* ≤ 2.0V threshold input = '1': U*in* ≥ 3.0V
input current	Since the inputs and outputs are connected in parallel on the board, the input current depends on the fact, whether the supply voltage is connected to the output driver LMD18400: input current/channel at U*vcc* = 24 V (typical values at 20 °C): input = '1': (5 V) I*in* = 7.7 mA (12 V) I*in* = 9.9 mA (22 V) I*in* = 10.0 mA input current/channel at U*vcc* not supplied (typical values at 20 °C): input = '1': (5 V) I*in* = 8.0 mA (12 V) I*in* = 14.0 mA (24 V) I*in* = 30.0 mA (30 V) I*in* = 40.0 mA

digital inputs (part 2)	
input frequency	input circuit (max.): 1 MHz (1:1) counter frequency of controller HD63143 (depends on the complexity of the functions): just one function: t*high* > 0.5 µs, t*low* > 0.5 µs f*max* < 1 MHz (duty cycle 1:1) 16 functions: t*high* > 5.0 µs, t*low* > 5.0 µs f*max* < 100 kHz (duty cycle 1:1) counter frequency of controller CIO 8536 max. 3 MHz
protective circuit	overvoltage protection by Transsil diode voltage-proof up to... statically: U*max* = 36 V dynamically: U*max* = 95 V (duty cycle 1/100, t*on* = 10 µs) U*max* = 225 V (duty cycle 1/1000, t*on* = 10 µs)
electrical isolation from VMEbus potential	by optocouplers, acc. to VDE 0110b §8, isolation class C: 250 V(AC)/300 V(DC)

Table 1.1.1: Technical Data of VME-DPIO32

1.1.3 Software Support

Driver packages for DPIO32 are available e.g. for operating systems VxWorks and OS9.

1.2 Order Information

Type	Features	Order no.
VME-DPIO32	32 digital inputs/outputs, PWM, counter, timer	V.1607.02
VME-DIOC-ADAPT1	terminal blocks for P2	V.1601.01
VME-DIOC-ADAPT2	terminal blocks for P2	V.1601.02
VME-DPI32-P2VCC	24 V connection for P2	V.1604.90
VME-DPI32-OS9	C driver for OS-9 as source code	P.1607.50
VME-DPI32-T	test program PEARL	P.1607.54
VME-DPIO32-MD	additional German user's manual	M.1607.20
VME-DPIO32-ME	additional English user's manual	M.1607.21

Table 1.2.1: Order Information

1.3 Address Covering of VME-DPIO32

address range	D15-D8	D7-D0
nn ss FE nn ss F8	CIO2 (Z8536)	CIO1 (Z8536)
nn ss F6 nn ss F0	RAM of HD2 (HD63143)	RAM of HD1 (HD63143)
nn ss DE nn ss 00	HD2 (HD63143)	HD1 (HD63143)

nn ss ....basic address of DPIO32 for 'standard address accesses'
via VMEbus (A08 - A23 = CARD-ADDRESS)
ss .....basic address of DPIO32 for 'short address accesses'
via VMEbus (A08 - A15 = CARD-ADDRESS)

Table 1.3.1: Address Covering of VME-DPIO32

1.4 Jumpers Configuration

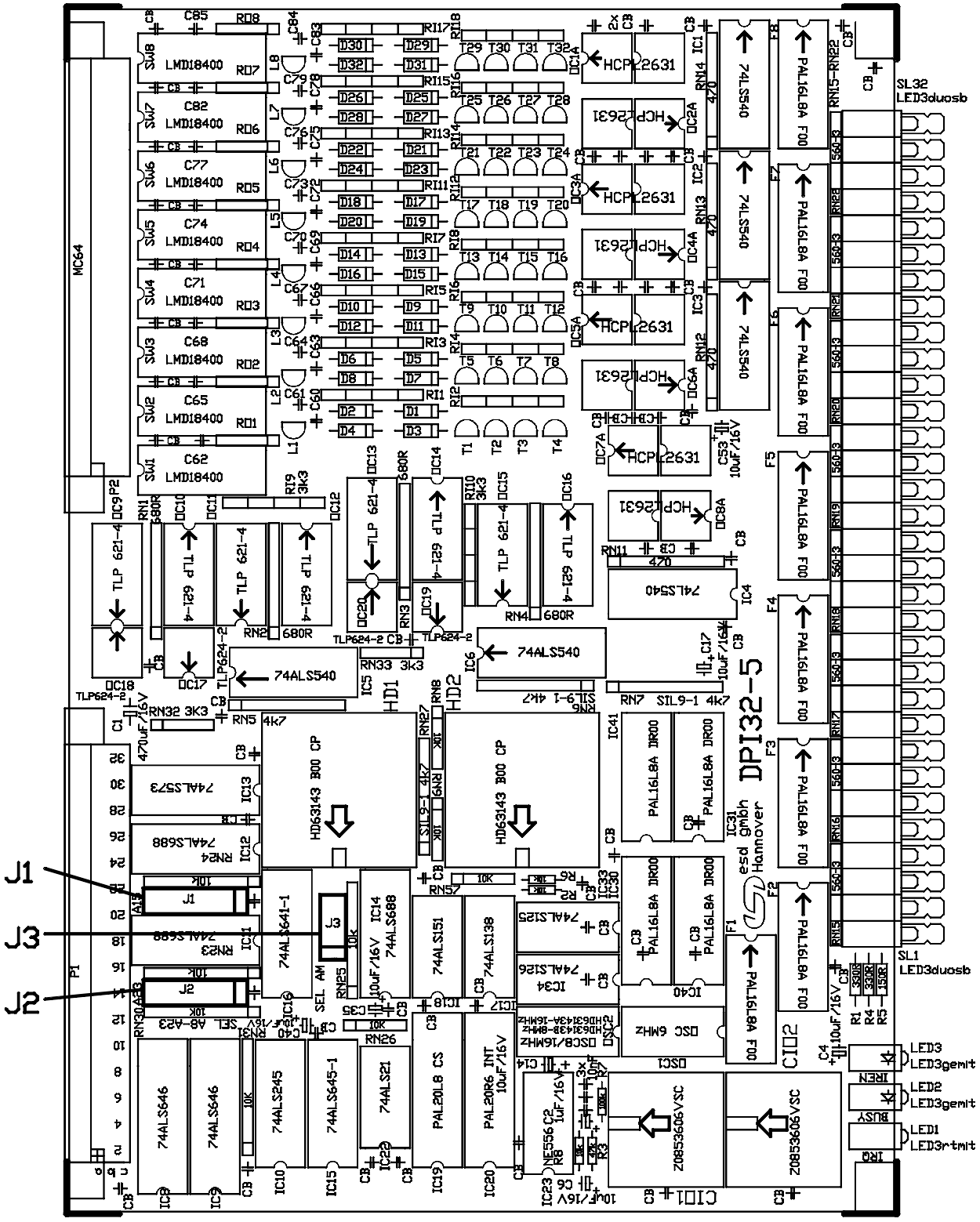


Fig. 1.4.1: Jumpers Position on VME-DPIO32

1.4.1 Default Setting

The particular factory-settings (of the jumpers see following table) are marked in the table.

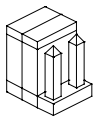
The jumpers configuration can be obtained from the insertion diagram.
An inserted jumper corresponds to '0' (low) level of a signal.

In the following the jumpers are displayed in a position, as seen by the user, if he has the board lying in front of himself with the VMEbus connectors to the rear end.

Default jumper setting of jumpers J1 to J4:

jumper	function	setting
J1	basic address A08-A15	basic address of DPIO32 set to $xxE14000
J2	basic address A16-A23	
J3	address modifier	AM2 don't care, i.e. access in the supervisory mode or user mode VME access A24/D16

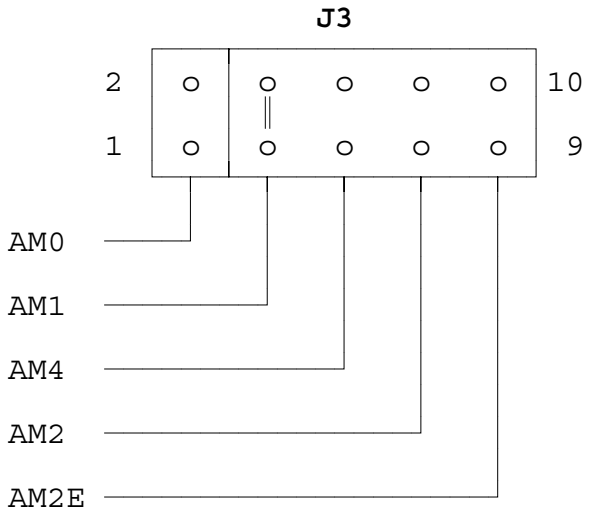
Table 1.4.1: Default Jumper Setting



1.4.2 The Address-Modifier AM Jumper J3

The DPIO32 can be operated with access modes A24/D16 (standard) or A16/D16 (short).
At the default setting of jumpers displayed below A24/D16 accesses to the board are enabled. AM2 will be ignored, so user mode as well as supervisory mode can be used for addressing.

Default setting: Standard supervisory and nonprivileged data access (A24-Mode)



The jumpers AM0, AM1 and AM4 are evaluated 'separately'. The jumpers AM2 and AM2E form a unit and are always evaluated together.

The jumpers AM0, AM1 and AM4 are evaluated as follows:

jumper/ pins	signal decoding	
	not inserted	inserted
AM0 1-2	1	0
AM1 2-3		
AM4 4-5		

Table 1.4.2: Evaluation of Jumpers AM0, AM1 and AM4

Permissible Positions of Jumpers AM2 and AM2E are as follows:

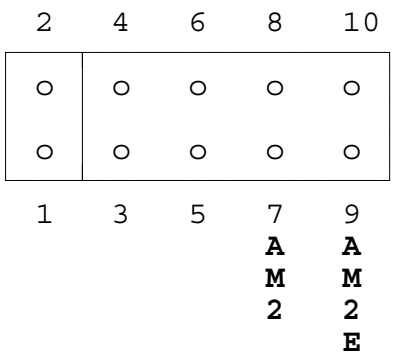
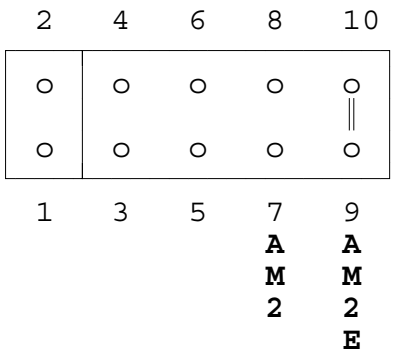
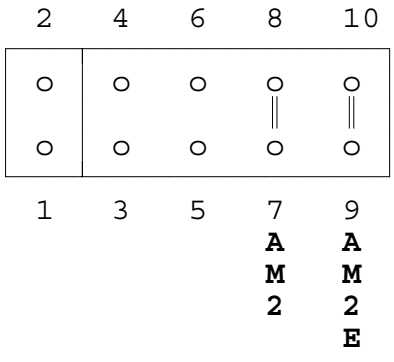
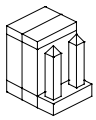
Position of jumpers AM2 and AM2E	evaluation
	AM2 = don't care
	AM2 = 1 (supervisory modes only)
	AM2 = 0 (non-privileged modes only)

Table 1.4.3: Permissible Positions of Jumpers AM2 and AM2E



Meaningful address modifier jumpers combinations for 24 accesses are recommended as follows:

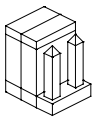
jumper J3	permissible AM codes		addressing mode
	AM5 AM4 AM3 AM2 AM1 AM0	HEX	
2 4 6 8 10 o o o o o o ‖ o o o o o o o o o 1 3 5 7 9	1 1 1 0 0 1 1 1 1 1 0 1	39 3D	standard non-privileged data access or standard supervisory data access
2 4 6 8 10 o o o o o o ‖ o o o ‖ o o o o o 1 3 5 7 9	1 1 1 1 0 1	3D	standard supervisory data access
2 4 6 8 10 o o o o o o ‖ o ‖ ‖ o o o o o 1 3 5 7 9	1 1 1 0 0 1	39	standard non-privileged data access

Table 1.4.4: Recommended Access Modes for Standard Accesses (A24)

Meaningful address modifier jumpers combinations for 16 accesses are recommended as follows:

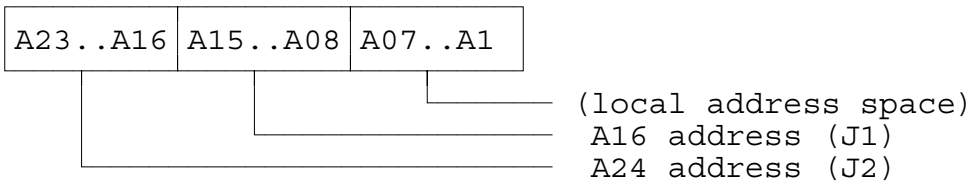
jumper J3	permissible AM codes AM5 AM4 AM3 AM2 AM1 AM0	HEX	addressing mode
2 4 6 8 10 o o o o o o o o o o 1 3 5 7 9	1 0 1 0 0 1 1 0 1 1 0 1	29 2D	short non-privileged access or short supervisory access
2 4 6 8 10 o o o o o o o o o o 1 3 5 7 9	1 0 1 1 0 1	2D	short supervisory access
2 4 6 8 10 o o o o o o o o o o 1 3 5 7 9	1 1 1 0 0 1	29	short non-privileged access

Table 1.4.5: Recommended Access Modes for Short Accesses (A16)

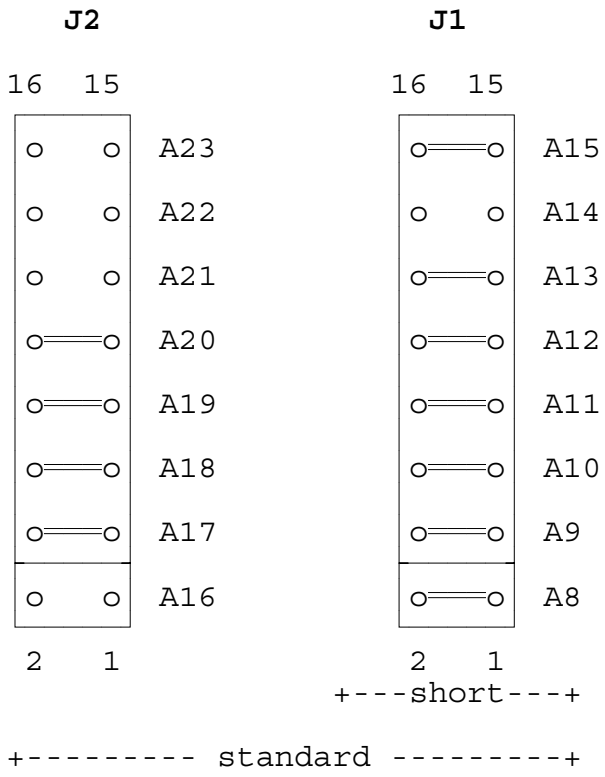


1.4.3 Basic Address Decoding via the Jumpers J1 and J2

The basic address of VME-DPIO32 is set as follows:



Default setting = $E14000



An inserted jumper corresponds to the 'low' level of an address bit.

1.5 Interrupt Processing

The CIO Z8536 components CIO1 and CIO2 can generate an interrupt on a rising or falling edge of their input signals. The programming of the CIOs determines, at which edge the interrupt shall be generated.

The two local interrupt requests are combined in the interrupt logic. If the interrupt enable bit is set, an interrupt can be generated on the VMEbus, the level of which is freely programmable.

Via port 5 of HD2 (HD63143) the interrupt enable bit is set and the determination of the interrupt levels vorgenommen:

Local address: $000C HEX

Bit	D7	D6	D5	D4	D3	D2	D1	D0
	x	x	x	x	IREN	LEV3	LEV2	LEV1

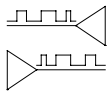
LEV1, LEV2, LEV3: VMEbus interrupt level:

LEV3 (D2)	LEV2 (D1)	LEV1 (D0)	VMEbus interrupt level
0	0	1	IRQ1*
0	1	0	IRQ2*
0	1	1	IRQ3*
1	0	0	IRQ4*
1	0	1	IRQ5*
1	1	0	IRQ6*
1	1	1	IRQ7*

IREN: interrupt enable bit:

IREN = ’1’ - interrupt enabled
IREN = ’0’ - interrupt disabled
The interrupt enable bit is displayed via a yellow LED on the front panel. The LED lights, if the IREN bit is ’1’ (interrupt enabled).

x: ’not used’



1.6 The Digital Inputs and Outputs

1.6.1 Controller Assignment to Inputs and Outputs

The DPIO32 is equipped with 4 controller components. The two CIO Z8536 controllers handle the digital inputs and together offer two timers/counters with a maximum input frequency of 3 MHz each.

Two HD63143 supply the digital outputs. The operating modes 'digital output' or 'pulse width modulated output' are possible.
The HD63143 can also process input signals via multiplexers. Moreover they make available a total of 16 counters with a maximum counter frequency of 100 kHz (duty cycle 1:1) each.
If the HD63143 controllers shall generate VMEbus interrupts, then their interrupt outputs are fed to the CIO Z8536 port A7. The interrupt handling on the VMEbus is processed via the CIO.

Fig. 1.6.1 displays the assignment of inputs and outputs on the VME-DPIO32. The designations 'IN...' and 'OUT...' in column P2 display the input and output numbers, **where inputs and outputs with the same number physically cover the same pin on the P2 connector.**

The multiplexers for input or output operation of HD63143 ports U0...U7 and for the interrupt output of HD63143 are driven by ports P40...P44. The following tables indicate the multiplexer functions, which are identical for both HD63143 controllers:

HD63143 port P40	HD63143 port U0...U3
0	input
1	output

HD63143 port P44	HD63143 port U4...U7
0	input
1	output

Table 1.6.1: Switching of Ports U0...U7 Data Direction (corresponds to channels 1...8, or 17...24)

HD63143 port P41	CIO Z8536 port A7
0	port A7 is used by HD63143 for VMEbus interrupt generation
1	reserved

Table 1.6.2: CIO Z8536 Input Port A7 Covering

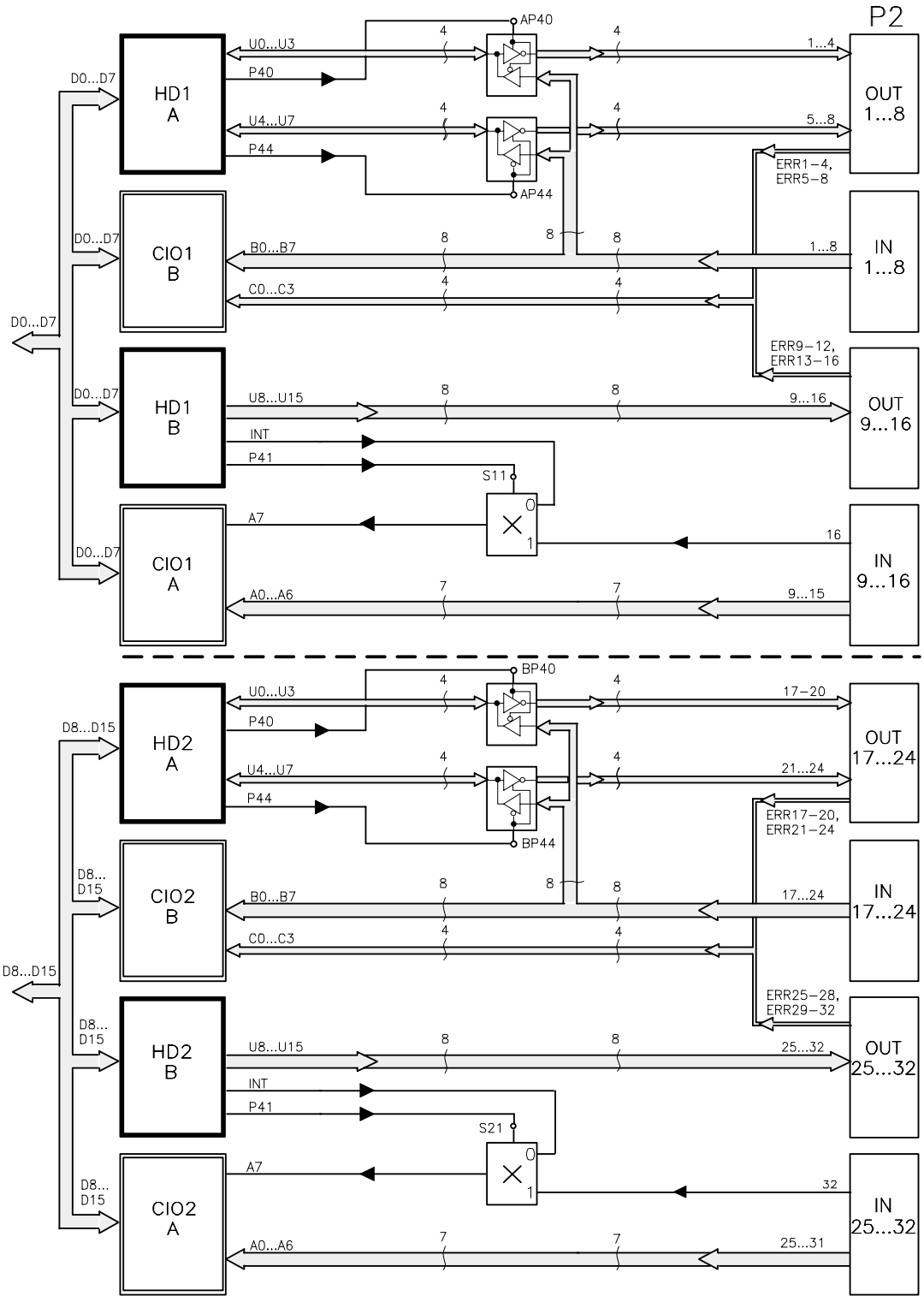
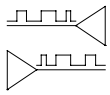


Fig. 1.6.1: Assignment of Inputs and Outputs to the Controllers



1.6.2 Pulse Processor HD63143 Structure

The HD63143 mainly consists of three functional units: The universal pulse processor, two serial interfaces and a RAM of 1024.

The serial interfaces are not used on the DPIO32. The HD63143 RAM is not available to the user in PCB version DPI32-5.

The internal pulse processor disposes of an own 16 bit wide ALU (Arithmetic Logik Unit). The principal pulse processor function can be illustrated by a scheme, which builds up on a process table:

The HD63143 continuously runs the instructions of a process table, where up to 16 process descriptions can be listed. Each of these process descriptions contains informations (parameters) on a desired function.

These parameters contain e.g. the registers to be used, the used pins and functions assigned to the pins.

The following figure displays this construction again as a survey. A complete listing of all possible parameters can be obtained from the software description.

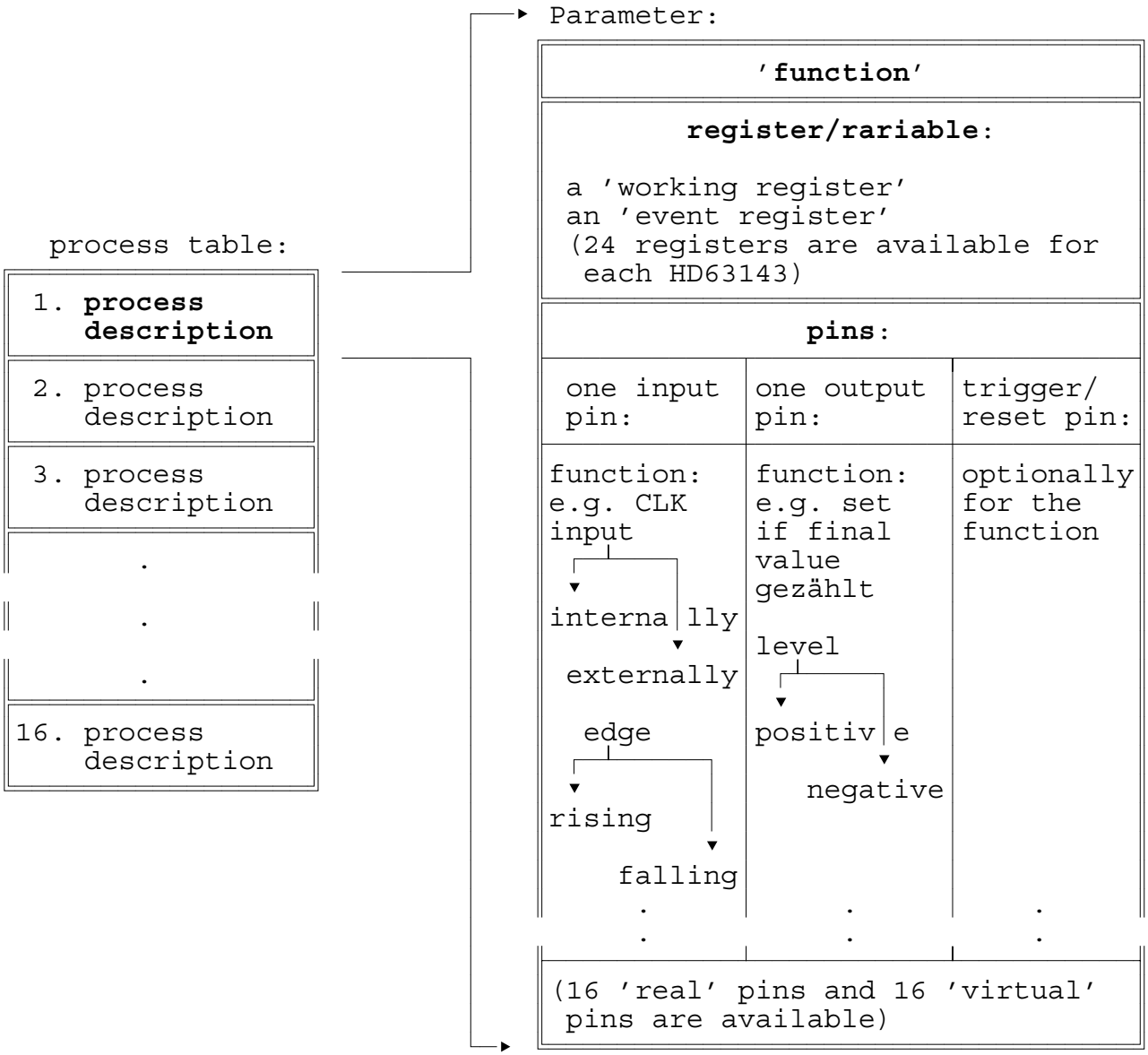
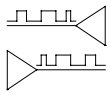


Fig. 1.6.2: Functional Construction of HD63143



1.6.3 Input and Output Circuit of DPIO32

1.6.3.1 General

The DPIO32 is designed for 32 input or output channels. Each of the 32 channels can be operated either as input or output.

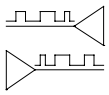
If a channel is operated as output, then the signal condition of the output can be read-back 'online' via the input circuit, which is connected in parallel.

The channels are configured in groups of four, because each 4 outputs are supplied by one driver component. If a channel group shall operate as input group, all outputs of this group must be set to '0'.

If at input operation of an I/O group no power supply is connected to the corresponding output driver, a part of the input current will flow into the output driver. In this case the input current consumption will increase. Thus it is recommended to connect a power supply to the output drivers of an I/O group as well when operating this group as inputs only.
The input voltage in this case may not exceed a maximum equal to U*vccout* - 2V because otherwise the output drivers might be destroyed!

As output driver a LMD18400 is used. The driver component can connect voltages of 6V to 28V (HIGH level) to GND.
The output driver supply voltage must be supplied externally. Each 4 of 32 channels are connected to one voltage supply. With this, 8 different output groups, optoisolated from each other, are possible.

Each of the 8 output drivers disposes of an error output, which will be triggered on occurence of an error at one or several channels. The error outputs are connected to the C ports of the two CIO Z8536.



error signal of the outputs	at CIO/Port
1...4	CIO1/PC0
5...8	CIO1/PC1
9...12	CIO1/PC2
13...16	CIO1/PC3
17...20	CIO2/PC0
21...24	CIO2/PC1
25...28	CIO2/PC2
29...32	CIO2/PC3

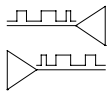
Table 1.6.3: Connection of the Error Signals to the CIO Ports

An error output will be triggered at the following operating troubles:

- no load
- short-circuit to VCC or GND
- overvoltage
- overtemperature of the driver component

Comment to error handling:
If the error conditions ’overtemperature’ or ’supply voltage too high’ occor, the LMD18400 switches off all 4 outputs. If the error condition is no longer valid and the inputs of the driver are still active, the LMD18400 switches automatically the outputs on again.

The error condition ’unloaded output’ will not be detected: The outputs are connected to the inputs and therefore the outputs are continously loaded with the small load of the input circuits.



1.6.3.2 Front Panel LEDs and Test Sockets

The channel status is displayed by two-colored LEDs on the front panel:

LED display	meaning of the front panel LEDs at the various operating modes	
	channel = input	channel = output
LED OFF	no input signal	output signal = ’0’ and no error
LED GREEN	input active (’1’)	output signal = ’1’ and no error, or all outputs of this group (of four) are set to ’0’ and feeding at the output
LED RED	-	error condition occurred

Table 1.6.4: Meaning of the Channel Status LEDs on the Front Panel

Via a test socket on the front panel for each channel the input or the error signal can be controlled.

test socket plug connector	affect to the channels at the various operating modes	
	channel = input	channel = output
not inserted	applied input level will be read	occurring errors will be evaluated
inserted	input level will always be read as ’1’	occurring errors will be ignored

Table 1.6.5: Meaning of the Channel Status Test Sockets on the Front Panel

1.6.3.3 Input and Output Circuit Diagram

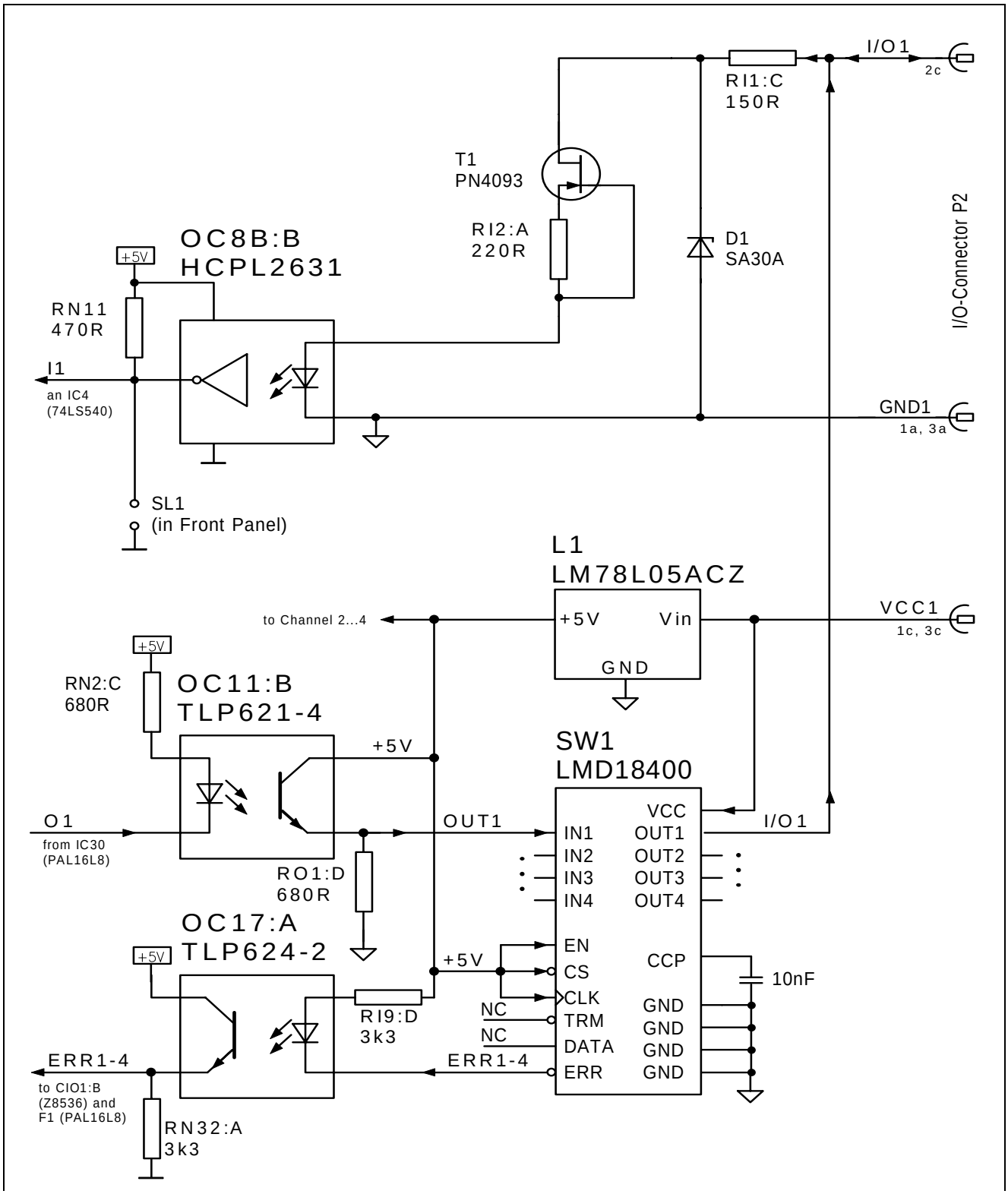
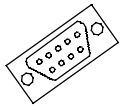


Fig. 1.6.3: Input and Output Circuit (example: channel 1)



2. Appendix

2.1 Connector Pin Assigments

2.1.1 VMEbus P1

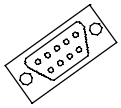
pin	row a	row b	row c
1	DATA 0	-	DATA 8
2	DATA 1	-	DATA 9
3	DATA 2	-	DATA 10
4	DATA 3	BG0 IN* ┐	DATA 11
5	DATA 4	BG0 OUT* ┘	DATA 12
6	DATA 5	BG1 IN* ┐	DATA 13
7	DATA 6	BG1 OUT* ┘	DATA 14
8	DATA 7	BG2 IN* ┐	DATA 15
9	GND	BG2 OUT* ┘	GND
10	-	BG3 IN* ┐	-
11	GND	BG3 OUT* ┘	-
12	DS1*	-	SYSRESET*
13	DS0*	-	LWORD*
14	WRITE*	-	AM5
15	GND	-	ADDR 23
16	DTACK*	AM0	ADDR 22
17	GND	AM1	ADDR 21
18	AS*	AM2	ADDR 20
19	GND	AM3	ADDR 19
20	IACK*	GND	ADDR 18
21	IACKIN*	-	ADDR 17
22	IACKOUT*	-	ADDR 16
23	AM4	GND	ADDR 15
24	ADDR 7	IRQ7*	ADDR 14
25	ADDR 6	IRQ6*	ADDR 13
26	ADDR 5	IRQ5*	ADDR 12
27	ADDR 4	IRQ4*	ADDR 11
28	ADDR 3	IRQ3*	ADDR 10
29	ADDR 2	IRQ2*	ADDR 9
30	ADDR 1	IRQ1*	ADDR 8
31	-	-	-
32	+ 5V	+ 5V	+ 5V

P1 connector according to DIN 41 612-C 96 / a+b+c

Signals with * : active low
Current rating : max 1.0 A per pin

-....pin is not connected on the PCB

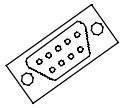
┐┘....signals are connected on the PCB



2.1.2 I/O Connector P2

pin	row a	row c
1	GND1	VCC1
2	I/O2	I/O1
3	GND1	VCC1
4	I/O4	I/O3
5	GND2	VCC2
6	I/O6	I/O5
7	GND2	VCC2
8	I/O8	I/O7
9	GND3	VCC3
10	I/O10	I/O9
11	GND3	VCC3
12	I/O12	I/O11
13	GND4	VCC4
14	I/O14	I/O13
15	GND4	VCC4
16	I/O16	I/O15
17	GND5	VCC5
18	I/O18	I/O17
19	GND5	VCC5
20	I/O20	I/O19
21	GND6	VCC6
22	I/O22	I/O21
23	GND6	VCC6
24	I/O24	I/O23
25	GND7	VCC7
26	I/O26	I/O25
27	GND7	VCC7
28	I/O28	I/O27
29	GND8	VCC8
30	I/O30	I/O29
31	GND8	VCC8
32	I/O32	I/O31

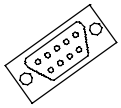
P1 connector according to DIN 41 612-C 96 / a+c



2.1.3 Terminal Block I/O Connector P2 Phönix FLKM64 or FLKMS64

pin	signal	pin	signal
2	GND1	1	VCC1
4	I/O2	3	I/O1
6	GND1	5	VCC1
8	I/O4	7	I/O3
10	GND2	9	VCC2
12	I/O6	11	I/O5
14	GND2	13	VCC2
16	I/O8	15	I/O7
18	GND3	17	VCC3
20	I/O10	19	I/O9
22	GND3	21	VCC3
24	I/O12	23	I/O11
26	GND4	25	VCC4
28	I/O14	27	I/O13
30	GND4	29	VCC4
32	I/O16	31	I/O15
34	GND5	33	VCC5
36	I/O18	35	I/O17
38	GND5	37	VCC5
40	I/O20	39	I/O19
42	GND6	41	VCC6
44	I/O22	43	I/O21
46	GND6	45	VCC6
48	I/O24	47	I/O23
50	GND7	49	VCC7
52	I/O26	51	I/O25
54	GND7	53	VCC7
56	I/O28	55	I/O27
58	GND8	57	VCC8
60	I/O30	59	I/O29
62	GND8	61	VCC8
64	I/O32	63	I/O31

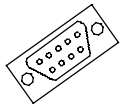
Signal description see 2.1.4.



2.1.4 Description of the Signals at the I/O Connector P2 (or Terminal Block)

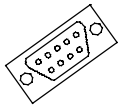
GNDx, VCCx.....power supply (U*vcc*) for the digital I/O circuits to be fed externally. Each 4 channels are locally connected to the same power supply (x = 1, 2,...,8)

I/Ox.....I/O channels of VME-DPIO32. (x = 1, 2, ..., 32)



2.1.5 Wiring Diagrams

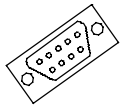
System						
VME-DPIO32 No. ☐ 5(6)V ☐ 12V ☐ 24V Page 1 32 input or output channels channel 1-8						
- Digital Input/Output			WAGO/ PHÖNIX	I N T E R N A L		
designation	chan.	Pol	terminal	P2 pin a	P2 pin c	signal
external supply required (only if channel 1 ... 4 are outputs)	-	+ ⊥	1 2	1	1	VCC GND
	1	+ ⊥	3 2	1	2	I/O1 GND
	2	+ ⊥	4 2	2 1		GND
external supply required (only if channel 1 ... 4 are outputs)	-	+ ⊥	5 6	3	3	VCC GND
	3	+ ⊥	7 6	3	4	I/O3 GND
	4	+ ⊥	8 6	4 3		I/O4 GND
external supply required (only if channel 5 ... 8 are outputs)	-	+ ⊥	9 10	5	5	VCC GND
	5	+ ⊥	11 10	5	6	I/O5 GND
	6	+ ⊥	12 10	6 5		I/O6 GND
external supply required (only if channel 5 ... 8 are outputs)	-	+ ⊥	13 14	7	7	VCC GND
	7	+ ⊥	15 14	7	8	I/O7 GND
	8	+ ⊥	16 14	8 7		I/O8 GND



System

VME-DPIO32 No. ☐ 5(6)V ☐ 12V ☐ 24V
Page 2 32 input or output channels channel 9-16

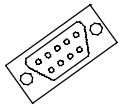
- Digital Input/Output			WAGO/ PHÖNIX	I N T E R N A L		
designation	chan.	Pol	terminal	P2 pin a	P2 pin c	signal
external supply required (only if channel 9 ... 12 are outputs)	-	+ ⊥	17 18	9	9	VCC GND
	9	+ ⊥	19 18	9	10	I/O9 GND
	10	+ ⊥	20 18	10 9		I/O10 GND
external supply required (only if channel 9 ... 12 are outputs)	-	+ ⊥	21 22	11	11	VCC GND
	11	+ ⊥	23 22	11	12	I/O11 GND
	12	+ ⊥	24 22	12 11		I/O12 GND
external supply required (only if channel 13 ... 16 are outputs)	-	+ ⊥	25 26	13	13	VCC GND
	13	+ ⊥	27 26	13	14	I/O13 GND
	14	+ ⊥	28 26	14 13		I/O14 GND
external supply required (only if channel 13 ... 16 are outputs)	-	+ ⊥	29 30	15	15	VCC GND
	15	+ ⊥	31 30	15	16	I/O15 GND
	16	+ ⊥	32 30	16 15		I/O16 GND



System

VME-DPIO32 No. ☐ 5(6)V ☐ 12V ☐ 24V
Page 3 32 input or output channels channel 17-24

- Digital Input/Output			WAGO/ PHÖNIX	I N T E R N A L		
designation	chan.	Pol	terminal	P2 pin a	P2 pin c	signal
external supply required (only if channel 17 ... 20 are outputs)	-	+ ⊥	33 34	17	17	VCC GND
	17	+ ⊥	35 34	17	18	I/O17 GND
	18	+ ⊥	36 34	18 17		I/O18 GND
external supply required (only if channel 17 ... 20 are outputs)	-	+ ⊥	37 38	19	19	VCC GND
	19	+ ⊥	39 38	19	20	I/O19 GND
	20	+ ⊥	40 38	20 19		I/O20 GND
external supply required (only if channel 21 ... 24 are outputs)	-	+ ⊥	41 42	21	21	VCC GND
	21	+ ⊥	43 42	21	22	I/O21 GND
	22	+ ⊥	44 42	22 21		I/O22 GND
external supply required (only if channel 21 ... 24 are outputs)	-	+ ⊥	45 46	23	23	VCC GND
	23	+ ⊥	47 46	23	24	I/O23 GND
	24	+ ⊥	48 46	24 23		I/O24 GND

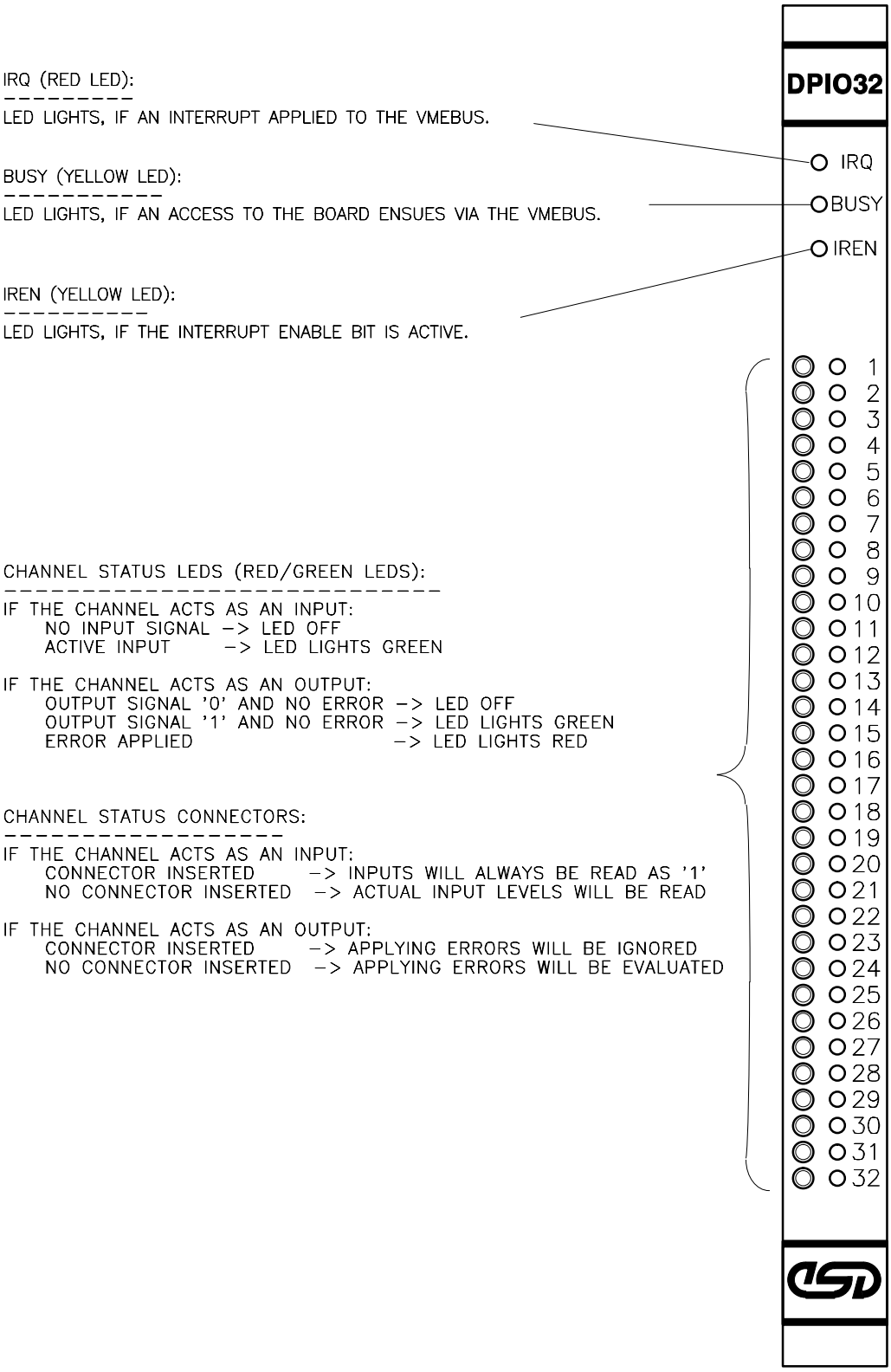


System

VME-DPIO32 No. ☐ 5(6)V ☐ 12V ☐ 24V
Page 4 32 input or output channels channel 25-32

- Digital Input/Output			WAGO/ PHÖNIX	I N T E R N A L		
designation	chan.	Pol	terminal	P2 pin a	P2 pin c	signal
external supply required (only if channel 25 ... 28 are outputs)	-	+ ⊥	49 50	25	25	VCC GND
	25	+ ⊥	51 50	25	26	I/O25 GND
	26	+ ⊥	52 50	26 25		I/O26 GND
external supply required (only if channel 25 ... 28 are outputs)	-	+ ⊥	53 54	27	27	VCC GND
	27	+ ⊥	55 54	27	28	I/O27 GND
	28	+ ⊥	56 54	28 27		I/O28 GND
external supply required (only if channel 29 ... 32 are outputs)	-	+ ⊥	57 58	29	29	VCC GND
	29	+ ⊥	59 58	29	30	I/O29 GND
	30	+ ⊥	60 58	30 29		I/O30 GND
external supply required (only if channel 29 ... 32 are outputs)	-	+ ⊥	61 62	31	31	VCC GND
	31	+ ⊥	63 62	31	32	I/O31 GND
	32	+ ⊥	64 62	32 31		I/O32 GND

2.2 Front Panel



IRQ (RED LED):

LED LIGHTS, IF AN INTERRUPT APPLIED TO THE VMEBUS.

BUSY (YELLOW LED):

LED LIGHTS, IF AN ACCESS TO THE BOARD ENSUES VIA THE VMEBUS.

IREN (YELLOW LED):

LED LIGHTS, IF THE INTERRUPT ENABLE BIT IS ACTIVE.

CHANNEL STATUS LEDS (RED/GREEN LEDS):

IF THE CHANNEL ACTS AS AN INPUT:
NO INPUT SIGNAL -> LED OFF
ACTIVE INPUT -> LED LIGHTS GREEN

IF THE CHANNEL ACTS AS AN OUTPUT:
OUTPUT SIGNAL '0' AND NO ERROR -> LED OFF
OUTPUT SIGNAL '1' AND NO ERROR -> LED LIGHTS GREEN
ERROR APPLIED -> LED LIGHTS RED

CHANNEL STATUS CONNECTORS:

IF THE CHANNEL ACTS AS AN INPUT:
CONNECTOR INSERTED -> INPUTS WILL ALWAYS BE READ AS '1'
NO CONNECTOR INSERTED -> ACTUAL INPUT LEVELS WILL BE READ

IF THE CHANNEL ACTS AS AN OUTPUT:
CONNECTOR INSERTED -> APPLYING ERRORS WILL BE IGNORED
NO CONNECTOR INSERTED -> APPLYING ERRORS WILL BE EVALUATED

2.3 Circuit Diagrams

2.4 Data Sheets

LMD18400

CIO Z8536

HD63143