PM7380

FREEDM™-32P672

DEVELOPMENT KIT

USER MANUAL

RELEASED

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1 OVERVIEW

The FREEDM™-32P672 Development Kit consists of an add-on PCI card that can be used to test the functionality of the FREEDM™-32P672 chip. The PCI card consists of all the necessary components used for testing the various functions of the FREEDM™-32P672 device.

This document provides the necessary information for configuring the FREEDM™-32P672 Development Kit Board Rev 2.0. jumper settings.

1.1 Features

- The Development Kit supports a 33/66 MHz, 32 bit Peripheral Component Interconnect (PCI) 2.1 compliant bus for configuration, monitoring and transfer of packet data.
- The Development Kit supports both unchannelized H-MVIP as well as non-H-MVIP traffic. Channelized T1/E1 traffic on the 32 links is not directly supported since there is no provision for gapping of the link clocks. Channelized H-MVIP mode is not directly supported since the frame pulses are not generated on the Development Kit card.
- Channelized T1/E1 operation can be supported only with an external gapped clock (i.e. gapped clock from an external source). Channelized H-MVIP mode can be supported with external frame pulses and frame pulse clocks.

2 HARDWARE CONFIGURATION

Jumper settings are used to configure the Development Kit board for various modes of operation. The supported modes include:

- Unchannelized T1 mode
- Unchannelized E1 mode
- Unchannelized 52 MHz mode
- Unchannelized 2.048 Mbit/s H-MVIP mode
- Mixed mode

For non-H-MVIP modes, only the following configurations can be achieved using jumper settings:

- 32 T1 links
- 32 E1 links
- 16 T1 links and 16 E1 links
- 3 DS-3/unchannelized 52 Mbit/s links
- Mixed mode – 1 DS-3 link and T1/E1 links

With external gapped clock/frame pulse signals, channelized non H-MVIP as well as H-MVIP mode can be supported. This includes channelized 8 Mbit/s H-MVIP mode, for which an external frame pulse as well as frame pulse clocks are required. Note that the supplied software does not include support for includes channelized 8 Mbit/s H-MVIP mode. This section gives a detailed description of the jumper settings on the various headers.

Figure 1 represents the block diagram for the FREEDM™-32P672 development kit board.

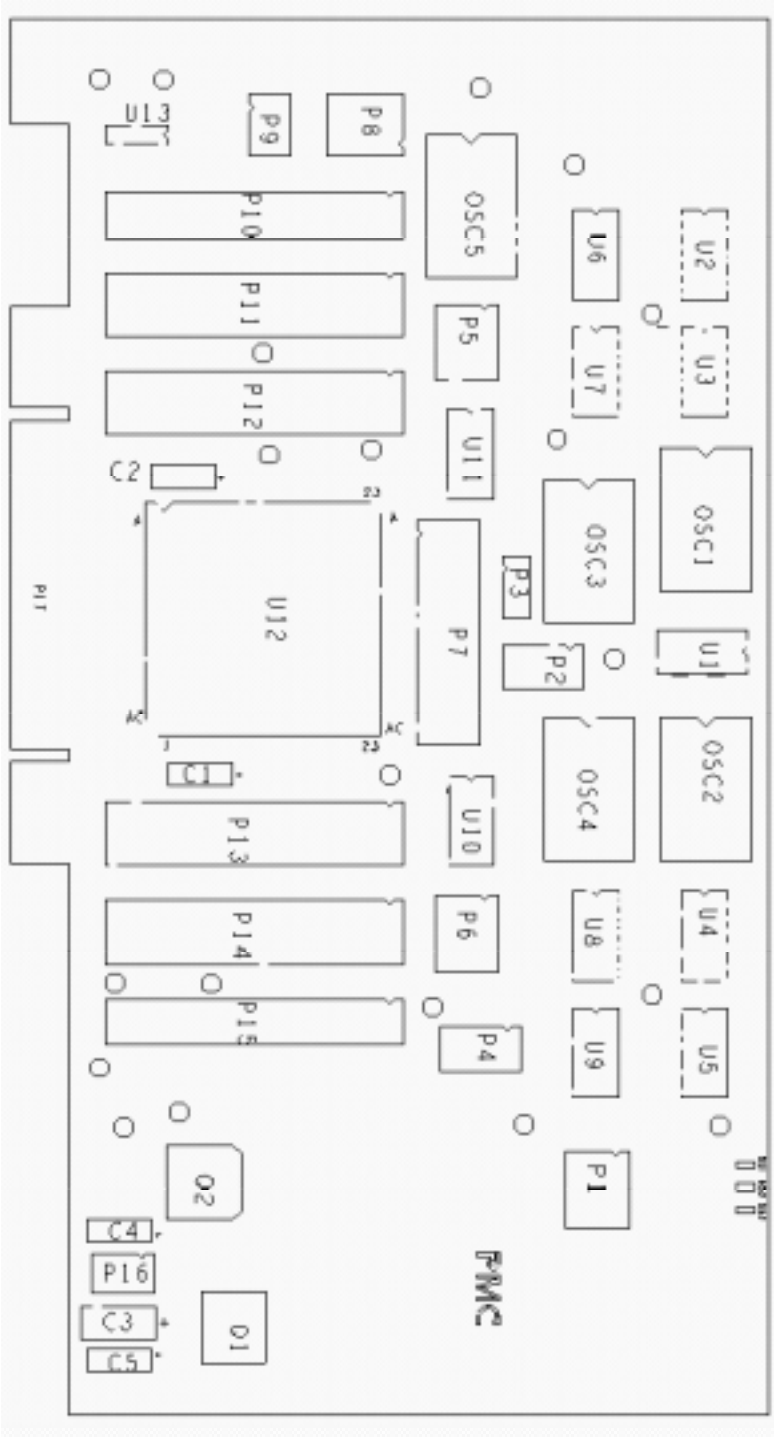


Figure 1 FREEDM™-32P672 Development Kit Board Diagram

2.1 Voltage Selection

The FREEDM™-32P672 requires a 3.3 V source. The user has the option of using either the 3.3 V provided by the PCI connector or a board regulated 3.3 V source. The jumper settings for achieving these configurations are shown in Figure 2.

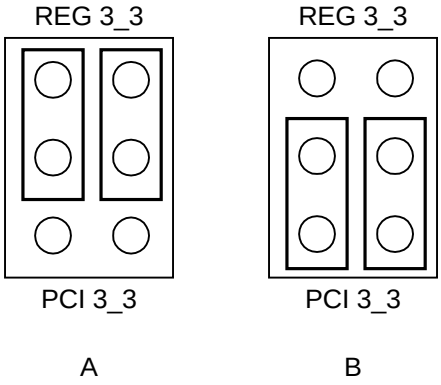


Figure 2 3.3V Selection Header (P16).

There are three LED's near the upper right corner on the topside of the Development Kit board. Plugging the Development Kit board into the PCI slot causes the green LED (indicating 5 V) to light upon power up. The two other LED's will light only if the 3.3 V source is selected. Figure 3 shows the location of these LED's on the board.

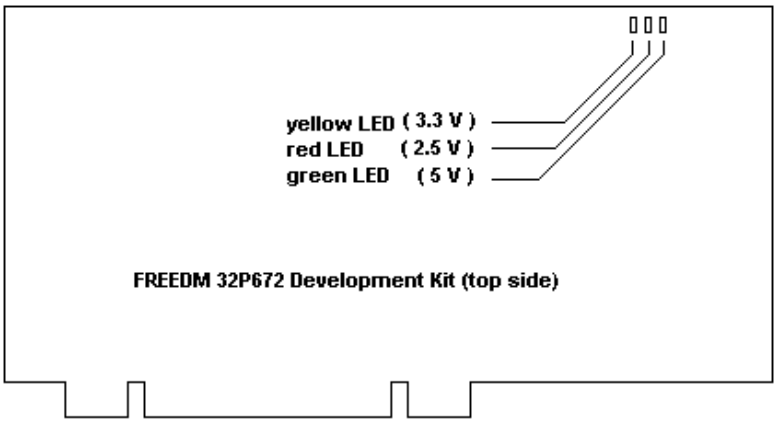


Figure 3 LED's on the FREEDM™-32P672 Development Kit

2.2 SYSCLK Jumper Setting

The SYSCLK input of the FREEDM™-32P672 chip can be provided with either a 40 MHz clock from an oscillator, or the PCICLKO clock output of the FREEDM™-32P672 chip (provided that a 33 MHz PCI bus is in use). The jumper settings on header P3 to achieve these configurations are shown in Figure 4. The jumper settings are also listed in Table 1.

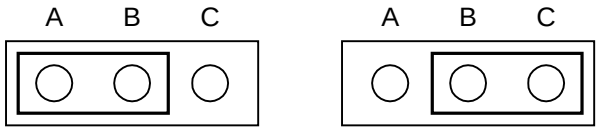


Figure 4 Jumper setting for SYSCLK (P3)

Table 1 Jumper setting for SYSCLK

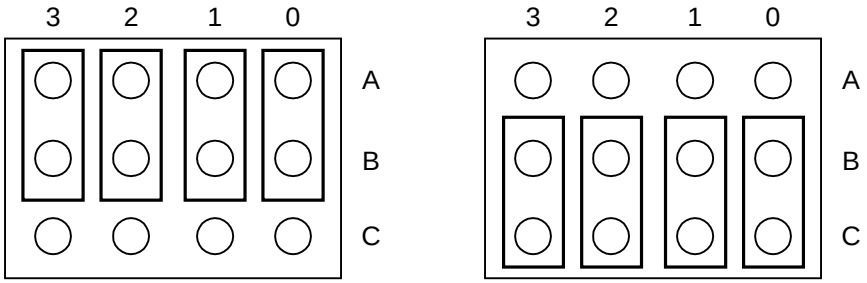
HEADER	JUMPER SETTING	CONFIGURATION
P3	Shorting jumper over pins A and B	SYSCLK from oscillator
P3	Shorting jumper over pins B and C	SYSCLK from PCICLKO

Note: Pins B and C should only be shorted when the card is installed in a system with a 33 MHz PCI bus.

2.3 Jumper setting for RMVCK[3:0] provision

Each of the four RMVCK inputs to the FREEDM™-32P672 chip can be configured independently. Each RMVCK input to the FREEDM™-32P672 chip can either be grounded or provided with a 4.096 MHz clock from an oscillator. The jumper settings on header P5 to achieve these configurations are as shown in Figure 5. The jumper settings are also listed in Table 2.

In non-H-MVIP or 8.192 Mbit/s H-MVIP mode, RMVCK[3:0] should be grounded. To ground RMVCK[n] ($0 \leq n \leq 3$), pin B-n should be shorted to pin C-n on header P5. 4.096 MHz clock from an oscillator can be provided to RMVCK[n] by shorting pins B-n and A-n. The jumper settings in Figure 5 (a) correspond to 4.096 MHz on RMVCK[3:0], whereas the jumper settings in Figure 5(b) correspond to grounded RMVCK[3:0].



Note : Numbers written above the header represent the link groups.

Figure 5 Jumper settings for RMVCK[3:0] (P5).

Table 2 Jumper settings for RMVCK[3:0]

HEADER	JUMPER SETTINGS	CONFIGURATION
P5	Shorting jumper over pins A-n and B-n ($0 \leq n \leq 3$)	4.096 MHz input to RMVCK[n]. ($0 \leq n \leq 3$) Unchannelized 2.048 Mbit/s H-MVIP mode .
P5	Shorting jumper over pins C-n and B-n ($0 \leq n \leq 3$)	RMVCK[n] grounded. ($0 \leq n \leq 3$) Non – 2.048 Mbit/s H-MVIP mode.

Note : Each of the RMVCK inputs can be configured independent of the other RMVCK inputs.

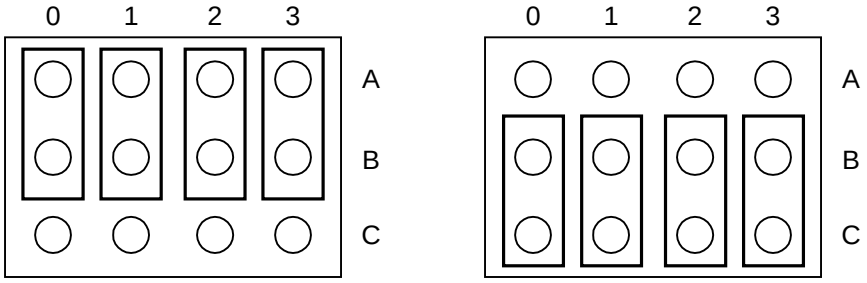
For channelized 2.048 Mbit/s H-MVIP mode, external RMVCK should be provided by means of a wire to board connector plugged into pins of rows B and C on header P5. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P5.

2.4 Jumper setting for TMVCK[3:0] provision

Similar to RMVCK, each of the four TMVCK inputs to the FREEDM™-32P672 device can be configured independently. Each TMVCK input to the FREEDM™-

32P672 device can either be grounded or provided with a 4.096 MHz clock from an oscillator. The jumper settings on header P6 to achieve these configurations are shown in Figure 6. The jumper settings are also listed in Table 3.

In non-H-MVIP or 8.192 Mbit/s H-MVIP mode, TMVCK[3:0] should be grounded. To ground TMVCK[n] ($0 \leq n \leq 3$), pin B-n should be shorted to pin C-n on header P6. The 4.096 MHz clock from an oscillator can be provided to TMVCK[n] by shorting pins B-n and A-n. The jumper settings in Figure 6(a) correspond to 4.096 MHz on TMVCK[3:0], whereas the jumper settings in Figure 6(b) correspond to grounded TMVCK[3:0].



Note : Numbers written above the header represent the link groups.

Figure 6 Jumper setting for TMVCK[3:0] (P6).

Table 3 Jumper setting for TMVCK[3:0]

HEADER	JUMPER SETTINGS	CONFIGURATION
P6	Shorting jumper over pins A-n and B-n ($0 \leq n \leq 3$)	4.096 MHz input to TMVCK[n]. ($0 \leq n \leq 3$) Unchannelized 2.048 Mbit/s H-MVIP mode .
P6	Shorting jumper over pins C-n and B-n ($0 \leq n \leq 3$)	TMVCK[n] grounded. ($0 \leq n \leq 3$) Non – 2.048 Mbit/s H-MVIP mode.

Note : Each of the TMVCK inputs can be configured independent of the other TMVCK inputs.

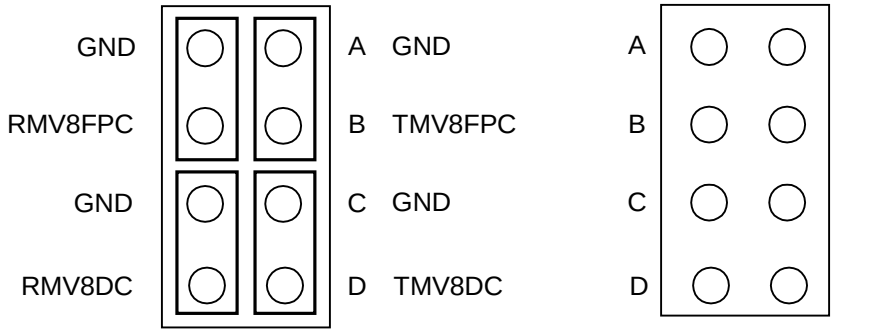
For channelized 2.048 Mbit/s H-MVIP mode, external TMVCK is provided by means of a wire to board connector plugged into pins of rows B and C on header P6. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P6.

2.5 Jumper settings for TMV8DC, RMV8DC, TMV8FPC and RMV8FPC provision

The RMV8DC input to the FREEDM™-32P672 chip can either be grounded or provided with a 16.384 MHz clock from an external source by means of a wire to board connector. Similarly, the TMV8DC input to the FREEDM™-32P672 chip can either be grounded or provided with a 16.384 MHz clock from an external source. The RMV8FPC and TMV8FPC pins of the chip can either be grounded or provided with frame pulse clock signals from an external source. The jumper settings on header P4 to achieve these configurations are shown in Figure 7. They are also listed in Table 4.

In non-H-MVIP or 2.048 Mbit/s H-MVIP mode, TMV8DC and RMV8DC should be grounded. To ground these inputs, pins in row D should be shorted to corresponding pins in row C on header P4. Also, RMV8FPC and TMV8FPC should be grounded by shorting pins in row B to the corresponding pins in row A.

For 8.192 Mbit/s H-MVIP mode, external TMV8DC, RMV8DC, TMV8FPC and RMV8FPC should be provided by means of a wire to board connector plugged into pins on header P4. The ground plugs on the wire to board connector should mate with the ground pins (rows A and C) on header P4. Note that this mode is not presently supported in software.



RMV8DC = GND
TMV8DC = GND
RMV8FPC = GND
TMV8FPC = GND

RMV8DC = EXTERNAL
TMV8DC = EXTERNAL
RMV8FPC = EXTERNAL
TMV8FPC = EXTERNAL

Figure 7 Jumper settings for enabling of RMV8FPC, TMV8FPC, TMV8DC, and RMV8DC (P4)

Table 4 Jumper settings for enabling of RMV8FPC, TMV8FPC, TMV8DC, and RMV8DC

HEADER	JUMPER SETTING	CONFIGURATION
P4	Pins in row A shorted to corresponding pins in row B Pins in row C shorted to corresponding pins in row D	TMV8DC and RMV8DC grounded. TMV8FPC and RMV8FPC grounded. Non-8.192 Mbit/s H-MVIP mode.
P4	Wire to board connector plugged into pins on header P4.	16.384 MHz clock provided to RMV8DC and TMV8DC. 4.096 MHz clock provided to RMV8FPC and TMV8FPC.

Note : The falling edges of RMV8FPC and TMV8FPC should be aligned respectively with the falling edges of RMV8DC and TMV8DC, with no more than 10 ns skew.

2.6 Jumper settings for TFP8B and RFP8B

TFP8B and RFP8B should be pulled down to ground when unchannelized 8.192 Mbit/s H-MVIP mode is not used. Both TFP8B and RFP8B should be pulled high for unchannelized 8.192 Mbit/s H-MVIP mode. The jumper settings on header P9 to achieve this configuration are shown in Figure 8. They are also listed in Table 5.

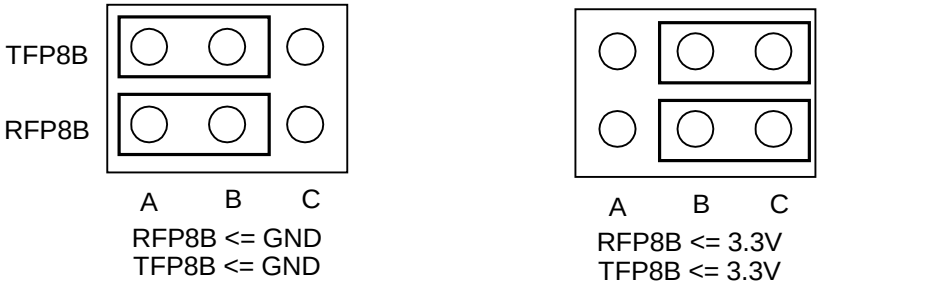


Figure 8 Jumper settings for RFP8B and TFP8B (P9)

Table 5 Jumper settings for RFP8B and TFP8B

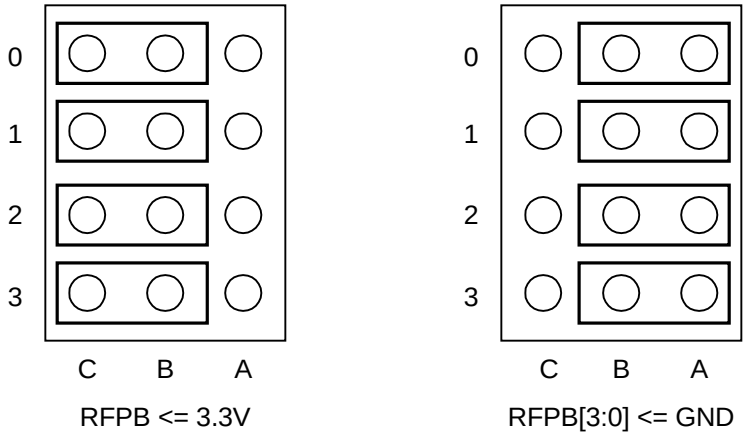
HEADER	JUMPER SETTING	CONFIGURATION
P9	Pins in column C shorted to	TFP8B and RFP8B pulled high

	corresponding pins in column B	(3.3 V).
P9	Pins in column A shorted to corresponding pins in column B	TFP8B and RFP8B grounded. Non - 8.192 Mbit/s H-MVIP mode.

For 8.192 Mbit/s H-MVIP mode, external TFP8B and RFP8B have to be provided by means of a wire to board connector plugged into pins of columns A and B on header P9. The ground plugs on the wire to board connector should mate with the ground pins (column A) on header P9.

2.7 Jumper settings for RFPB[3:0]

RFPB[3:0] should be pulled down to ground when unchannelized 2.048 Mbit/s H-MVIP mode is not used. If the links in one or more link groups are used for unchannelized 2.048 Mbit/s H-MVIP mode, RFPB inputs for these link groups should be pulled high. RFPB for each link group can be configured independently. The jumper settings on header P8 to achieve these configurations are listed in Figure 9. They are also listed in Table 6.



Note : RFPB for each link group can be independently configured with a single shorting jumper.

Figure 9 Jumper settings for RFPB[3:0] (P8)

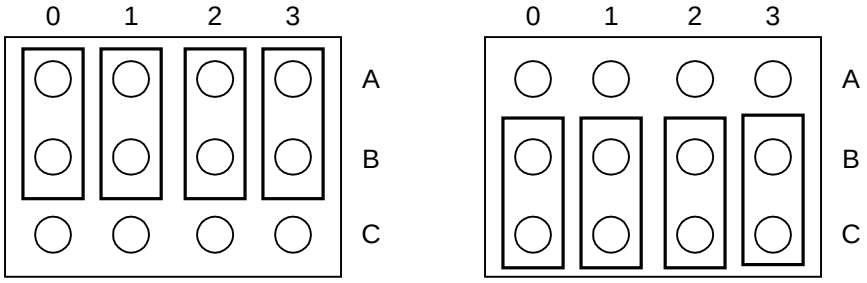
For channelized 2.048 Mbit/s H-MVIP mode, external RFPB[3:0] has to be provided by means of a wire to board connector plugged into pins of columns A and B on header P8. The ground plugs on the wire to board connector should mate with the ground pins (column A) on header P8.

Table 6 Jumper settings for RFPB[3:0]

HEADER	JUMPER SETTINGS	CONFIGURATION
P8	Pin A-n shorted to pin B-n ($0 \le n \le 3$)	RFPB[n] grounded. ($0 \le n \le 3$) Non- 2.048 Mbit/s H-MVIP mode.
P8	Pin C-n shorted to pin B-n ($0 \le n \le 3$)	RFPB[n] pulled high (3.3 V). ($0 \le n \le 3$) Unchannelized 2.048 Mbit/s H-MVIP mode on link group n.

2.8 Jumper settings for TFPB[3:0]

TFPB[3:0] should be pulled down to ground when unchannelized 2.048 Mbit/s H-MVIP mode is not used. If the links in one or more link groups are used for unchannelized 2.048 Mbit/s H-MVIP mode, the TFPB inputs for these link groups should be pulled high. TFPB for each link group can be configured independently. The jumper settings on header P1 to achieve these configurations are listed in Figure 10. They are also listed in Table 7.



Note : TFPB for each link group can be independently configured with a single shorting jumper.

Figure 10 Jumper settings for TFPB[3:0] (P1)

Table 7 Jumper settings for TFPB[3:0]

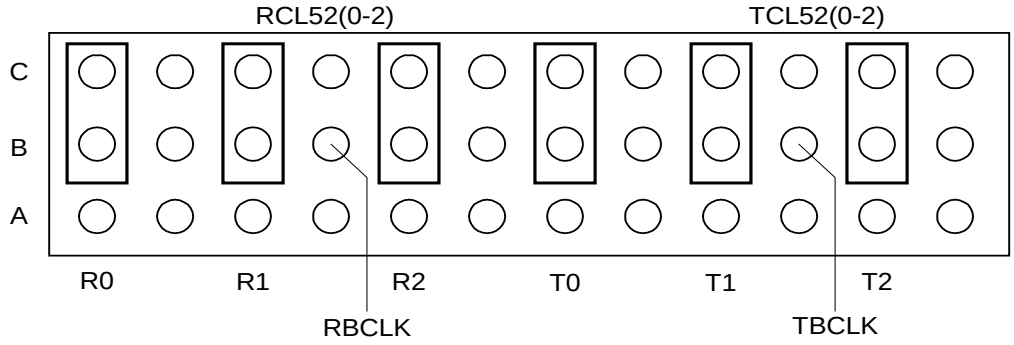
HEADER	JUMPER SETTINGS	CONFIGURATION
P1	Pin A-n shorted to pin B-n ($0 \le n \le 3$)	TFPB[n] grounded . ($0 \le n \le 3$) Non- 2.048 Mbit/s H-MVIP mode.
P1	Pin C-n shorted to	TFPB[n] pulled high (3.3 V).

HEADER	JUMPER SETTINGS	CONFIGURATION
	pin B-n (0 ≤ n ≤ 3)	(0 ≤ n ≤ 3) Unchannelized 2.048 Mbit/s H-MVIP mode on link group n.

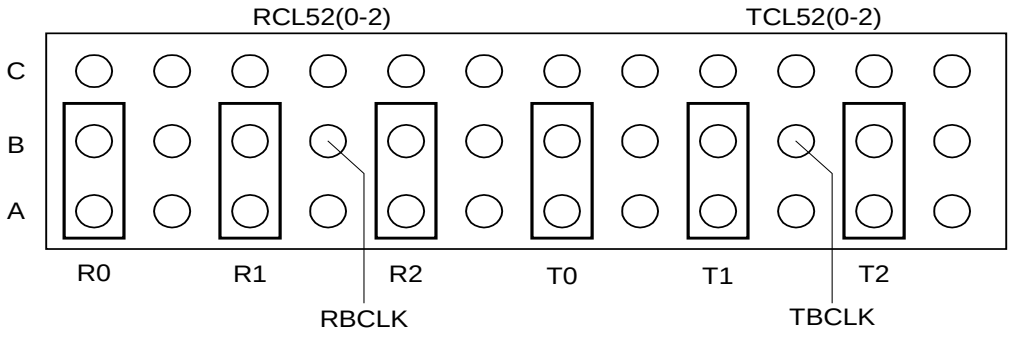
For channelized 2.048 Mbit/s H-MVIP mode, external TFPB[3:0] has to be provided by means of a wire to board connector plugged into pins of rows A and B on header P1. The ground plugs on the wire to board connector should mate with the ground pins (row A) on header P1.

2.9 Jumper settings for selection of RCLK[2:0] and TCLK[2:0]

In non-H-MVIP mode, RCLK[2:0] and TCLK[2:0] can be set to either T1/E1 clock frequency or DS-3/52 MHz clock frequency. Jumper settings on header P7 to make this selection are listed in Table 8. Figure 11 shows how the jumpers are used on header P7.



A) T1/E1 Frequency on RCLK[2:0] and TCLK[2:0]



B) DS-3/52 MHz Frequency on RCLK[2:0] and TCLK[2:0]

Figure 11 Jumper settings for selection of RCLK[2:0] and TCLK[2:0] (P7)

Note : The numbers T0, T1 and T2, corresponding to TCL52 (0-2) and R0, R1 and R2, corresponding to RCL52 (0-2), shown in Figure 11, respectively represent transmit and receive links 0, 1 and 2.

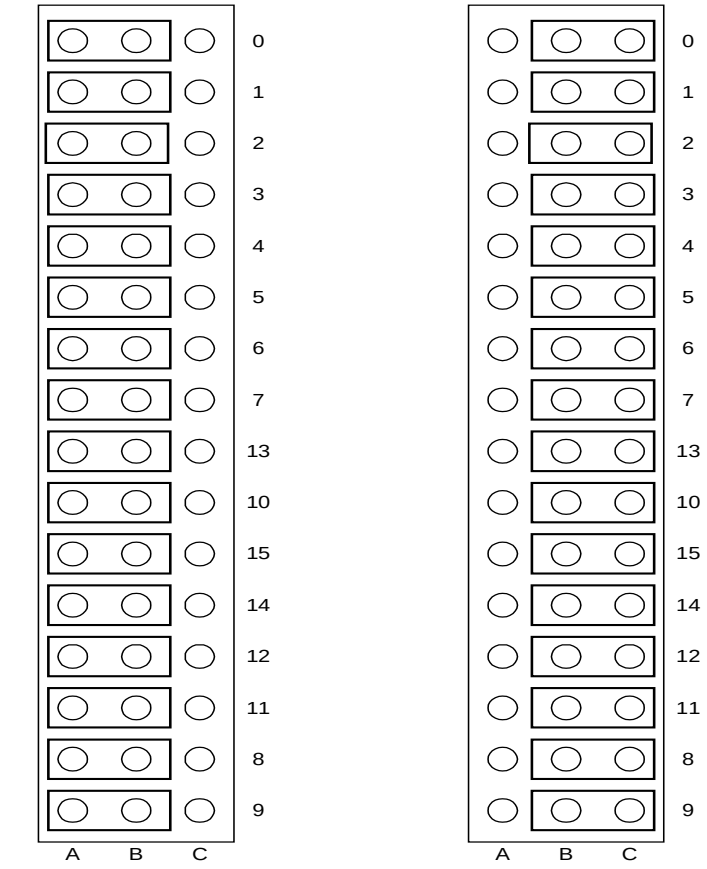
Table 8 Jumper settings for selection of RCLK[2:0] and TCLK[2:0]

HEADER	JUMPER SETTINGS	CONFIGURATION
P7	Pin A-Rn shorted to pin B-Rn ($0 \leq n \leq 2$) under RCL52 (0-2) label	DS-3/52 MHz frequency on RCLK[2:0]
P7	Pin C-Rn shorted to pin B-Rn ($0 \leq n \leq 2$) under RCL52 (0-2) label	T1/E1 frequency on RCLK[2:0]
P7	Pin A-Tn shorted to pin B-Tn ($0 \leq n \leq 2$) under TCL52 (0-2) label	DS-3/52 MHz frequency on TCLK[2:0]
P7	Pin C-Tn shorted to pin B-Tn ($0 \leq n \leq 2$) under TCL52 (0-2) label	T1/E1 frequency on TCLK[2:0]

Note : Each RCLK or TCLK selection can be configured independently.

2.10 Jumper settings for enabling of RCLK[15:0]

RCLK[15:0] should be grounded when unchannelized H-MVIP mode is used on links 0 through 15. If one or more links from 0 through 15 is used for receiving non-H-MVIP traffic, the corresponding receive link clocks (i.e. RCLK[n] where $0 \leq n \leq 15$) should be enabled. The jumper settings on header P12 for enabling RCLK[15:0] are listed in Table 9. Figure 12 shows the jumper settings for enabling all 16 receive link clocks from RCLK[15] through RCLK[0].



Note : The pins for links from 0 through 15 are not in sequential order. Each of the RCLK inputs to FREEDM™-32P672 chip can be independently enabled.

Figure 12 Jumper settings for enabling of RCLK[15:0] (P12)

Table 9 Jumper settings for enabling of RCLK[15:0]

HEADER	JUMPER SETTING	CONFIGURATION
P12	Pin A-n shorted to pin B-n ($0 \le n \le 15$)	RCLK[n] connected to FREEDM™-32P672 ($0 \le n \le 15$)
P12	Pin C-n shorted to pin B-n ($0 \le n \le 15$)	RCLK[n] grounded ($0 \le n \le 15$)

For channelized non-H-MVIP mode, externally gapped RCLK[15:0] should be provided by means of a wire to board connector plugged into pins of rows B and C on header P12. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P12.

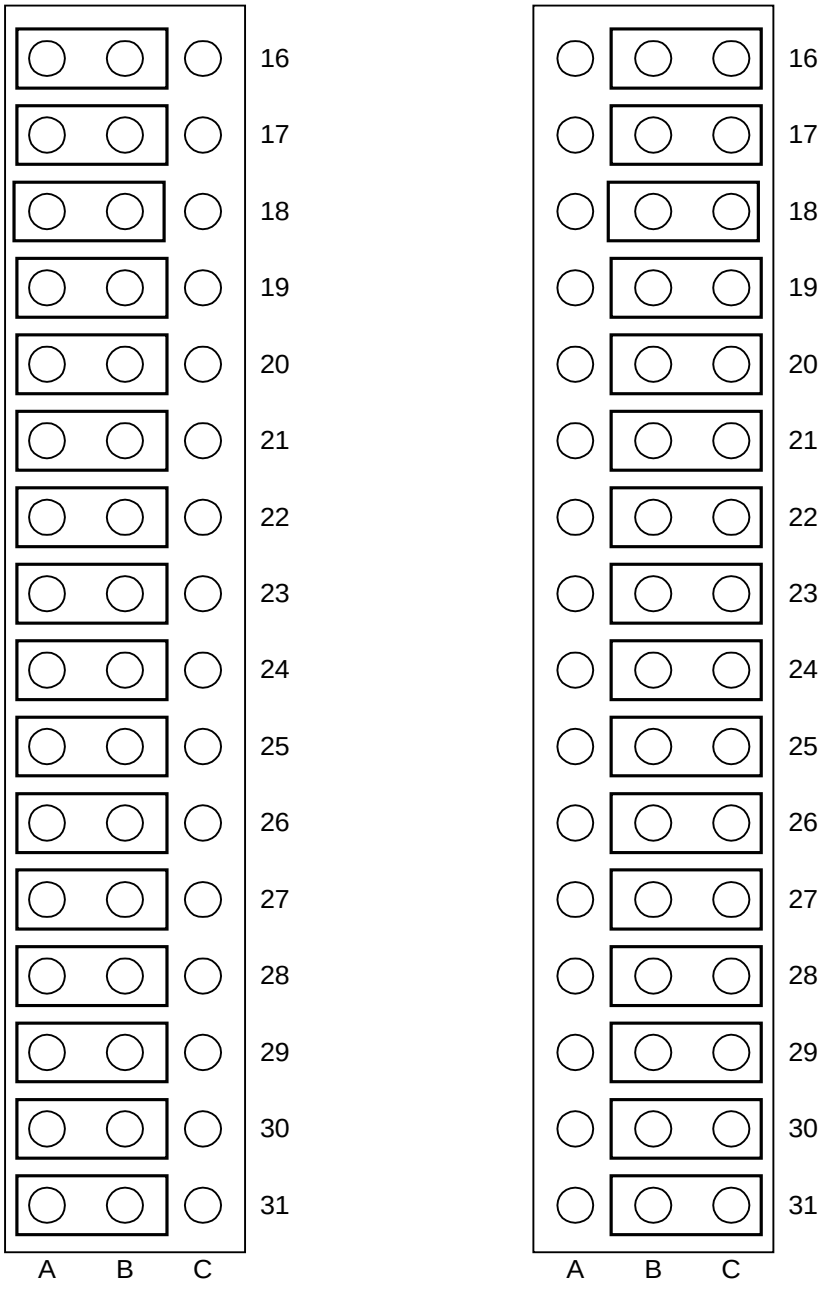
2.11 Jumper settings for enabling of RCLK[31:16]

RCLK[31:16] should be grounded when unchannelized H-MVIP mode is used on links 16 through 31. If one or more links from 16 through 31 are used for receiving non-H-MVIP traffic, the corresponding receive link clocks (i.e. RCLK[n] where $16 \leq n \leq 31$) should be enabled. The jumper settings on header P11 for enabling RCLK[31:16] are listed in Table 10. Figure 13 shows the jumper settings for enabling all 16 receive link clocks from RCLK[31] through RCLK[16].

Table 10 Jumper settings for enabling of RCLK[31:16]

HEADER	JUMPER SETTING	CONFIGURATION
P11	Pin A-n shorted to pin B-n ($16 \leq n \leq 31$)	RCLK[n] connected to FREEDM™-32P672 ($16 \leq n \leq 31$)
P11	Pin C-n shorted to pin B-n ($16 \leq n \leq 31$)	RCLK[n] grounded ($16 \leq n \leq 31$)

For channelized non-H-MVIP mode, externally gapped RCLK[31:16] should be provided by means of a wire to board connector plugged into pins of rows B and C on header P11. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P11.



RCLK[31:16] <= T1/E1

Non H-MVIP Mode

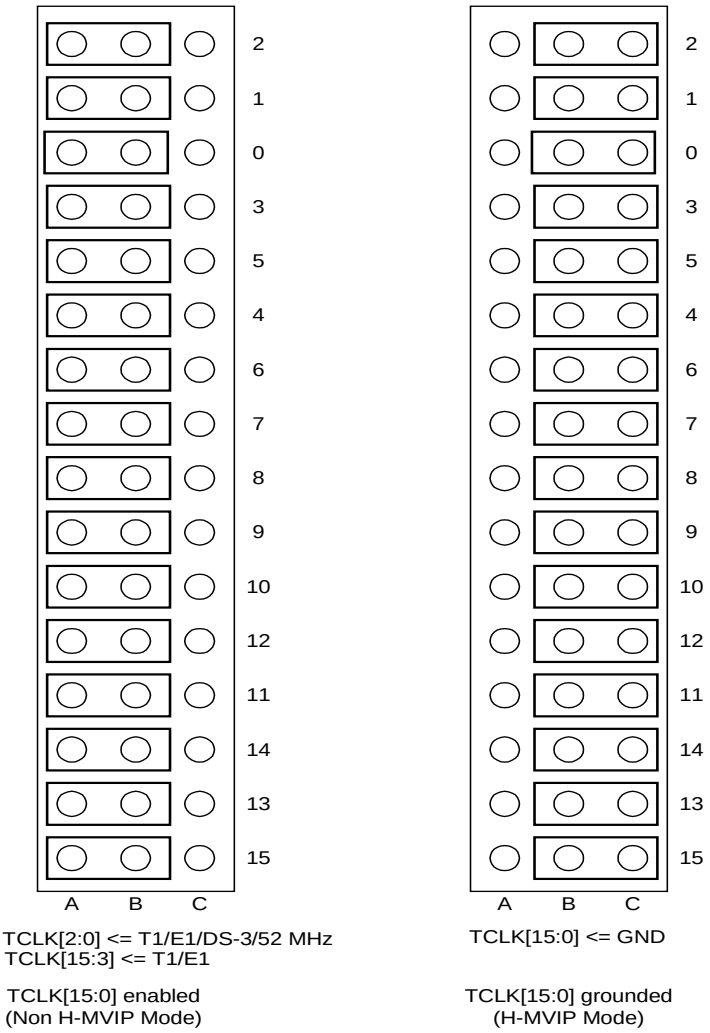
RCLK[31:16] grounded
(H-MVIP Mode)

Note : Each of the RCLK inputs to FREEDM™-32P672 chip can be independently enabled.

Figure 13 Jumper settings for enabling of RCLK[31:16] (P11)

2.12 Jumper settings for enabling of TCLK[15:0]

TCLK[15:0] should be grounded when unchannelized H-MVIP mode is used on links 0 through 15. If one or more links from 0 through 15 is used for transmitting non-H-MVIP traffic, the corresponding transmit link clocks (i.e. TCLK[n] where $0 \leq n \leq 15$) should be enabled. The jumper settings on header P13 for enabling TCLK[15:0] are listed in Table 11. Figure 14 shows the jumper settings for enabling all 16 transmit link clocks from TCLK[15] through TCLK[0].



Note : The pins for links 0 through 15 are not in sequential order. Each of the TCLK inputs to FREEDM™-32P672 chip can be independently enabled.

Figure 14 Jumper settings for enabling of TCLK[15:0] (P13)

Table 11 Jumper settings for TCLK[15:0]

HEADER	JUMPER SETTING	CONFIGURATION
P13	Pin A-n shorted to pin B-n ($0 \leq n \leq 15$)	TCLK[n] connected to FREEDM™-32P672 ($0 \leq n \leq 15$)
P13	Pin C-n shorted to pin B-n ($0 \leq n \leq 15$)	TCLK[n] grounded ($0 \leq n \leq 15$)

For channelized non-H-MVIP mode, externally gapped TCLK[15:0] should be provided by means of a wire to board connector plugged into pins of rows B and C on header P13. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P13.

2.13 Jumper settings for enabling of TCLK[31:16]

TCLK[31:16] should be grounded when unchannelized H-MVIP mode is used on links 16 through 31. If one or more links from 16 through 31 are used for transmitting non-H-MVIP traffic, the corresponding transmit link clocks (i.e. TCLK[n] where $16 \leq n \leq 31$) should be enabled. The jumper settings on header P14 for enabling TCLK[31:16] are listed in Table 12. Figure 15 shows the jumper settings for enabling all 16 transmit link clocks from TCLK[31] through TCLK[16].

For channelized non-H-MVIP mode, externally gapped TCLK[31:16] should be provided by means of a wire to board connector plugged into pins of rows B and C on header P14. The ground plugs on the wire to board connector should mate with the ground pins (row C) on header P14.

Table 12 Jumper settings for enabling TCLK[31:16]

HEADER	JUMPER SETTING	CONFIGURATION
P14	Pin A-n shorted to pin B-n ($16 \leq n \leq 31$)	TCLK[n] connected to FREEDM™-32P672 ($16 \leq n \leq 31$)
P14	Pin C-n shorted to pin B-n ($16 \leq n \leq 31$)	TCLK[n] grounded ($16 \leq n \leq 31$)

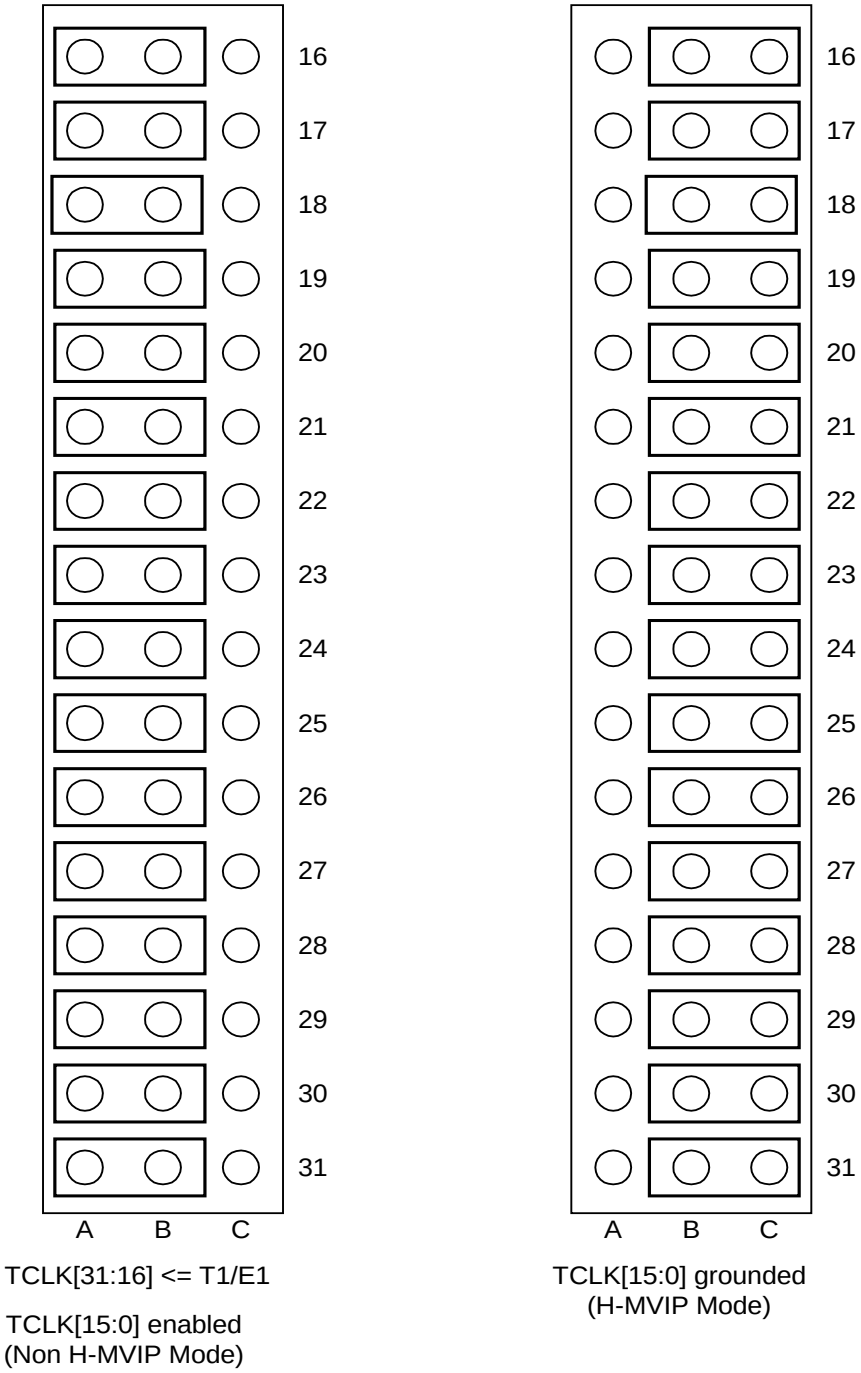


Figure 15 Jumper settings for TCLK[31:16] (P14)

2.14 Jumper settings for Data loopback on links 2 through 31

Data loopback can be performed on a per link basis on links 2 through 31. The jumper settings for loopback on these links, are listed in Table 13. Figure 16 shows the jumper settings for loopback on all the links from 2 to 31.

Table 13 Jumper settings for data loopback on links 2 through 31

HEADER	JUMPER SETTING	CONFIGURATION
P10	Pins in row ‘n’ shorted with each other (where $16 \leq n \leq 31$)	Loopback on link ‘n’ (where $16 \leq n \leq 31$)
P15	Pins in row ‘n’ shorted with each other (where $2 \leq n \leq 15$)	Loopback on link ‘n’ (where $2 \leq n \leq 15$)

Note : Loopback can be performed on any link, independent of the other links. Pins on headers P10 and P15, corresponding to link ‘n’ (where $2 \leq n \leq 31$), need not be shorted if loopback is not to be performed on link ‘n’.

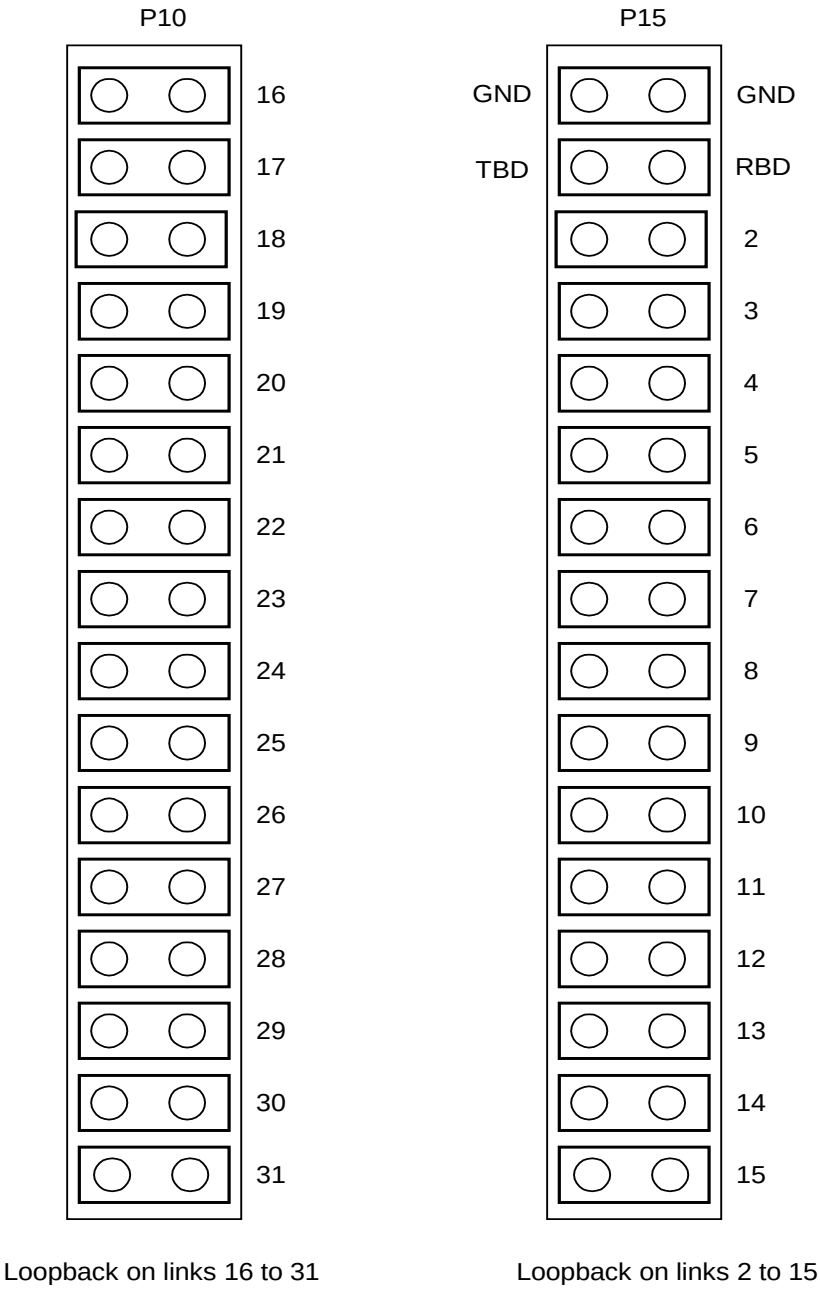
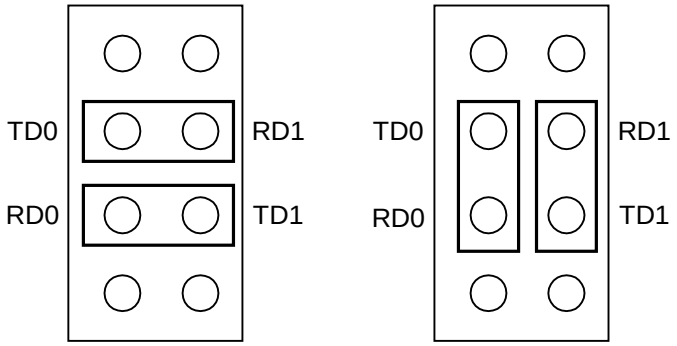


Figure 16 Jumper settings for data loopback on links 2 to 31

2.15 Jumper settings for Data loopback/cross-connect on links 0 and 1

Placement of shorting jumpers over header P2 result in configuration of either loopback or cross-connect of data on links 0 and 1. This is shown in Figure 17. The jumper settings are also listed in Table 14.



Simultaneous Cross Connect Simultaneous Loopback

Figure 17 Jumper settings for loopback/cross-connect on links 0 and 1 (P2)

Table 14 Jumper settings for loopback/cross-connect on links 0 and 1

HEADER	JUMPER SETTING	CONFIGURATION
P2	TD0 shorted to RD1, TD1 shorted to RD0	Cross-connect on links 0 and 1
P2	TD0 shorted to RD0, TD1 shorted to RD1	Loopback on links 0 and 1

2.16 Jumper settings for BERT Emulation

Link 2 is used to emulate the BERT interface. To emulate BERT interface, link 2 should act as the source of TBD data, and at the same time, receive data on RBD output of FREEDM™-32P672 chip. RBCLK and TBCLK are respectively shorted to RCLK[2] and TCLK[2]. The jumper settings on headers P15 and P7 for BERT Emulation are listed in Table 15 and are also shown in Figure 18 and Figure 19.

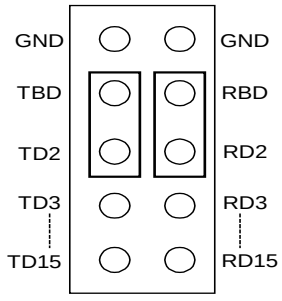


Figure 18 Jumper settings for BERT data emulation (P15)

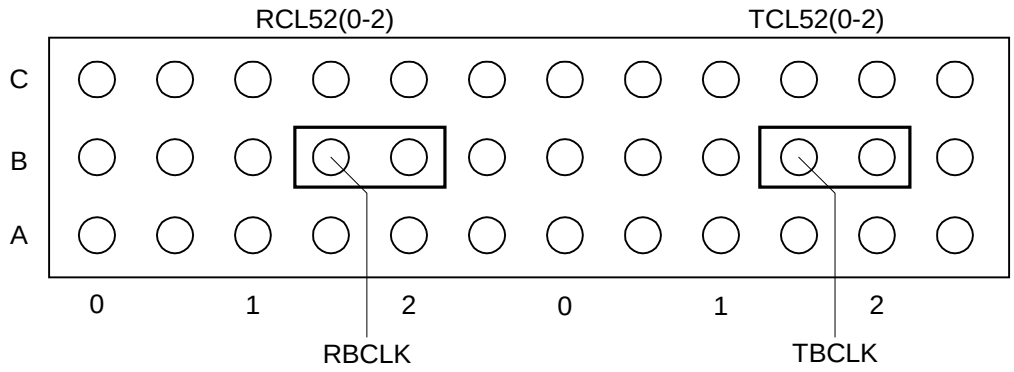


Figure 19 Jumper settings for BERT Clock Emulation (P7).

Table 15 Jumper settings for BERT Clock Emulation

HEADER	JUMPER SETTING	CONFIGURATION
P15	TD2 shorted to TBD, RD2 shorted to RBD	BERT data emulation
P7	Pin B2 (under RCL52(0-2)) shorted to RBCLK.	RBCLK shorted to RCLK[2]
P7	Pin B2 (under TCL52(0-2)) shorted to TBCLK.	TBCLK shorted to TCLK[2]

2.17 Placement of oscillators in the sockets

Table 16 lists the oscillators to be placed in the sockets, prior to the card being plugged into the socket.

Table 16 Oscillator placement in sockets

SOCKET	OSCILLATOR FREQUENCY	TEST CASE
OSC 1	1.544 MHz	Unchannelized T1 on links 0 through 15
	2.048 MHz	Unchannelized E1 on links 0 through 15
OSC 2	4.096 MHz	Unchannelized 2.048 Mbit/s H-MVIP mode
OSC 3	52 MHz	Unchannelized 52 Mbit/s traffic on links 0 through 2
	44.736 MHz	Unchannelized 44.736 Mbit/s traffic on links 0 through 2
OSC 4	1.544 MHz	Unchannelized T1 on links 16 through 31
	2.048 MHz	Unchannelized E1 on links 16 through 31
OSC 5	40 MHz	SYSCLK for FREEDM™-32P672

Note: Clocks are not provisioned to the clock inputs of the FREEDM™-32P672 chip simply by placing the oscillators in the appropriate sockets. Frequency selection and clock provision has to be done by means of jumpers, as mentioned in earlier sections.

3 CONFIGURATIONS FOR THE TEST CASES

3.1 Configuration for PCI Interface Test

Table 17 lists the required configuration for the PCI Interface Test.

Table 17 Configuration for the PCI Interface Test

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in row A shorted to pins in row B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	1.544 MHz provision to RCLK[15:0] inputs of FREEDM™-32P672
P11	RCLK[31:16]	Pins A16 through	1.544 MHz provision to

		A31 shorted to pins B16 through B31 respectively	RCLK[31:16] inputs of FREEDM™-32P672
P13	TCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	1.544 MHz provision to TCLK[15:0] inputs of FREEDM™-32P672
P14	TCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	1.544 MHz provision to TCLK[31:16] inputs of FREEDM™-32P672
P7	RCL52[2:0]	Pins B-R0, B-R1 and B-R2 shorted to pins C-R0, C-R1 and C-R2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for RCLK[2:0]
P7	TCL52[2:0]	Pins B-T0, B-T1 and B-T2 shorted to pins C-T0, C-T1 and C-T2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for TCLK[2:0]
P15	TD RD[15:2]	Jumpers not used	No loopback on links 2 through 15
P10	TD RD[31:16]	Jumpers not used	No loopback on links 16 through 31
P2	TD RD[1:0]	Jumpers not used	No loopback on links 0 and 1

3.2 Configuration for unchannelized T1 loopback mode

Each of the 32 transmit/receive links can be configured independently to transmit/receive unchannelized T1 data. This is done by the software. Loopback can be performed on any of these 32 links by using shorting jumpers appropriately over headers provided on the PCI card. Table 18 shows the jumper settings for performing loopback on all the 32 links.

Table 18 Configuration for simultaneous loopback of T1 data on 32 links

HEADER	SIGNAL	JUMPER	CONFIGURATION ACHIEVED

		SETTINGS	
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in row A shorted to pins in row B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	1.544 MHz provision to RCLK[15:0] inputs of FREEDM™-32P672
P11	RCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	1.544 MHz provision to RCLK[31:16] inputs of FREEDM™-32P672
P13	TCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	1.544 MHz provision to TCLK[15:0] inputs of FREEDM™-32P672
P14	TCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31	1.544 MHz provision to TCLK[31:16] inputs of FREEDM™-32P672

		respectively	
P7	RCL52[2:0]	Pins B-R0, B-R1 and B-R2 shorted to pins C-R0, C-R1 and C-R2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for RCLK[2:0]
P7	TCL52[2:0]	Pins B-T0, B-T1 and B-T2 shorted to pins C-T0, C-T1 and C-T2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for TCLK[2:0]
P15	TD RD[15:2]	Pins A2 through A15 shorted to pins B2 through B15 respectively	Loopback on links 2 through 15
P10	TD RD[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	Loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0, TD1 shorted to RD1	Loopback on links 0 and 1

Note: 1.544 MHz oscillators should be placed in sockets OSC 1 and OSC 4. If loopback is not to be performed on each of the 32 links, jumper settings will be similar to those shown in Table 18, except for the unused RCLK, TCLK, RD and TD. Unused RCLK and TCLK should be grounded by placing jumpers over pins of columns B and C, of the unused links. Unused RD and TD need not be shorted.

3.3 Configuration for unchannelized E1 loopback mode

Each of the 32 transmit/receive links can be configured independently to transmit/receive unchannelized E1 data. This is done by the software. Loopback can be performed on any of these 32 links by using shorting jumpers

appropriately over headers provided on the PCI card. Table 18 shows the jumper settings for performing loopback on all the 32 links.

Table 18 Configuration for simultaneous loopback of E1 data on 32 links

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins A0 through A15 shorted to pins B0 through	2.048 MHz provision to RCLK[15:0] inputs of FREEDM™-32P672

		B15 respectively	
P11	RCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	2.048 MHz provision to RCLK[31:16] inputs of FREEDM™-32P672
P13	TCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	2.048 MHz provision to TCLK[15:0] inputs of FREEDM™-32P672
P14	TCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	2.048 MHz provision to TCLK[31:16] inputs of FREEDM™-32P672
P7	RCL52[2:0]	Pins B-R0, B-R1 and B-R2 shorted to pins C-R0, C-R1 and C-R2 respectively (Columns 0, 1 and 2)	2.048 MHz selection for RCLK[2:0]
P7	TCL52[2:0]	Pins B-T0, B-T1 and B-T2 shorted to pins C-T0, C-T1 and C-T2 respectively (Columns 0, 1 and 2)	2.048 MHz selection for TCLK[2:0]
P15	TD RD[15:2]	Pins A2 through A15 shorted to pins B2 through B15 respectively	Loopback on links 2 through 15
P10	TD RD[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	Loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0, TD1 shorted to RD1	Loopback on links 0 and 1

Note: 2.048 MHz oscillators should be placed in sockets OSC 1 and OSC 4. If loopback is not to be performed on each of the 32 links, jumper settings will be similar to those shown in Table 18, except for the unused RCLK, TCLK, RD and TD. Unused RCLK and TCLK should be grounded by placing shorting jumpers

over pins of columns B and C, of the unused links. Unused RD and TD need not be shorted.

3.4 Configuration for 16 T1/ 16 E1 unchannelized loopback mode

With 1.544 MHz oscillator placed in socket OSC 1, and 2.048 MHz oscillator placed in OSC 4, simultaneous loopback of 16 unchannelized T1 links (links 0-15) and 16 unchannelized E1 links (links 16-31) can be performed. The jumper settings for this loopback are shown in Table 19.

Table 19 Configuration for 16 T1/E1 unchannelized loopback

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins A0 through	1.544 MHz provision to

		A15 shorted to pins B0 through B15 respectively	RCLK[15:0] inputs of FREEDM™-32P672
P11	RCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	2.048 MHz provision to RCLK[31:16] inputs of FREEDM™-32P672
P13	TCLK[15:0]	Pins A0 through A15 shorted to pins B0 through B15 respectively	1.544 MHz provision to TCLK[15:0] inputs of FREEDM™-32P672
P14	TCLK[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	2.048 MHz provision to TCLK[31:16] inputs of FREEDM™-32P672
P7	RCL52[2:0]	Pins B-R0, B-R1 and B-R2 shorted to pins C-R0, C-R1 and C-R2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for RCLK[2:0]
P7	TCL52[2:0]	Pins B-T0, B-T1 and B-T2 shorted to pins C-T0, C-T1 and C-T2 respectively (Columns 0, 1 and 2)	1.544 MHz selection for TCLK[2:0]
P15	TD RD[15:2]	Pins A2 through A15 shorted to pins B2 through B15 respectively	Loopback on links 2 through 15
P10	TD RD[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	Loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0, TD1 shorted to RD1	Loopback on links 0 and 1

Note: If links 0 through 15 are to be configured for unchannelized E1 data and links 16 through 31 are to be configured for T1 data, 2.048 MHz oscillator should

be placed in socket OSC 1, whereas 1.544 MHz oscillator should be placed in OSC 4.

3.5 Configuration for unchannelized 52 Mbit/s

Links 0 through 2 can be configured for supporting 52 Mbit/s data. The jumper settings for simultaneous loopback of 52 Mbit/s on links 0 through 2, is shown in Table 20.

Table 20 Simultaneous loopback of unchannelized 52 Mbit/s data on links 0 through 2

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and A	SYSCLK set to 40 MHz
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins Ay shorted to pins By	52 MHz provision to RCLK[2:0] inputs of FREEDM™-32P672.

		respectively, where y = link to be operated at 52 MHz The pins Bz shorted to pins Cz where z = link to be disabled	(select 2 links to provision, disable the third)
P11	RCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	RCLK[31:16] grounded
P13	TCLK[15:0]	Pins Ay shorted to pins By respectively, where y = link to be operated at 52Mhz. The pins Bz shorted to pins Cz where z = link to be disabled	52 MHz provision to TCLK[2:0] inputs of FREEDM™-32P672. (select 2 links to provision and disable the third)
P14	TCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	TCLK[31:16] grounded
P7	RCL52[2:0]	Pins A-R0, A-R1 and A-R2 shorted to pins B-R0, B-R1 and B-R2 respectively (Columns 0, 1 and 2)	52 MHz selection for RCLK[2:0]
P7	TCL52[2:0]	Pins B-T0, B-T1 and B-T2 shorted to pins A-T0, A-T1 and A-T2 respectively (Columns 0, 1 and 2)	52 MHz selection for TCLK[2:0]
P15	TD RD[15:2]	Pin A2 shorted to pin B2 respectively	Loopback on link 2
P10	TD RD[31:16]	Jumpers not used	No loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0, TD1 shorted	Loopback on links 0 and 1

		to RD1	

Note 1: All unused RCLK and TCLK should be grounded, by placing shorting jumpers over pins of columns B and C, of the unused links. Shorting jumpers need not be placed over receive/transmit links 3 through 31 (RD[31:3] and TD[31:3]). If not all three RCLK and TCLK are used, unused RCLK and TCLK should be grounded.

Note 2: If simultaneous cross-connect of data on links 0 and 1 is to be performed, TD0 should be shorted to RD1, whereas TD1 should be shorted to RD0, on header P2.

Note 3: Software support is provided for 52Mbit/s data loopback on only 2 of the 3 possible links, RCLK and TCLK inputs for the third link should be disabled. Also, SYSCLK can be connected to PCICLKO output of the FREEDM™-32P672 chip, provided that PCI frequency is 33 MHz.

3.6 Configuration for unchannelized Mixed DS3/T1/E1 data loopback

Links 0 through 2 can be configured for supporting DS-3 data. The jumper settings for simultaneous loopback of Mixed DS3/T1/E1, is shown in Table 21

Table 21 Simultaneous loopback of unchannelized Mixed DS3/T1/E1 data

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and A	SYSCLK set to 40 MHz
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and	RFPB[3:0] grounded

		A3 shorted to pins B0, B1, B2 and B3 respectively	
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins Ay shorted to pins By respectively, where y = link to be operated at DS3, T1 or E1. The pins Bz shorted to pins Cz where z = link to be disabled	DS3 provision to RCLK[2:0] inputs of FREEDM™-32P672. T1/E1 clocks connected to selective links for Mixed DS3/T1/E1 operation
P11	RCLK[31:16]	Pins Ay shorted to pins By respectively, where y = link to be operated at T1 or E1. The pins Bz shorted to pins Cz where z = link to be disabled	Selected Links enabled for T1/E1 operation (Mixed mode)
P13	TCLK[15:0]	Pins Ay shorted to pins By respectively, where y = link to be operated at DS3, T1 or E1. The pins Bz shorted to pins Cz where z = link to be disabled	DS3 provision to TCLK[2:0] inputs of FREEDM™-32P672. T1/E1 clocks connected to selective links for Mixed DS3/T1/E1 operation
P14	TCLK[31:16]	Pins Ay shorted to pins By respectively, where y = link to be operated at T1 or E1. The pins Bz	Selected Links enabled for T1/E1 operation (Mixed mode)

		shorted to pins Cz where z = link to be disabled	
P7	RCL52[2:0]	Pins A-Ry shorted to pins B-Ry, respectively, where y [y = 0,1 or 2] is the link to be operated at DS3. Pins B-Rz shorted to C-Rz where z = links not used for DS3	DS3 selection for RCLK[2:0] (One of the links 0, 1 or 2 is operated at DS3 rate)
P7	TCL52[2:0]	Pins A-Ty shorted to pins B-Ty, respectively, where y [y = 0,1 or 2] is the link to be operated at DS3. Pins B-Tz shorted to C-Tz where z = links not used for DS3	DS3 selection for TCLK[2:0] (One of the links 0, 1 or 2 is operated at DS3 rate)
P15	TD RD[15:2]	Pins Ay shorted to pins By respectively, where y = link to be operated at DS3/T1/E1	Loopback on selected links
P10	TD RD[31:16]	Pins Ay shorted to pins By respectively, where y = link to be operated at T1/E1	Loopback on selected links
P2	TD RD[1:0]	TDy shorted to RDy respectively, where y = link to be operated at DS3/T1/E1	Loopback on selected links

Note 1: All unused RCLK and TCLK should be grounded, by placing shorting jumpers over pins of columns B and C, of the unused links. Shorting jumpers need not be placed over unused receive/transmit links.

Note 2: The aggregate instantaneous clock rate over all 32 possible links is limited to 64 MHz.

3.7 Configuration for unchannelized 2.048 Mbit/s H-MVIP data loopback

One or more link groups can be configured to receive/transmit unchannelized 2.048 Mbit/s H-MVIP data. The jumper settings for performing loopback of 2.048 Mbit/s H-MVIP data on all the 32 links, is shown in Table 22.

Table 22 Configuration for unchannelized 2.048 Mbit/s H-MVIP data loopback

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins A0, A1, A2 and A3 respectively	4.096 MHz provision to RMVCK inputs of FREEDM™-32P672
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins A0, A1, A2 and A3 respectively	4.096 MHz provision to TMVCK inputs of FREEDM™-32P672
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins C0, C1, C2 and C3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] pulled high
P1	TFPB[3:0]	Pins C0, C1, C2 and C3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] pulled high
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins C0 through	RCLK[15:0] grounded

		C15 shorted to pins B0 through B15 respectively	
P11	RCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	RCLK[31:16] grounded
P13	TCLK[15:0]	Pins C0 through C15 shorted to pins B0 through B15 respectively	TCLK[15:0] grounded
P14	TCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	TCLK[31:16] grounded
P7	RCL52[2:0]	No shorting jumper placed on this header	
P7	TCL52[2:0]	No shorting jumper placed on this header	
P15	TD RD[15:2]	Pins A2 through A15 shorted to pins B2 through B15 respectively	Loopback on links 2 through 15
P10	TD RD[31:16]	Pins A16 through A31 shorted to pins B16 through B31 respectively	Loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0, TD1 shorted to RD1	Loopback on links 0 and 1

Note 1: 4.096 MHz oscillator should be placed in socket OSC 2.

Note 2: If all the link-groups are not configured for unchannelized 2.048 Mbit/s H-MVIP mode, unused RMVCK and TMVCK should be grounded. No shorting jumpers should be used over unused RD and TD. For example, if link-group 0 alone is configured for unchannelized 2.048 Mbit/s H-MVIP mode, 4.096 MHz clock should be provided to RMVCK[0] only. Hence, on header P5, pin B0 should be shorted to A0, whereas pins B1, B2 and B3 should be shorted to pins C1, C2 and C3 respectively (i.e. RMVCK[3:1] grounded). Also, pins corresponding to TD[31:8] and RD[31:8] are not shorted to each other.

3.8 Configuration for unchannelized 8.192 Mbit/s H-MVIP data loopback

Unchannelized H-MVIP data at 8.192 Mbit/s can be transmitted/received by the FREEDM™-32P672 chip on links 4m ($0 \leq m \leq 7$) only. The configuration for loopback of 8.192 Mbit/s H-MVIP data on links 4m is shown in Table 23.

Table 23 Configuration for unchannelized 8.192 Mbit/s H-MVIP data loopback

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK [3:0] grounded
P4	RMV8DC & TMV8DC	Wire to board connector plugged into pins of rows C and D	16.384 MHz provision to RMV8DC &TMV8DC
P4	RMV8FPC & TMV8FPC	Wire to board connector plugged into pins of rows A and B	4.096 MHz provision to RMV8FPC & TMV8FPC
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column C shorted to pins in column B respectively	RFP8B and TFP8B pulled high
P12	RCLK[15:0]	Pins C0 through C15 shorted to pins	RCLK[15:0] grounded

		B0 through B15 respectively	
P11	RCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	RCLK[31:16] grounded
P13	TCLK[15:0]	Pins C0 through C15 shorted to pins B0 through B15 respectively	TCLK[15:0] grounded
P14	TCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	TCLK[31:16] grounded
P7	RCL52[2:0]	No shorting jumper placed on this header	
P7	TCL52[2:0]	No shorting jumper placed on this header	
P15	TD RD[15:2]	Pins A4, A8 and A12 shorted to pins B4, B8 and B12 respectively	Loopback on links 4, 8 and 12
P10	TD RD[31:16]	Pins A16, A20, A24 and A28 shorted to pins B16, B20, B24 and B28 respectively	Loopback on links 16, 20, 24 and 28
P2	TD RD[1:0]	TD0 shorted to RD0	Loopback on link 0

Note : If all the links in the group 4m ($0 \leq m \leq 7$), are not used, the unused TD and RD pins should not be shorted. For example, if only link 0 is used for 8.192 Mbit/s H-MVIP mode, then only RD0 and TD0 should be shorted by a jumper. The remaining RD and TD header pins should not be shorted.

3.9 BERT Signal Verification

Configure links 0 and 2 for unchannelized 52 MHz (or 1.544 MHz or 2.048 MHz) mode. Hardware provision for 52 MHz (or 1.544 MHz or 2.048 MHz) clock at RCLK [0] and TCLK[0] of the FREEDM™-32P672 chip is made for BERT signal

verification test. Also, RBCLK and TBCLK are shorted respectively to RCLK[2] and TCLK[2]. Loopback of data on link 0 is enabled in hardware. Hardware configuration is done by shorting header pins corresponding to TBD and RBD, with header pins corresponding to TD[2] and RD[2], respectively. The idea is to make link 2 to emulate the BERT data, which may then be looped back externally by link 0. The jumper settings for BERT signal verification test are shown in Table 24.

Table 24 Configuration for BERT signal verification test

HEADER	SIGNAL	JUMPER SETTINGS	CONFIGURATION ACHIEVED
P3	SYSCLK	Jumper over pins B and C	SYSCLK connected to PCICLKO (only for 33 MHz operation)
P5	RMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	RMVCK[3:0] grounded
P6	TMVCK[3:0]	Pins B0, B1, B2 and B3 shorted to pins C0, C1, C2 and C3 respectively	TMVCK[3:0] grounded
P4	RMV8DC & TMV8DC	Pins in row C shorted to pins in row D respectively	RMV8DC &TMV8DC grounded
P4	RMV8FPC & TMV8FPC	Pins in row A shorted to pins in row B respectively	RMV8FPC & TMV8FPC grounded
P8	RFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	RFPB[3:0] grounded
P1	TFPB[3:0]	Pins A0, A1, A2 and A3 shorted to pins B0, B1, B2 and B3 respectively	TFPB[3:0] grounded
P9	RFP8B & TFP8B	Pins in column A shorted to pins in column B respectively	RFP8B and TFP8B grounded
P12	RCLK[15:0]	Pins A0 and A2 shorted to pins B0 and B2	1.544 MHz provision to RCLK[0] and RCLK[2] inputs of FREEDM™-32P672

		respectively; Bx shorted to Cx where x=(1,3 to 15)	
P11	RCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	RCLK[31:16] grounded
P13	TCLK[15:0]	Pins A0 and A2 shorted to pins B0 and B2 respectively; Bx shorted to Cx where x=(1,3 to 15)	1.544 MHz provision to TCLK[0] and TCLK[2] inputs of FREEDM™-32P672
P14	TCLK[31:16]	Pins C16 through C31 shorted to pins B16 through B31 respectively	TCLK[2] grounded
P7	RCL52[2:0]	Pin B-R2 shorted to RBCLK. Pin B-R0 shorted to pin C0.	RBCLK shorted to RCLK[2]
P7	TCL52[2:0]	Pin B-T2 shorted to TBCLK Pin B-T0 shorted to pin C0.	TBCLK shorted to TCLK[2]
P15	TD RD[15:2]	TBD shorted to TD[2] RBD shorted to RD[2]	BERT Emulation by link 2
P10	TD RD[31:16]	Jumpers not used	No loopback on links 16 through 31
P2	TD RD[1:0]	TD0 shorted to RD0	Loopback on link 0

Note : 1.544 MHz clock is used on links 0 and 2 for this particular test case.

4 HOW TO PROCEED WITH THE TEST CASES

Prior to plugging the card into the slot, the user has to place all the oscillators in the appropriate sockets as mentioned in section 2.17. The user also has to select the voltage source as mentioned in section 2. Tables in section 3 of the manual only mention the jumper settings for each test case. The user should go through section 2 to know how the jumpers are placed over the headers. The bitmap image of the Development Kit, provided in section 2, can be used to locate the positions of the headers. Ground marks are provided on the PCB to indicate the position of ground pins on the various headers. These ground marks are aligned with the rows (or columns) carrying only ground pins.

NOTES

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