

# ***RTE-200-TP***

## **Hardware User's Manual**

***RealTimeEvaluator***

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## 1. OVERVIEW

RTE-200-TP is an in-circuit emulator for NEC's RISC processor. By controlling the debugging control circuit (DCU) incorporated into the processor from the outside, RTE-200-TP enables highly transparent emulation on the board.

The debugger may be Multi developed by GHS or PARTNER, developed by MIDAS LAB.,INC, both of which operate under Windows 95/98/NT. The host system may be either a PC-9800 series or DOS/V machine.

The PC and RTE-200-TP can be connected using a dedicated PCMCIA card, host card designed for a bus, LAN-BOX, etc., depending on the environment.

This product comes with the following components. First check that none of the components are missing.

1. RTE-200-TP	1
2. User's manual	1
3. N-Wire cable	1
4. Power supply (RTE-PS01: +5V, 2A)	1

The following are required to use RTE-200-TP, although they are not supplied with the product.

5. KIT-xxxx-TP	<required.>
<ul style="list-style-type: none"> <li>• RTE for Win32 Setup Disk</li> <li>• User's manual</li> <li>• License sheet</li> </ul>	
6. ROM emulator probes	<Must be obtained as required.>
Four types of probe are available:	
<ul style="list-style-type: none"> <li>• DIP-32-ROM probe</li> <li>• DIP-40-ROM probe</li> <li>• DIP-42-ROM probe</li> <li>• STD-16BIT-ROM probe</li> </ul>	
7. Host interface	<One of the following is required.>
One of the following is required:	
<ul style="list-style-type: none"> <li>• PC card interface kit</li> <li>• PC 9800 Series DeskTop PC interface kit</li> <li>• DOS/V DeskTop PC ISA-bus interface kit</li> <li>• DOS/V DeskTop PC PCI-bus interface kit</li> <li>• LAN-BOX</li> </ul>	
8. Debugger	<Either is required.>
<ul style="list-style-type: none"> <li>• GHS Multi</li> <li>• PARTNER/Win</li> </ul>	

## 2. MAIN FEATURES

### High-level language debuggers

Both Multi and PARTNER are high-performance, high-level language debuggers that enable program execution, break point setting, variable inspection, and other operations to be performed at the source level.

### Easy connection

RTE-200-TP provides debugging capabilities equivalent to those of conventional in-circuit emulators, with the user system connected to the designated connector and the processor mounted on the board.

### Highly transparent emulation

By controlling the debugging control circuit (DCU) incorporated into CPU from the outside, RTE-200-TP provides highly transparent emulation, eliminating the problems associated with electrical interfaces.

### ROM emulation

RTE-200-TP incorporates up to 4MB of emulation memory for emulating ROMs. ROM probes for packages with 32 to 42 pins are available. (All probes are options.)

### Real-time trace

RTE-200-TP enables real-time trace, which is useful for debugging built-in systems. This capability uses a technique in which trace information conforming to the N-Wire specifications is recorded into memory, and supports trace clocks with frequencies of up to 66 MHz.

### Communication with the host system via a dedicated card or LAN-BOX

Three types of cards and LAN-BOX are available.

- The PC card is of Type II, as defined in version 2.1 of the PCMCIA specifications (version 4.2 of the JEIDA specification), and is for note-type PCs.
- The host card is for desktop PCs equipped with the PC 9800 C bus or DOS/V ISA or DOS/V PCI bus.
- LAN-BOX is connected via a LAN, and is a 10Base-T interface.

### 3. HARDWARE SPECIFICATIONS

#### Emulation

Target device	Depends on the KIT-xxxx-TP specifications
Emulation functions	
Operating frequency	Depends on the CPU specifications
Interface	JTAG/N-Wire
Break functions	
H/W break points (execution addresses)	Depends on the CPU specifications
S/W break points	100
Breaks that can be set using access events	Depends on the CPU specifications
Step breaks	Supported
Manual breaks	Supported
Trace functions	
Trace data bus	4 bits
Trace memory	4 bits x 128K words
Trigger that can be set using an execution address	Depends on the CPU specifications
Start that can be set using an execution address	Depends on the CPU specifications
Stop that can be set using an execution address	Depends on the CPU specifications
Trace delay	0 - 1FFFFh
Trace clock	66 MHz (max.)
Data trace conditions	Depends on the CPU specifications
Disassembled trace data display function	Depends on the CPU specifications
ROM emulation functions	
Memory capacity	4 M-Byte
Access time	50 ns
Number of ROMs that can be emulated	
DIP-32pin-ROM (8-bit ROM)	4 (max.)
DIP-40/42pin-ROM (16-bit ROM)	2 (max.)
STD16BIT-ROM connector	2 (max.)
Types of ROMs that can be emulated	
DIP-32-ROM probe(bits)	1M, 2M, 4M, 8M (27C010/020/040/080)
DIP-40-ROM probe(bits)	1M, 2M, 4M (27C1024/2048/4096)
DIP-42-ROM probe(bits)	8M, 16M (27C8000/16000)
Bus width specification (bits)	8/16/32
Target ROM capacity (bits)	512K, 1M, 2M, 4M, 8M, 16M(*1)
Pin mask functions	Depends on the CPU specifications

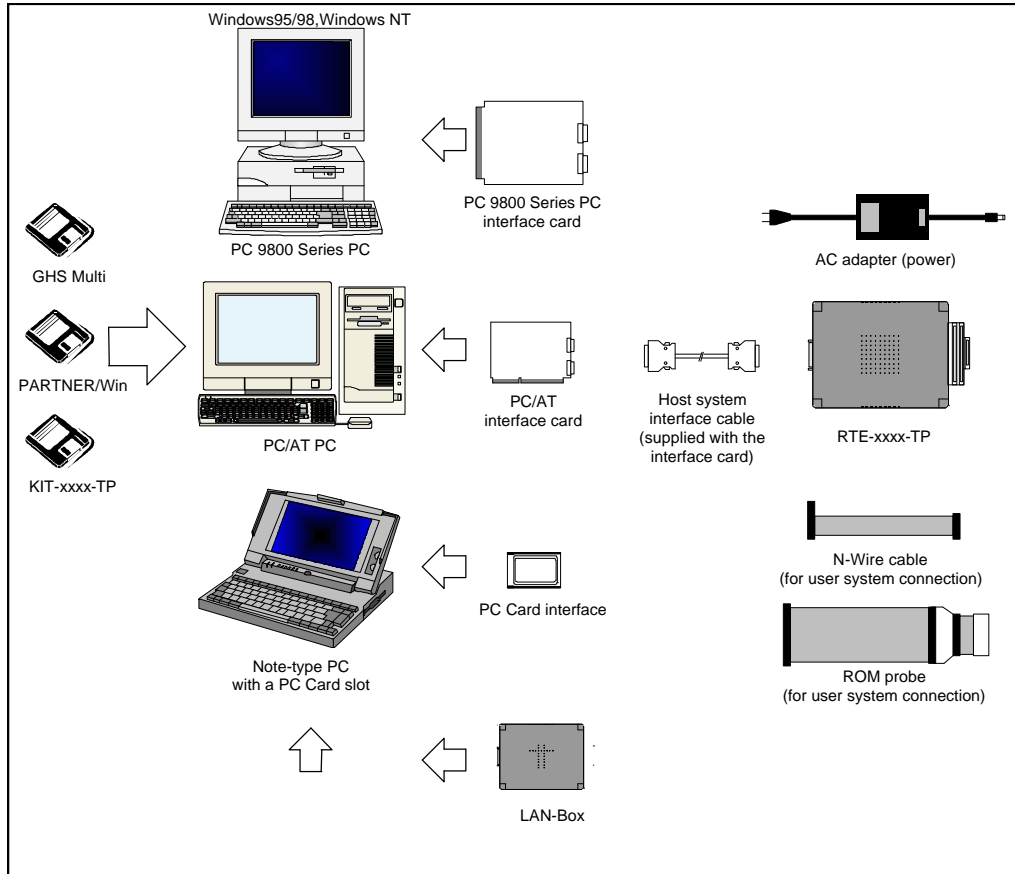
\*1 An 8-bit ROM probe supports ROMs of up to 8M bits.

#### Host system and interface

Item	Description
Target host machine	PC 9800 Series and DOS/V PCs
Debugger	GHS-Multi , Partner/Win(Windows 95/98/NT)
Interface	PC card Type II (version 2.1 of the PCMCIA specifications/version 4.2 of the JEIDA specification or later) PC 9800 (C bus), PC/AT (ISA bus and PCI bus), or LAN-BOX
Power supply	AC adapter (in: 100 V out: +5 V, 2A)

### 4. SYSTEM CONFIGURATION

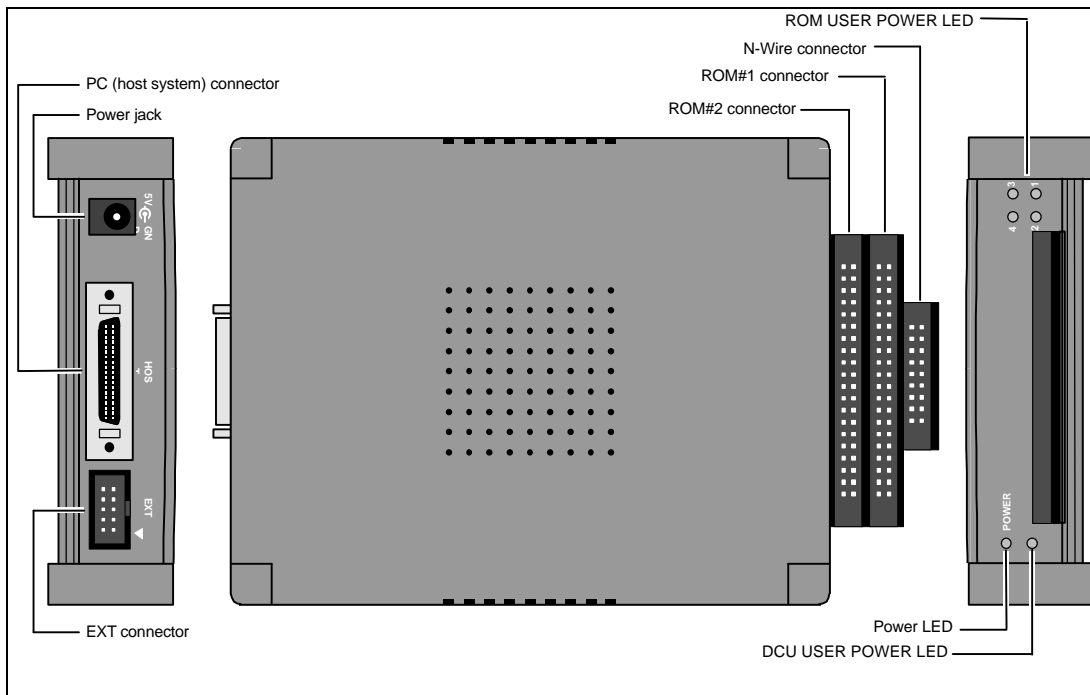
The following figure shows the configuration of a system in which RTE-200-TP is used.



- |                                   |   |
|-----------------------------------|---|
| GHS-multi,PARTNER/Win:            | High-level language debuggers for RTE-xxxx-TP   |
| KIT-xxxx-TP                       | Control software for each processor   |
| PC:                               | PC capable of running Windows 95  |
| PC 9800 Series PC interface card: | Card supporting the PC 9800 C bus   |
| PC/AT interface card:             | Card supporting the PC/AT ISA bus or PCI bus  |
| PC Card interface:                | Type II card (version 2.1 of the PCMCIA specifications/<br>version 4.2 of the JEIDA specification or later) |
| LAN-Box                           | Lan supporting the PC(10base-T)   |
| Host system interface cable:      | Cable for connecting RTE-200-TP to the host card  |
| AC adapter:                       | Dedicated power supply  |
| RTE-xxxx-TP:                      | RTE-200-TP  |
| N-Wire cable:                     | Cable for connecting to the user system used for<br>debugging   |
| ROM probe:                        | Probe for ROM emulation   |

## 5. COMPONENT NAMES AND FUNCTIONS

This chapter shows the appearance of RTE-200-TP, as well as the names and functions of its components.



### Power jack

This is a connector for the power supply. Power is supplied by inserting the plug of the supplied power supply into the jack.



**Do not connect any device other than the supplied AC adapter (RTE-PS01) to the power jack.**

### PC (host) connector (HOST)

This connector is used for connecting RTE-200-TP to the PC (host system). The host system interface cable is connected to this connector.

### EXT connector (EXT)

This connector is used for external signal input and internal signal output.

### N-Wire connector (N-Wire connector: JDCU1)

This connector is used for connecting RTE-200-TP to the user system via N-Wire.

### ROM emulator connector #1 (ROM#1 connector: JROM1)

This is connector No. 1 for connecting RTE-200-TP to the user system to emulate ROMs.

### ROM emulator connector #2 (ROM#2 connector: JROM2)

This is connector No. 2 for connecting RTE-200-TP to the user system to emulate ROMs.

### Power LED (POWER)

This LED lights steadily while the power to RTE-200-TP is on.

### DCU user system power LED (DCU USER POWER LED: DCU POWER)

This LED lights steadily while the power to the user system connected with the N-Wire connector is on.

**ROM user system power LEDs (ROM USER POWER LEDs: ROM POWER 1/2/3/4)**

These LEDs light steadily while the power to the power pins of the ROM sockets connected with the ROM emulator connectors is on. The four LEDs have the following meanings:

If an 8-bit ROM probe is used:

LED1 to LED4 correspond to sockets ROM1 to ROM4 at the end of ROM probes, and light steadily when the power to the power pins of the sockets is on.

If a 16-bit ROM probe is used:

LED1 and LED2 light steadily at the same time while:

The power to ROM socket #1 connected with connector ROM#1 is on.

LED3 and LED4 light steadily at the same time while:

The power to ROM socket #2 connected with connector ROM#2 is on.



## 6. INSTALLATION PROCEDURE

This chapter describes the procedure for installing RTE-200-TP.

### 1. Mount the interface card.

**Note** For information, refer to the manual provided with the interface card.

### 2. Install RTE for WIN32.

**Note** For information, refer to the manual provided with RTE for WIN32.



**At this point, do not start CHK RTE32.EXE.**

### 3. Connect RTE-200-TP.

Connect RTE-200-TP to the host interface card (or LAN-BOX) using the host system interface cable. Make the AC adapter ready for connection.

### 4. Connect RTE-200-TP to the user system.

**Note** For details, see Chapter 7.

### 5. Turn on the power.

**Note** For details, see Chapter 8.

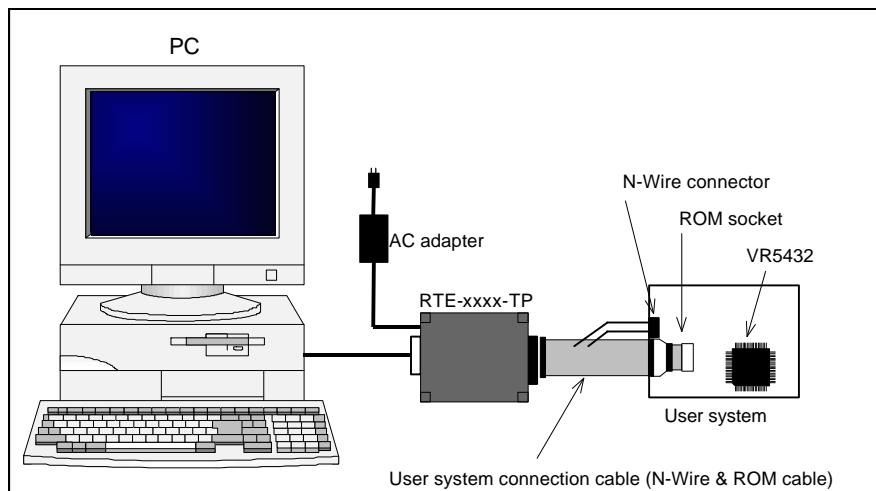
### 6. Set RTE for WIN32.

Start CHK RTE32.EXE and set the necessary parameters. For details, refer to the manual provided with RTE for WIN32 or see Chapter 9 of this manual.

### 7. Run the debugger.

**Note** For information, refer to the manual provided with the debugger.

The following figure shows an example how the devices are connected.



## 7. CONNECTION TO THE USER SYSTEM

The procedure for connecting RTE-200-TP to the user system is described below.

### **Connection with the N-Wire cable**

Connect the JDCU1 connector of RTE-200-TP to the user system using the N-Wire cable supplied with RTE-200-TP.

### **Connection with a ROM probe**

Connect the JROM1 or JROM2 connector of RTE-200-TP to the ROM socket of the user system, using a ROM probe of a type appropriate for the ROM of the user system. (ROM probes are options.)

Four types of ROM probe are available:

<DIP-32-ROM probe>

This probe allows emulation of up to four 8-bit ROMs.

On the RTE-200-TP side, connect a probe labeled ROM1 and ROM2 to JROM1 and a probe labeled ROM3 and ROM4 to JROM2.

On the user system side, connect ROM1, ROM2, ROM3, and ROM4 to the ROM sockets with the lowest, second lowest, second highest, and highest addresses, respectively, if an 8-bit bus is used. If a 16-bit bus is used, connect ROM1/ROM2 to the ROM sockets corresponding to D0-D7/D8-D15 of the lower addresses and ROM3/ROM4 to the ROM sockets corresponding to D0-D7/D8-15 of the higher addresses.

<DIP-40-ROM, DIP-42-ROM probes and STD16BIT-ROM probes>

These probes enable the emulation of up to two 16-bit ROMs.

On the RTE-200-TP side, connect a probe labeled ROM1 to JROM1 and a probe labeled ROM2 to JROM2.

On the user system side, connect a probe labeled ROM1 to the ROM socket with the lower address and a probe labeled ROM2 to the ROM socket with the higher address, if a 16-bit bus is used.



**When connecting probes to ROM sockets, pay careful attention to the ROM orientation. The dot mark indicates pin 1.**

### **Note on the DIP-32-ROM probe**

For 32-pin ROMs of 1MB or greater, there are two possible pin assignment schemes. Set the jumper on the board for the ROM cable according to the ROM being used.

OE-:24-pin,A16:2-pin : 1-2 Jumpered (factory setting)

OE-:2pin,A16:24-pin : 2-3 Jumpered

## 8. POWERING ON AND OFF

The procedures for powering the system on and off are described below. Complete all the steps in the installation procedure (such as cable connection) before powering the system on.

### **Powering on**

1. Turn on the power to the host system.
2. Turn on the power to RTE-200-TP. (Connect the dedicated AC adapter to the power jack of RTE-200-TP.)
3. Turn on the power to the user system.
4. Start the debugger.

### **Powering off**

1. Quit the debugger.
2. Turn off the power to the user system.
3. Turn off the power to RTE-200-TP. (Disconnect the AC adapter from RTE-200-TP.)
4. Turn off the power to the host system.



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**Do not turn on the power to the user system before powering on RTE-200-TP. Doing so may cause a malfunction.**

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## 9. RTE FOR WIN32

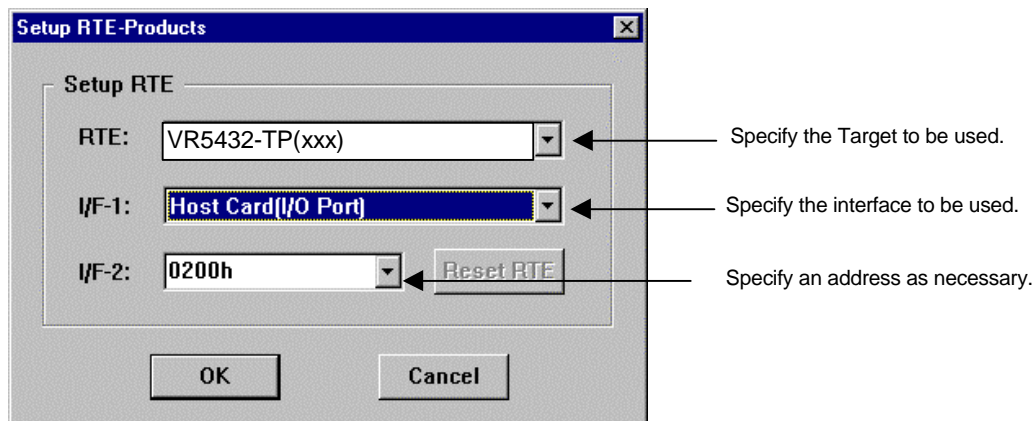
This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to RTE-200-TP.

### Starting ChkRTE32.exe

Start ChkRTE32.exe after RTE-200-TP has been connected to the user system and the power to all the devices is on. When RTE-200-TP is installed for the first time, ChkRTE32.exe must be started once to select RTE.

<Selecting RTE>

Set the Setup dialog box of ChkRTE32.exe, as follows.



\*RTE: section is an example in case of using with KIT-VR5432-TP

<Function test>

If RTE-200-TP is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.



If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.



**Perform the ChkRTE32.exe function test after the RTE-200-TP has been connected to the user system and the power to all the devices has been turned on.**

## 10. INITIALIZATION COMMANDS

Before debugging can be started, initialization is required normally. The following explains initialization using the appropriate internal commands with KIT-VR5400-TP. Method of initialization is different from KIT.

See KIT-xxxx-TP.'s manual.

### **env command**

[Format]

```
env [[!]auto] [[!]nmi] [[!]int] [jtag{25|12}] [[!]verify] [[!]hispeed]
      [work ADDR]
```

[Parameters]

- [!]auto: If a break point is encountered during execution, the break point causes a temporary break. Choose [Auto] to automatically perform the subsequent execution. Choose [!auto] to suppress it.
- [!]nmi: Specifies whether the NMI pin is to be masked. Enter ! if it is not to be masked.
- [!]int: Specifies that pins INTxx are to be masked. Enter ! if they are not to be masked.
- jtag[12|25]: Specifies the JTAG clock (12.5 MHz|25 MHz) for N-Wire. Initial value of rte4win32 is 12.5 MHz (Ver. 4.37 or later) or 25 MHz (before Ver. 4.37).
- [!]verify: Specifies the verification after writing memory is set. Enter ! if it is not to be set.

**Remark** The CPU also accesses an area that emulates ROM (jread or equivalent). Therefore, this command is useful for testing the area during downloading. Note, however, that the processing speed slows down.

[[!]hispeed]: Specifies high-speed mode to write data to memory. ! specifies the normal mode.

**Remark** The high-speed mode can be specified on condition that the ROM probe be connected. If this mode is specified, a control program temporarily located in the ROM emulated is executed in the foreground only when data of 128 bytes or more are contiguously written. Use this mode after the hardware has been completely debugged because the CPU must be able to access the ROM correctly. In normal mode, data can be written to ROM via JTAG.

[work ADDR]: Specifies an area for clearing the cache or executing initialization processing. Be sure to specify the RAM on uncache immediately after starting the system. The VR5400 requires RAM on the user system for cache processing. The monitor uses an area of 128 bytes from the specified address destructively.

**Remark** As this area is not used unless the cache area is accessed, confirm that the RAM can be accessed in the uncache area before accessing the cache area.

[Function]

The env command sets the emulation environment. Enter only those parameters that need to be changed. Parameters may be entered in any order. If the same parameter is entered twice, only the last entry is valid.

**rom command**

[Format]

rom [ADDR [LENGTH]] [512k|1m|2m|4m|8m|16m] [rom8|rom16] [bus8|bus16|bus32]  
[little|big]

[Parameters]

ADDR [LENGTH]: Specifies an area to be emulated.  
 ADDR: Specifies a start address. An error occurs if the specified start address does not match the lowest address of the ROM to be emulated (boundary of the ROM).  
 LENGTH: Number of bytes of the ROM to be emulated. (Must be specified in boundary units of 4 bytes.)  
 512k|1m|2m|4m|8m|16m: Specifies the bit size of the ROM to be emulated. Sizes from 512K bits to 16M bits can be specified. For the 27C1024, for example, specify 1M bits.  
 rom8|rom16: Specifies the number of data bits of the ROM to be emulated. Either 8 bits or 16 bits can be specified. If a DIP-32-ROM probe is used, choose rom8; if a DIP-40/42-ROM probe is used, choose rom16.  
 bus8|bus16|bus32: Specifies the ROM bus size in the system to be emulated. 8 bits, 16 bits, or 32 bits can be specified.  
 Little|big: Specifies the endian of the rom data. If little endian is specified during downloading, the binary image of a file is written as is. If big endian is specified, the data of the high-order bytes and low-order bytes are exchanged depending on the bus size of the ROM.

[Function]

The rom command sets the ROM emulation environment. Enter only the parameters that need to be changed. Parameters may be entered in any order. If the same parameter is entered twice, only the last entry is valid. The initial value of LENGTH is 0 (not used).

## 11. INTERFACE SPECIFICATIONS

This chapter describes the standard specifications of the connectors used for control that are required for the user system. Detail is depend on the CPU. See Kit-xxx-TP's manual.

### Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	CLKOUT	Output	22 - 33 $\Omega$ series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 $\Omega$ series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 $\Omega$ series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 $\Omega$ series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 $\Omega$ series resistor (recommended)
A6	TRCEND	Output	22 - 33 $\Omega$ series resistor (recommended)
A7	DDI	Input	4.7 K - 10 k $\Omega$ pullup
A8	DCK	Input	4.7 K - 10 k $\Omega$ pullup
A9	DMS	Input	4.7 K - 10 k $\Omega$ pullup
A10	DDO	Output	22 - 33 $\Omega$ series resistor (recommended)
A11	DRST-	Input	Open or connected to ColdReset* via external circuit (outputs the reset signal of negative logic from TP).
A12	Rmode*/ BkTGIO*	Input/Output	4.7 k - 10 k $\Omega$ pullup
A13	NC.	-----	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	-----	Connection to the power GND
B11	NC.	-----	Open
B12	NC.	-----	Open
B13	+3.3V	-----	Connection to the power

### Connectors

Manufacturer: KEL

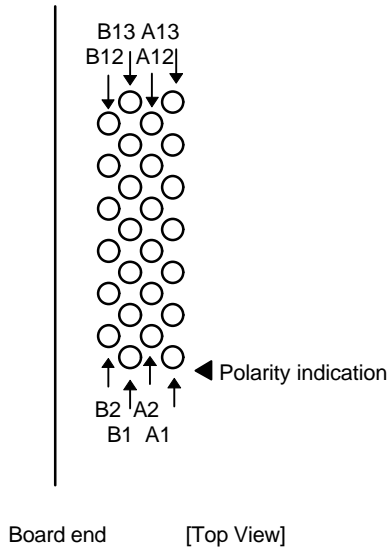
Models: 8830E-026-170S (straight)  
8830E-026-170L (right angle)  
8831E-026-170L (right angle, fixing hardware attached)

### Wire length

Keep the wire from CPU to the connector as short as possible.  
>>100 mm or shorter is recommended.

**Layout of the connectors on the board**

The figure below shows the physical layout of the connectors on the board.



**Note:** When actually arranging the pins, design them according to the connector dimensional information.



## 12. EXT CONNECTOR

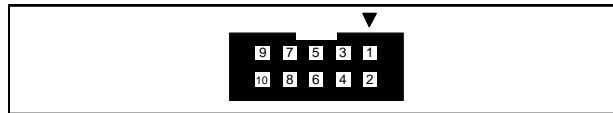
The specifications of the EXT connector are given below.

Pin number	Signal name	Input/output	Description
1	Factory Use	Output	Must be left unconnected.
2	EXI0	Input	External input signal #0 (pulled up with a 1-kΩ resistor). Edge detectable.
3	Factory Use	Output	Must be left unconnected.
4	EXI1	Input	External input signal #1 (pulled up with a 1-kΩ resistor)
5	Factory Use	Output	Must be left unconnected.
6	EXI2	Input	External input signal #2 (pulled up with a 1-kΩ resistor)
7	Factory Use	Output	Must be left unconnected.
8	EXI3	Input	External input signal #3 (pulled up with a 1-kΩ resistor)
9	GND	--	Ground signal
10	TRG-	Output	Trigger output (goes low upon detection of a trace trigger)

**Notes:**

1. The inputs to EXI0, EXI1, EXI2, and EXI3 are at 5V-TTL level.
2. The TRG- signal is an open-collector signal (pulled up with a 1-kΩ resistor).
3. EXI0 can be specified as a trace trigger.
4. EXI0 to EXI3 are recorded in memory as trace information.

**Pin arrangement:**



JEXT pin arrangement

**Applicable connector:**

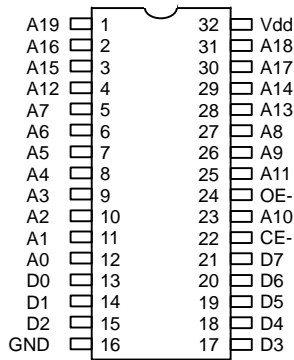
XG4M-1031 manufactured by Omron Corporation (or equivalent)

### 13. ROM PROBE SPECIFICATIONS

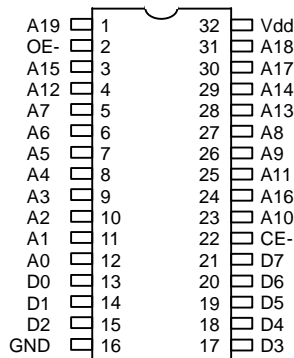
#### DIP-32-ROM probe

The DIP-32-ROM probe supports the following two pin arrangements. The arrangement to support is determined with the jumper on JP1.

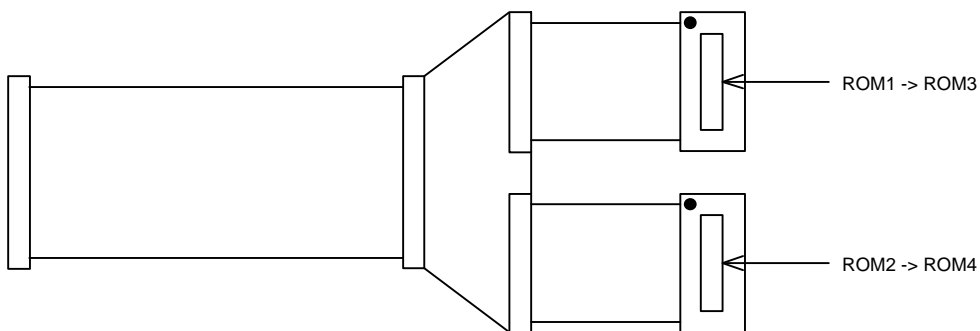
JP1 1-2 jumpered



JP1 2-3 jumpered

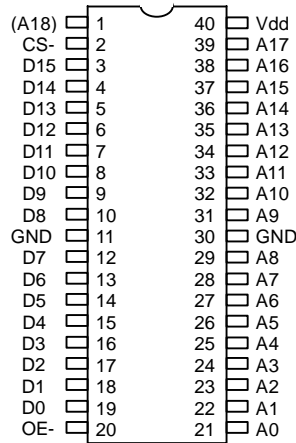


The labels at the end are marked ROM1 and ROM2 at the factory. If you purchase another DIP-32-ROM probe, replace the labels with those supplied to distinguish it from the first one, as shown in the figure below.



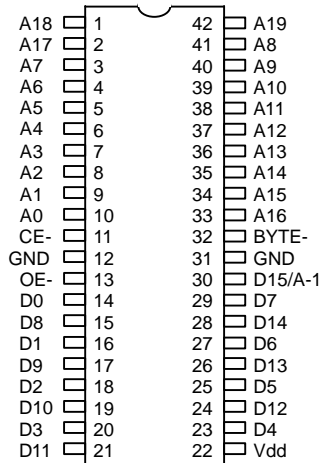
**DIP-40-ROM probe**

The DIP-40-ROM probe supports the following pin arrangement.

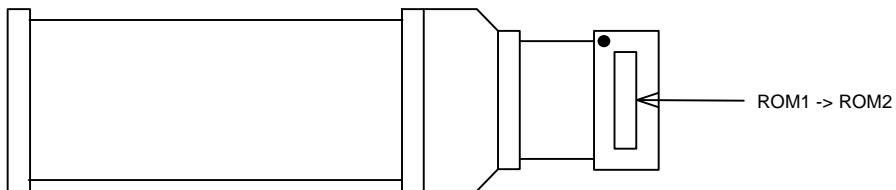


**DIP-42-ROM probe**

The DIP-42-ROM probe supports the following pin arrangement.



The label at the end is labeled ROM1 or ROM2 at the factory. If you purchase another DIP-40-ROM or DIP-42-ROM probe, replace the label with that supplied to distinguish it from the first one, as shown in the figure below.



**STD-16BIT-ROM probe****Signal description:**

signal	IN/OUT	name	description
A0 - A20	IN	ADDRESS BUS	Connect to rom address. Not used address connect to gnd.
A21 – A22	IN	ADDRESS BUS	Connect to ground level.
D0 - D15	OUT	DATA BUS	Connect to rom data
CE-	IN	CHIP ENABLE	Low active signal.
OE-	IN	OUTPUT ENABLE	Low active signal.
WRL- WRH-	IN	Write low-byte Write High-byte	No use
PSENSE	IN	POWER SENSE	Connect to rom VDD
INH-	OUT	INHBIT-	Always low level.
GND	-----	GND	Connect to ground.

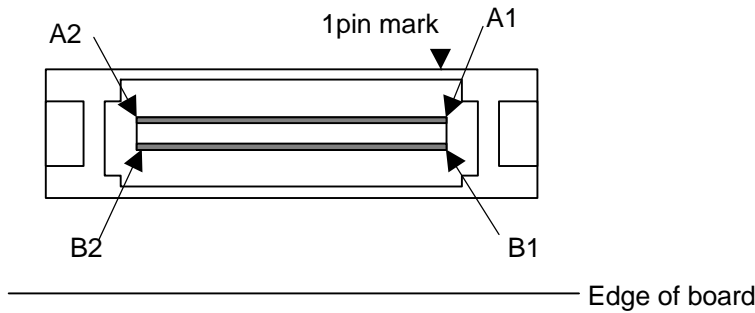
**Pin arrangement table:**

A side	signal	B side	signal
A1	GND	B1	A0
A2	A1	B2	A2
A3	A3	B3	A4
A4	A5	B4	A6
A5	A7	B5	A8
A6	A9	B6	A10
A7	A11	B7	A12
A8	A13	B8	A14
A9	A15	B9	A16
A10	A17	B10	A18
A11	A19	B11	A20
A12	GND(A21)	B12	GND(A22)
A13	NC.(WRH-)	B13	INH-(GND)
A14	NC.(WRL-)	B14	GND
A15	CE-	B15	GND
A16	OE-	B16	PSENSE(VCC IN)
A17	D0	B17	D1
A18	D2	B18	D3
A19	D4	B19	D5
A20	D6	B20	D7
A21	D8	B21	D9
A22	D10	B22	D11
A23	D12	B23	D13
A24	D14	B24	D15
A25	GND	B25	GND

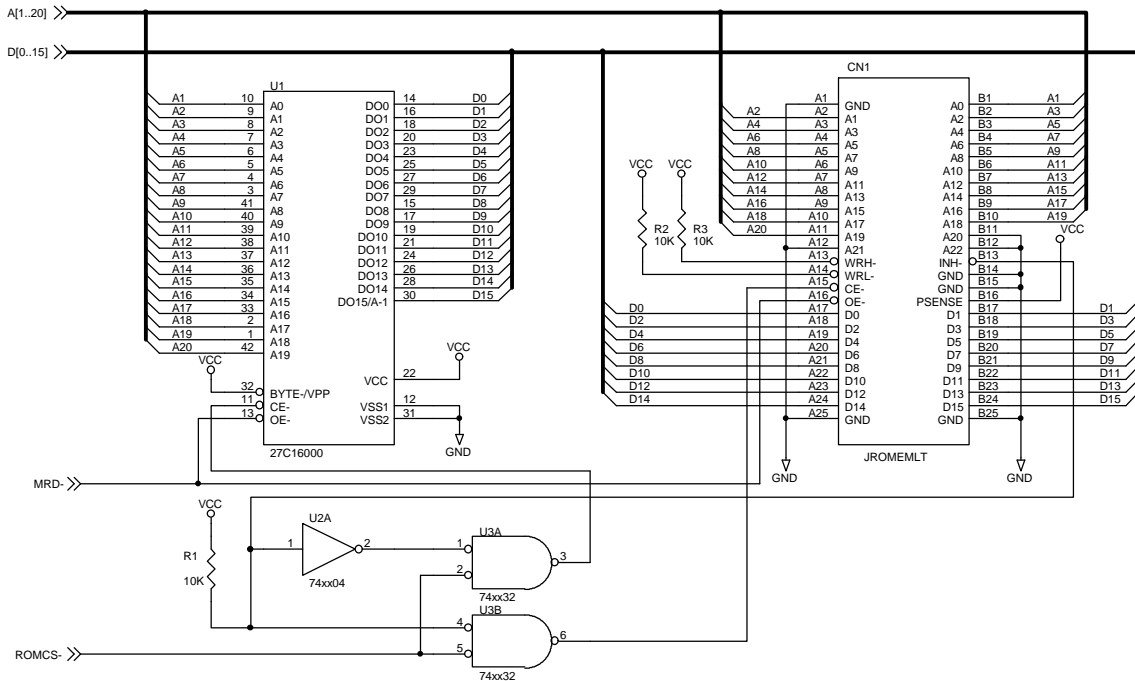
**Connectors:**

- Manufacturer: KEL
- Models: 8931E-050-178S (straight)
- 8931E-050-178L (right angle)
- 8930E-050-178MS(SMT straight)

**Layout of the connectors on the board:**

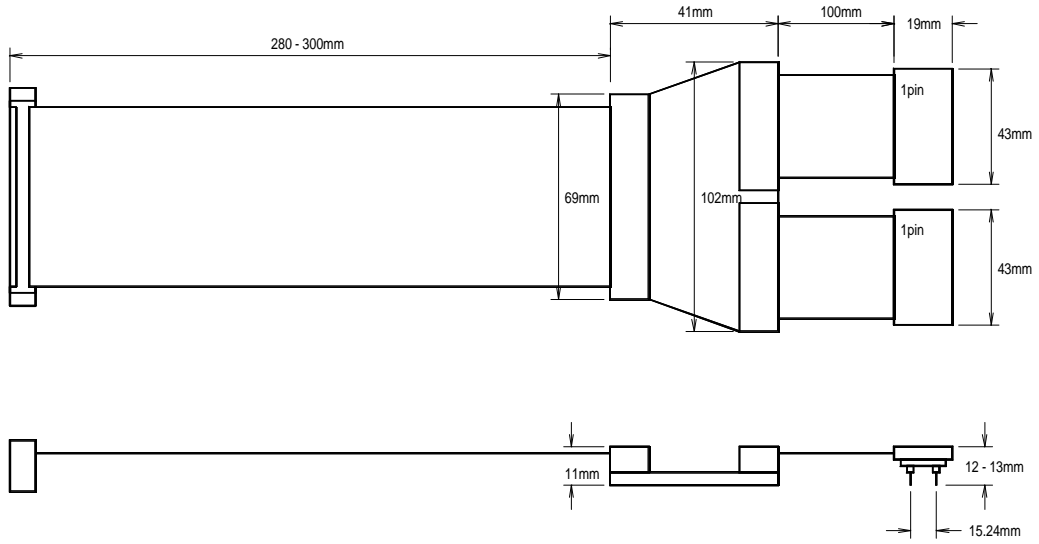


**Reference of the schematic:**

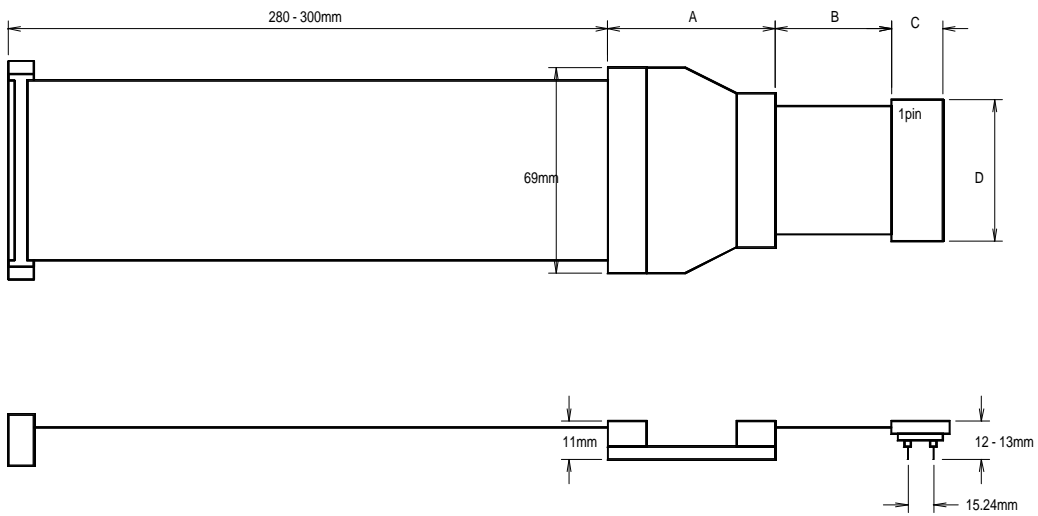


**APPENDIX-A APPEARANCE of ROM PROBE**

**DIP-32-ROM probe**



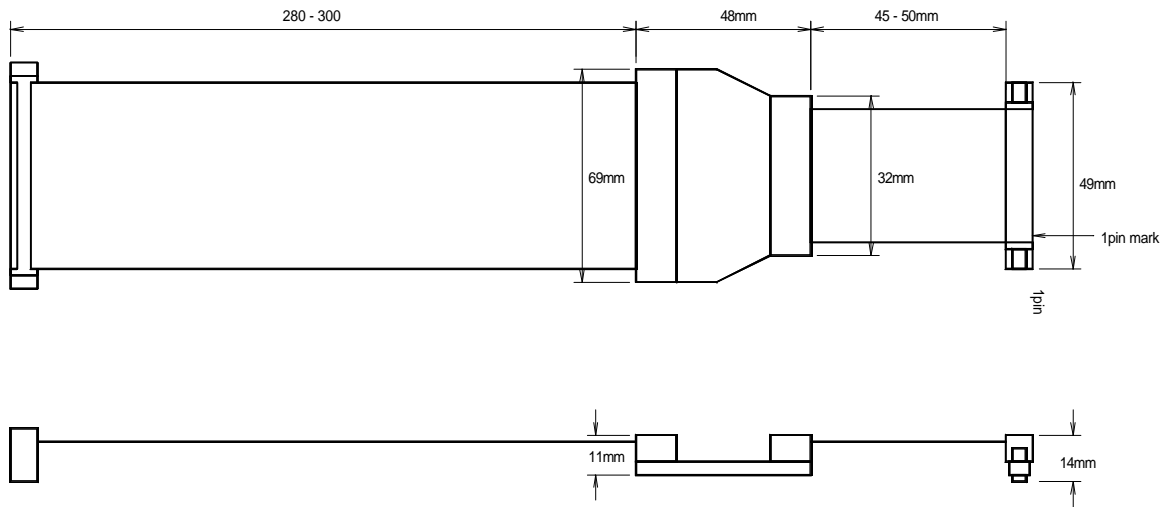
**DIP-40/42-ROM probe**



[mm]

Kind	A	B	C	D
CBL-ROM40	41	30	19	53
CBL-ROM42	46	30	19	56

**STD-16BIT-ROM probe**



Revision History

Rev.1.0 Dec. 15 1999 1<sup>st</sup> edition

<b>RTE-200-TP Hardware User's Manual</b>	M781MNL02
Date of preparation: Jun 15, 1998 Rev2.0	