
# LIDAR-Lite Operating Manual

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## Introduction

PulsedLight has targeted the need for high performance, very compact optical distance measurement sensors for cost sensitive markets such as UAV's, robotics and automotive. These applications benefit from substantially improved measurement range, high accuracy and reduced size over competing technology. Our single chip processing solution in combination with minimal supporting hardware enables a new class of optical distance measurement sensors that exceed the performance of current solutions at a substantially lower cost. PulsedLight's signal processing technology can be applied to applications ranging from single beam distance measurement to multi-pixel applications such as line scanning or complex 3-D imaging.

Our single board implementation of less than one square inch allows the use of a variety of optical sources such as LED's, VCSEL's (Vertical-Cavity Surface-Emitting Lasers) or edge emitting lasers. Our standard detector is based on a Si PIN diode but optionally; a Si APD can be used to provide greater sensitivity and range.

## LIDAR-Lite Specifications

| General | Technical Specifications |
|---|---|
| Power | 4.75-5.5V DC Nominal, Maximum 6V DC |
| Weight | PCB 4.5 grams, Module 22 grams with optics and housing |
| Size | PCB 44.5 X 16.5mm (1.75" by .65")<br>Housing 20 X 48 X 40mm (.8" X 1.9" X 1.6") |
| Current Consumption | <2ma @ 1Hz (shutdown between measurements),<br><100ma (continuous operation) |
| Max Operating Temp. | 70° C |
| External Trigger | 3.3V logic, high-low edge triggered |
| PWM Range Output | PWM signal proportional to range, 1msec/meter, 10µsec step size |
| I2C Machine Interface | 100Kb – Fixed, 0xC4 slave address. Internal register access & control. |
| Supported I2C Commands | Single distance measurement, velocity, signal strength |
| Mode Control | Busy status using I2C, External Trigger input / PWM outputs |

### Laser Sensor PCB Technical Specifications – PIN detector without optics

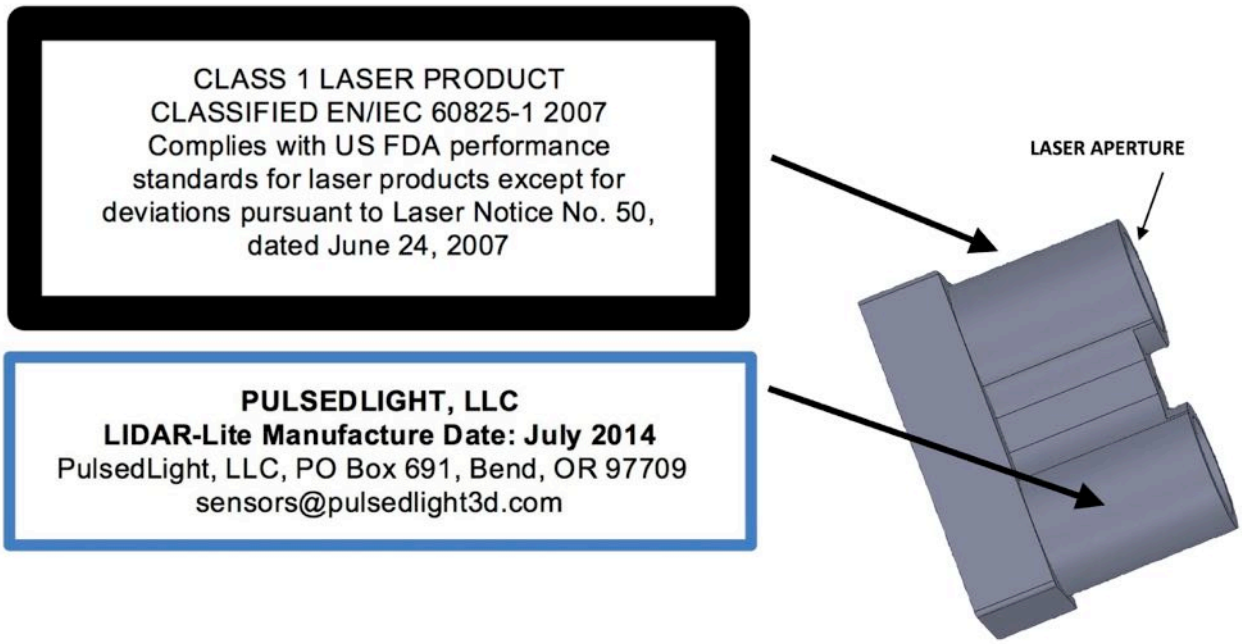
| General | Technical Specifications |
|---|---|
| NEP (PIN detector) | 12nW rms, 1.5pF detector capacitance, 1mm virtual detector size |
| Min Detectable signal | 1nW – 256 integrated bursts (maximum integration time) |
| Transmit Power (laser) | 1.5Watts peak 14mm @ 3amps drive, 75um single stripe laser junction |
| Transmit Power (LED) | 200mW within +/- 3 degree beam @ 1amp |

## LIDAR-Lite Specifications (Continued)

| System Parameters | LED/Pin | LED/Pin with Optics[1] | Laser/Pin with Optics[2] |
|---|---|---|---|
| TX Emitter | 5mm Plastic LED, 6° divergence | 5mm Plastic LED, 6° divergence | 75um, 1 watt, 4mrad, 14mm optic |
| RX Detector | 5mm Plastic Si PIN, 30° FOV | 12mm diameter 8mm effective aperture, 10° FOV | 14mm diameter aperture, 3° FOV |
| Detector Gain | 1x | 1x | 1x |
| TX /RX Focal Length | n/a | n/a | 25mm/25mm |
| Max Range @ 1Hz 30% target | 3 meters | 10 meters | 30 meters |
| Max Range @ 1Hz 90% target | 5 meters | 20 meters | 60 meters |
| Accuracy | +/- 0.025 meter | +/- 0.025 meter | +/- 0.025 meter |
| Acquisition Time | <0.02 sec | <0.02 sec | <0.02 sec |
| Max Rep Rate | 100 Hz | 100 Hz | 100 Hz, 10Hz Class 1 |

**1) Uses standard surface mount PIN detector instead of T 1 ¾ lamp style detector.**
**2) Uses custom laser housing & optics with surface mount PIN detector instead of T 1 ¾ lamp style detector.**

## Laser-Safety




LIDAR-Lite is a laser rangefinder that emits laser radiation. This Laser Product is designated Class 1 during all procedures of operation. This means that the laser is safe to look at with the unaided eye. However, it is *very* advisable to avoid looking into the beam and power the module off when not in use.

No regular maintenance is required for LIDAR-Lite. In the event that the unit becomes damaged or is inoperable, repair or service of LIDAR-Lite is only to be handled by authorized, factory-trained technicians. No service of LIDAR-Lite by the user is allowed. Attempting to repair or service the unit on your own can result in direct exposure to laser radiation and the risk of permanent eye damage. For repair or service please contact PulsedLight directly for a return authorization.

No user should modify LIDAR-Lite or operate it without it's housing or optics. The Operation of LIDAR-Lite without a housing and optics or modification of the housing or optics that exposes the laser source may result in direct exposure to laser radiation and the risk of permanent eye damage. Removal or modification of the diffuser in front of the laser optic may result in the risk of permanent eye damage.

**Caution** – Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure. PulsedLight is not responsible for injuries caused through the improper use or operation of this product.

**Class 1 Laser Product**

This Laser Product is designated Class 1 during all procedures of operation.

| Laser Parameters | |
|---|---|
| Wavelength | 905nm (nominal) |
| Total Laser Power - Peak | 1.3Watts |
| Mode of operation | Pulsed (max pulse train 256 pulses) |
| Pulse Width | 0.5uSec (50% duty Cycle) |
| Pulse Repetition Frequency | 10-20KHz nominal |
| Energy per Pulse | <280nJ |
| Beam Diameter at laser aperture | 12mm x 2mm |
| Divergence | 4mRadian x 2mRadian (Approx) |
| | |

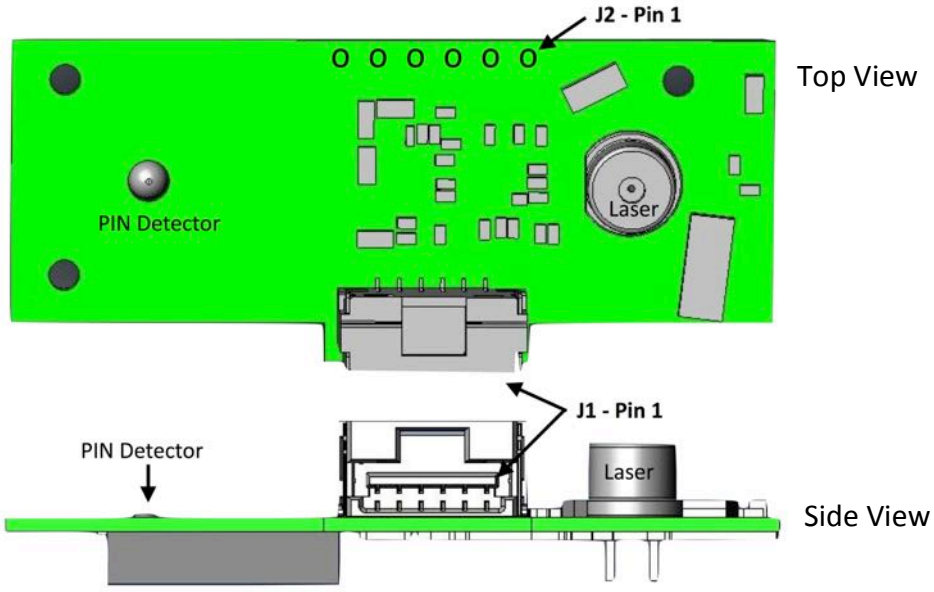
## Quick Start Guide

1. Make Power and I2C Data Connections as per J1 connector pin out diagram. Pins 2 & 3 are optional connections and not required.
2. Initialization: Apply Power to the Module. The sensor operates at 4.75-5.5V DC Nominal, Maximum 6V DC
3. Measurement: Write register 0x00 with value 0x04 (This performs a DC stabilization cycle, Signal Acquisition, Data processing). Refer to the section "I2C Protocol Summary" in this manual for more information about I2C Communications
4. Periodically poll the unit and wait until an ACK is received. The unit responds to read or write requests with a NACK when the sensor is busy processing a command or performing a measurement. (Optionally, wait approx. 20 milliseconds after acquisition and then proceed to read of high and low bytes)
5. Read: register 0x0f, returns the upper 8 bits of distance in cm, register 0x10, returns the lower 8 bits of distance in cm. (Optionally a 2-Byte read starting at 0x8f can be done)

### Sample Code

Sample code for LIDAR-Lite can be downloaded by visiting https://github.com/PulsedLight3D .

## LIDAR-Lite Signal & Power Interface Definitions




### J1 - Primary signal/power interface

Board Connector: Molex part #5023860670 Mating Connector: Molex # 5023800600 PLUG HSG 6POS

| | |
|---|---|
| **PIN 1** | POWER_IN – 4.75-5.5V DC Nominal, Maximum 6V DC. Peak current draw from this input is typically <100 milliamps over a duration from 4 to 20ms depending on received signal strength. Typical measurement times are roughly 10ms corresponding to a 2% one-time using one measurement per second. |
| **PIN 2** | POWER_EN - Active high, enables operation of the 3.3 V microcontroller Regulator. Low puts board to sleep, draws <40 microamperes. (Internal 100K pull-up) |
| **PIN 3** | Mode Select – Provides sensor busy status (active low) & trigger (high-low edge) PWM out (high) |
| **PIN 4** | I2C Clock (SCL) |
| **PIN 5** | I2C Data (SDA) |
| **PIN 6** | Signal/power ground. |

### J2 - Secondary signal/power - .1” spacing Molex style through hole

| | |
|---|---|
| **PIN 1** | Laser Bypass 5-20V max (nominally connected to pin2 through inductor L8 – removed for external power) |
| **PIN 2** | POWER_IN – 4.75-5.5V DC Nominal, Maximum 6V DC |
| **PIN 3** | POWER_EN - Active high |
| **PIN 4** | External reference clock input (Factory Option – Consult Factory) |
| **PIN 5** | Signal/power ground. |
| **PIN 6** | Detector bias – up to 25V external bias for PIN, external bias input 200V for APD (consult factory) |

## I2C Protocol Summary

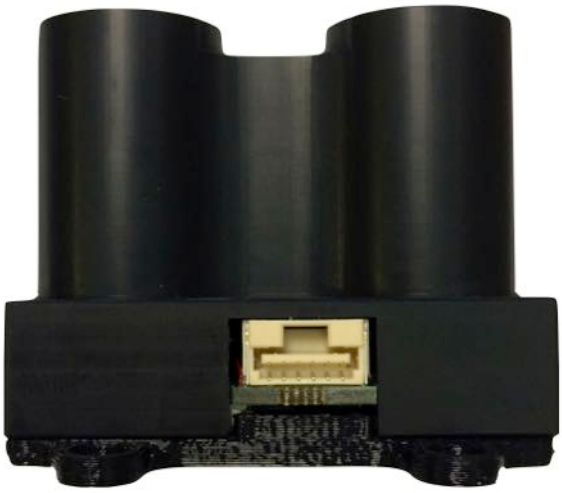
LIDAR-Lite has a 2-wire I2C-compatible serial interface (refer to *I2C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). It can be connected to an I2C bus as a slave device, under the control of an I2C master device. It supports standard 100 kHz data transfer mode. Support is not provided for 10-bit addressing.

The Sensor module has a 7-bit slave address with a default value of 0x62 in hexadecimal notation. The effective 8 bit I2C address is: 0xC4 write, 0xC5 read. The unit will not presently respond to a general call.

The I2C serial bus protocol operates as follows:

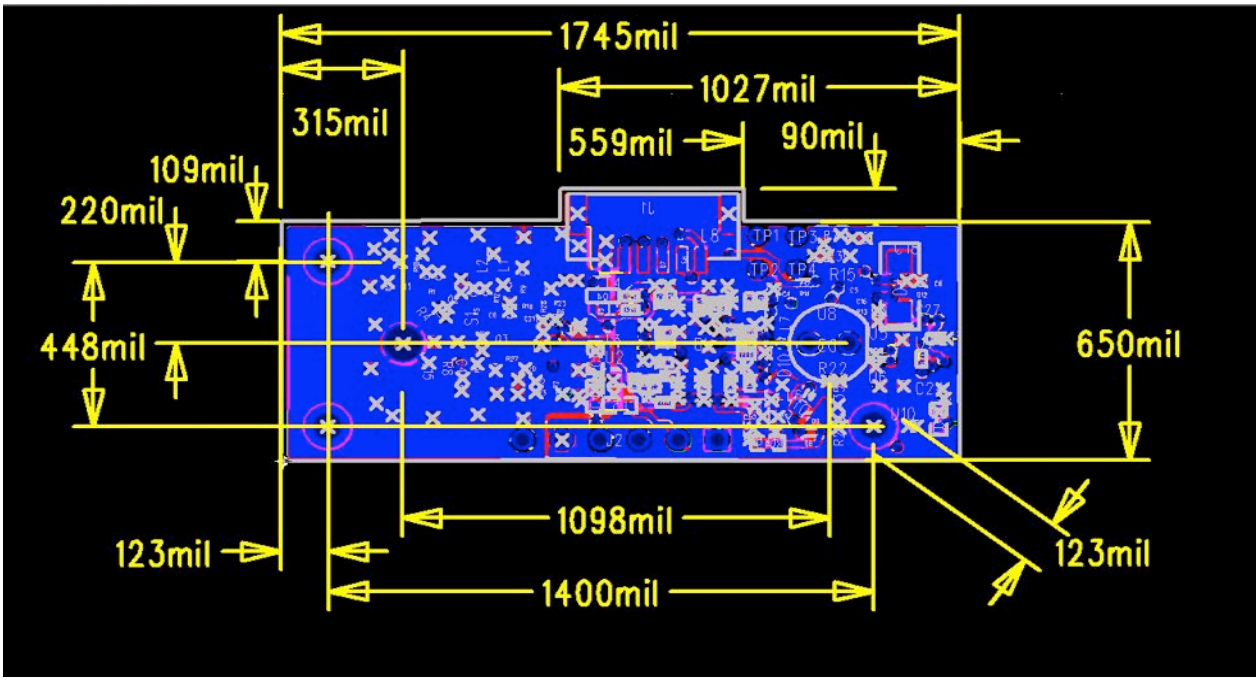
1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address followed by a read/write bit with a zero state indicating a write request. A write operation is used as the initial stage of both read and write transfers. If the slave address corresponds to the module's address the unit responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. An 8 bit data byte following the address loads the I2C control register with the address of the first control register to be read along with flags indicating if auto increment of the addressed control register is desired with successive reads or writes; and if access to the internal micro or external correlation processor register space is requested. Bit locations 5:0 contain the control register address while bit 7 enables the automatic incrementing of control register with successive data blocks. Bit position 6 selects correlation memory external to the microcontroller if set. (Presently an advanced feature)
4. If a read operation is requested, a stop bit is issued by the master at the completion of the first data frame followed by the initiation of a new start condition, slave address with the read bit set (one state). The new address byte is followed by the reading of one or more data bytes succession. After the slave has acknowledged receipt of a valid address, data read operations proceed by the master releasing the I2C data line SDA with continuing clocking of SCL. At the completion of the receipt of a data byte, the master must strobe the acknowledge bit before continuing the read cycle.
5. For a write operation to proceed, Step 3 is followed by one or more 8 bit data blocks with acknowledges provided by the slave at the completion of each successful transfer. At the completion of the transfer cycle a stop condition is issued by the master terminating operation.
6. Note: The unit responds to read or write requests with a NACK when the sensor is busy processing a command or performing a measurement. For proper operation the I2C peripheral driver needs to handle the NACK condition without a producing error condition.

## Module Dimensions



20mm X 48mm X 40 mm (to top of optics)

## PCB Dimensions – (backside viewed through board)



# Overview

## Technology

PulsedLight's "Time-of-flight "distance measurement technology is based on the precise measurement of the time delay between the transmission of an optical signal and its reception. Our patented, high accuracy measurement technique enables distance measurement accuracy down to 1cm by the digitization and averaging of two signals; a reference signal fed from the transmitter prior to the distance measurement and a received signal reflected from the target. The time delay between these two stored signals is estimated through a signal processing approach known as correlation, which effectively provides a signature match between these two closely related signals. Our correlation algorithm accurately calculates the time delay, which is translated into distance based on the known speed-of-light. A benefit of PulsedLight's approach is the efficient averaging of low-level signals enabling the use of relatively low power optical sources, such as LEDs or VCSEL (Vertical-Cavity Surface-Emitting) lasers, for shorter-range applications and increased range capability when using high power optical sources such as pulsed laser diodes.

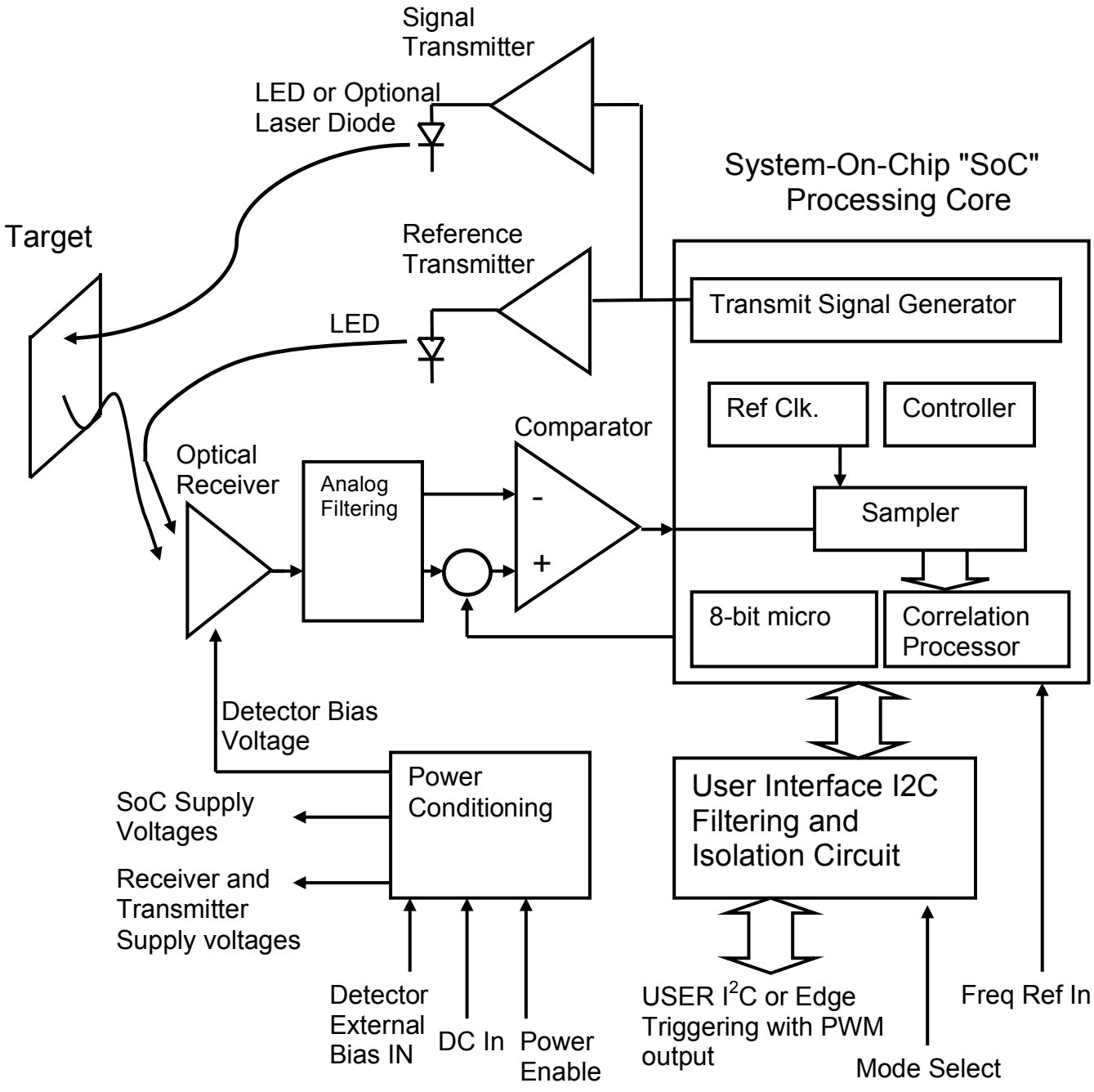
## System Hardware Overview

The Single Board Sensor provides distance and velocity measurements in an ultra-small form factor. This small size is the result of PulsedLight's System-On-Chip (SoC) signal processing technology, which beyond being small reduces the complexity and power consumption of supporting circuitry. The system consists of three key functionalities;

- A Signal Processing Core (SPC) System-on-Chip solution encapsulating all the required functions in support of our proprietary range finding system architecture.
- An optical transmitter and receiver tied to the SPC emit and receive a proprietary optical signal pattern generated by the SPC.
- Power Conditioning and I2C signal filtering and buffering.

Please refer to the following block diagram for a full overview of the system architecture.

## LIDAR-Lite Block Diagram



## Signal Processing Core (SPC)

The key component within the system is our SPC chip which implements PulsedLight's signal processing algorithms and primary system architecture. The SPC contains four major subsystems;

1. An 8-bit microcontroller provides system control and communications. It contains an I2C slave peripheral.
2. A 500 MHz sampling clock and an associated sampler capture the logic state of the external comparator and convert the data into a slower speed 125 MHz four bit word which is sent to a correlation processor.
3. A correlation processor stores the incoming signal and performs a correlation operation against a stored signal reference with optical burst reception and stores the result in the correlation memory with data points every 2 nanoseconds.
4. A transmit signal generator produces an encoded signal waveform with an overall duration of 500ns that consists of a varying interval pattern of ones and zeroes. These outgoing signal pulses occur at a 20 KHz repetition rate and become either the reference signal or outgoing signal pulse depending on the state of the transmitter.

## Optical Transmitter and Receiver

The optical transmitter and receiver have been designed around the requirements of our signal-processing algorithm. The transmitter produces optical pulse bursts using signal patterns generated by the SPC. When an optical reference signal is desired, a separate reference transmitter is enabled and driven with the signal pattern using a reference LED fed to the optical receiver. The reference transmitter has been designed to match the delay and signal shape produced by the higher power signal transmitter. The signal transmitter can drive a variety of optical sources ranging from high speed LEDs, higher power VCSEL laser or much higher power pulsed laser diodes. For the LIDAR-Lite module, the signal transmit driver drives a T1-3/4 plastic packaged laser diode with a three-amp peak, 50% average duty cycle modulation over a burst duration of 500ns. The driver has a capability to drive sources at up to 6 amps using an external DC power supply.

| Parameter | Transmitter specification |
|---|---|
| Bandwidth | 50 MHz, on-off modulation, arbitrary pattern |
| Burst Time/rate | 500nsec/20KHz |
| Typology | High side current source (programmable), low-side differential current steering |
| Reference Channel | 1 amp peak (nominal setting) |
| Signal Channel | 3 amp peak (nominal setting) |
| Transmit Power Control | 16 steps ea. Channel |
| Rise/fall | 4ns |

The receiver incorporates a state-of-the-art low-noise preamplifier that is coupled to either a PIN photodiode or, optionally, an avalanche photodiode (APD). When using the higher performance APD, an external regulated high voltage bias voltage is needed. The APD is used to increased system sensitivity allowing either increased operating range or reduced measurement times. Before reaching the high-speed digital comparator, specialized analog filtering shapes the return signal originating from the output of the preamplifier.

| Parameter | Receiver specification |
|---|---|
| Bandwidth | 50 MHz |
| Detector | PIN diode, 500um by 500um , 1.5pF, 1.8mm diameter lens |
| Virtual Detector size | 1mm – roughly 2X magnification of the package lens |
| Detector Bias Voltage | 8V DC nom. External |
| Preamp Noise Floor | 1pA/Hz-2 |
| Transimpedance Gain | 40K ohm |
| Noise Equivalent Power | 12nW rms |

## Background Light

LIDAR-Lite has been designed to operate effectively under a variety of indoor and bright outdoor solar background lighting conditions. The internal optical absorption filter in combination with the detector spectral response provides a transmission band from 800nm to 1000um. Outdoors, this Spectral window allows roughly 14% of the total solar Irradiance to pass to the detector. Assuming a solar constant of roughly 1Kwatt per meter$^2$, and a full receiver field of view of two degrees, we get the following calculated DC solar current and detector shot noise:

$((1000W/m^2)\ (1/\pi))(.14)(1.1e\text{-}4m^2)(2\pi\ (1\text{-}\cos\ (\alpha/2))\ (.9)$ ... where α is the Receiver FOV in degrees (2 degrees)

RCVR Transmission

Solar radiance off diffuse reflections in W/m$^2$/Srad

14% of solar

Area of RCVR lens in m$^2$

Solid angle of RCVR FOV

**Bright solar optical background** = 6uW
**Solar DC current** = (6e-6 Watts)(.6A/watt) = 3.6e-6 A
**Shot noise** = $((3.6e\text{-}6\ A)(2)(1.6e\text{-}19)(1/Hz))^{1/2}$ = $1pA/Hz^{1/2}$

Under the bright solar conditions and highly reflective diffuse background calculated above, the equivalent receiver input noise floor of 1pA/Hz would increase by a factor of 1.4 resulting in a slight reduction in maximum range. A 20nm spectral width narrow band optical filter is available as a factory option and results in a 10 fold reduction in solar DC current or a $(10)^{1/2}$ = 3 fold decrease in the resulting noise. The narrowband filter is of most benefit in applications where specular, “mirror like” reflective surfaces, are present.

### Power Conditioning

Multiple voltage references are required by various functions on the LIDAR-Lite board. The standard PIN detector requires a DC bias voltage of roughly 8V generated by an internal voltage multiplier. The use of optional APD detector requires a temperature dependent bias from 100V up to 240V depending on the selected detector. This voltage bias is varied based on the temperature compensation coefficient and is applied through the external detector bias input pin. A factory modification is required to allow external application of detector voltages above 30V DC. A 3.7V power supply is used by the receiver circuitry and is enabled by the SPC. Transmitter circuitry typically uses the 5V nominal supply voltage, but can be modified at the factory for an external LED Supply from 5 to 10 Volts DC. By default the LED supply pin is coupled to the 5V input through isolation inductor. An enable pin allows the internal 3.3 V regulator to be disabled allowing very low power consumption under shutdown conditions.

## Operational Overview

Operation of LIDAR-Lite can be separated into two phases; initialization and triggered acquisitions as initiated by the user.

During initialization the microcontroller goes through a self-test sequence followed by initialization of the internal control registers with default values. Internal control registers can be customized by the user through the I2C interface after initialization. After the internal control registers are initialized the processor goes into sleep state reducing overall power consumption to under 10 milliamps. Initiation of a user command, through external trigger or I2C command, awakes a processor allowing subsequent operation.

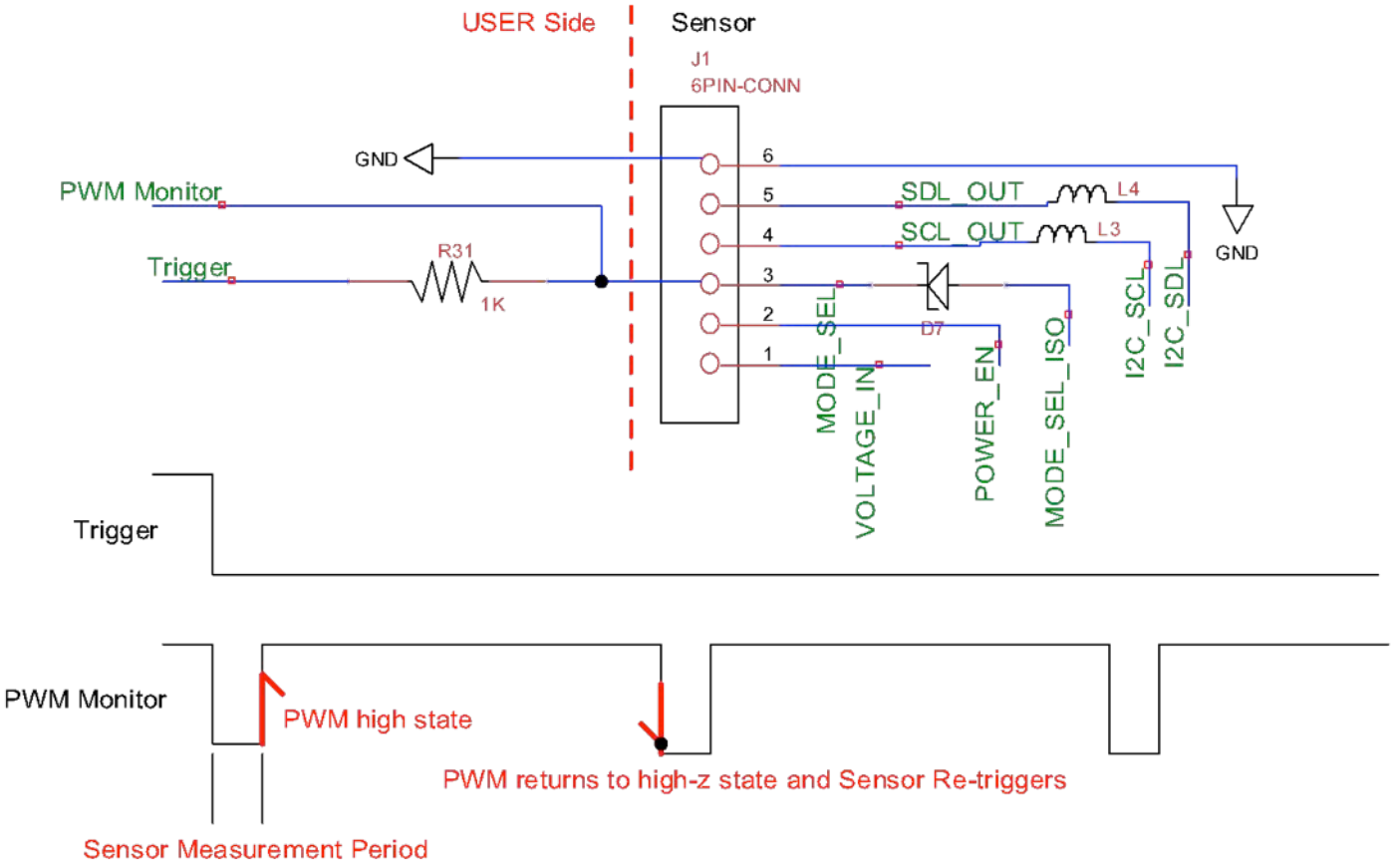
The input of a command through the I2C interfaces may initiate an acquisition or an operation to monitor or modify system parameters. In the event of an acquisition request, the system must first power up and initialize the external functions such as the SPC and transmit/receive circuitry. Acquisition begins with the transmission of a reference burst followed by a signal burst. These signal bursts occur over interval of roughly 50- 100µs depending on the length of the selected correlation record. These signal bursts are repeated until the maximum number of acquisitions have been reached, as defined in the default or user settings or a sufficient number of acquisitions have been performed to achieve a maximum signal strength level. At the completion of the required number of acquisition cycles, the correlation results are processed to calculate the effective time delay of the reference and return within in the correlation records. The total acquisition time for the reference and signal acquisitions is typically between 5 and 20ms depending the desired number of integrated pulses and the length of the correlation record. The acquisition time plus the required 1msec to download measurement parameters establish a roughly 100Hz maximum measurement rate.

### Mode Control Pin

A bi-directional control and status pin provides a means to trigger acquisitions and return the measure distance without having to use the I2C interface.

The pin driver in the processor has an internal current source pull-up of roughly 50uA with the driver output coupled to the user pin through a protection diode allowing only sourcing current into the pin. A low-going transition on the mode control pin will trigger a single measurement, and the pin will be actively pulled high with a pulse width proportional to distance. A 1K to 10K ohm termination resistance will solidly pull the pin low to trigger an acquisition state while allowing the pin to still be pulled high during the PWM output pulse. The pulse width follows a 10usec/cm relationship to the measured distance or 1msec per meter.

A simple trigging method using a standard microcontroller interface uses a 1K ohm resistor in series with an output pin to pull the mode pin low initiating a measurement with a second port pin used to monitor the low-to-high output pulse width. If the pin is held low, the acquisition process will repeat indefinitely producing a variable frequency output proportional to distance.




## Acquisition Settings

Signal acquisition parameters can be easily changed to trade-off system performance parameters. If a high measurement rate is required, then the maximum signal integration time can be reduced to decrease measurement times at the expense of somewhat reduced sensitivity and maximum range. Optical transmit power can be increased by the setting loaded into the Laser Power Register. High pulse power may need to be compensated with an increased spacing between pulse bursts to maintain an acceptable laser duty cycle based on thermal derating requirements. If the length of the correlation record is increased to allow for longer range measurements, increased processing time will decrease the measurement rate.

Key control registers impacting acquisitions

Internal register space -

control_reg [2] – Maximum acquisition count sets the maximum number of acquisition cycles with a maximum value of 255. In most cases an acquisition of 128 is adequate.

control_reg [3] – Correlation record length establishes the portion of correlation memory allocated to the return signal. The value is broken in to upper and lower nibbles where the lower indicates the starting location and the upper nibble the end point. The nibble value multiplied by 64 is its location in memory. A value of 0xf indicates the end of the record with a value of 1024.

control_reg [4] – Acquisition mode control establish the enabled acquisition functions such as velocity measurement, lower power consumption states and inhibiting the reference.

External register space

control_reg [0x43] – Laser power control.

control_reg [0x4b] – Range Processing Criteria for two echoes. Max signal, Max/Min Range.

control_reg [0x65] – Power management – Sleep states.

## Signal Acquisition Process

After loading new acquisition parameters or retaining default values, a command is sent to the SPC to initiate a signal acquisition. The steps of the acquisition are as follows:

1. Power is applied to the receiver preamp and, after a prescribed delay, the DC offset at the threshold detector is adjusted to set the effective slicing level or threshold in the middle of the noise distribution. The adjustment process is based on the measurement of the one/zero duty cycle at the comparator output. When the signal offset is nulled, the duty cycle of the noise pattern approaches an average of 50%. In more sophisticated applications the threshold can be offset as part of an algorithm to measure the approximate rms value of the noise supporting diagnostics or as part of a voltage control feedback signal supporting an avalanche photo detector biasing.

2. Prior to starting signal acquisition, the correlation memory is cleared and the transmitter is activated to generate a burst signal pattern that is stored in a signature memory that is used as key element in the correlation process.

3. Signal acquisition begins with the activation of the reference portion of the transmitter, followed by the feeding of the signal pattern necessary to generate the optical reference signal which then passes directly to the receiver photo detector. After amplification and zero-crossing detection, this record is stored in the signal memory.

4. The stored reference signal record is then correlation processed using the transmit pattern stored in the signature memory as a template which is then added to any correlation data previously processed and residing the reference portion of the correlation memory.

5. Next the signal transmit portion of the transmitter is enabled and the outgoing optical signal goes out to a target and the signal return is amplified, detected and stored in signal memory.

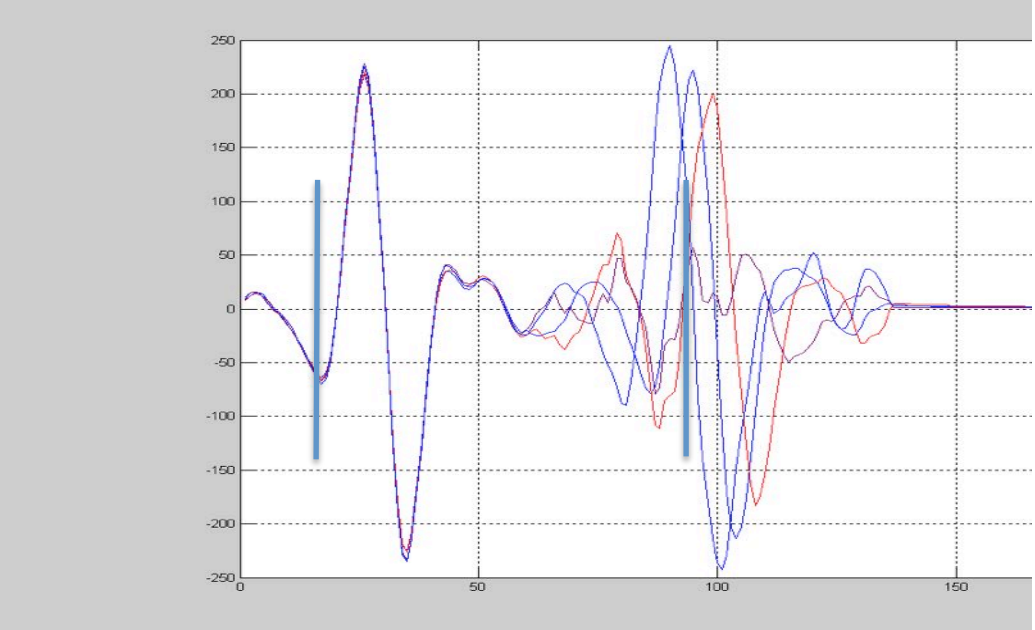
6. As in step 4, the stored signal record is correlation processed and then added to any correlation data previously processed and residing the signal portion of the correlation memory.

7. As the signal and reference acquisitions are repeated, the peak correlation values in the correlation record increase and would ultimately overflow the 12-bit word size. To prevent this overflow condition, the correlation process is terminated for either the signal or reference records when a peak signal within the record exceeds a preset maximum value slightly under overflow. Once both the reference and signal records have reached their maximum values or that maximum acquisition count has been exceeded the acquisition process is terminated.

8. After the signal acquisition process is complete, a low-pass and DC restoring filtering process typically cleans-up the waveform to improve the final measurement accuracy at low signal conditions and short range. This function can be disabled by resetting the filter enable bit in control register 4 for improved accuracy and resolution at longer ranges.

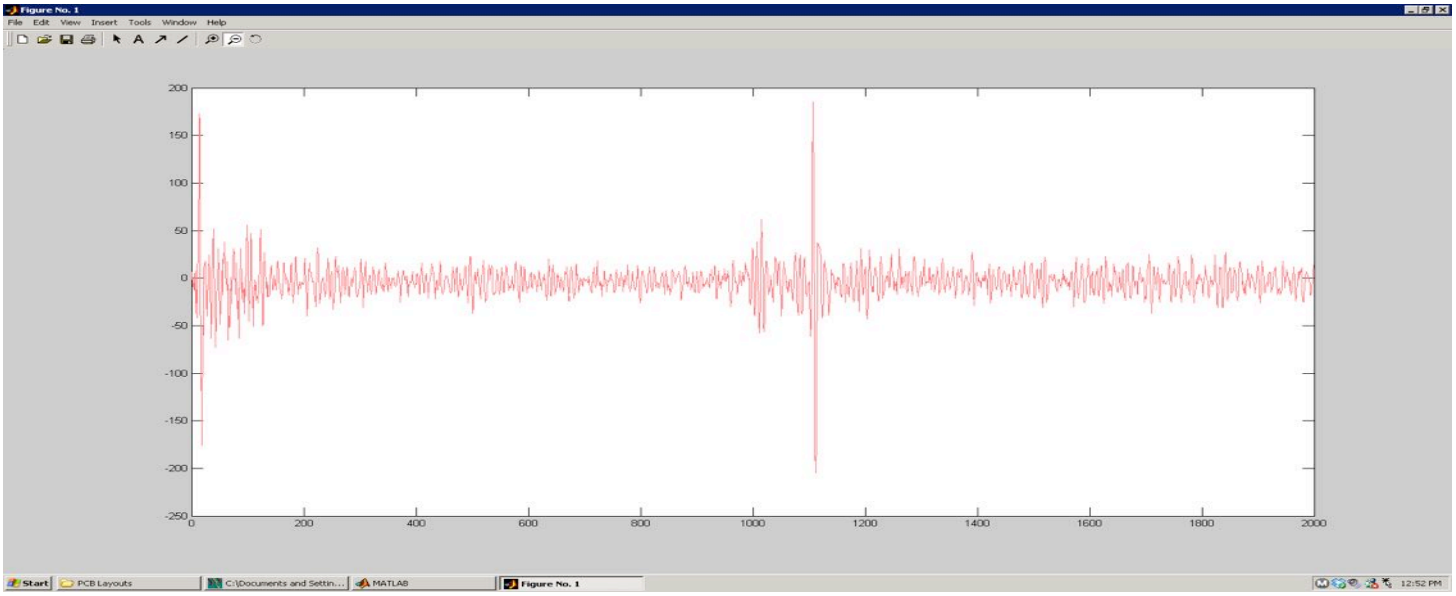
## Correlation Record

Distance measurements are based on the storage and processing of reference and signal correlation records. The figure below shows a correlation record for a sensor without optics at short distances of 0, 4 and 8 feet. The reference record runs from 0-63 and the signal record from 64 to 130. Each sample point represents 2nsec or roughly one foot.

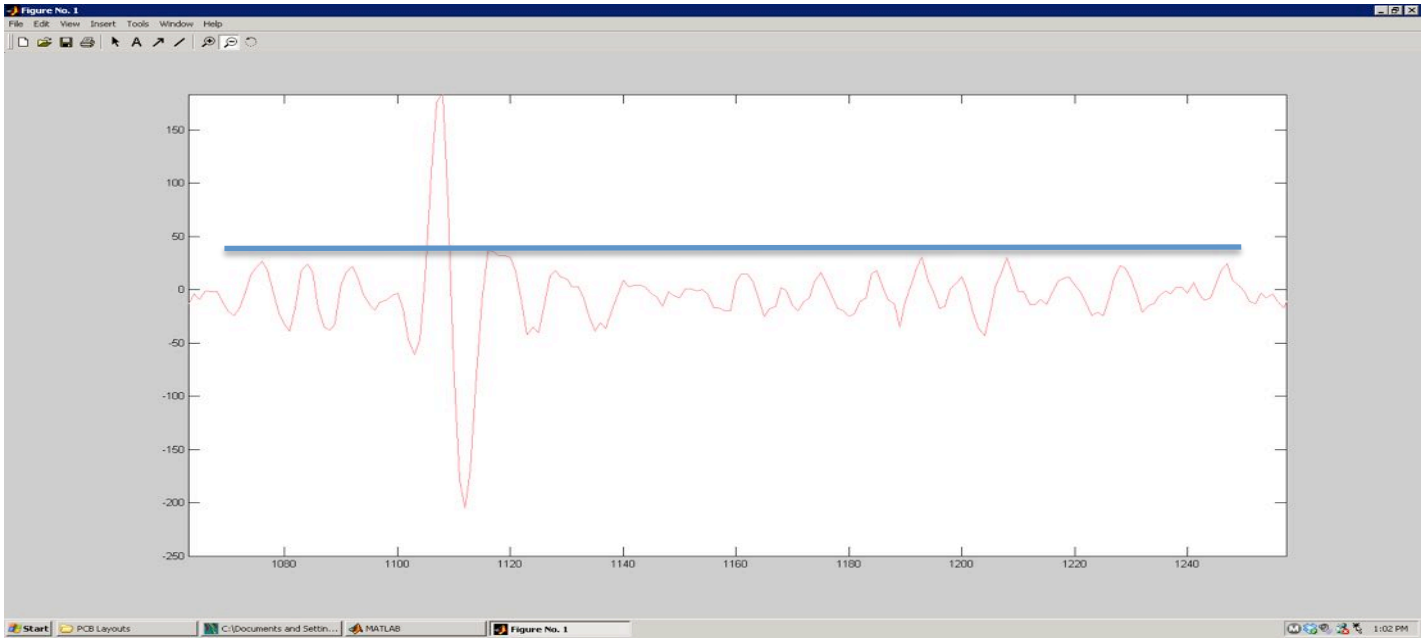



The correlation waveform has a bipolar wave shape, transitioning from a positive going portion to a roughly symmetrical negative going pulse. The point where the signal crosses zero represents the effective delay for the reference and return signals. Processing with the SPC determines the interpolated crossing point to a 1cm resolution along with the peak signal value.

The figure below illustrates a correlation record example for long-range system using an avalanche photodiode or APD and laser with a processing chip with a half resolution 2-foot/correlation steps and two-thousand element signal record. The target is at 660 meters and forms the same bipolar correlation wave shape as in the short-range system, but in practice the correlation waveform must be distinguished from background noise present in the correlation record. A correlation record detection threshold is established based on the background noise and if no signals are detected above this threshold, a no signal status indication is provided.



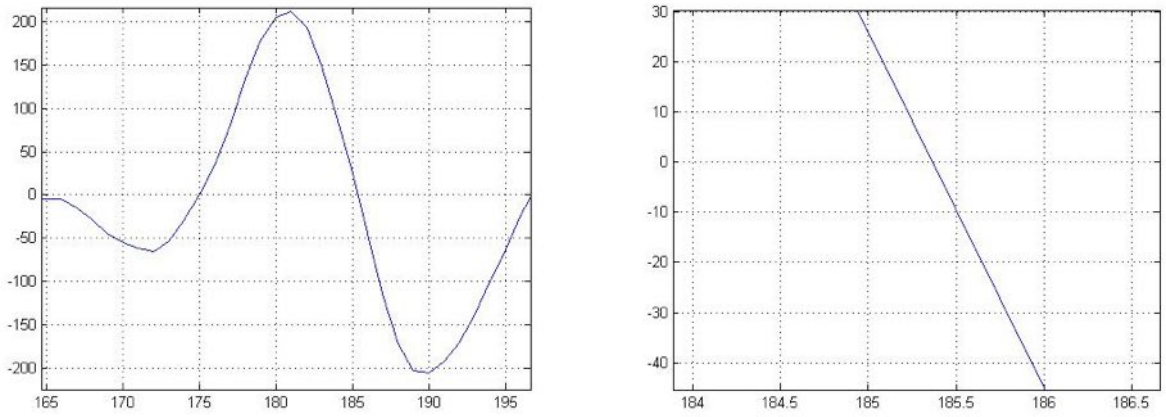

The correlation waveform is shown in more detail below. To distinguish the correlation pulse from the background noise, a specialized processing filter follows the envelope of the noise without being significantly effected by signal correlations present in the record. This noise reference is scaled by 1.25 to provide a detection threshold for the correlation.




If more than one signal is detected within the correlation record, the return with the next highest signal strength is stored and is available for additional processing. A flag within the status register indicates the presence of a valid second reflection such as from a window or from a shorter-range object illuminated by the beam. The on-board processing of secondary returns is limited to weaker target reflections in the foreground. The correlation record can be downloaded by the user to examine target details in post processing.

## Processing the Correlative Pulse

The calculation of the effective delay is based on the course location within the correlation record and the interpolated crossing between sample points. For the full resolution correlation record used in the LIDAR-Lite processor, each sample represents 2nsec in time or roughly one foot or .3 meters. To obtain a result in cm requires 30 resolution points obtained by interpolating between data points. The figure below illustrates a single correlation pulse obtained by processing either the reference or signal.

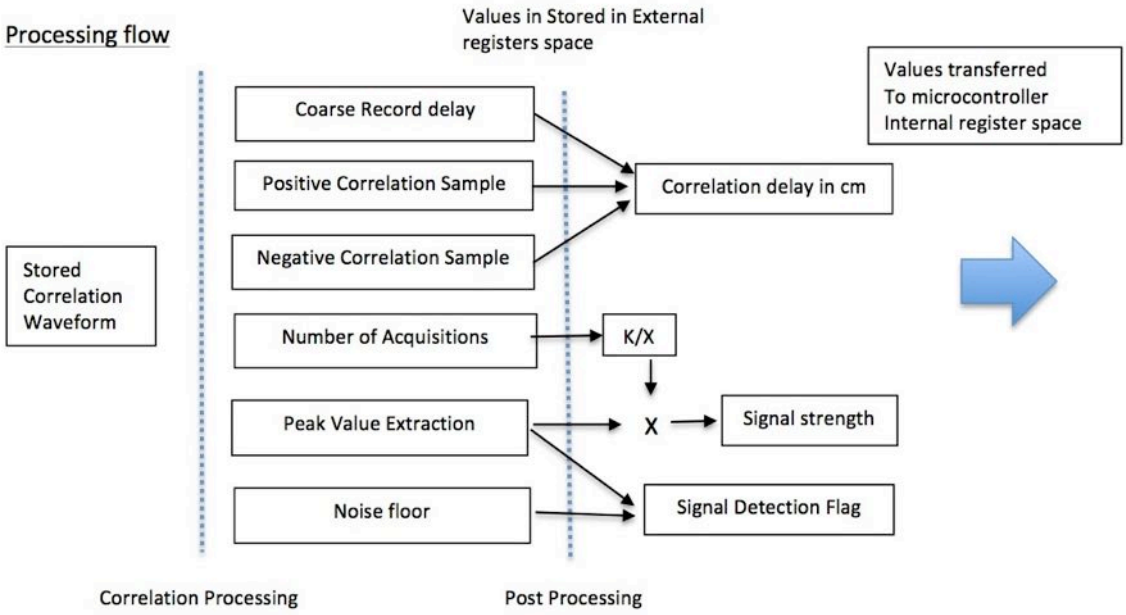



The correlation waveform on the left shows a zero crossing on the falling edge around the location 185. The detail of the crossing on the right shows a linear fit from the upper crossing point at 185 with a value of 26 and a negative value at 106 of 44. The calculation of the crossing is equal to (26/ (26- -44))*30 or 11.14cm.
To get the total delay we multiply the index of the upper point 185 and multiple by 30 to get the course delay in cm. The total delay is then 30*185 +10 = 5550. If we have a delay for the reference waveform, with a crossing at 30*30 +15 or 915cm we get a measured delay of 5550-915 = 46.35 meters.

## Processing

A module within the processor analyses the correlation record looking for the largest peak waveform within the record. As it moves through the record, the crossing characteristics of each new larger peak is sampled. At each peak, the course delay to the positive sample prior to the zero crossing along with correlation values above and below the crossing and the peak value are stored. With each new peak sample, the previous peak and the crossing data (now the next largest peak sample) is stored to allow the post processing the data to extract the distance and peak value. The secondary peak in some cases may be the small reflection of the beam passing through a window or possibly the reflection off objects in the foreground.

The figure below details the processing flow within the correlation processor after a final correlation waveform is complete.




The processed correlation waveform is processed and the various extracted parameters are stored in the external register space. For both the reference and signal records, the course record delay and the positive and negative correlation samples are processed to determine the delay in the record to the correlative peak. The difference between the delay measured for the signal and reference determine the effective round trip delay to the target. The delay is scaled to produce a result in centimeters. Signal strength is determined by multiplying the peak value of the correlation by the scaled inverse of the number of acquisitions. It is an inverse relationship because more samples are required to increase the strength of a small signal than a larger one. A valid signal is determine is determined by comparing the signal peak value with the value of the noise floor observed in the range record.

# Special Topics

## Velocity measurement

A velocity is measured by observing the change in distance over a fixed time period. The default time period is 100msec resulting in a velocity calibration of .1meters/sec. Velocity mode is selected by setting the most significant bit of register 4 to one. When a distance measurement is initiated by writing a 3 or 4 (no dc compensation/or update compensation respectively) to command register 0, two successive distance measurements result with a time delay defined by the loaded value into register at address 0x68.

| Measurement Period (msec) | Velocity Scaling (meters/sec) | Register (0x68) Load Value |
|---|---|---|
| 100 | .1m/s | 0xC8 |
| 40 | .25m/s | 0x50 |
| 20 | .5m/s | 0x28 |
| 10 | 1m/s | 0x14 |

Velocity is output as an 8-bit 2's complement signed value read out from register [0x09]. Velocity is the difference between the last two 16-bit distance measurements. The previous distance measurement used in the velocity calculation is available from registers [0x14] and [0x15] with [14] containing the most significant byte and [15] the least.

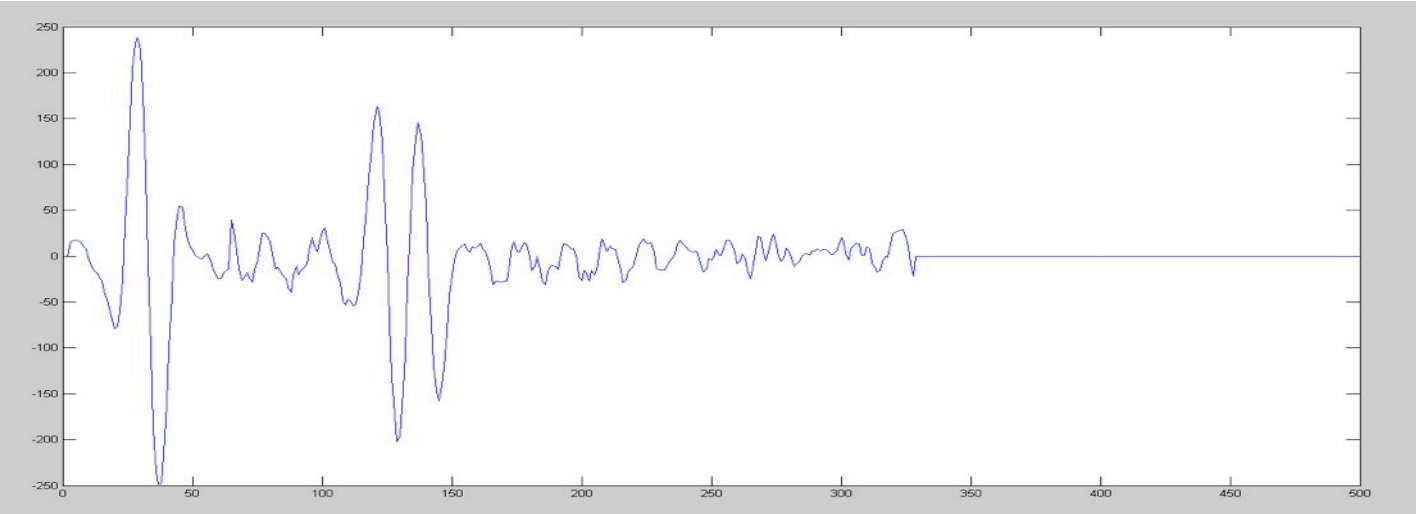
To measure velocity with measurement period less than 20msec, adjustment of the acquisition parameters will likely be necessary. The nominal acquisition is between 10-15msec allowing insufficient time to complete the first velocity acquisition period before starting the second.

Measurement acquisition times can be reduced by the elimination of the reference pulse acquisition and performing the acquisition without a prior DC compensation step. The setting of bit position 6 (adjacent to the velocity mode selection bit) in register [4] suppresses the acquisition of the reference pulse and the loading of 3 into the command register 0 performs an acquisition without the normal DC compensation step. The DC compensation needs to be performed every few seconds when the sensor is first warming up, but once thermally stable compensation can occur at a much slower rate.

## Processing of multiple reflections

It is possible to receive multiple valid return signals from a single measurement if the beam illuminates more than one surface along the beam path. This situation may be encountered when the beam clips or passes through an object in the foreground. Because of the inverse square law behavior of the return signal (double the distance get four times less signal) a very small area illuminated area near the sensor may produce a much stronger signal than that from the desired target. Ranging objects through a window can produce a strong shorter range signal masking the longer target or conversely it may be desirable to detect a window in the foreground that may only produce a small reflective signal relative to a larger distant reflection.

The sensor has the capability to process two distinct reflections as long as they are separated by more than 3.5 meters and the reflection at the shorter distance does not saturate the correlation record masking the more distant object. The "Secondary return" flag in bit position 4 in the status register [1] indicates that a second pulse has been detected. The figure below shows an example of two reflections in the signal correlation record (record address locations greater than 64) separated by approximately 3.5 meters.




The sensor detection criteria may be selected to pick the shorter signal, longer or the strongest strength. In addition, when a second pulse is encountered the other reflection can be read from the system without having to perform a new measurement with different detection criteria. Control register 75, summarized below, sets up the criteria for selection of the desired return when two are present.

| **Control Register #75**(0x4b) (control_reg [75]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | Select Max Range | Select Range Criteria | Select Second Return |

| **Description (Default value is 0x00)** | |
|---|---|
| control_reg[0x4b]: | Range Processing Criteria for two echoes. Max signal, Max/Min Range. |
| Select Second Return | Controls echo processing selection :"1" switches to alternative return; "0" Selects data associated with detection criteria |
| Select Range Criteria | "1" selects return data based on distance; "0" selects strongest return, regardless of distance |
| Select Max Range | "1" selects the longer distance; "0" selects the shorter distance |

The detection criteria is controlled by bit positions 1 and 2. If “Select Range Criteria” is zero, the system will always select the strongest signal present. In this case, regardless of the number of returns, the strongest return will be measured. If “Select Range Criteria” is one, than the longer or shorter valid return will be selected without consideration of relative signal strength. “Select Max Range” selects the longer or shorter return. “Select Second Return” selects the raw data associated with the rejected return pulse allowing the reprocessing of the second data set to extract distance and signal strength.

To reprocess the data “Select Second Return” is set to one without changing the state of bits 1 and 2 of register 75. This followed by sending a value of 1 to the command register [0] initiating a reprocessing of the pulse return data. After reading the second pulse distance data, “Select Second Return” should be set back to zero to return to the desired pulse detection criteria.

## Power Management

Two registers can be used to manage power consumption over the acquisition cycle and during idle time between measurements. Bit positions 0-3 of the Mode Control Register [4] control the power state automatically entered after the completion of an acquisition while Power Control Register [101] sets the present power saving state without requiring a distance measurement. The table below summarizes the control bits of register 4 associated with power management.

| **Control Register #4** (0x04) – Mode Control (control_reg[4]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Velocity | Inhibit Reference | Velocity Scale factor | N/A | DET OFF | FPGA SLEEP | CLK SHUT | Preamp Off |

| **Description** (default 0x00) | |
|---|---|
| Preamp Off | Shutdown preamp between measurements |
| CLK SHUT | External Clock Shutdown – Not used in standard LidarLite |
| FPGA SLEEP | Full FPGA sleep after measurement |
| DET OFF | Turns off detector bias after measurement |

| **Control Register #101** (0x65) (control_reg [101]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | Det Bias Disable | SLEEP | RCVR PWR Disable | OSC Disable |

| **Description** (default 0x00) | |
|---|---|
| control_reg[65]: | Power control (write only) |
| OSC Disable | Disables oscillator reference – Not used in LidarLite SPC |
| RCVR PWR Disable | Turns on receiver regulator – decreases power consumption by 30mA when inhibited |
| SLEEP | Processor sleep – Reduces power to 20mA with other hardware disabled (wakes on I2C transaction) Send dummy prior to any command or register access operation. |
| Det Bias Disable | Turns off detector bias charge pump |

At the completion of a normal distance measurement or at the completion of the two measurements associated with a velocity measurement, the first 4 bits of register 4 are loaded into Power Control register 101. Loading values into register 101 results in immediate action execution. The loading of power control register occurs after completion of the reading of the lower byte of the distance measurement register 16. When pulling data from the unit after a measurement, read all other registers before reading register 16. Placing the FPGA into a sleep state results in shutting down of all internal clocks making the internal registers unavailable until the system is waken. The system will automatically wake from the sleep state if a read operation is initiated using the I2C interface. A dummy read command should be sent to the unit to wake it, followed after roughly 10msec with the desired read or write command. A measurement initiated by a write to command register 0 will return the system to full power operation prior to a measurement, followed by a return to a sleep state afterwards. Depending on the bit status various degrees of power savings are possible, however larger power savings increased the time necessary for the system to return to normal operation.

| Power Saving Mode | Savings | Wake-up Time |
|---|---|---|
| Nominal Power Draw | 80mA | |
| Preamp off | 30mA | 2msec |
| Clock Disable | 10mA | 1msec |
| FPGA Sleep | 40mA | 10msec |
| Det. Off | 1mA | 1msec |

**Summary**

**Preamp off**: Shutting down the preamp shuts disables the 3.7V regulator supporting the preamplifier circuitry. The power is stable in 1- 2msec after re-enabling after shutdown. The advantage for powering down the preamp between measurements is reduced power consumption and less thermal rise above ambient temperature when operating at low pulse rates 1-10 Hz.

**Clock Disable**: Is not used in the LIDAR-Lite product. On high performance long range product a crystal oscillator reference in included on the circuit board

**FPGA Sleep**: Disables the phase lock loop based internal clock, resulting in the shutdown of all the internal circuitry, except for I2C interface. The I2C interface still monitors buss activity and when its address is detected it initiates the activation of the internal clock. The wake-up time is necessary for the PLL to re-lock on its internal frequency reference.

**Detector Off**: Shuts off the on-board charge-pump generating the 8V bias to the photodiode. Disabling the charge-pump has negligible impact on power consumption, however it eliminates the last of the periodic potential noise sources on the board.

## Downloading a Correlation Record

The following details simplified C-code routine to download three types of record stored in the system memory. The first selection is a memory bank where the last correlation template pattern is stored. The last received signal record stored is in bank 2 while bank 3 stores the full correlation record. See detailed descriptions of the accessed control registers in Appendix A for a detailed explanation of their function.

Note: Only external registers are accessed using this command and the correlation processor cannot be in a sleep state.

**Sample C Code - Download Correlation Data to a Serial Port Using Put**

This pseudo code can be used as a basis for the download of correlation data for analysis.

bank_num – memory banks in the correlation processor
1: template memory
2: last signal record
3: correlation record
Function - write_twi (register address (hex), value);
Function - read_twi (register address (hex), number of bytes)
Elements – number of words to be transferred
read_val is 16 bit integer

```
 if (bank_num == 3)   write_twi (0x51, 0x10);  //  points to the base of the correlation record address
 write_twi (0x53, (char) (bank_num <<6));       // selects memory bank
 write_twi (0x40, 0x06);   //sets test mode select
For (i=0; i<elements; i++) {
    read_val = (unsigned char) read_twi (0x52, 1); // added to select single byte
   if (read_twi (0x5d, 1)) read_val |= 0xff00; // if upper byte lsb is set, the value is negative
   put_dec (read_val);
   T0_Wait_ms (1); //hold longer than the transfer time for the serial transfer.
  }
write_twi (0x40, 0x00); // return to normal control – null command to control register
```

# Appendix A - Control Registers

## Overview

The rangefinder configured using an I2C machine interface. Settings control the acquisition and processing of ranging data. The I2C interface supports a transfer rate up to 100kb per second. Control Registers are divided between "internal" u/P registers and "external" registers residing in Correlation processor. The internal registers are mapped to register addresses from 0 to 15 hex and external registers from 40 to 68 hex. Internal registers are both read and write, while external registers are read or write only. The most signal bit of the address byte in the I2C 2nd byte triggers the auto incrementing of register addresses with successive register reads or writes within an I2C block transfer.

## µP internal Control Registers

control_reg [0x0] – Command Control

control_reg [0x1] –Status – system status.

control_reg [0x2] – Maximum acquisition count

control_reg [0x3] – Correlation record length setting

control_reg [0x4] – Acquisition mode control

control_reg [0x5] – Measured threshold offset during acquisition

control_reg [0x6-7] – Measured delay of reference in correlation record

control_reg [0x8] – Reference correlation measured peak value

control_reg [0x9] – Velocity Measurement Output

control_reg [0xa-b] – Measured delay of signal return in correlation record

control_reg [0xc] – Signal correlation measured peak value

control_reg [0xd] – Correlation record noise floor * 1.25 (for setting valid signal threshold)

control_reg [0xe] – Received signal strength (typical range 10 min - 128 maximum)

control_reg [0xf-10] – Calculated distance in cm (difference between signal and reference delay)

control_reg [0x11] – DC threshold command value

control_reg [0x12] – Added delay to reduce signal acquisition burst frequency

control_reg [0x13] – Distance calibration. Signed 8 bit value adds or subtracts from distance

control_reg [0x14-15] – Previous measured distance

## Correlation Core External Control Registers

control_reg [0x40] – Command register

control_reg [0x41] – Hardware Version

control_reg [0x42] – Preamp DC control

control_reg [0x43] – Transmit power control

control_reg [0x44] – Processing range gate (low byte)

control_reg [0x45] – Processing range gate (high byte)

control_reg [0x46] – Range Measurement PWM output pin bit[0] used

control_reg [0x47] – Acquisition status

control_reg [0x49] – Measured preamp DC offset

control_reg [0x4a] – Output port

control_reg [0x4b] – Range Processing Criteria for two echoes. Max signal, Max/Min Range.

control_reg [0x4c] – 2$^{nd}$ largest detected peak in signal correlation record.

control_reg [0x4f] – Software Version.

control_reg [0x51] – Correlation record size select – (reference and signal return)

control_reg [0x52] – Correlation Data access port (low byte)

control_reg [0x53] – Acquisition Settings – selects ext. memory access, signal record select

control_reg [0x57-8] – Measured delay of reference or signal in correlation window

control_reg [0x59] – Correlation peak value of reference or signal

control_reg [0x5a] – Correlation record noise floor * 1.25 (for setting valid signal threshold)

control_reg [0x5b] – Received signal strength (typical range 10min -255 maximum)

control_reg [0x5c] – Reset correlator / increment transmit signal pattern

control_reg [0x5d] – Correlation Data access port (sign bit)

control_reg [0x5e] – Clock synchronizer control

control_reg [0x5f] – Measured transmit power – Supports Laser safety monitoring

control_reg [0x60] – Measured fine delay (used as part of measured delay calculation)

control_reg [0x61-62] – Coarse delay (used as part of measured delay calculation)

control_reg [0x63] – Positive correlation sample before zero crossing (correlation pulse falling edge)

control_reg [0x64] – Negative correlation sample after zero crossing (correlation pulse falling edge)

control_reg [0x65] – Power control settings

control_reg [0x68] – Velocity measurement window setting register

## Detailed Register Descriptions – Internal

| **Control Register #0** (0x00) (control_reg[0]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x00]: | Command register | | | | | | |
| | 0: Reset FPGA. Re-loads FPGA from internal Flash memory – all registers return to default values | | | | | | |
| | 1: Correlation processing without new acquisition – used to process delay of second peak after bit 0 in control register 0x4b is set to 1 | | | | | | |
| | 2: Process correlation without new acquisition – used to reprocess | | | | | | |
| | 3: Take acquisition& correlation processing without DC correction | | | | | | |
| | 4: Take acquisition & correlation processing with DC correction | | | | | | |

| **Control Register #1** (0x01) - Mode/Status (control_reg[1]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Eye Safe | External Trigger Complete | Velocity complete | Secondary return | Signal not valid | Sig overflow flag | Ref overflow flag | Health |
| **Description** | | | | | | | |
| Health* | "1" state indicates that all health monitoring criteria were met on the last acquisition. "0" possible problem | | | | | | |
| Ref overflow flag | Overflow detected in correlation process associated with a reference acquisition | | | | | | |
| Sig overflow flag | Overflow detected in correlation process associated with a signal acquisition | | | | | | |
| Signal not valid | Indicates that the signal correlation peak is equal to or below correlation record noise threshold | | | | | | |
| Secondary return | Secondary return detected above correlation noise floor threshold | | | | | | |
| Velocity complete | Velocity measurement completed | | | | | | |
| External trigger complete | External measurement performed | | | | | | |
| Eye Safe | This bit will go high if eye-safety protection has been activated | | | | | | |

*Health status indicates that the preamp is operating properly, transmit power is active and a reference pulse has been processed and has be stored.

| **Control Register #2** (0x02) (control_reg[2]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| (default 0x80) | | | | | | | |
| **Description** | | | | | | | |
| control_reg[2]: | Maximum Acquisition Count - 0-255. Control the FPGA maximum signal integration time. Stronger signal results in reduced acquisition count to prevent internal register overflow. Sig overflow flag and Ref overflow flag in control register 1 are set when automatic limiting occurs. | | | | | | |
| | | | | | | | |

| **Control Register #3**(0x03) (control_reg [3]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Stop address (default 5 corresponding to 512) | | | | Start address (default 1 corresponding to 64) | | | |
| **Description** | | | | | | | |
| control_reg[0x51]: | Correlation start and stop locations used for signal acquisition (write only) | | | | | | |
| Start address | Value in the range from 0x00-0x0f – starting point in correlation record (record broken into 64 element segments 1024 total | | | | | | |
| Stop address | Value in the range from 0x00-0x0f – stopping point in correlation record | | | | | | |

Note: With longer correlation records, burst pulse period is roughly proportional to the length of the correlation record. Unnecessarily long record length increases the probability of false detections.

| **Control Register #4** (0x04) – Mode Control (control_reg[4]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Velocity | Inhibit Reference | Velocity Scale factor | N/A | DET OFF | FPGA SLEEP | CLK SHUT | Preamp Off |
| **Description** | | | | | | | |
| (default 0x00) | | | | | | | |
| Preamp Off | Shutdown preamp between measurements | | | | | | |
| CLK SHUT | External Clock Shutdown – Not used in standard LidarLite | | | | | | |
| FPGA SLEEP | Full FPGA sleep after measurement | | | | | | |
| DET OFF | Turns off detector bias after measurement | | | | | | |
| N/A | Note used presently | | | | | | |
| Velocity Scale factor | "1" sets the velocity measurement separation to 10msec resulting in a velocity calibration in meters/sec. A "0" value results in a measurement separation of 100msec. | | | | | | |
| Inhibit Reference | If "1" inhibits the acquisition of reference pulses reducing measurement times and reducing measurement variations at the expense of decreasing accuracy over time. "0" allows normal operation | | | | | | |
| Velocity | Enable velocity measurement | | | | | | |

| **Control Register #5** (0x05) (control_reg[5]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| (nominal 128) | | | | | | | |
| **Description** | | | | | | | |
| control_reg[5]: | Measured DC value out of correlation sampler input. Value based on the ratio of 1's and 0's (read only) preamp – Parameter used as part of health flag criteria | | | | | | |
| | | | | | | | |

| **Control Register #6** (0x06) (control_reg [6]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[6]: | High byte of calculated delay of reference– calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #7** (0x07) (control_reg [7]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[7]: | low byte of calculated delay of reference– calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #8** (0x08) (control_reg [8]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[8]: | Correlation Peak value reference (scaled to 0 – 0xff max peak value) - (read only) | | | | | | |
| | – Parameter used as part of health flag criteria | | | | | | |

| **Control Register #9** (0x09) (control_reg [9]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[9]: | Velocity in .1 meters/sec - (read only , 8 bit signed value) See Mode control, Register 4 for information on changing the scale factor to 1m/sec | | | | | | |
| | | | | | | | |

| **Control Register #10**(0x0a) (control_reg [10]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[10]: | High byte of calculated delay of signal correlation – calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #11** (0x0b) (control_reg [11]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg11]: | low byte of calculated delay of signal correlation – calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #12** (0x0c) (control_reg [12]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[12]: | Correlation Peak value of signal correlation (scaled to 0 – 0xff max peak value) - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #13** (0x0d) (control_reg [13]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[13]: | Maximum noise within correlation record scaled by 1.25 (typically between 0x10 – 0x30 - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #14** (0x0e) (control_reg [14]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[14]: | Calculated signal strength - (read only) | | | | | | |
| | Note: calculation based on the number of averaged samples and correlation peak value | | | | | | |

| **Control Register #15**(0x0f) (control_reg [15]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg15]: | high byte of calculated delay of signal - reference – calculated after correlation record processing - (read only) | | | | | | |
| | Note: if the MSB is 1 then the reading is not considered valid. | | | | | | |

| **Control Register #16** (0x10) (control_reg [16]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg16]: | low byte of calculated delay of signal - reference – calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #17** (0x11) (control_reg [17]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[17]: | Register shows the required DC compensation command value to maintain zero crossing offset at preamp – Parameter used as part of health flag criteria | | | | | | |
| | | | | | | | |

| **Control Register #18** (0x12) (control_reg [18]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[18]: | Added delay between signal bursts – Used to lower transmission duty cycle and pulse frequency (write only) | | | | | | |
| | | | | | | | |

| **Control Register #19** (0x13) (control_reg [19]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| (default values 10 for laser products, 0 for led) | | | | | | | |
| control_reg[19]: | Distance Calibration value. The value is added to measured distance. 8bit signed value allows increasing or decreasing the measured value. | | | | | | |
| | | | | | | | |

| **Control Register #20**(0x14) (control_reg [20]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg120]: | Previous high byte of calculated delay of signal - reference - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #21** (0x15) (control_reg [21]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg21]: | Previous low byte of calculated delay of signal - reference - (read only) | | | | | | |
| | | | | | | | |

## Detailed Register Descriptions -External

| **Control Register #64** (0x40) - Command Control (control_reg[64]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | bit2 | bit1 | bit0 |
| **Description** | | | | | | | |
| Bit 0…Bit 2 | Starting action address | | | | | | |
| Bit3 | Store template pattern enable | | | | | | |
| Bit4 | Signal acquisition enable | | | | | | |
| Bit5 | Clear Correlation memory | | | | | | |
| Bit6 | Perform Correlation process | | | | | | |
| Bit7 | Perform Delay calculation Processing | | | | | | |

| Bits 0 through 2 Definitions | |
|---|---|
| **Value** | **Description** |
| 000 | No Operation |
| 001 | Start processes at template store |
| 010 | Start processes at signal acquisition |
| 011 | Start processes at clear correlation memory |
| 100 | Start processes at Perform Correlation process |
| 101 | Start processes at Delay calculation Processing |
| 110 | Perform only memory bank access enable |
| 111 | Perform only correlation record filtering |

Command control register - Writing to this register through the I2C interface immediately initiates a command operation. Thus it is important to initiate this command only at the completion of defining other registers.

| **Control Register #65** (0x41) (control_reg[65]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x41]: | Hardware Version | | | | | | |
| | laser units revisions begin with 0x01 (short range ) , 0x20 for long range lasers, and Led units begin with 0x40 | | | | | | |

| **Control Register #66** (0x42) (control_reg[66]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x42]: | Preamp DC control 0-255 – used in DC compensation servo loop | | | | | | |
| | | | | | | | |

| **Control Register #67** (0x43) (control_reg[67]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Ref led power level control 0x0-0xf | | | | Signal laser or led power level control 0x0-0xf | | | |
| **Description** | | | | | | | |
| (Default – 0x69h) | | | | | | | |
| control_reg[0x43]: | Transmit power control, Led/Laser drive control bits (7 through 4) ref, bits (3 through 0) signal. | | | | | | |
| | | | | | | | |

**Note:** Maximum value set at factory 1amp LED and 3amps Laser product. The maximum output power of the optical source is set through a factory selected resistor which limits available current to the transmit source. When using laser devices, which have a much higher operating current, do not increase the reference control level beyond the factory settings. Increasing the reference control level may cause premature failure of the internal LED reference diode.

| **Control Register #68** (0x44) (control_reg[68]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x44]: | Processing range gate (low byte) – sets the staring location for range processing in the correlation | | | | | | |
| | | | | | | | |

| **Control Register #69** (0x45) (control_reg[69]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x44]: | Processing range gate (high byte) | | | | | | |
| | | | | | | | |

| **Control Register #70**(0x46) (control_reg [70]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | PWM bit |
| **Description** | | | | | | | |
| PWM bit | Single bit passed from microcontroller PWM output. High at mode pin returns pulse width proportional distance | | | | | | |
| | | | | | | | |

| **Control Register #71** (0x47) - Mode/Status (control_reg[71]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Eye safe | Signal Invalid | Timestamp | Second Peak | PIN Status | Sig Overflow | Ref Overflow | Busy |
| **Description** | | | | | | | |
| Busy | Busy, indicates that the processor is actively performing an acquisition process. | | | | | | |
| Ref Overflow | Overflow detected in correlation process associated with the reference acquisition | | | | | | |
| Sig Overflow | Overflow detected in correlation process associated with a signal acquisition | | | | | | |
| PIN Status | Indicates the state of the Mode Select external pin. De-bounced, masked from output signals, inverted | | | | | | |
| Second Peak | Indicates a second peak was detected. 2nd peak value compared to noise floor | | | | | | |
| Timestamp | Active between velocity measurement pairs | | | | | | |
| Signal Invalid | Signal Invalid – “1” No signal detected, “0’ signal detected | | | | | | |
| Eye safe | Indicates that eye safety average power limit has been exceeded and power reduction is in place | | | | | | |

| **Control Register #73**(0x49) (control_reg [73]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x49]: | Measured DC value out of correlation sampler input. Value based on the ratio of 1's and 0's (read only) | | | | | | |
| | | | | | | | |

| **Control Register #74**(0x4a) (control_reg [74]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | Busy flag | Detector sel | Preamp gain | xmt 1 en | xmt 1 en |
| **Description** | | | | | | | |
| control_reg[0x49]: | Output port (write only) | | | | | | |
| xmt 1 en | Enables transmit channel 1 high-side current source | | | | | | |
| xmt 2 en | Enables transmit channel 2 high-side current source | | | | | | |
| Preamp gain | Selects high 2x or low gain 1x setting – not used in laser lite product | | | | | | |
| Detector sel | Select receiver detector 1 or 2 – not used in laser lite product | | | | | | |
| Busy flag | Busy flag outputs on mode select pin with I2C initiated acquisition. High causes pin output to be driven low | | | | | | |

| **Control Register #75**(0x4b) (control_reg [75]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | Select Max Range | Select Range Criteria | Select Second Return |
| **Description (Default value is 0x00)** | | | | | | | |
| control_reg[0x4b]: | Range Processing Criteria for two echoes. Max signal, Max/Min Range. | | | | | | |
| Select Second Return | Controls echo processing selection :"1" switches to alternative return; "0" Selects data associated with detection criteria | | | | | | |
| Select Range Criteria | "1" selects return data based on distance; "0" selects strongest return, regardless of distance | | | | | | |
| Select Max Range | "1" selects the longer distance; "0" selects the shorter distance | | | | | | |

| **Control Register #75**(0x4c) (control_reg [76]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x4c]: | Peak Value of 2nd largest pulse in the signal correlation record (read only) | | | | | | |
| | | | | | | | |

| **Control Register #79** (0x4f) (control_reg[79]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[0x41]: | Software Version | | | | | | |
| | laser units revisions begin with 0x01 (short range ) , 0x20 for long range lasers, and Led units begin with 0x40 | | | | | | |

| **Control Register #81**(0x51) (control_reg [81]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Stop address | | | | Start address | | | |
| **Description** | | | | | | | |
| control_reg[0x51]: | Correlation start and stop locations (write only) | | | | | | |
| Start address | Value in the range from 0x00-0x0f – starting point in correlation record ( record broken into 64 element segments 1024 total | | | | | | |
| Stop address | Value in the range from 0x00-0x0f – stopping point in correlation record | | | | | | |

| **Control Register #82** (0x52) (control_reg [82]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[52]: | Data from memory records. Template memory, Signal memory or Correlation memory ( low byte of 9 bit value) read only) | | | | | | |
| | | | | | | | |

| **Control Register #83**(0x53) (control_reg [83]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Memory bank | | n/a | n/a | n/a | Signal stop | Signal start | Reset xmt pattern |
| **Description** | | | | | | | |
| control_reg[0x53]: | Acquisition and control settings (write only) | | | | | | |
| Reset xmt pattern | Resets rotating transmit pattern to base state | | | | | | |
| Signal start | 0: starts signal acquisition at zero in signal memory 1: starts at location 64 – 8 single bit samples per location | | | | | | |
| Signal stop | 0: stops signal acquisition at 63 in signal memory 1: stops at location 256 – 8 single bit samples per location | | | | | | |
| Memory bank | 0:n/a 1: template memory selected, 2: signal memory selected, 3: correlation memory selected. | | | | | | |

| **Control Register #87** (0x57) (control_reg [87]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[57]: | High byte of calculated delay of reference or signal return – calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #88** (0x58) (control_reg [88]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[58]: | Low byte of calculated delay of reference or signal return – calculated after correlation record processing - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #89** (0x59) (control_reg [89]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[59]: | Correlation Peak value reference or return ( scaled to 0 – 0xff max peak value) - (read only) | | | | | | |
| | - Used in both signal strength calculation and stored in the appropriate uP control register | | | | | | |

| **Control Register #90** (0x5a) (control_reg [90]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[5a]: | Maximum noise within correlation record scaled by 1.25 ( typically between 0x10 – 0x30 - (read only) | | | | | | |
| | | | | | | | |

| **Control Register #91** (0x5b) (control_reg [91]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[5b]: | Calculated signal strength - (read only) | | | | | | |
| | Note: calculation based on the number of averaged samples and correlation peak value | | | | | | |

| **Control Register #92** (0x5c) (control_reg [92]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | Reset Peak Det | Inc xmt pattern |
| **Description** | | | | | | | |
| control_reg[5c]: | Reset - (write only) | | | | | | |
| | Soft reset of system always occurs with write to register. FPGA Core reset – any write to this register | | | | | | |
| Inc xmt pattern | Increments transmit pattern to next in sequence | | | | | | |
| Reset Peak Det | Resets peak detectors used to process the correlation record | | | | | | |

| **Control Register #93** (0x5d) (control_reg [93]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | sign |
| **Description** | | | | | | | |
| control_reg[5d]: | Correlation sign bit - MSB of 9 bit signed result (read only) | | | | | | |
| sign | Most significant bit of signed correlation value | | | | | | |

| **Control Register #93** (0x5f) (control_reg [95]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[5f]: | Measured transmit power – using internal power monitor (read only) | | | | | | |

| **Control Register #96** (0x60) (control_reg [96]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[60]: | Fine delay - Interpolated fine delay (0-29) (read only) | | | | | | |
| | | | | | | | |

| **Control Register #97** (0x61) (control_reg [97]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[61]: | Peak Index high byte (read only) – course crossing point in the correlation record prior to zero crossing | | | | | | |
| | | | | | | | |

| **Control Register #98** (0x62) (control_reg [98]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[62]: | Peak Index low byte (read only) – course crossing point in the correlation record prior to zero crossing | | | | | | |
| | | | | | | | |

| **Control Register #99** (0x63) (control_reg [99]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[63]: | Positive crossing - Upper correlation pulse data value prior to zero crossing – used to interpolate fine delay | | | | | | |
| | | | | | | | |

| **Control Register #100** (0x64) (control_reg [100]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | | | | |
| **Description** | | | | | | | |
| control_reg[64]: | Negative crossing - Lower correlation pulse data value after zero crossing – used to interpolate fine delay | | | | | | |

| **Control Register #101** (0x65) (control_reg [101]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | | Det Bias Disable | SLEEP | RCVR PWR Disable | OSC Disable |
| **Description** | | | | | | | |
| control_reg[65]: | Power control (write only) | | | | | | |
| OSC Disable | Disables oscillator reference – Not used in LidarLite SPC | | | | | | |
| RCVR PWR Disable | Turns on receiver regulator – decreases power consumption by 30mA when inhibited | | | | | | |
| SLEEP | Processor sleep – Reduces power to 10mA with other hardware disabled (wakes on I2C transaction) Send dummy prior to any command or register access operation. | | | | | | |
| Det Bias Disable | Turns off detector bias charge pump | | | | | | |

| **Control Register #104** (0x68) (control_reg [104]:) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | | INTERPULSE SPACING | | | | |
| **Description** | | | | | | | |
| control_reg[68]: | Velocity measurement period setting | | | | | | |
| INTERPULSE SPACING | Five bit value defining the velocity interpulse spacing. 4msec/step | | | | | | |
| | 0xc8 : gives 100msec pulse separation for .1m/sec velocity register calibration value | | | | | | |
| | 0x14 : gives 10msec pulse separation for 1m/sec velocity register calibration value | | | | | | |