IB980

Intel ® 4th Generation Core / Q87 PCH
PICMG 1.3 SHB Express Full-Size CPU Card

USER'S MANUAL

Version 1.0

Acknowledgments

Table of Contents

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Introduction

Product Description

The IB980 PICMG1.3 SHB is based on the latest Intel® Q87 chipset. The platform supports 4th Generation Intel® Core processor family with LGA1150 packing and features an integrated dual-channel DDR3 memory controller as well as a graphics core.

Made with 22-nanometer technology, the latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The IB980 PICMG1.3 board utilizes the dramatic increase in performance provided Intel's latest cutting-edge technology. Measuring 338mm x122mm, the IB980 offers fast 6Gbps SATA support (6 ports), USB3.0 (4 ports) and interfaces for DVI-D, VGA and LVDS displays.

IB980 FEATURES:

- Supports Intel® 4th Generation Core i7/i5/i3 QC/DC desktop processors
- Two DDR3 DIMM, 1066/1333/1600MHz, Max. 16GB memory
- Dual Intel® PCI-Express Gigabit LAN
- Integrated graphics for VGA, DVI-D & LVDS displays
- 6x SATA 3.0, 10x USB 2.0, USB 3.0 (4 ports), 4x COM, Watchdog timer

Checklist

Your IB980 package should include the items listed below.

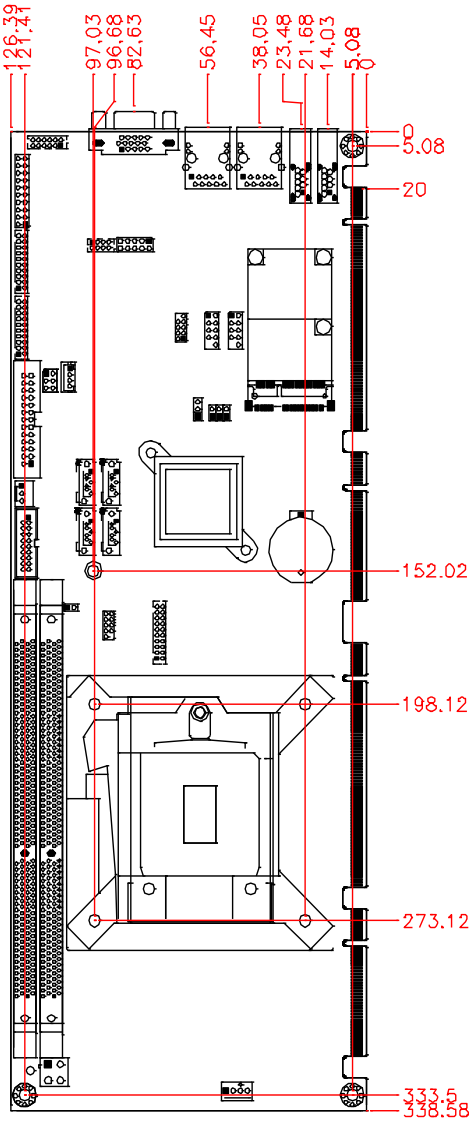
- The IB980 PICMG1.3 SHB
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Serial ATA cable

IB980 Specifications

Product Name	**IB980AF (Support LVDS & iAMT)** **IB980F (w/o LVDS, not support iAMT)**
Form Factor	PICMG 1.3 SHB Express Full size CPU card
CPU Type	- 4th Generation Intel® Core™ i7/i5/i3/Pentium DT processor - FCLGA1150 package [37.5 mm x 37.5mm] - TDP: QC=84W/45W ; DC=54W/35W
CPU Speed	Up to 4.0 GHz
Cache	Up to 8MB
BIOS	AMI BIOS
CPU Socket	LGA1150
Chipset	Intel® Lynx Point DT Platform Controller Hub, Q87 PCH Package =23 mm x 22 mm, 0.65 mm ball pitch
Memory	4th Generation Intel® Core™ i7/i5/i3 DT processor integrated memory controller, support dual channel DDR3-1333/1600 MHz (Non-ECC) - DDR3 240-pin DIMM x 2, Max. **16GB [8GB in per DIMM]**
VGA	4th Generation Intel® Core™ i7/i5/i3 DT processor integrated graphics device - 1x VGA [Support to 1920x1080@60Hz] - 1x DVI-D: (Thru port C, Reserve level shifter) [Support to 1920x1200@60Hz] - 1x LVDS (Thru port B, via NXP PTN3460), support 24-bit dual channel [Support to 1920x1200@60Hz]
LAN	1. Intel® I217LM GbE PHY (For IB980AF, support iAMT) Intel® I217V GbE PHY (For IB980F) 2. Intel® I211AT as 2nd GbE
USB	USB 2.0 host controller [Q87 Integrated], support 10 ports - 4 ports via onboard pin header - 1 port via Mini PCIe **4 ports on board, 4 ports to the backplane [Connector C]** USB 3.0 host controller [Q87 integrated] support 4 ports - 2 ports via the rear panel I/O - 2 ports via on board pin header [BLUE color box header]
Serial ATA Ports	Intel® Lynx Point Desktop PCH built-in SATA controller, support 6 ports 4x SATAIII (3.0) 6Gbps **2 ports to the backplane [Connector C]**
Audio	Intel® Q87 PCH built-in high definition audio w/ Realtek ALC662 Codec support 5.1 channel
LPC I/O	Fintek F81846AD-I (128-pin LQFP[14mm x 14 mm]) - COM #1 (RS232/422/485) support ring-in with power @500 mA (selectable for 5V or 12V) [EXAR SP339EER1 232/422/485 transceiver x 1 for jumper-less] - COM #2~COM #4 (RS232 only) Hardware Monitor (2 thermal inputs,4 voltage monitor inputs & 2 Fan headers) - CPU FAN x 1(PWM Fan type, 4-pin connector) - SYS FAN x 1 (DC Fan type, 3-pin connector)] - Supports parallel port
Digital IO	4 in & 4 out
Keyboard Mouse/ Connector	Supports PS/2 Keyboard/Mouse thru onboard pin-header
Expansion Slots	Mini PCIe socket x1@ component side [Full-sized] Support USB client & mSATA [share with onboard SATA] Support PCIe signal
Edge Connector	DB15 x1 for VGA RJ45 x 2 for LAN 1 & 2 USB 3.0 x 2

Onboard Header /Connector	DF11-20 pins pin-header x 2 for DVI-D x **1** DF20-20pins box-header x 2 for dual channel LVDS (IB980AF) 1 x 4 pins box header x 1 for LCD backlight control (IB980AF) 2x13 pins box-header x 1 for Printer port DF11-20 pins box-header x1 for COM1/2 DF11-20 pins box-header x1 for COM3/4 2x5 pins pin-header x **2** for USB 2.0 x 4 2x10 pins box-header x **1** for USB3.0 x 2 2x6 pins pin-header x1 for Audio (Line-Out, Line-In & Mic) 2x5 pins pin-header x 1 for Digital I/O 2x4 pins pin-header x 1 for PS/2 KB/MS 4 pins pin-header x1 for CPU fan (PWM mode) 3 pins pin-header x1 for system fan (DC mode) 4 ports x SATAIII (Blue connectors) 2X10 pins pin-header x 1 for front panel indicators 2 x 2 pin ATX power connector x 1
Interface	1x PCIe(16x) [Connector A & B] 4x PCIe(1x) **or** 1x PCIe(4x) [Connector C] 4x PCI masters (ITE IT8892E PCIe to PCI bridge, 14mm x 14mm LQFP128) [Connector D]
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
iSMART ver. 3.0	1. EuP / ErP(thru Super I/O) 2. Auto-scheduler 3. Power fail detector 4. Low temperature Guardian 5. IFUB (Intelligent Firmware Update from BIOS & NVRAM data)
Others	- RAID function (0, 1, 5, 10) - iAMT 9.0 - LAN wake up - TPM 1.2 (Infineon SLB9655) supported
Environment	Operation Temperature: 0~60 degree C Storage Temperature: -20~80 degree C Relative humidity: 0~90%, non-condensing
System Voltage	+5V, +3.3V, +12V, -12V & 5VSB
Operation System	Windows 7, Windows 8
Certification	CE /FCC/LVD
RoHS	Yes
Board Size	338mm x 126mm

Board Dimensions



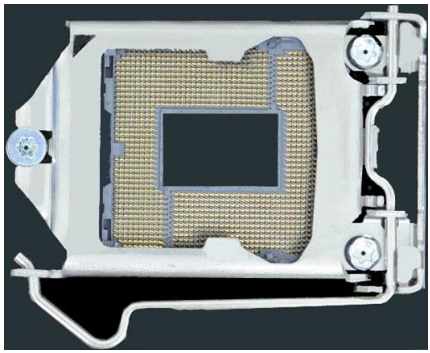
Installations

This section provides information on how to use the jumpers and connectors on the IB980 in order to set up a workable system. The topics covered are:

Installing the CPU

The IB980 board supports an LGA1150 Socket (shown below) for Intel Sandy Bridge processors.

To install the CPU, unlock first the socket by pressing the lever sideways, then lift it up to a 90-degree. Then, position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle. Carefully insert the CPU into the socket and push down the lever to secure the CPU. Then, install the heat sink and fan.



***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

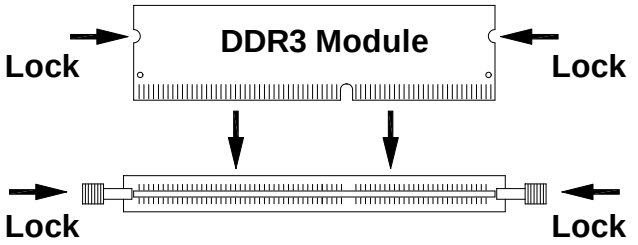
Installing the Memory

The IB980 board supports four DDR3 memory socket for a maximum total memory of 16GB in DDR3 DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

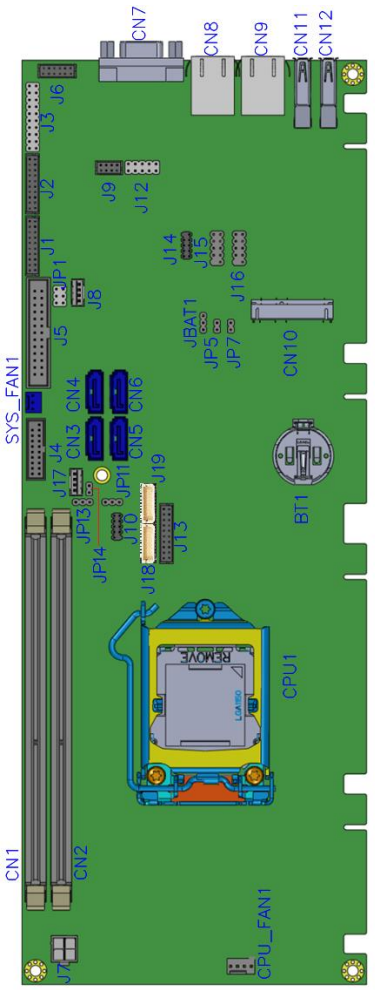
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



Setting the Jumpers

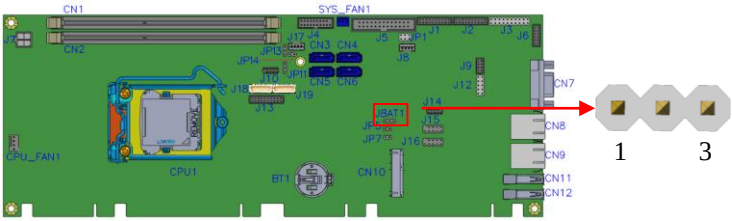
Jumpers are used on IB980 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB980 and their respective functions.

Jumper Locations on IB980

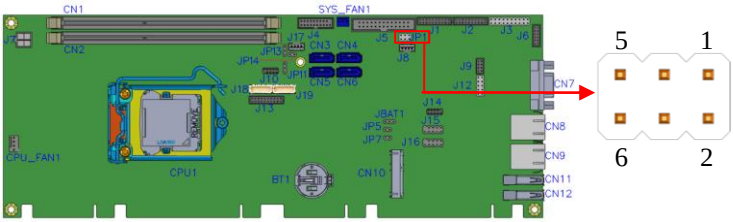


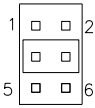
JBAT1: Clear CMOS Contents

JBAT1	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

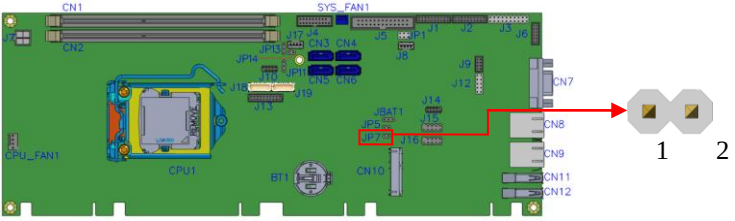


JP1: COM1 RS232 RI/+5V/+12V Power Setting



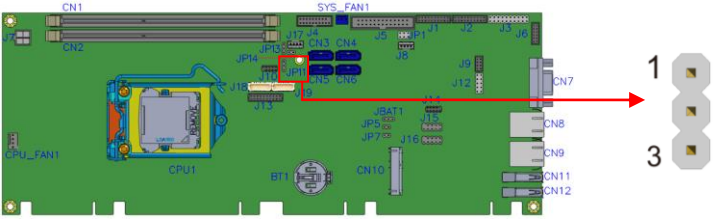
JP1	Setting	Function
	Pin 1-3 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-3 Short/Closed	+5V

JP7: Flash Descriptor Security Override (Factory use only)



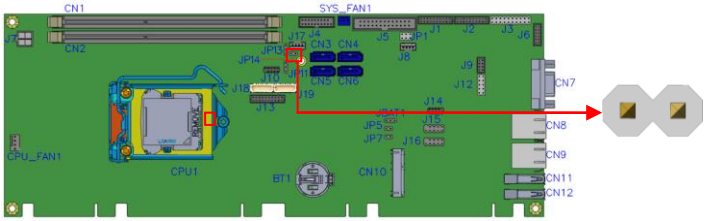
JP7	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

JP11: LVDS Panel Power Selection



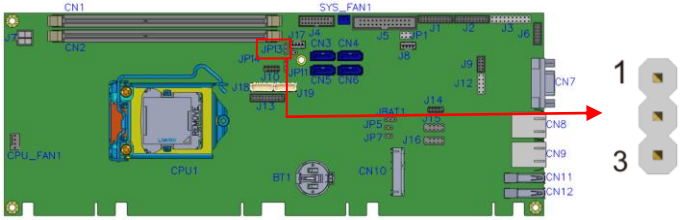
JP11	Setting	Panel Voltage
	Pin 1-2 Short/Closed	3.3V (default)
	Pin 2-3 Short/Closed	5V

JP14: BL_ADJ_LEVEL Setting



JP14	Function
Open	3.3V(default)
Close	5V

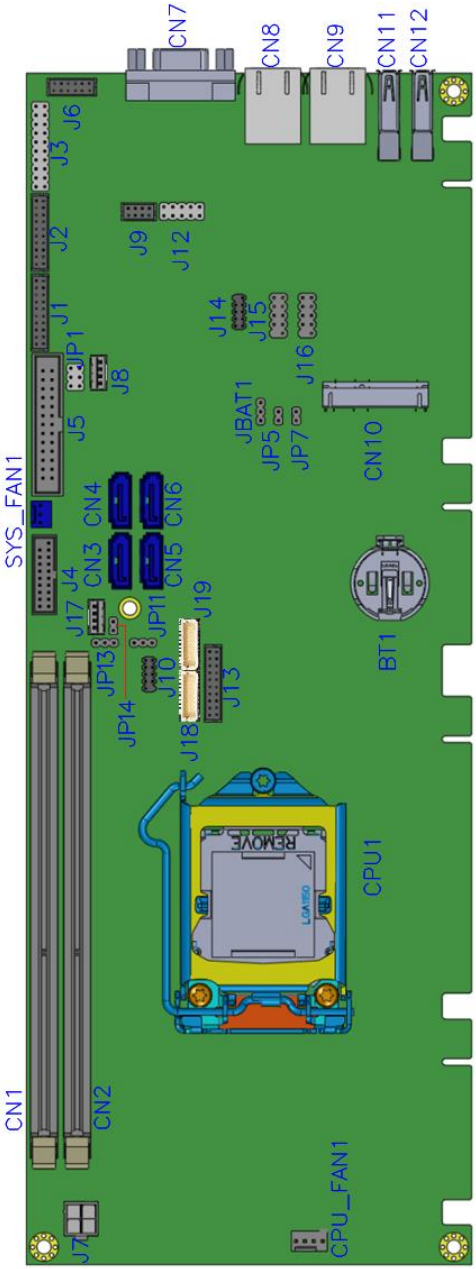
JP13: BL Voltage TYPE Setting



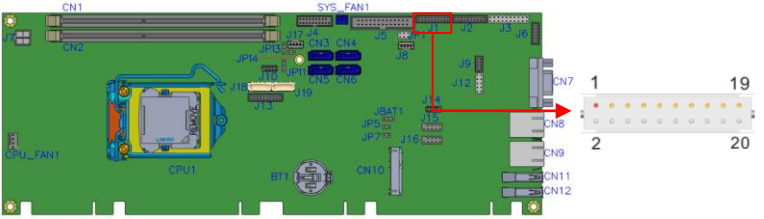
JP13	Setting	Function
	Pin 1-2 Short/Closed	DC Mode
	Pin 2-3 Short/Closed	PWM Mode

Connectors on IB980

Connector Locations on IB980

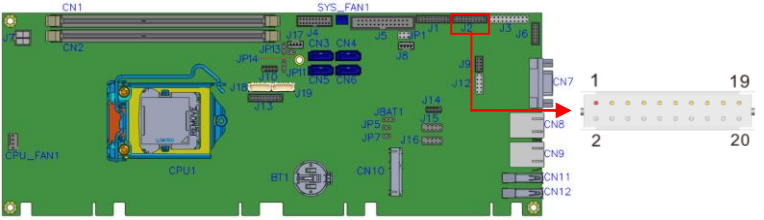


J1: COM1 and COM2 Serial Port [HRS_DF11-20DP-2DSA(08)]



Signal Name	Pin #	Pin #	Signal Name
DSR1	2	1	DCD1
RTS1	4	3	RXD1
CTS1	6	5	TXD1
RI1	8	7	DTR1
NC	10	9	Ground
DSR2	12	11	DCD2
RTS2	14	13	RXD2
CTS2	16	15	TXD2
RI2	18	17	DTR2
NC	20	19	Ground

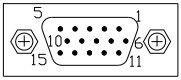
J2: COM3, COM4 Serial Port [HRS_DF11-20DP-2DSA(08)]



Signal Name	Pin #	Pin #	Signal Name
DSR3	2	1	DCD3
RTS3	4	3	RXD3
CTS3	6	5	TXD3
RI3	8	7	DTR3
NC	10	9	Ground
DSR4	12	11	DCD4
RTS4	14	13	RXD4
CTS4	16	15	TXD4
RI4	18	17	DTR4
NC	20	19	Ground

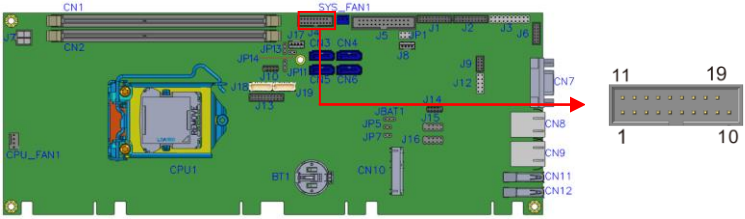
CN3, CN4, CN5, CN6: SATA3 Connectors

CN7: DB-15 VGA Connector



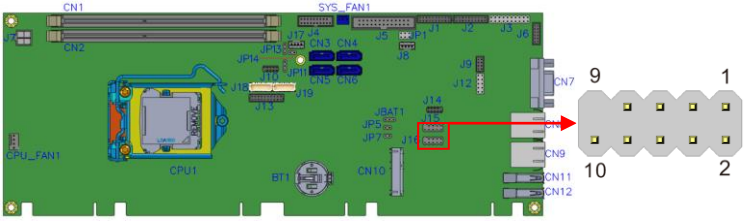
Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
VCC	9	10	GND
N.C.	11	12	DDCDATA
HSYNC	13	14	VSYNC
DDCCLK	15		

J4: USB3.0/2.0 Connector [PINREX_52X-40-20GU52]



Signal Name	Pin #	Pin #	Signal Name
VCC(900mA)	1	X	
P1_SSRX-	2	19	VCC(900mA)
P1_SSRX+	3	18	P2_SSRX-
GND	4	17	P2_SSRX+
P1_SSTX-	5	16	GND
P1_SSTX+	6	15	P2_SSTX-
GND	7	14	P2_SSTX+
P1_U2_D-	8	13	GND
P1_U2_D+	9	12	P2_U2_D-
NC	10	11	P2_U2_D+

J15,J16: USB2.0 Connectors

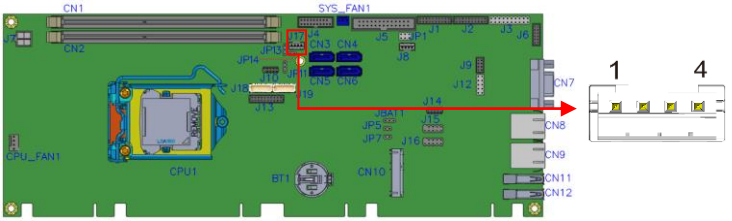


Signal Name	Pin #	Pin #	Signal Name
VCC(500mA)	1	2	VCC(500mA)
D0-	3	4	D1-
D0+	5	6	D1+
Ground	7	8	Ground
KEY	9	10	NC

CN8: Gigabit LAN (Intel I211AT) Connector

CN9: Gigabit LAN (Intel I217LM) Connector

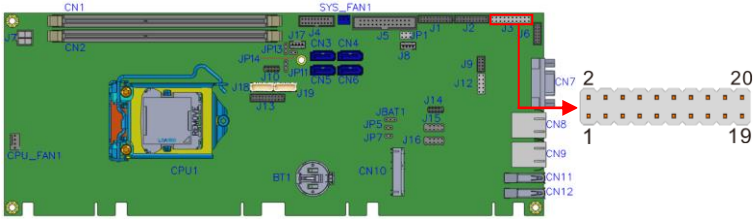
J17: LCD Backlight Connector [E-CALL_0110-161-040]



Pin #	Signal Name
1	Backlight Power +12V(2A)
2	Backlight Enable
3	Backlight Control
4	Ground

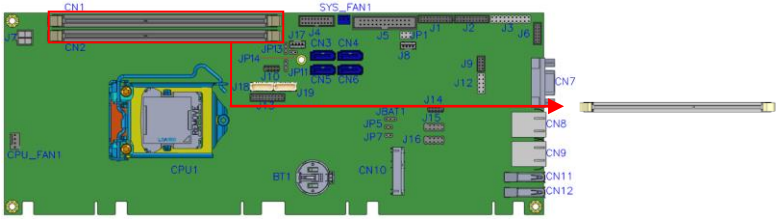
CN11, CN12: USB3.0 Connectors

J3: Front Panel Function Connector



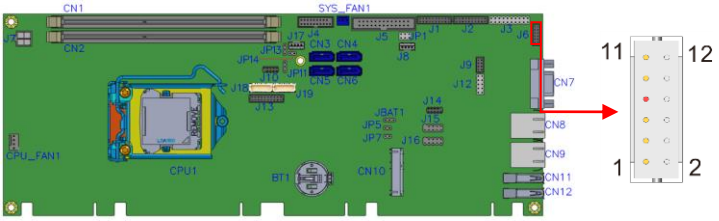
Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	Speaker Out
NC	3	4	NC
Ground	5	6	Ground
NC	7	8	VCC
Ground	9	10	NC
Ground	11	12	NC
Ground	13	14	PWR_SW
NC	15	16	NC
Ground	17	18	RST
HDD LED +	19	20	HDD LED -

CN1,CN2: DDR3 DIMM Socket



J6: External Audio Connector [HK_DF11-12S-PA66H]

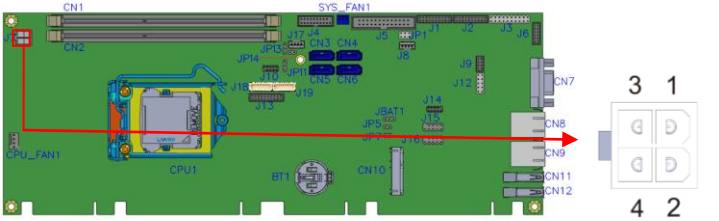
J6 is a 12-pin header that is used to connect to the optional audio cable.



Signal Name	Pin #	Pin #	Signal Name
LINE OUT_R	2	1	LINE OUT_L
Ground	4	3	JD_FRONT
LINE IN_R	6	5	LINE IN_L
Ground	8	7	JD_LINE IN
MIC-R	10	9	MIC-L
Ground	12	11	JD_MIC1

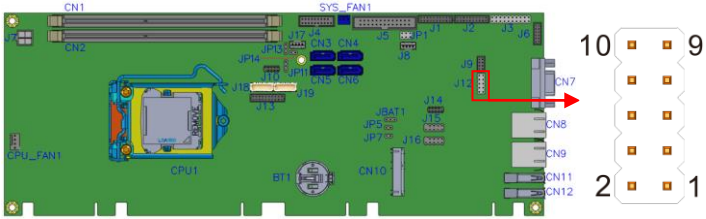
J7: ATX 12V Power Connector [Win Win_WPO-04D4TN431UW]

This connector supplies the CPU operating voltage.



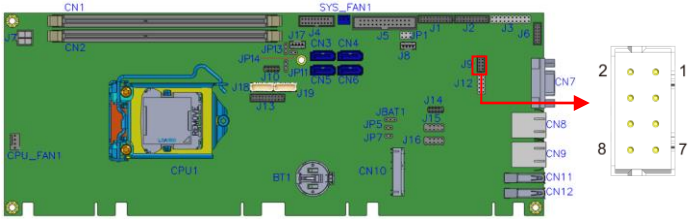
Pin #	Signal Name
1	Ground
2	Ground
3	+12V-IN
4	+12V-IN

J12: Digital I/O 4 In/4 Out



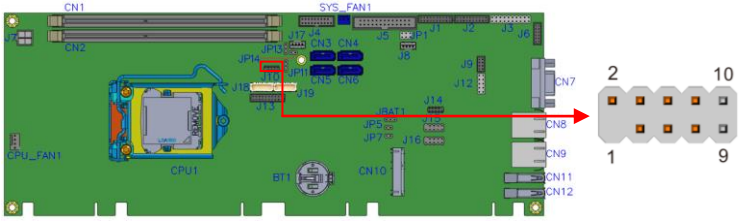
Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J9: PS/2 Keyboard and Mouse Connectors [HK_DF11-8S-PA66H]

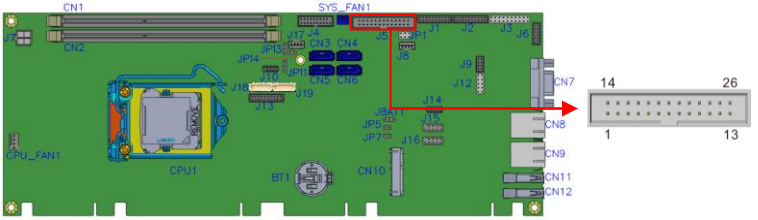


Signal Name	Pin #	Pin #	Signal Name
VCC(300mA)	2	1	VCC(300mA)
KB_DATA	4	3	MS_DATA
KB_CLK	6	5	MS_CLK
Ground	8	7	Ground

J10: SPI Flash Connector (Factory use only)

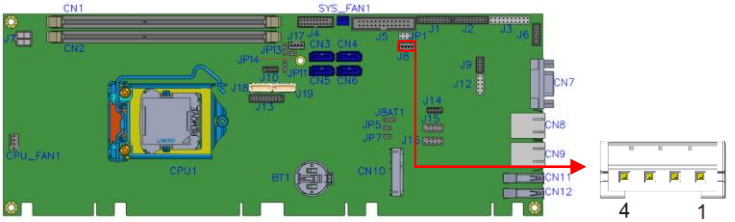


J5: Parallel Port [Win Win F-WBOX-26RN]



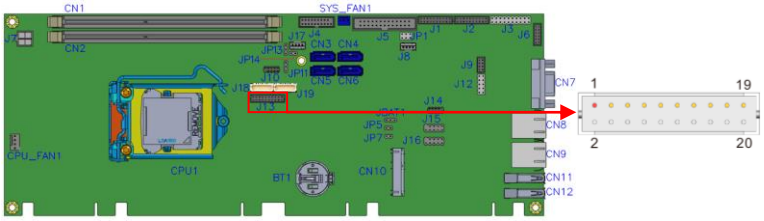
Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	Auto Feed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	26	Ground

J8: MCU Flash Connector (factory use only)



J13: DVI-D Port [HK_DF11-20S-PA66H]

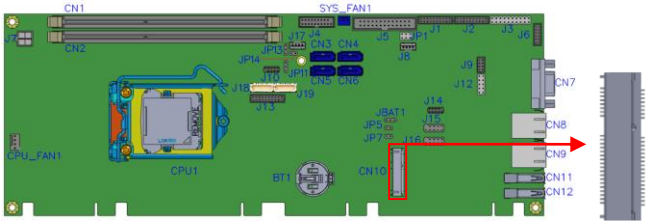
J13 is a 20-pin header that is used to connect to the optional DVI-D cable.



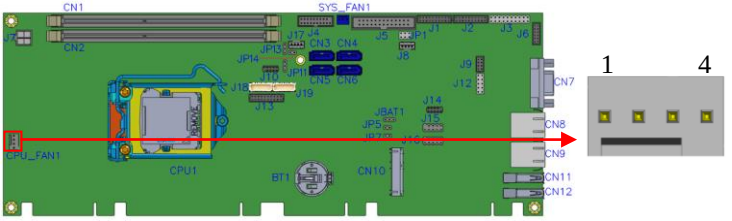
Signal Name	Pin #	Pin #	Signal Name
TDC1#_B	2	1	TDC1_B
Ground	4	3	Ground
TLC#_B	6	5	TLC_B
5V	8	7	Ground
N.C.	10	9	HPDET_B
TDC2#_B	12	11	TDC2_B
Ground	14	13	Ground
TDC0#_B	16	15	TDC0_B
N.C.	18	17	N.C.
SC_DDC_B	20	19	SD_DDC_B

CN10: Mini PCIE Connector (Support M-SATA with CN5)

CN10 also supports mSATA. However, when CN10 is used for mSATA, then CN5 SATA port cannot be used. Only one of them can be used at one time to support SATA.

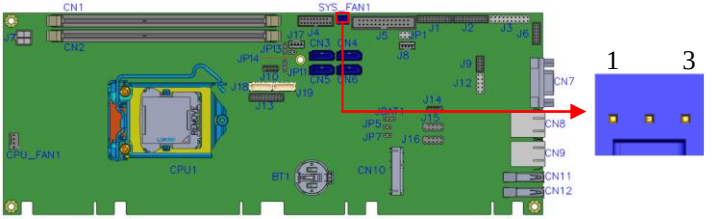


CPU_FAN1: CPU Fan Power Connector



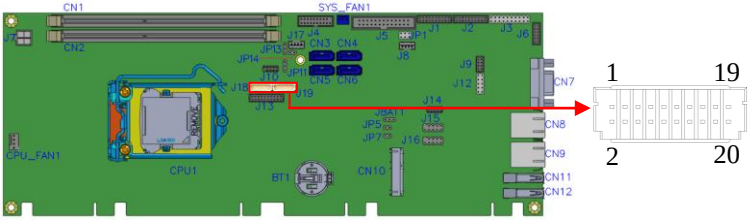
Pin #	Signal Name
1	Ground
2	+12V(1A)
3	Rotation detection
4	Control

SYS_FAN1: System Fan1 Power Connector



Pin #	Signal Name
1	Ground
2	+12V(1A)
3	Rotation detection

J18, J19: LVDS Connectors [HIROSE_DF20G-20DP-1V(56)]



Signal Name	Pin #	Pin #	Signal Name
LCD_PWR(1A)	19	20	LCD_PWR(1A)
LD3+	17	18	LD3-
GND	15	16	GND
CLK+	13	14	CLK-
GND	11	12	GND
LD2+	9	10	LD2-
GND	7	8	GND
LD1+	5	6	LD1-
GND	3	4	GND
LD0+	1	2	LD0-

J18(Odd Bus), J19(Even Bus)

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BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also has password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

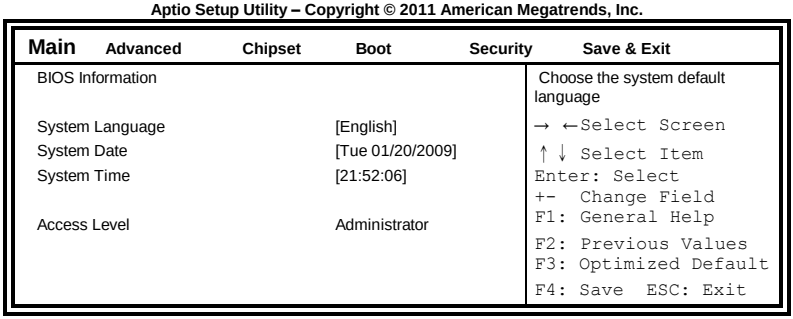
```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings



System Language

Choose the system default language.

System Date

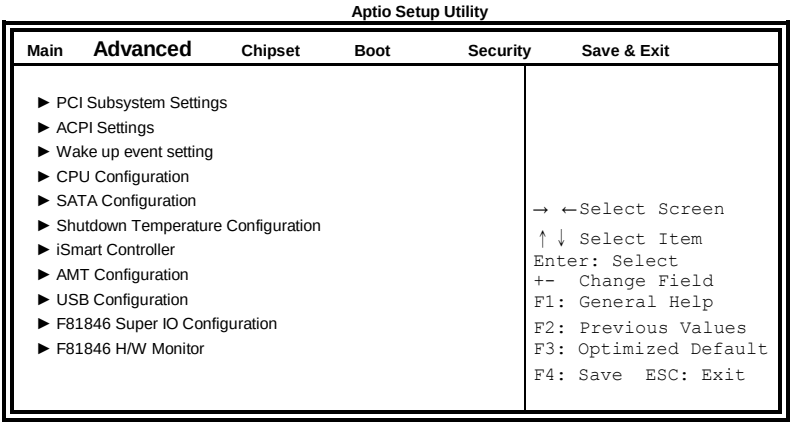
Set the Date. Use Tab to switch between Data elements.

System Time

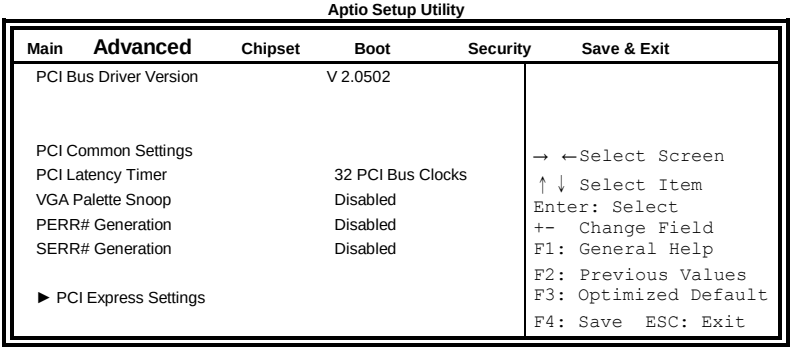
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCI Subsystem Settings



Above 4G Decoding

Enables or Disables 64bit capable devices to be decoded in above 4G address space (only if system supports 64 bit PCI decoding).

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

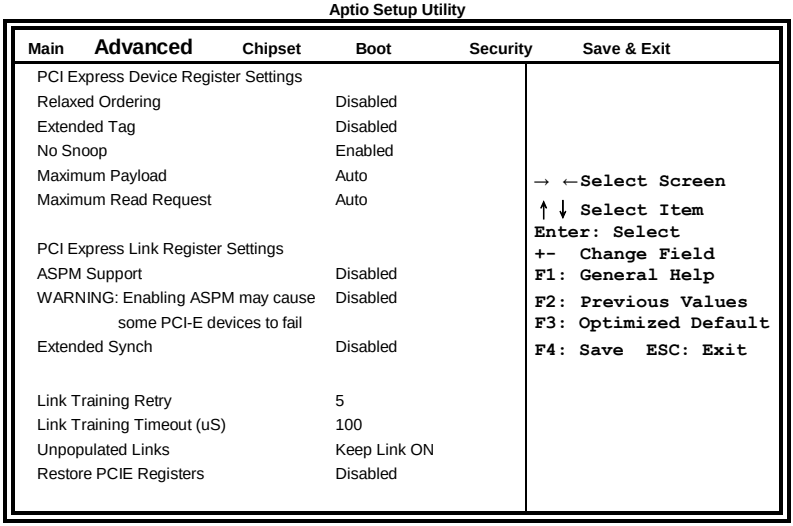
Enables or disables VGA Palette Registers Snooping.

PERR# Generation
Enables or disables PCI device to generate PERR#.

SERR# Generation
Enables or disables PCI device to generate SERR#.

PCI Express Settings
Change PCI Express devices settings.

PCI Express Settings



Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

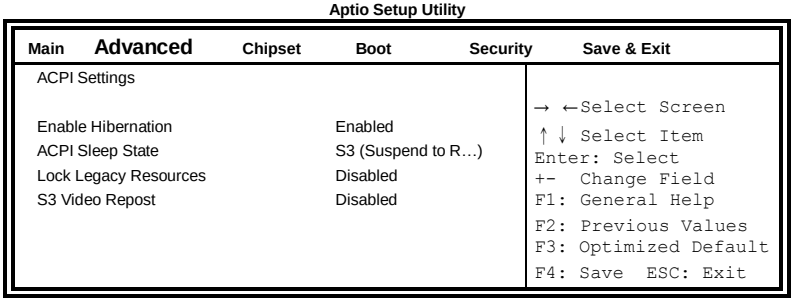
Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Restore PCIE Registers
On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3.Enabling this restors PCI Express device configuration on S3 resume
Warning: Enabling this may cause issues with other hardware after S3 resume.

ACPI Settings



Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost

Enable or disable S3 Video Repost.

Wake up event settings

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Wake on Ring			Disabled		→ ←Select Screen
Wake on PCI PME			Disabled		↑ ↓ Select Item
Wake on PCIE Wake Event			Disabled		Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Genuine Intel(R) CPU 0000 @ 2.6GHz					
CPU Signature			306c2		
Microcode Patch			Ffff0006		
Max CPU Speed			2600 MHz		
Min CPU Speed			800 MHz		
CPU Speed			3400 MHz		
Processor Cores			4		
Intel HT Technology			Not Supported		
Intel VT-x Technology			Supported		
Intel SMX Technology			Supported		
64-bit			Supported		
EIST			Supported		
CPU C3 State			Supported		
CPU C6 State			Supported		
CPU C7 State			Supported		
Active Processor Cores			All		
Limit CPUID Maximum			Disabled		→ ←Select Screen
Execute Disable Bit			Enabled		↑ ↓ Select Item
Intel Virtualization Technology			Enabled		Enter: Select
Hardware Prefetcher			Disabled		+- Change Field
Adjacent Cache Line Prefetch			Enabled		F1: General Help
EIST			Enabled		F2: Previous Values
Turbo Mode			Enabled		F3: Optimized Default
Intel TXT(LT) Support			Disabled		F4: Save ESC: Exit

Active Processor Cores
Number of cores to enable in each processor package.

Limit CPUID Maximum
Disabled for Windows XP.

Execute Disable Bit
XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hardware Prefetcher
To turn on/off the Mid level Cache (L2) streamer Prefetcher.

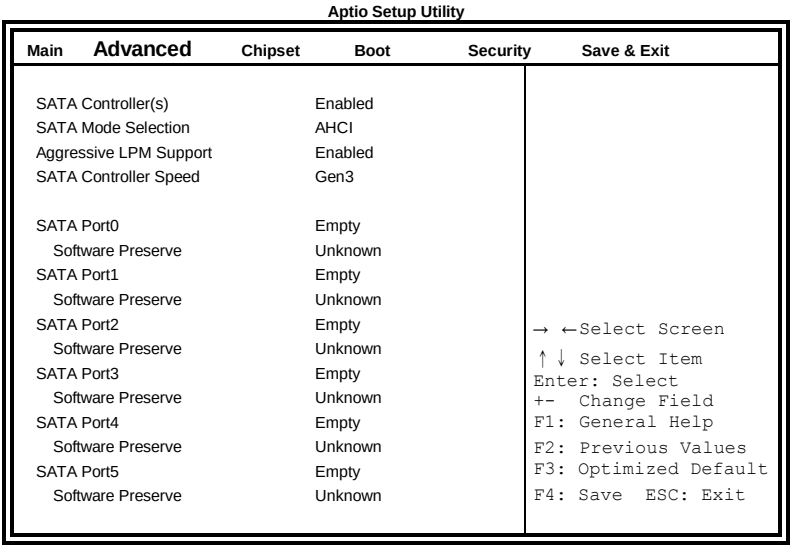
Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

EIST
Enabled/Disabled Intel Speedstep

Intel TXT(LT) Support
Enables or Disables Intel (R)TXT (LT) Support.

SATA Configuration

SATA Devices Configuration.



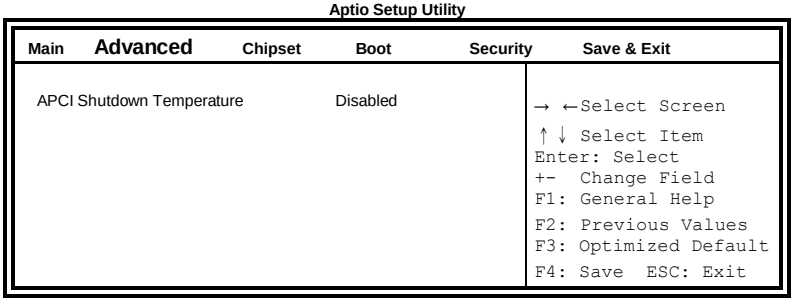
SATA Controller(s)

Enable / Disable Serial ATA Controller.

SATA Mode Selection

(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode.

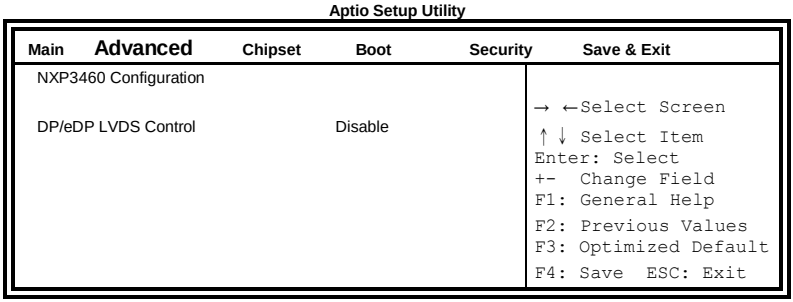
Shutdown Temperature Configuration



ACPI Shutdown Temperature

The default setting is Disabled.

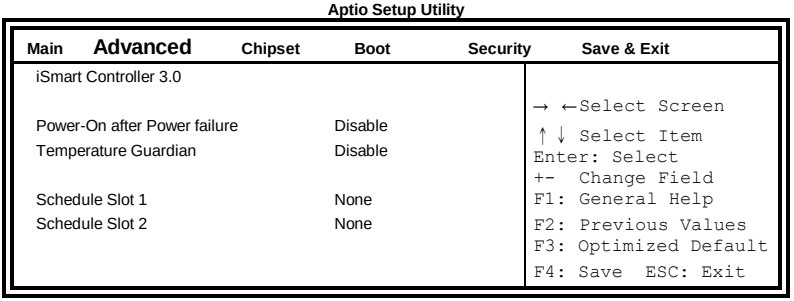
NXP3460 Configuration



DP/eDP LVDS Control

Enable / Disable DP(eDP) LVDS.

iSmart Controller 3.0



Power-On after Power failure

This field sets the system power status whether Disable or Enable when power returns to the system from a power failure situation.

Temperature Guardian

Generate the reset signal when system hangs up on POST.

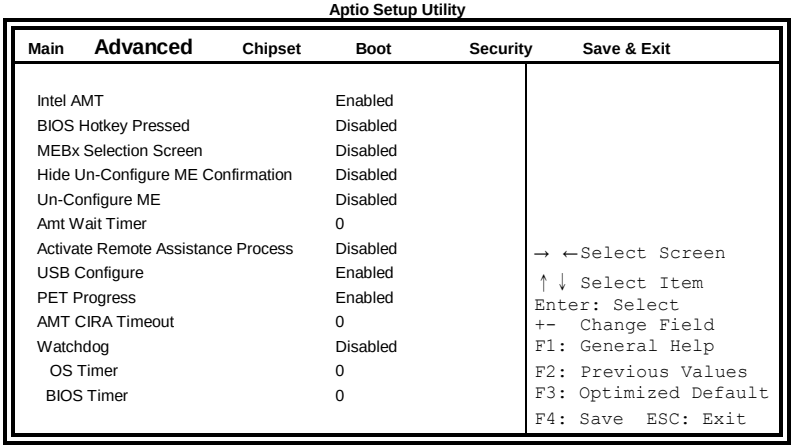
ISmart Controller

Setup the power on time for the system.

Schedule Slot 1 / 2

Setup the hour/minute for system power on.

AMT Configuration



AMT Configuration

This configuration is supported only with IB980VF (with iAMT function). Options are Enabled and Disabled.
Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME

This configuration is supported only with IB980VF (with iAMT function). Perform AMT/ME unconfigure without password operation.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process

Trigger CIRA boot.

PET Progress

User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer

This configuration is supported only with IB980VF (with iAMT function). Enable/Disable Watchdog Timer.

USB Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

USB Configuration		
USB Devices:		
2 Hubs		
Legacy USB Support	Enabled	
USB3.0 Support	Enabled	
XHCI Hand-off	Enabled	→ ←Select Screen
EHCI Hand-off	Enabled	↑ ↓ Select Item
USB Mass Storage Driver Support	Enabled	Enter: Select
		+- Change Field
USB hardware delays and time-outs:		F1: General Help
USB Transfer time-out	20 sec	F2: Previous Values
Device reset tine-out	20 sec	F3: Optimized Default
Device power-up delay	Auto	F4: Save ESC: Exit

Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

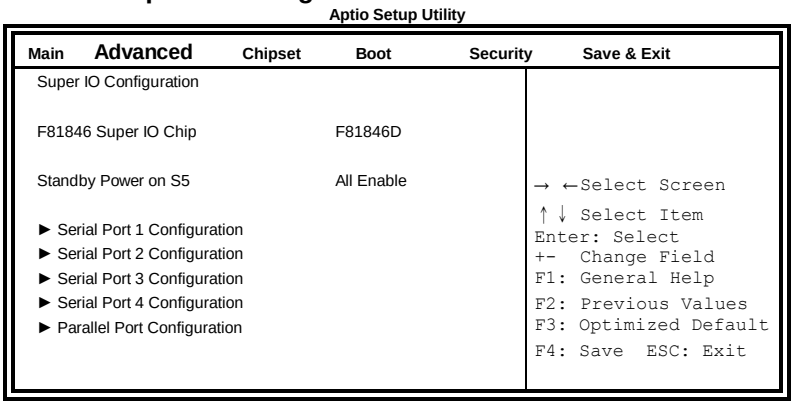
Device reset tine-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81846 Super IO Configuration



Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Standby Power on S5

[All Enable] Provide the Standby Power for devices.[All Disable] Shutdown the Standby power.

Parallel Port Configuration

Set parameters of Parallel port (LPT/LPTE)

F81846 H/W Monitor

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health Status					
CPU temperature			+29 C		
SYS temperature			+30 C		
FAN1 Speed			2170 RPM		
FAN2 Speed			N/A		
FAN3 Speed			N/A		
Vcore			+1.800 V		→ ←Select Screen
+5V			+5.087 V		↑ ↓ Select Item
+12V			+12.408 V		Enter: Select
1.5V			+1.560 V		+- Change Field
VSB5V			+5.016 V		F1: General Help
VCC3V			+3.392		F2: Previous Values
Fan 1 smart fan control			50 C		F3: Optimized Default
Fan 2 smart fan control			50 C		F4: Save ESC: Exit

Temperatures/Voltages

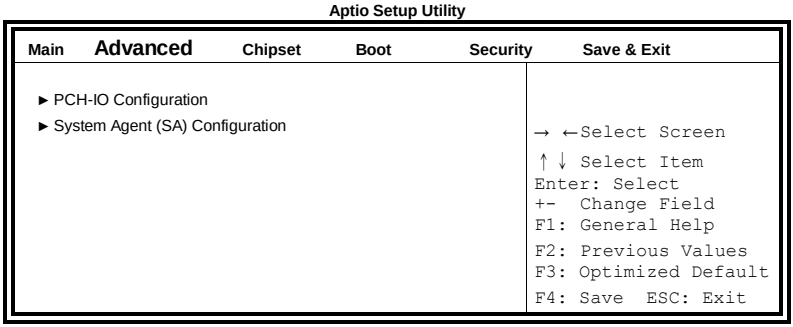
These fields are the parameters of the hardware monitoring function feature of the SHB. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

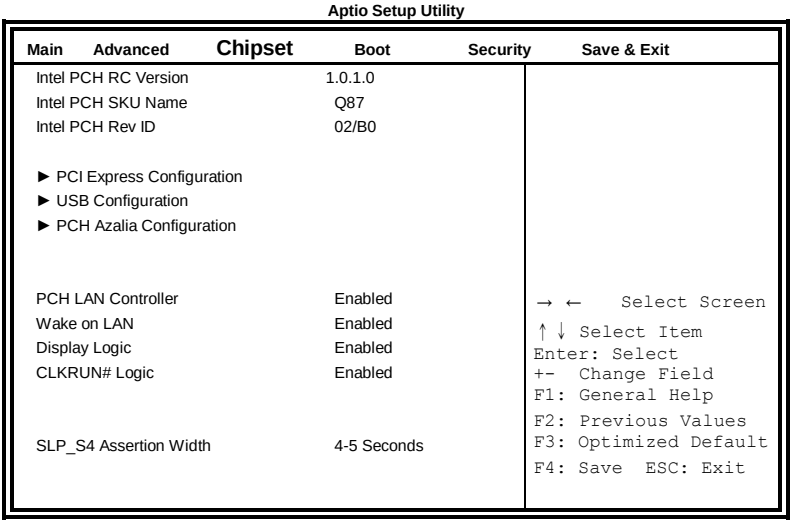
Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.



Toggle EC

Enable or Disable Toggle EC

PCH LAN Controller

Enable or disable onboard NIC.

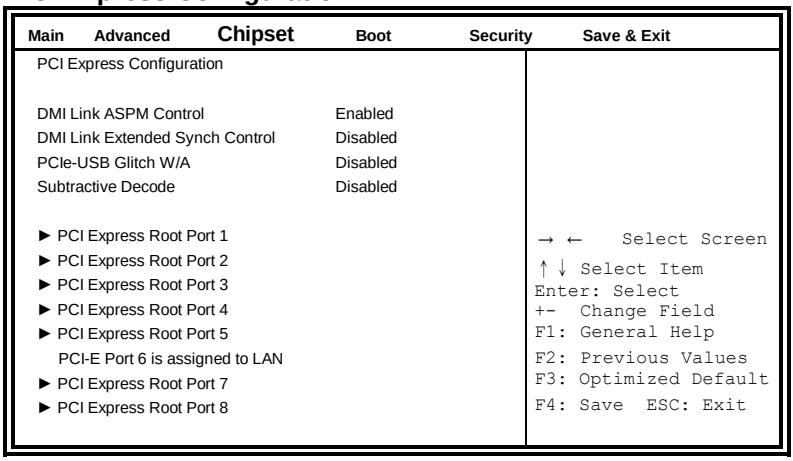
Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

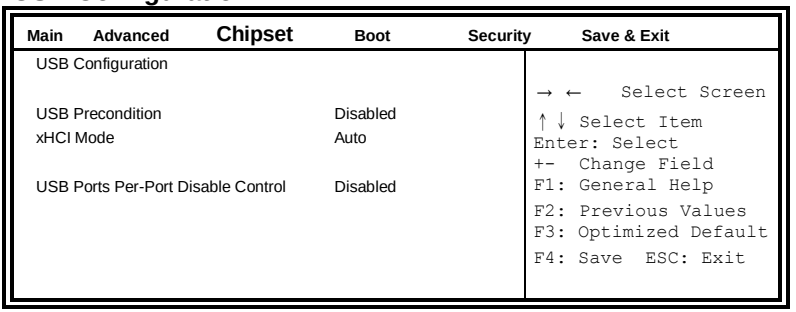
DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

USB Configuration



USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

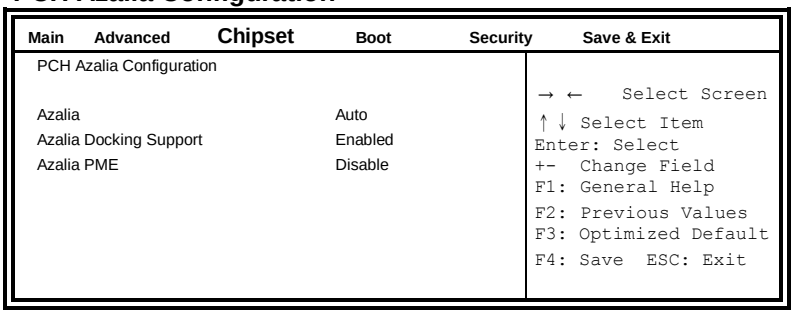
xHCI Mode

Mode of operation of xHCI controller.

USB Ports Per-Port Disable Control

Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration



Azalia

Control Detection of the Azalia device.
Disabled = Azalia will unconditionally be disabled.
Enabled Azalia will be unconditionally be enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

Azalia Docking Support

Enable or Disable Azalia Docking Support of Audio Controller.

Azalia PME

Enable or Disable power Management capability of Audio Controller.

System Agent (SA) Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
System Agent Bridge Name			IvyBridge		
System Agent RC Version			1.1.0.0		
VT-d Capability			Supported		
VT-d			Enabled		
CHAP Device (B0:D7:F0)			Disabled		
Thermal Device (B0:D4:F0)			Disabled		
Enable NB CRID			Disabled		
► Graphics Configuration					
► Memory Configuration					

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

VT-d

Check to enable VT-d function on MCH.

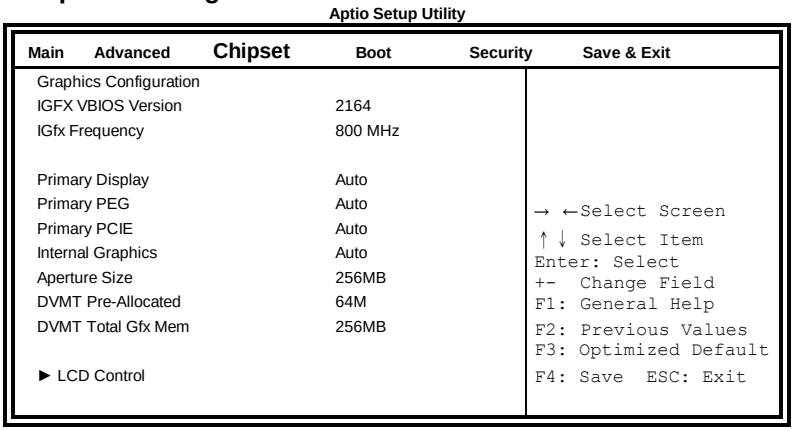
Enable NB CRID

Enable or disable NB CRID WorkAround.

C-State Pre-Wake

Controls C-State Pre-Wake feature for ARAT, in SSKPD[57].

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Primary PEG

Select PEGO/PEG1/PEG2/PEG3 Graphics device should be Primary PEG.

Primary PCIE

Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6PCIE7 Graphics device should be primary PCIE.

Internal Graphics

Keep IGD enabled based on the setup options.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

DVMT Total Gfx Mem

Select DVMT 5.0 total graphics memory size used by the internal graphics device.

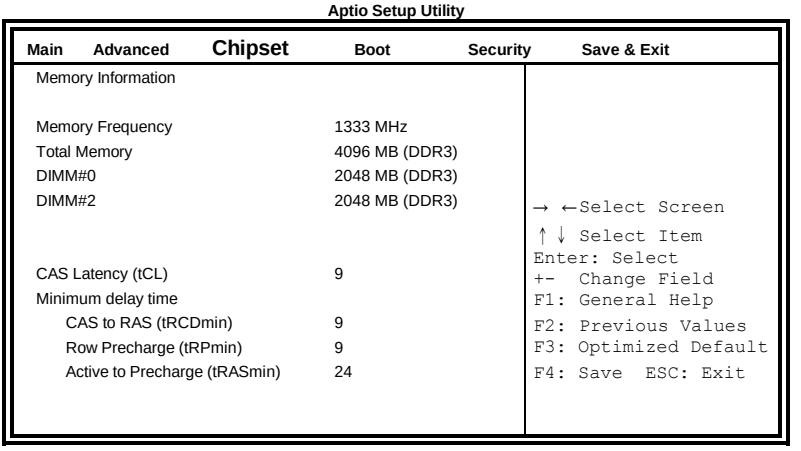
Gfx Low Power Mode

This option is applicable for SFF only.

Primary IGFX Boot Display (LCD Control)

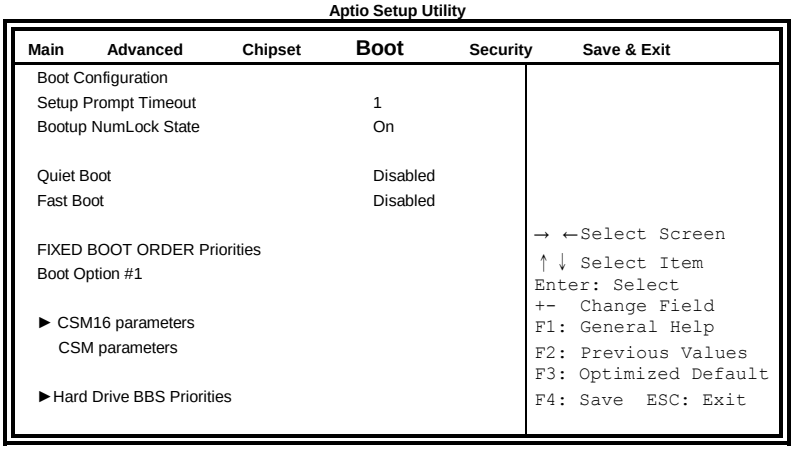
Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

Memory Configuration



Boot Settings

This section allows you to configure the boot settings.



Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

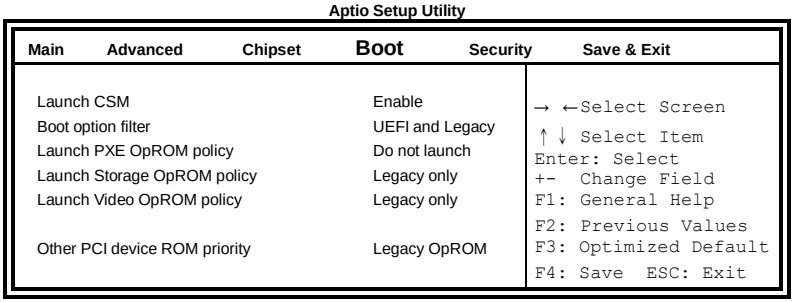
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot Option Priorities

Sets the system boot order.

CSM parameters

This section allows you to configure the boot settings.



Boot option filter

This option controls what devices system can boot to.

Launch PXE OpROM policy

Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM policy

Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy

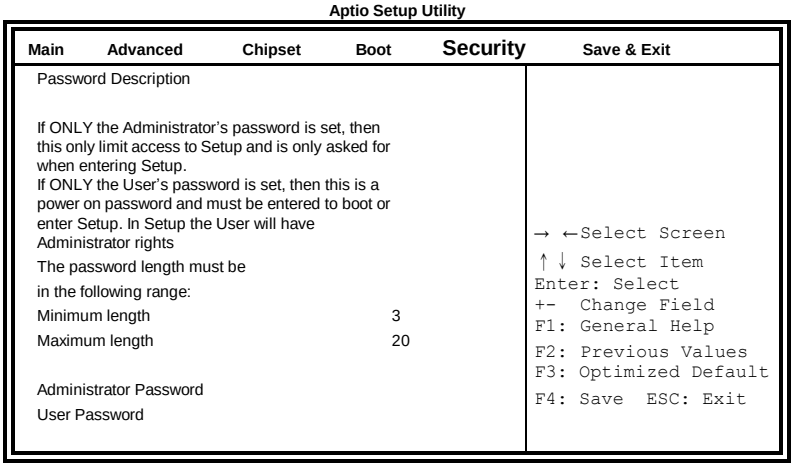
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority

For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



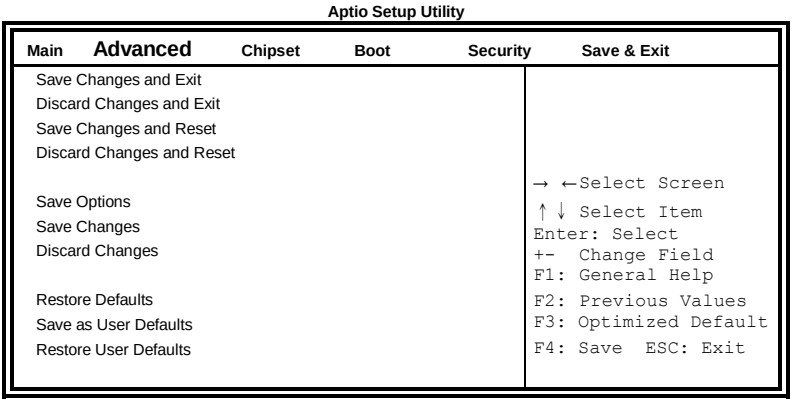
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the SHB. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

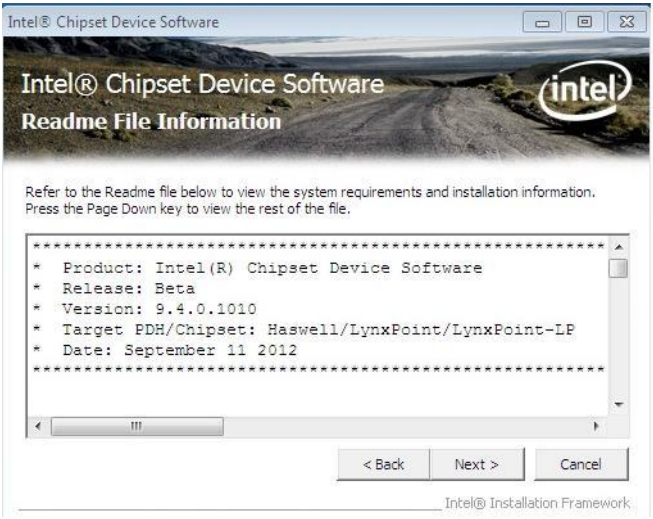
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.



6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

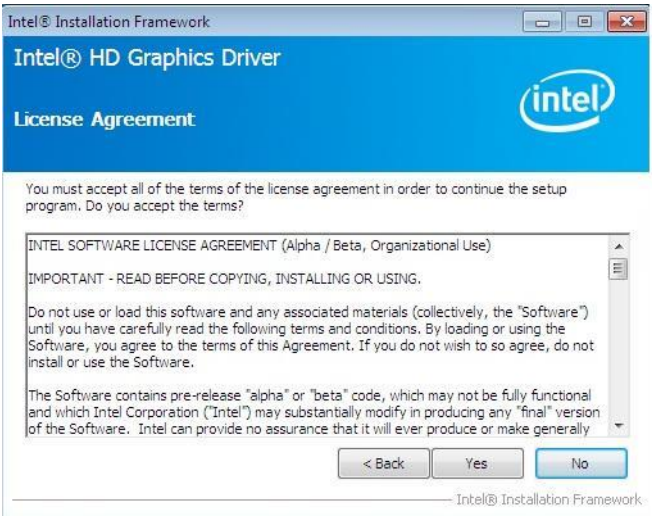
VGA Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Core(TM) i3/i5/i7 Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

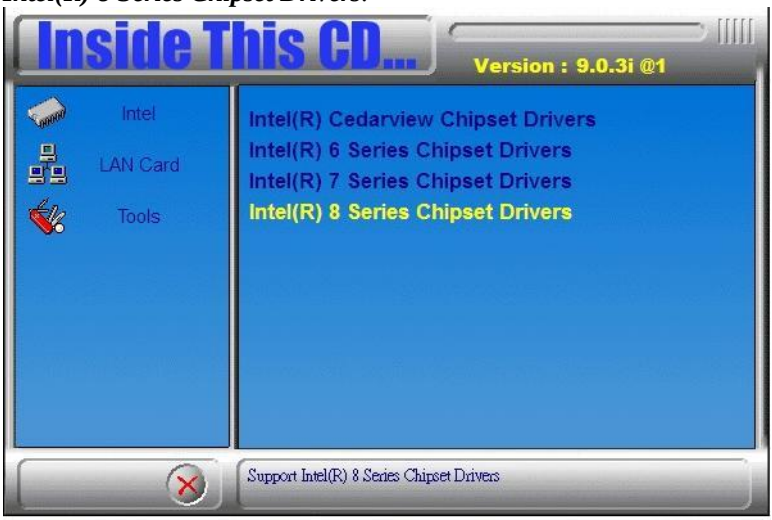


5. On the screen shown below, click ***Install*** to continue.

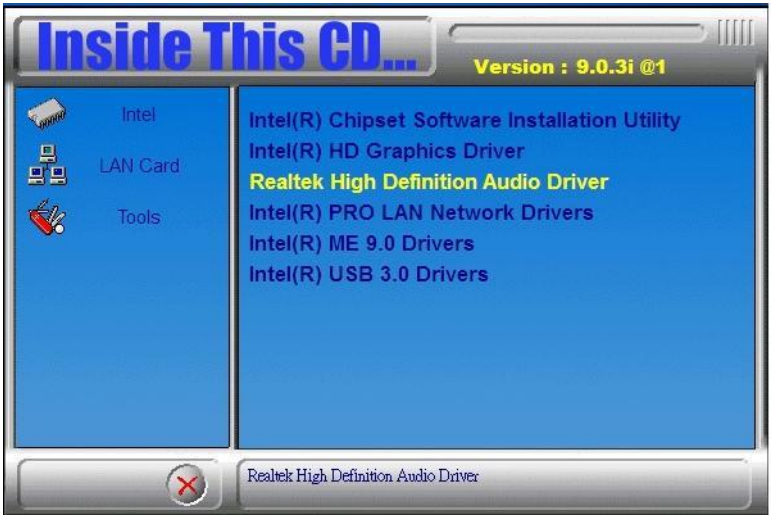
6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

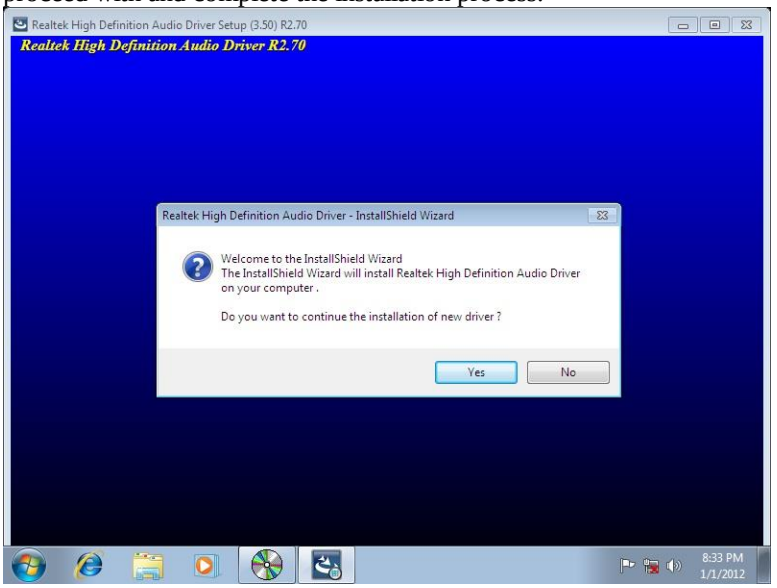
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.



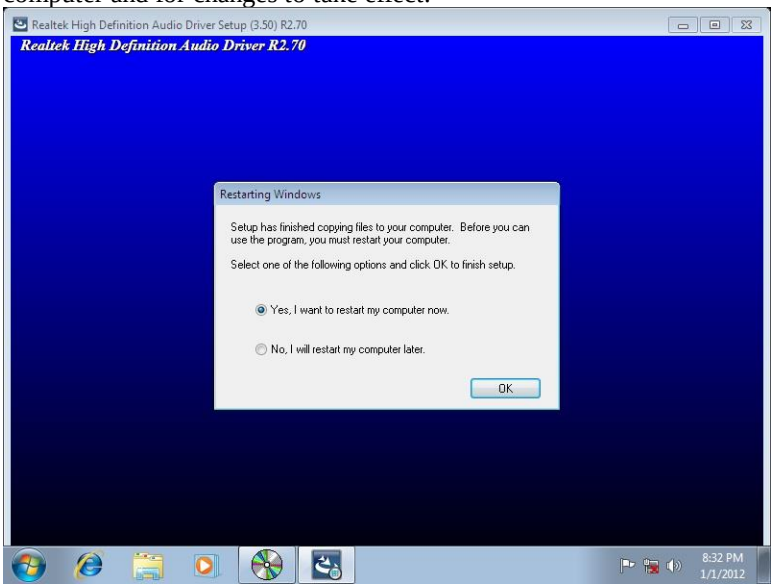
2. Click ***Realtek High Definition Audio Driver.***



3. On the Welcome to the InstallShield Wizard screen, click ***Yes*** to proceed with and complete the installation process.

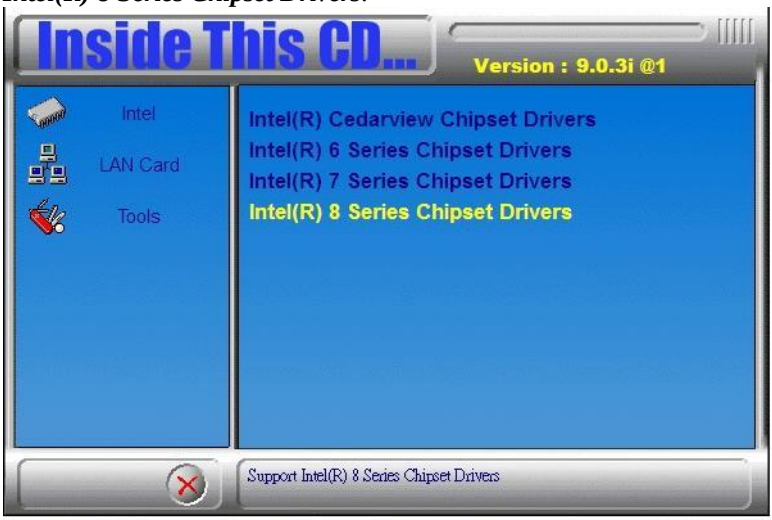


4. The InstallShield Wizard Complete. Click ***Finish*** to restart the computer and for changes to take effect.



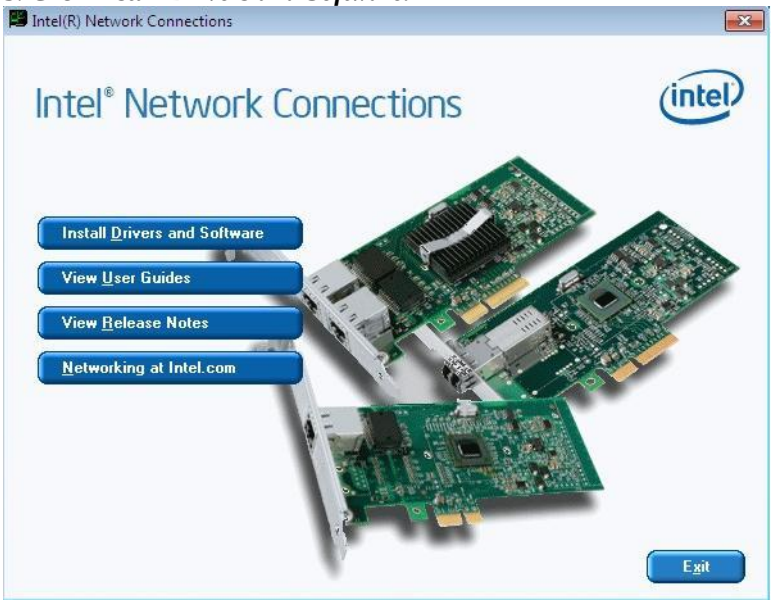
LAN Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.



2. Click ***Intel(R) PRO LAN Network Driver.***

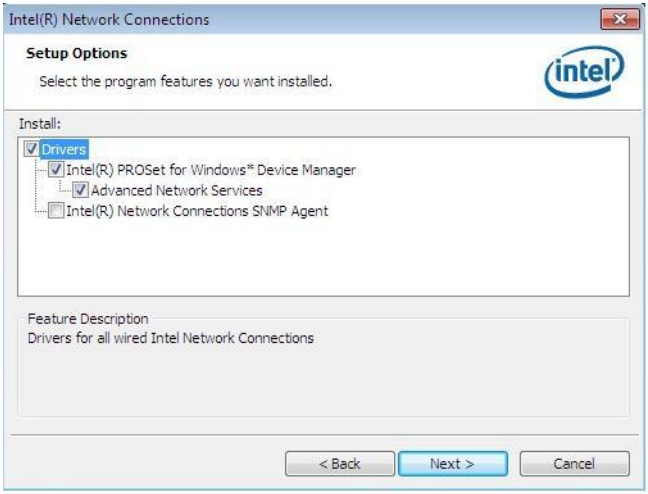
3. Click ***Install Drivers and Software.***



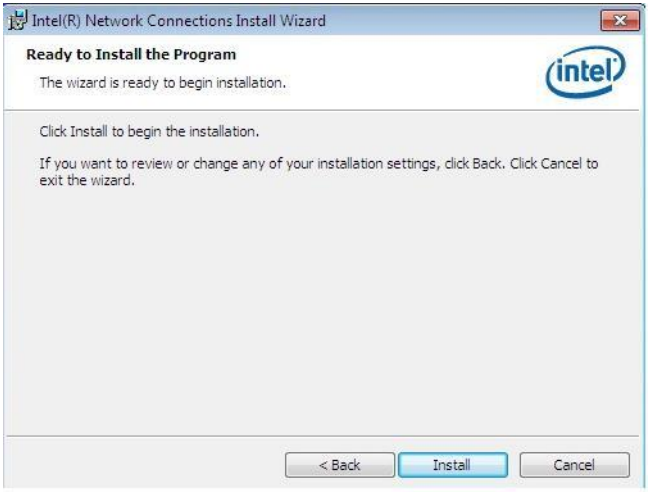
4. When the Welcome screen appears, click ***Next***.

5. Click ***Next*** to to agree with the license agreement.

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



7. The wizard is ready to begin installation. Click ***Install*** to begin the installation.



8. When InstallShield Wizard is complete, click ***Finish***.

Intel® Management Engine Interface

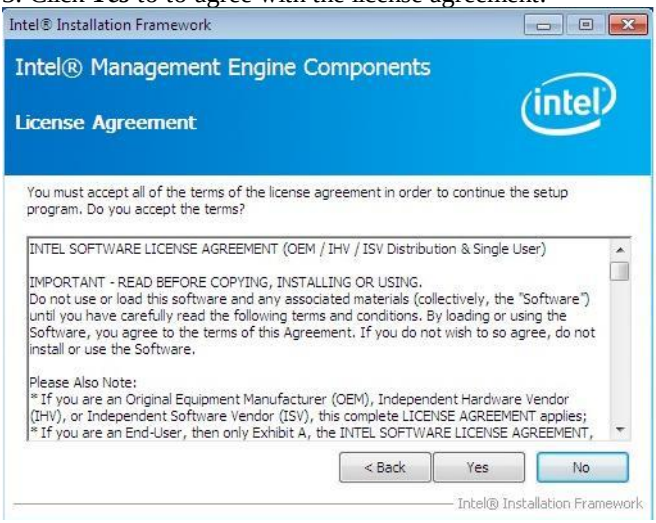
The following application requires Microsoft .NET Framework 3.5 or later: Intel® Management Engine Components. Please install the latest version of Microsoft .NET Framework from Microsoft Download Center to run this application correctly.

Follow the steps below to install the Intel Management Engine.

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers*** and then ***Intel(R) AMT 9.0 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click ***Next***.

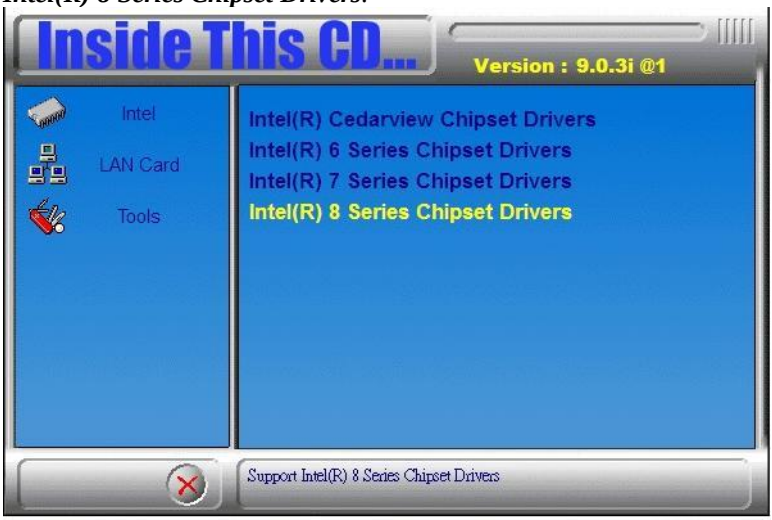
3. Click ***Yes*** to to agree with the license agreement.



4. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.

Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.



2. Click ***Intel(R) USB 3.0 Drivers.***

3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click ***Next***.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81846.H"
//-----------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//-----------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81846 watch dog program\n");

        SIO = Init_F81846();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81846, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT();           }

        return 0;
```

```
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
	unsigned char bBuf;

	bBuf = Get_F81846_Reg(0x2B);
	bBuf &= (~0x20);
	Set_F81846_Reg(0x2B, bBuf);			//Enable WDTO

	Set_F81846_LD(0x07);				//switch to logic device 7
	Set_F81846_Reg(0x30, 0x01);			//enable timer

	bBuf = Get_F81846_Reg(0xF5);
	bBuf &= (~0x0F);
	bBuf |= 0x52;
	Set_F81846_Reg(0xF5, bBuf);			//count mode is second

	Set_F81846_Reg(0xF6, interval);		//set timer

	bBuf = Get_F81846_Reg(0xFA);
	bBuf |= 0x01;
	Set_F81846_Reg(0xFA, bBuf);			//enable WDTO output

	bBuf = Get_F81846_Reg(0xF5);
	bBuf |= 0x20;
	Set_F81846_Reg(0xF5, bBuf);			//start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
	unsigned char bBuf;

	Set_F81846_LD(0x07);				//switch to logic device 7

	bBuf = Get_F81846_Reg(0xFA);
	bBuf &= ~0x01;
	Set_F81846_Reg(0xFA, bBuf);			//disable WDTO output

	bBuf = Get_F81846_Reg(0xF5);
	bBuf &= ~0x20;
	bBuf |= 0x40;
	Set_F81846_Reg(0xF5, bBuf);			//disable WDT
}
//-------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81846.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81846_BASE;
void Unlock_F81846 (void);
void Lock_F81846 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81846(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81846_BASE = 0x4E;
        result = F81846_BASE;

        ucDid = Get_F81846_Reg(0x20);
        if (ucDid == 0x07)                                      //Fintek 81846
        {       goto Init_Finish;       }

        F81846_BASE = 0x2E;
        result = F81846_BASE;

        ucDid = Get_F81846_Reg(0x20);
        if (ucDid == 0x07)                                      //Fintek 81846
        {       goto Init_Finish;       }

        F81846_BASE = 0x00;
        result = F81846_BASE;

Init_Finish:
        return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81846 (void)
{
        outportb(F81846_INDEX_PORT, F81846_UNLOCK);
        outportb(F81846_INDEX_PORT, F81846_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81846 (void)
{
        outportb(F81846_INDEX_PORT, F81846_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81846_LD( unsigned char LD)
{
        Unlock_F81846();
        outportb(F81846_INDEX_PORT, F81846_REG_LD);
        outportb(F81846_DATA_PORT, LD);
        Lock_F81846();
}
//---------------------------------------------------------------------------
void Set_F81846_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81846();
        outportb(F81846_INDEX_PORT, REG);
        outportb(F81846_DATA_PORT, DATA);
        Lock_F81846();
}
//---------------------------------------------------------------------------
```

```
unsigned char Get_F81846_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81846();
        outportb(F81846_INDEX_PORT, REG);
        Result = inportb(F81846_DATA_PORT);
        Lock_F81846();
        return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef __F81846_H
#define __F81846_H                     1
//---------------------------------------------------------------------------
#define         F81846_INDEX_PORT               (F81846_BASE)
#define         F81846_DATA_PORT                (F81846_BASE+1)
//---------------------------------------------------------------------------
#define         F81846_REG_LD                   0x07
//---------------------------------------------------------------------------
#define F81846_UNLOCK                   0x87
#define         F81846_LOCK                             0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81846(void);
void Set_F81846_LD( unsigned char);
void Set_F81846_Reg( unsigned char, unsigned char);
unsigned char Get_F81846_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif  //__F81846_H
```