EDP-AM-AN16 Analog Input Applications Module User Manual

This document contains information on the AN16 analog input module for the RS EDP system.

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1. Analog Input Module

The EDP-AM-AN16-A analog module allows up to 32 analog channels to be interfaced to the CM (CPU Module or Command Module). It has a mix of filtered and unfiltered inputs and two precision voltage sources for accurate absolute measurements.

The on-board MAX1138 ADC is accessible via I2C CNTRL bus and gives up to 12 extra channels of 10-bit analog to digital conversion. Each of the first 12 channels can be routed via jumpers to either the CM's own ADC or to the on-board ADC. In addition, any unused channels on the on-board ADC is available on a connector, meaning a total of 16 plus 12, i.e.28 channels are possible.

Two analog modules may be fitted simultaneously. If this is the case the 16 analog channels, which are fed directly down the backplane to the ADC on the MCU have to be allocated to each of the two modules respectively but the 12 additional ADC channels present on each of the AMs can be read independently, giving a total of 16 plus 12 plus a second 12. i.e. a total of 40 channels.
If a second module is fitted, the channels belonging to the CM remain the same, although the user can specify which channel will be routed through which analog module. The second analog module must use the second I2C channel, I2C_GEN0 as the MAX1138 ADC has a fixed I2C address. An alternative version of this device (MAX1138KEEE+) has a different I2C address and can be fitted to the second module if required.

The on-board ADC is by default the MAX1138 5V, 10-bit ADC but the alternative MAX1139 3V3 device can be fitted. The CM analog channels have a voltage range determined by the CPU fitted. The analog module inputs are able to cope with a 0-5V range, regardless of the CM type fitted. It is therefore up to the user to ensure that the voltage applied to the inputs does not exceed that required by the CM. A series protection resistor may optionally be fitted to reduce the chance of damaging a 3V3 ADC if 5V is applied.

The 5V and 3V3 precision references can be applied to the CM's ADC and the on-board ADC, although the latter will sacrifice one channel if this is used. They can also be fed back to the CM via the VAREF EDP signal.

Ratiometric conversions are possible using a special output pin on connector P201 pin1 for driving resistive sensors.

Quantity	Type
2	2 pole filters with digitally controlled cut-off
6	2-pole active filters with fixed cut-off
8	1-pole passive filters with fixed cut-off
12	Unfiltered channels
1	5V reference
1	3V3 reference

1.1 Anti-Aliasing Filters

Channels AN0 to AN7 are equipped with 2-pole, Sallen-Key anti-aliasing filters, configured in a Butterworth mode. The active filters are unity gain so they can be used for DC voltage measurements as well as for sampling rapidly changing signals. Channels AN0 and AN1 optionally have I2C-controlled 256 step digital potentiometers which allow the filter characteristics to be altered under software control. They can also be cascaded to yield a single 4-pole filter on channel AN0. The remaining active filters have a cut-off frequency of 12kHz.

By fitting the appropriate resistors to the potential dividers on the filter inputs (R301, R304 etc.), the input voltage range can be extended to suit the user's application on a channel-by-channel basis.

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AN8-AN15 have simple low-pass filter inputs. All inputs are protected against over-voltage conditions.

1.2 Additional Items

A trimmer potentiometer and light-dependent resistor and are fitted to channels AN0 and AN1 respectively for educational purposes.

1.3 Setting Jumper Options

Some options are made using black 2mm links. These are available from RS under part number 180-9353. The possible user settings are listed below, along with their default configurations.

Jumper	Type	Purpose	Default
J202	Solder	Set voltage for MAX1138 ADC	1-2
J204	Solder	Set I2C channel	1-2
J205	Solder	Set I2C channel	1-2
J301	Solder	Connect local VAGND to SGND on module rather on CPU module (NO)	1-2
J302	Solder	Route AN0_5V to CPU AN0 or MAX1138 AN0; enable 5V to 3V3 scaling for CPU AN0	1-2
J303	Solder	Enable shutdown mode for AD5263 (Default 2-3)	2-3
J305	Solder	Set AD5263 I2C address AD0	2-3
J306	Solder	Set AD5263 I2C address AD1	2-3
J307	Solder	Create 4-pole active filter from U301A and U301B	Open
J308	Solder	Route AN4_5V to CPU AN4 or MAX1138 AN4; enable 5V to 3V3 scaling for CPU AN4	1-2
J309	Solder	Route AN1_5V to CPU AN1 or MAX1138 AN1; enable 5V to 3V3 scaling for CPU AN1	1-2
J310	Solder	Route AN5_5V to CPU AN5 or MAX1138 AN5; enable 5V to 3V3 scaling for CPU AN5	1-2
J311	Solder	Route AN6_5V to CPU AN6 or MAX1138 AN6; enable 5V to 3V3 scaling for CPU AN6	1-2
J312	Solder	Route AN2_5V to CPU AN2 or MAX1138 AN2; enable 5V to 3V3 scaling for CPU AN2	1-2
J313	Solder	Route AN7_5V to CPU AN7 or MAX1138 AN7; enable 5V to 3V3 scaling for CPU AN7	1-2
J314	Solder	Route AN3_5V to CPU AN3 or MAX1138 AN3; enable 5V to 3V3 scaling for CPU AN3	1-2
J201	4W Link	Select source for MAX1138 REF	Open
JP201	Link	Select ADC for AN8_5V input	1-2
JP202	Link	Select ADC for AN9_5V input	1-2
JP203	Link	Select ADC for AN10_5V input	1-2
JP204	Link	Select voltage for VAREF	1-2
JP205	Link	Select ADC for AN11_5V input	1-2
JP206	Link	Select source for AN15 input	2-3
JP301	Link	Select AN0_5V or pot as AN0 input	1-2
JP302	Link	Select AN1_5V or LDR as AN1 input	1-2
P201	2-way	Power supply to ratiometric sensors	NC

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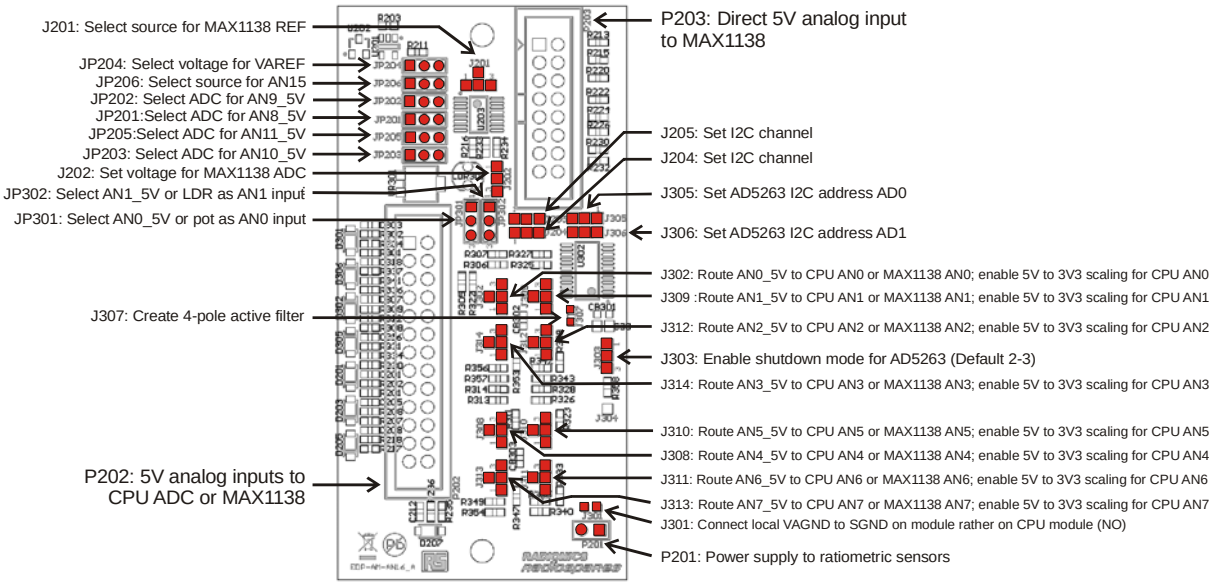
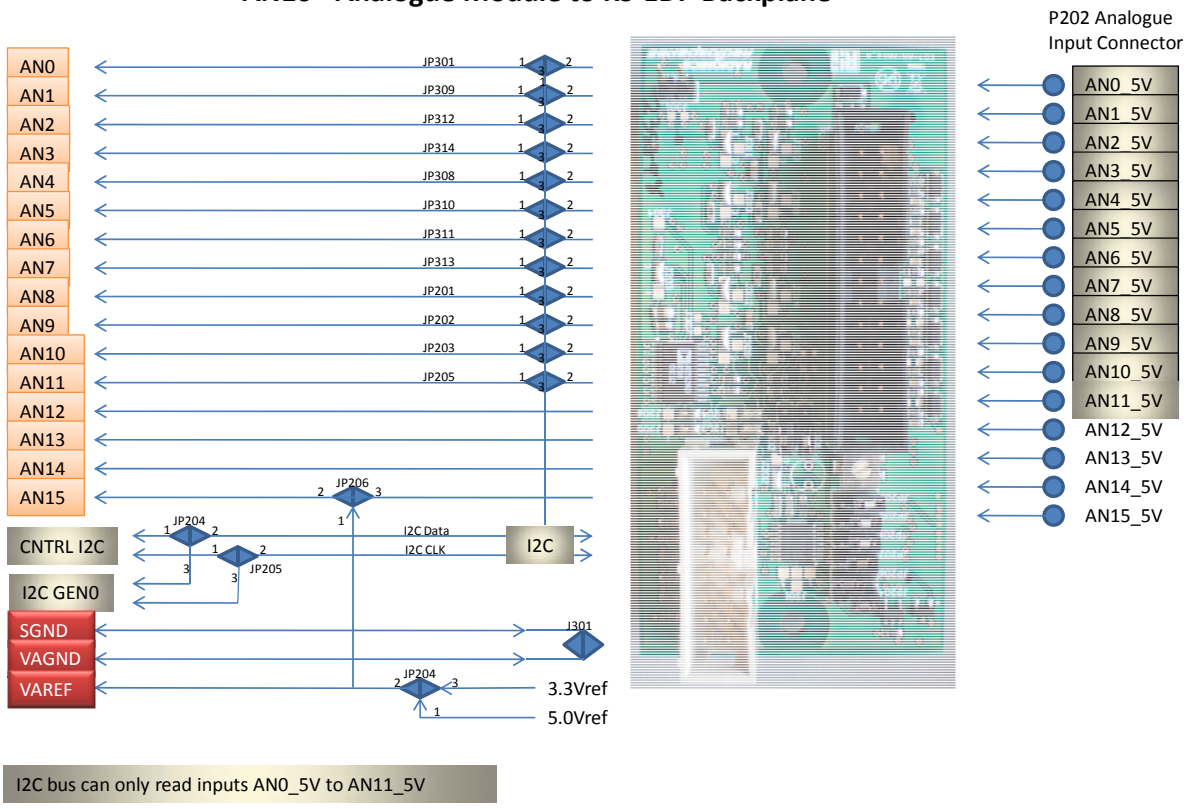
The locations of the most important user-selectable items are shown below.



AN16 - Analogue Module to RS-EDP Backplane



Block diagram of the Analog Module showing capability and basic link options. Normally AN0_5V to AN15_5V are used for the raw analog inputs. The processed analog signals are passed to the MCU via the backplane on AN0-AN15 or redirected into the on board ADC for reading via an I2C chip. With this implementation a total of 16 analog inputs are available, the first 12 of which are readable via I2C.

You can also see that the analog ground (VAGND) and the digital signal ground (SGND) can be connected via a zero ohm link. This link is normally left open as the same link is available on the CPU modules. The CPU modules should normally use this option to connect the two grounds. Most of the

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CPU modules should have this feature but check the circuit diagram and mapping aids on the respective CPU Modules.

The analogue board is capable of producing a very stable voltage reference signal. This signal can be passed down the backplane as required to other modules. The CPU modules for example can use this as a reference for their on board ADC's. The AM is fitted with both a 3.3V and 5.0V voltage reference source. The user selects between them as shown in the diagram. Some CPU Modules can output their own reference on to the backplane also so the user must also check for contention on this signal line.

The on board ADC and the digital potentiometers present on the AM can be controlled via I2C. Normally the user would use the CNTRL_I2C bus option rather than the I2C_GEN0 bus option. The I2C_GEN0 bus is provided as a secondary I2C interface for the customers own I2C network. Not all CPU Modules can support the second I2C bus.

The drawing is from a Mapping Aid document which is provided for each of the CPU Modules.

1.3 Software Drivers For Analog Module

The module has two I2C devices, both of which require special software drivers to access. The software drivers are provided for the CNTRL_I2C bus for each of the Command Modules currently in production. The software drivers allow for the easy access to the resources available on this Application Modules. As each piece of software is different for each of the CMs, you will need to refer to the software pack for each of these CMs for more details.

1.4 Mapping Of CPU Peripheral Pins To The Analog Module

The analog module passes down the backplane the processed analog signals AN0 to AN15. These may well have been processed by the on board filters on the AM for example.
The AN0-AN15 signals can be directly read by the CPU module. Not all of the CMs can read all of the AN0-AN15 signals as the resources available on each MCU are all different. To help with the matching up of CMs and Application Modules (AMs) a Mapping Aid document exists for each of the Command Modules. This details the resources that are available on the MCU with the resources available on the AMs. The page relating to the Analogue Module is shown below

The analog inputs on connector P202 on the analog IO module are connected to the CPU module as shown below. The mapping is shown for the STR9 and XC167 modules below.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
42 GUARD/AN GND	AVSS Analog GND	VAGND
P3.5	P5.7	IRQ_GPIO18_I2C GEN0 INT
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT
Digital GND	Digital GND	Digital GND
37 AN8	NC	AN8
39 AN6	P4.6	AN6
33 AN4	P4.4	AN4
31 AN2	P4.2	AN2
45 AN14	NC	AN14
43 AN12	NC	AN12
35 AN10	NC	AN10
29 AN0	P4.0	AN0
41 VAREF	AVREF - Analog	AN_REF
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator

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Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

Pin	XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
126	Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
20	GUARD/AN GND	AVSS Analog GND	VAGND
132	Digital GND	Digital GND	Digital GND
12	38 AN9	NC	AN9
10	40 AN7	P4.7	AN7
8	34 AN5	P4.5	AN5
6	32 AN3	P4.3	AN3
18	46 AN15	NC	AN15
16	44 AN13	NC	AN13
14	36 AN11	NC	AN11
4	30 AN1	P4.1	AN1
130	Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
128	Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
2	NC		
22	80 P4.0	P8.1	
24	81 P4.1	P8.2	

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
23 SDA1	P2.3	I2C GEN0 SDA
24 SCL1	P2.2	I2C GEN0 SCL
Digital GND	Digital GND	Digital GND
25 SDA2	P2.1	CNTRL I2C SDA
26 SCL2	P2.0	CNTRL I2C SCL

Refer to the Mapping Aids to get an overview of what resources the module can connect to.

1.5 Analog Module Input Characteristics

1.5.1 Channels AN0-AN7

These are over-voltage protected and buffered with unity gain, 2nd order filters. The characteristics of the OP amps fitted mean that the usable voltage input range is 24mV to 4.49V, with a linear and monotonic response. With a 5V, 10-bit ADC the decimal value range is from 9 to 804 bits. With a 3V3, 10-bit ADC, the upper value is 1023 bits.

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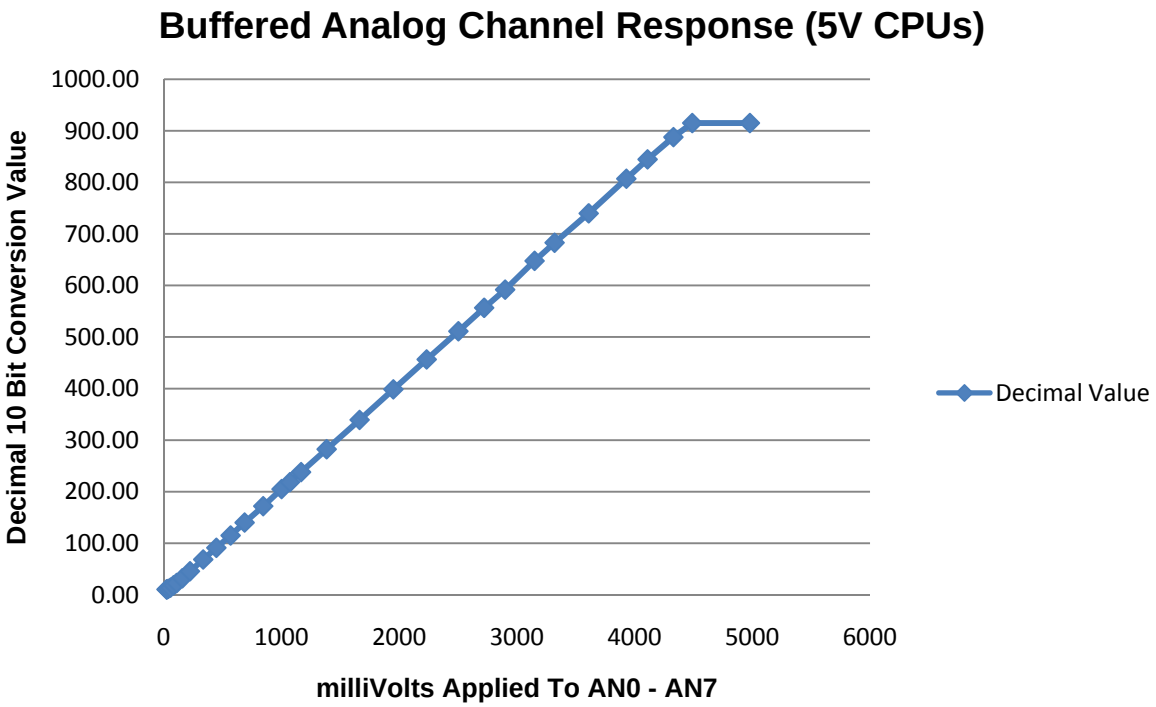

1.5.2 Channels AN8- AN15

These are un-buffered but still have over-voltage protection. The usable range is determined entirely by the characteristics of the ADC used.

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1.6 Analog Module Hints

For best performance when using the CPU's own ADC, i.e. least noise and greatest conversion accuracy, ensure that the analog module is placed in the EDP baseboard position immediately adjacent to the CPU module. Also, solder bridge J301 can be closed to ensure that the analog ground is connected to the system ground (SGND) on the analog module rather than on the CPU module. However to avoid ground loops though, the link on the CPU module that connects these two grounds must be opened (XC167 only).

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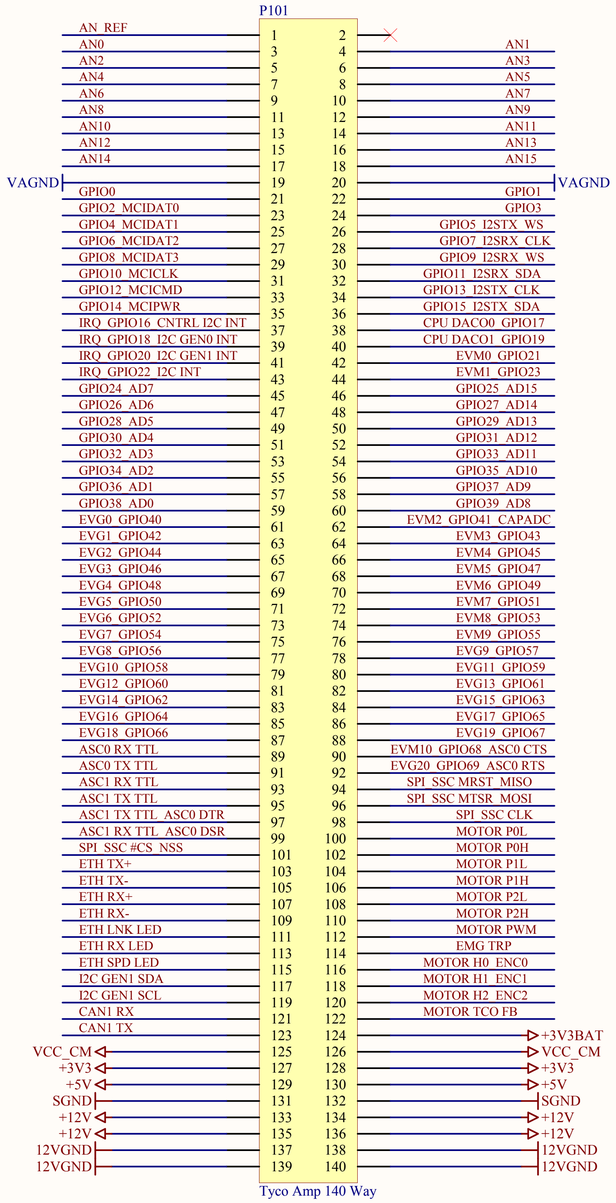
Module Position 1

EDPCON1 IO Connector



Tyco Amp 140 Way

EDPCON2 Bus/Control Connector

Tyco Amp 100 Way

Checked By:	Title: ***EDP Connectors***		*Hitex (UK) Ltd.* *Sir William Lyons Road* *University of Warwick Science Park* *Coventry*
Approved By:	Size: A3	Number: EDP-AM-AN16 Ar1	Revision: Ar1
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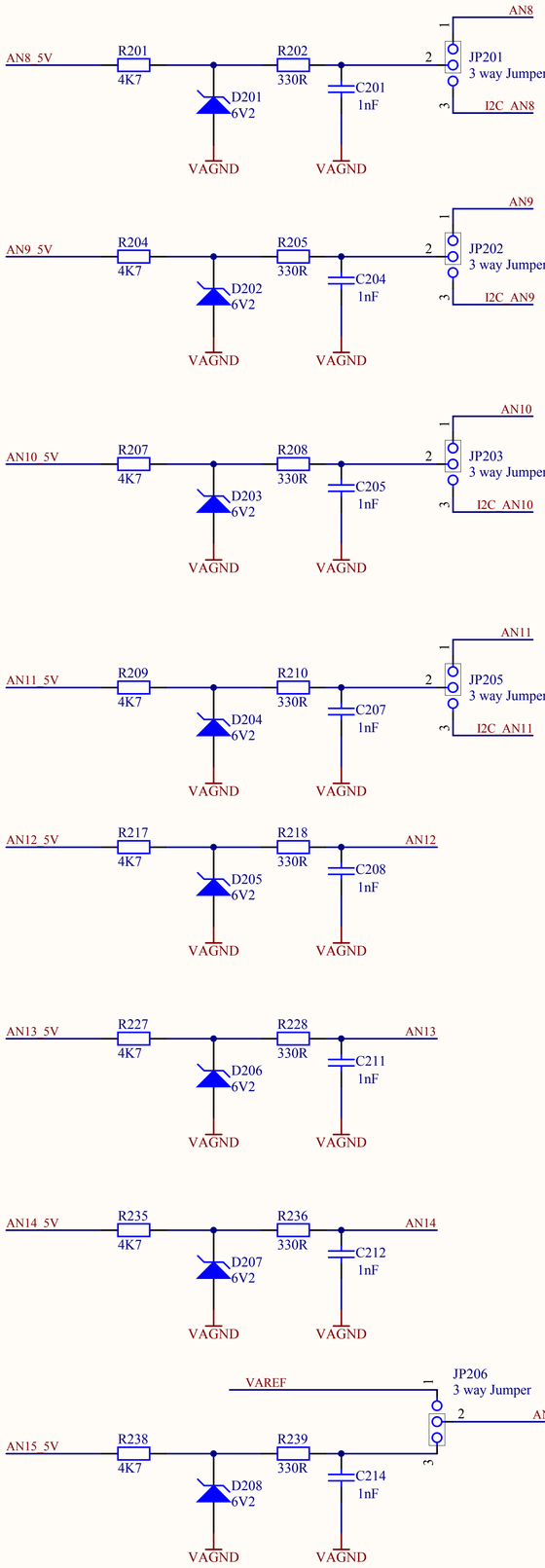
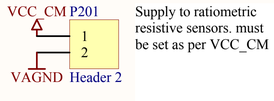
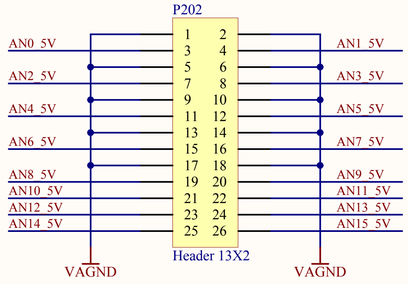
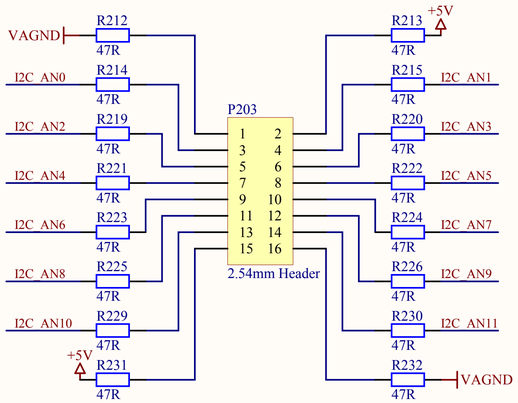


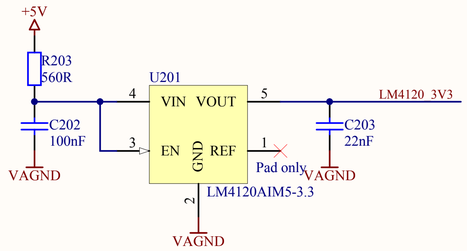


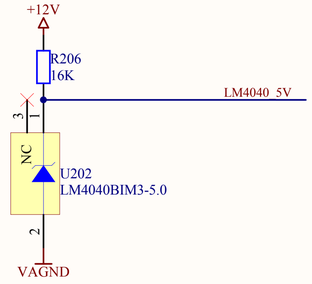
Supply to ratiometric resistive sensors. must be set as per VCC_CM

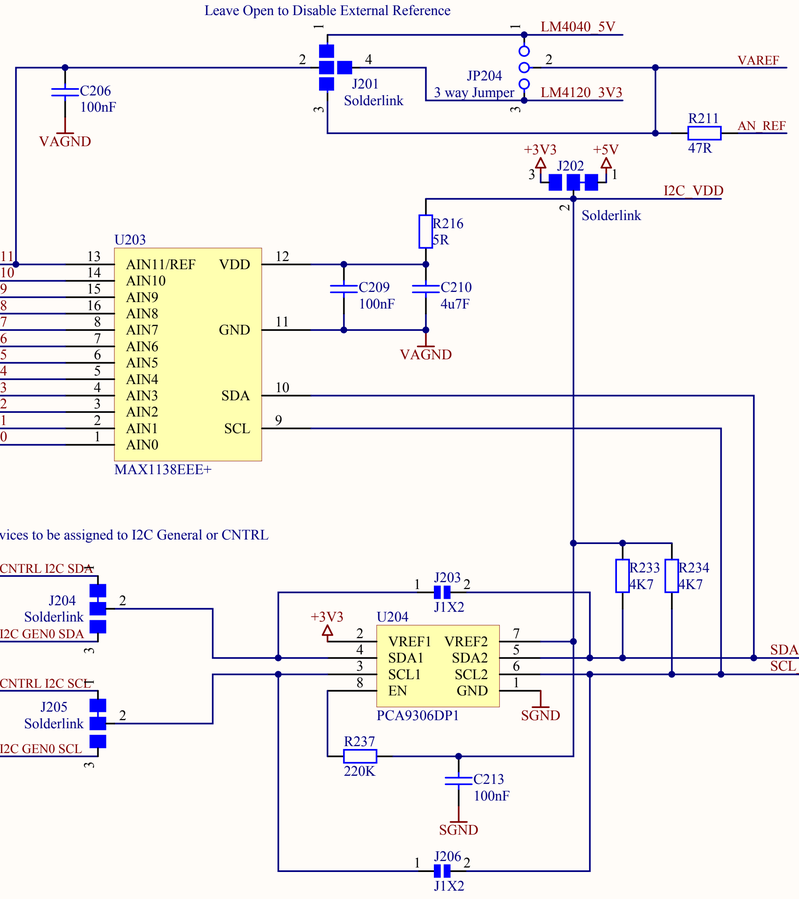




Access to I2C ADC Channels that are not being used elswhere (no Filtering)







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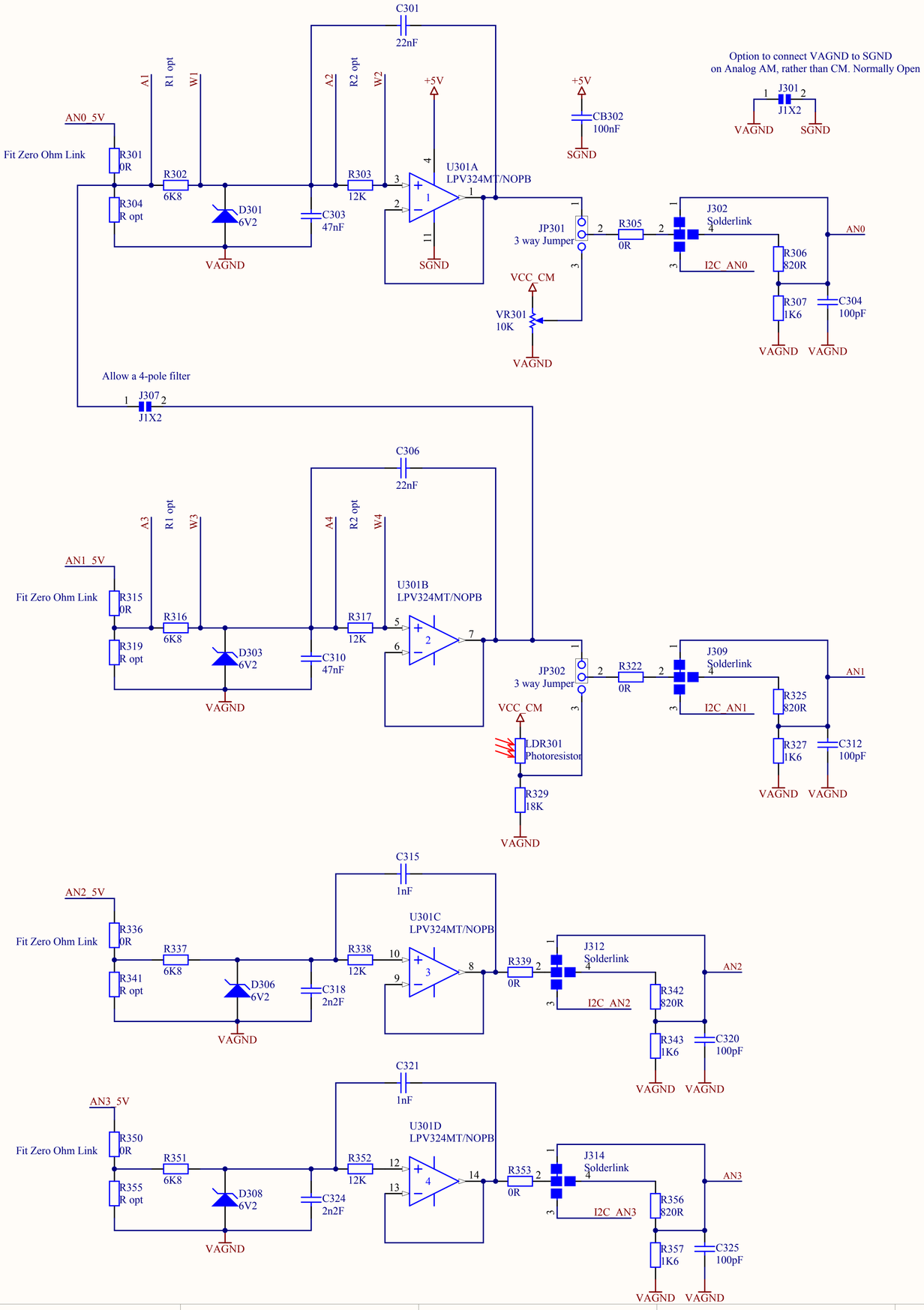

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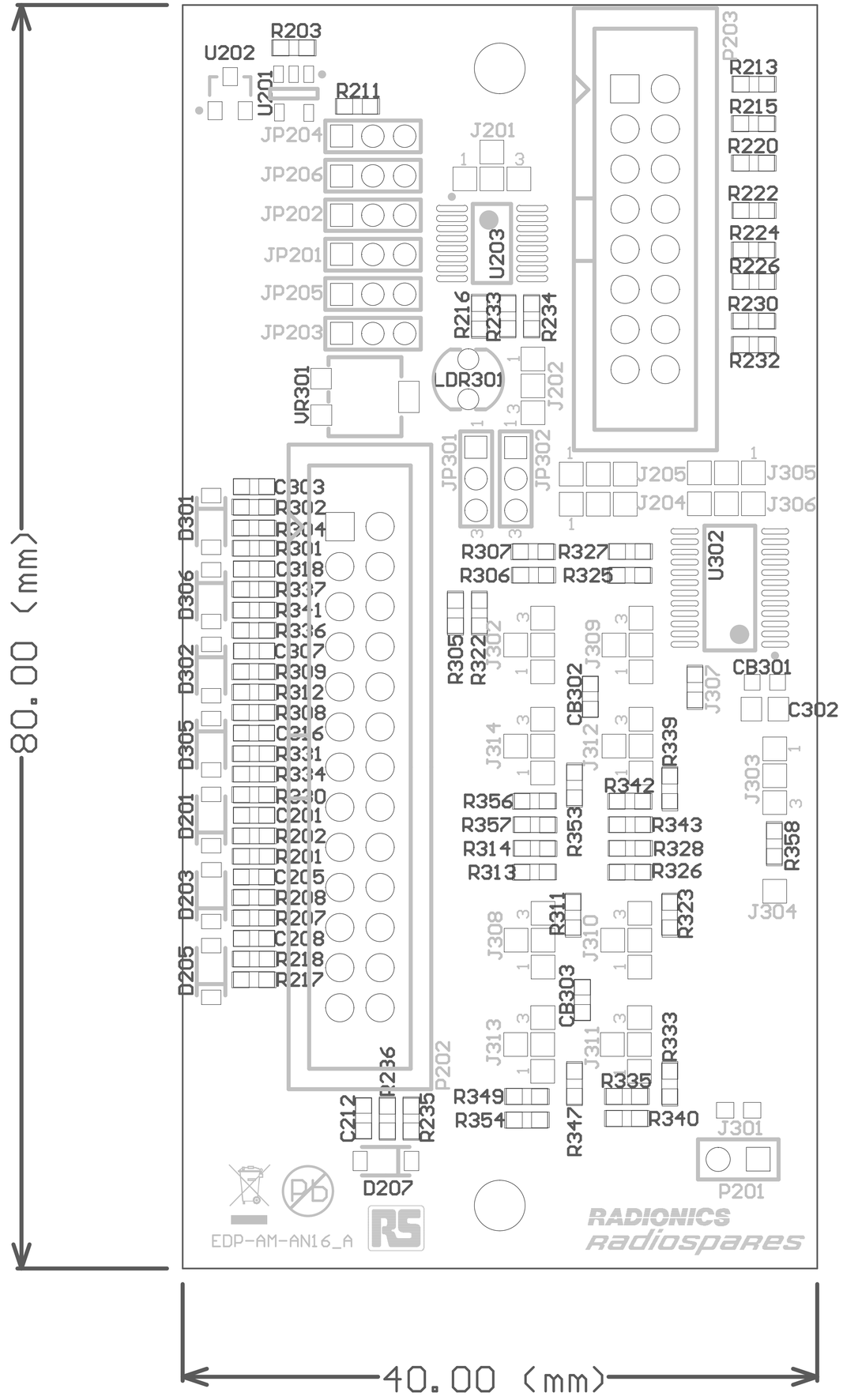
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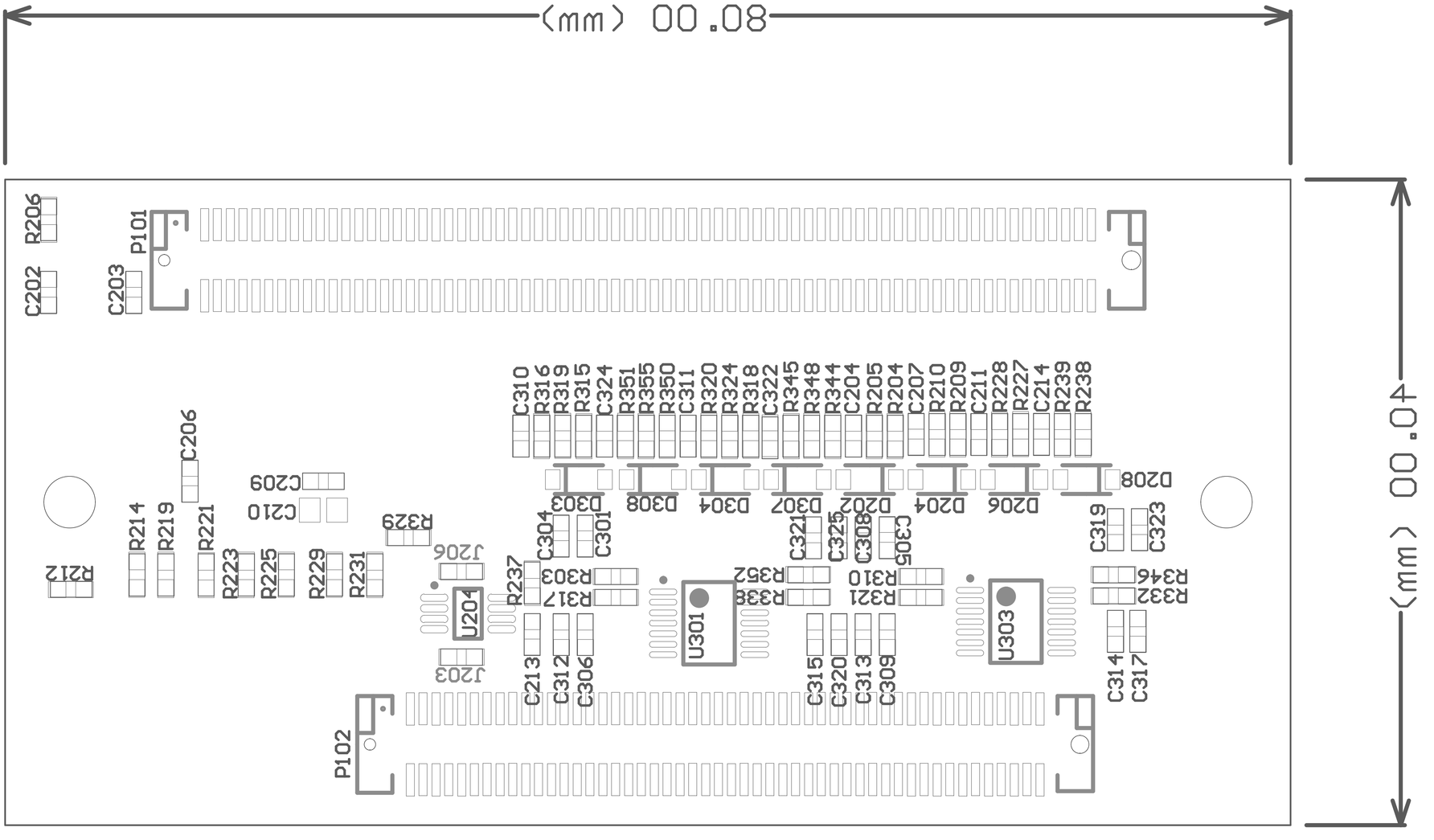
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