EDK2638

USER MANUAL

FOR H8S/2638UF
ON-CHIP FLASH MICROCONTROLLER

Preface

Cautions

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Document Information

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Global: http://www.hitachisemiconductor.com

Europe: http://www.hmse.com

1. TABLE OF CONTENTS

2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

http://www.hmse.com/products/edk/support/

Installing the EDK requires power and serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer requires 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

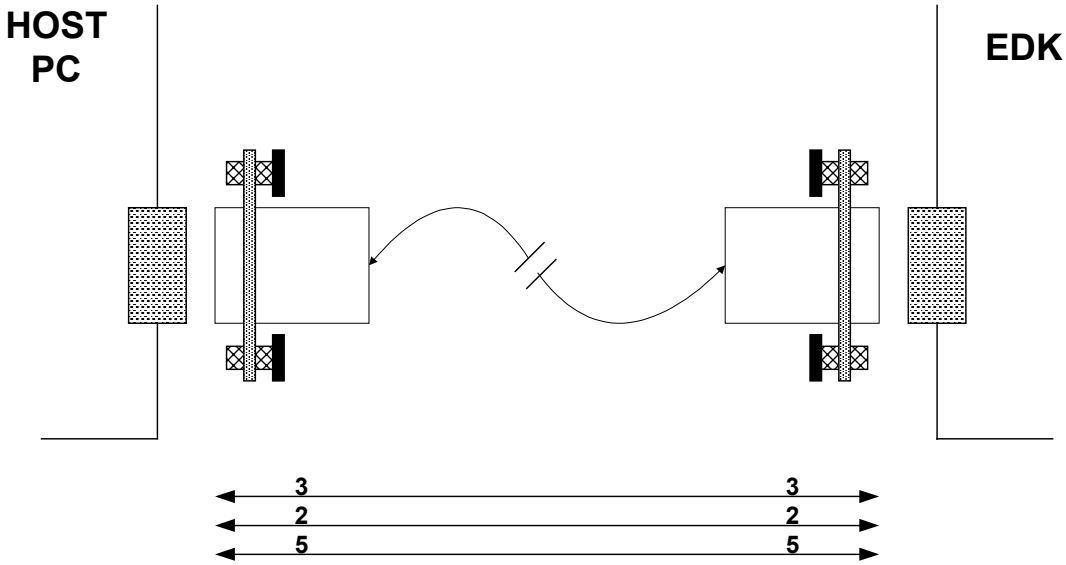


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.

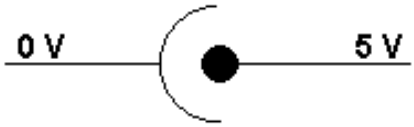


FIGURE 2-1: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

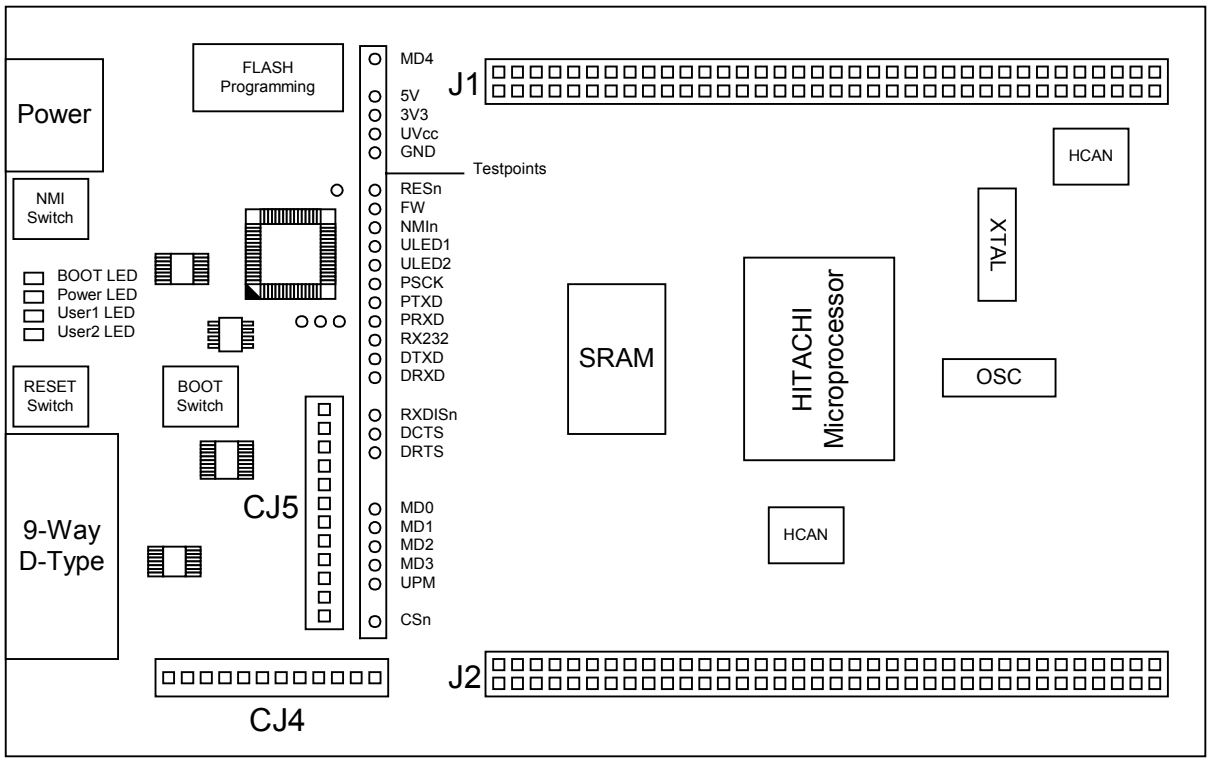


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

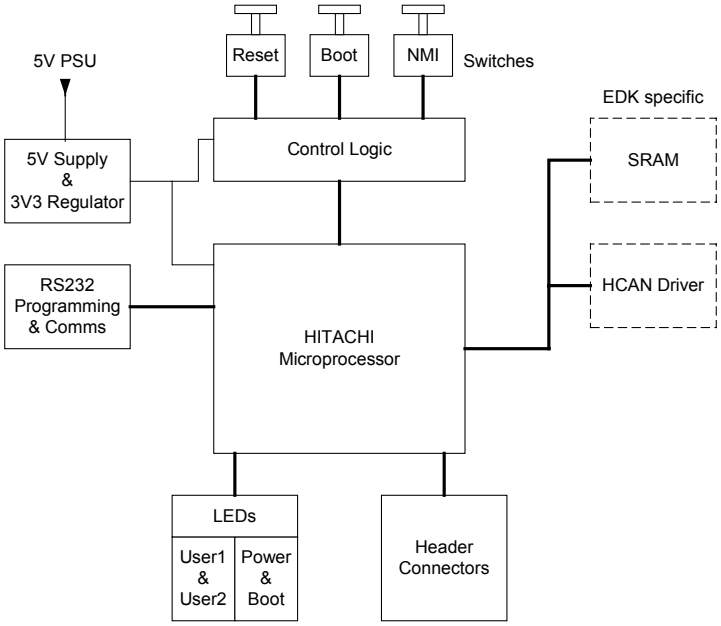


FIGURE 3-1: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides three buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a timed reset pulse of at least 250mS.

2. Boot Switch

This button toggles the operating mode of the microcontroller. A complete description of this function is given in section 5.6.

3. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no minimum or maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial interface on the EDK board has several functions. The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins. Other board option links allow users to control the entry and exit from boot mode using the same handshaking signals. Refer to section 5 for details on setting serial interface options.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

EDK DB9 Connector Pin	Signal	Host DB9 Connector Pin
1	No Connection	1
2	EDK Tx Host Rx	2
3	EDK Rx Host Tx	3
4	No Connection	4
5	Ground	5
6	No Connection	6
7	* EDK CTS Host RTS	7
8	* EDK RTS Host CTS	8
9	No Connection	9

TABLE 4-1: RS232 INTERFACE CONNECTIONS

* These are not connected on the EDK by default. See section 5.4 for more details.

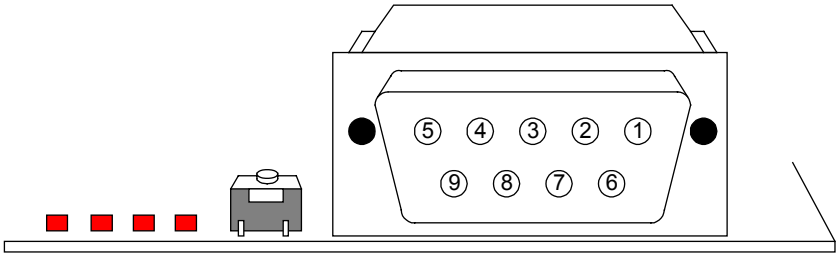


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 18.432MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

Baud Rate Register Settings for Serial Communication Rates												
SMR Setting:	**0**			**1**			**2**			**3**		
Comm. Baud	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**
110	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	81	109.76	-0.22
300	invalid	invalid	invalid	invalid	invalid	invalid	119	300	0.00	29	300	0.00
1200	invalid	invalid	invalid	119	1200	0.00	29	1200	0.00	7	1125	-6.25
2400	239	2400	0.00	59	2400	0.00	14	2400	0.00	3	2250	-6.25
4800	119	4800	0.00	29	4800	0.00	7	4500	-6.25	1	4500	-6.25
9600	59	9600	0.00	14	9600	0.00	3	9000	-6.25	invalid	Invalid	invalid
19200	29	19200	0.00	7	18000	-6.25	1	18000	-6.25	invalid	Invalid	invalid
38400	14	38400	0.00	3	36000	-6.25	invalid	invalid	invalid	invalid	invalid	invalid
57600	9	57600	0.00	2	48000	-16.67	invalid	invalid	invalid	invalid	invalid	invalid
115200	4	115200	0.00	0	144000	25.00	invalid	invalid	invalid	invalid	invalid	invalid
230400*	2	192000	-16.67	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid
460800*	0	576000	25.00	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid

TABLE 4-1 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

** Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.*

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

Component	Cct. Ref	Value	Rating	Manufacturer
Load Resistor (X1)	R19	1MΩ	0805 1%	Welwyn WCR Series
Load Resistor (X2)	R22	1MΩ	0805 1%	Welwyn WCR Series
Load capacitors (X1)	C16,C17	15pF	0603 10% 25V	AVX 0603 3 A 150 KAT
Load capacitors (X2)	C19,C20	15pF	0603 10% 25V	AVX 0603 3 A 150 KAT

TABLE 4-1: REMOVABLE COMPONENT INFORMATION

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SRAM

The SRAM device fitted to the board is a 4Mbit device allowing 256kx16 or 256kx8 operation.

Address line 0 (A0) of the H8S/2638 is connected to the A0 line of the SRAM to allow both 8 bit and 16 bit accesses, as supported by the H8S/2638. Although each address line on the SRAM references 16-bits, A0 on the H8S/2638 references 8-bits. As such, the available address space is halved from 4Mbit to 2Mbit.

Provision has been made for disabling the connection between the glue logic and the lower-byte select of the SRAM via jumper link CJ4 (pins 10-12).

Fitting the jumper in the default position (10-11) allows the lower byte of the SRAM to be selected during memory access. When a read is performed, the glue logic enables both the upper and lower byte select lines, in both 8-bit and 16-bit mode. By fitting the jumper in position (11-12), the output from the glue logic is disabled, and the low byte select line on the SRAM is pulled high via a 4k7 resistor and the lower half of the data bus is unused.

The H8S/2638 microcontroller multiplexes the functions of Port-A bit-1 (PA1) between the external address bus A17 and Serial Port 2 transmit pin. The EDK is configured to allow access to the SRAM by default. This means that A17 is normally available to the SRAM. R5 connects PA1 on the microcontroller to address line A17 on the SRAM. Removing this link disables A17 on the SRAM and allows the use of PA1 on the Microcontroller.

Option Jumpers for PA1		
Zero-ohm link	**Default**	**Function**
R5	Fitted	PA1 connected to SRAM A17

The H8S/2638 microcontroller has no chip-select management built in. There is no external chip selection hardware associated with this device. The chip select of the SRAM is connected to address strobe (AS) of the microcontroller.

In 8 bit mode, the address range is H'40 000 – H'7F FFF in area 0, (h'40 000 + h'3F FFF (256K)) using A0 to A17

In 16-bit mode, the address range is H'40 000 – H'7F FFF in area 0, (h'40 000 + h'3F FFF (256K)) using A1 to A17

Aliasing of the address space is possible in areas (Area1 - Area7) as the address strobe is used as a chip select for the SRAM without address decoding.

To use 16-bit mode, ensure that A0 line of the H8S/2638 is not used to drive A0 of the SRAM, as A0 may not be resolved in time for 16 bit addresses. A0 should be tied high by the microcontroller by setting Port-C bit-0 as an input, and setting the internal MOS pull up register to pull this bit high.

4.4. MEMORY MAP

Table 4-1 illustrates the EDK memory map for mode 2.

Section End **Section Start**	**Section Allocation**
H'0000 0000 H'0003 FFFF	On-Chip ROM
H'0004 0000 H'0007 FFFF	External SRAM
H'0008 0000 H'00FF AFFF	Reserved
H'00FF B000 H'00FF EFBF	On-Chip RAM
H'00FF EFC0 H'00FF F7FF	Reserved
H'00FF F800 H'00FF FF3F	I/O Registers
H'00FF FF40 H'00FF FF5F	Reserved
H'00FF FF60 H'00FF FFBF	I/O Registers
H'00FF FFC0 H'00FF FFFF	On-Chip RAM

TABLE 4-1: MEMORY MAP (DEFAULT MODE 2)

4.5. SRAM ACCESS TIMING

External access timing is defined by several registers, allowing different types of devices to be addressed. The registers for the selection of wait states and signal extensions are given below with recommended values for the EDK.

Register	Address	Recommended Setting for EDK	Function
ABWCR	FED0	H'FE	Address Bus Width Control Register (Set Area 0(SRAM) to 16-bit access)
ASTCR	FED1	H'FF	Access State Control Register (Initial values - 3 State Access)
WCRL	FED3	H'FC	Wait Control Register (Wait not inserted when external space area 0 is accessed)
BCRH	FED4	H'10	Bus Control Register (No Idle cycle added in external access)
PFCR	FDEB	H'0A	Pin Function Control Register (Enable A8–A17 address output)

TABLE 4-1: SRAM ACCESS CONTROL REGISTERS

Please refer to the hardware manual for the microcontroller for more information on these register settings.

4.6. LEDS

The EDK has four red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate. The Boot mode indication LED will illuminate when the microcontroller has been placed into Boot mode. Please see section 0 for more details of this function.

There are two LEDs dedicated for user control these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical high state.

The user LEDs are connected to the following ports:

LED Identifier	Port Pin	Microcontroller Pin	Pin Functions on Port Pin
USR1	P14	93	P14/PO12/TIOCA1/IRQ0
USR2	P15	94	P15/PO13/TIOCB1/TCLKC

TABLE 4-1: LED PORT CONNECTIONS

5. BOARD OPTIONS

The EDK has a number of configuration settings set by jumpers CJ4 (A, B, C, D) CJ5 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.3 and 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

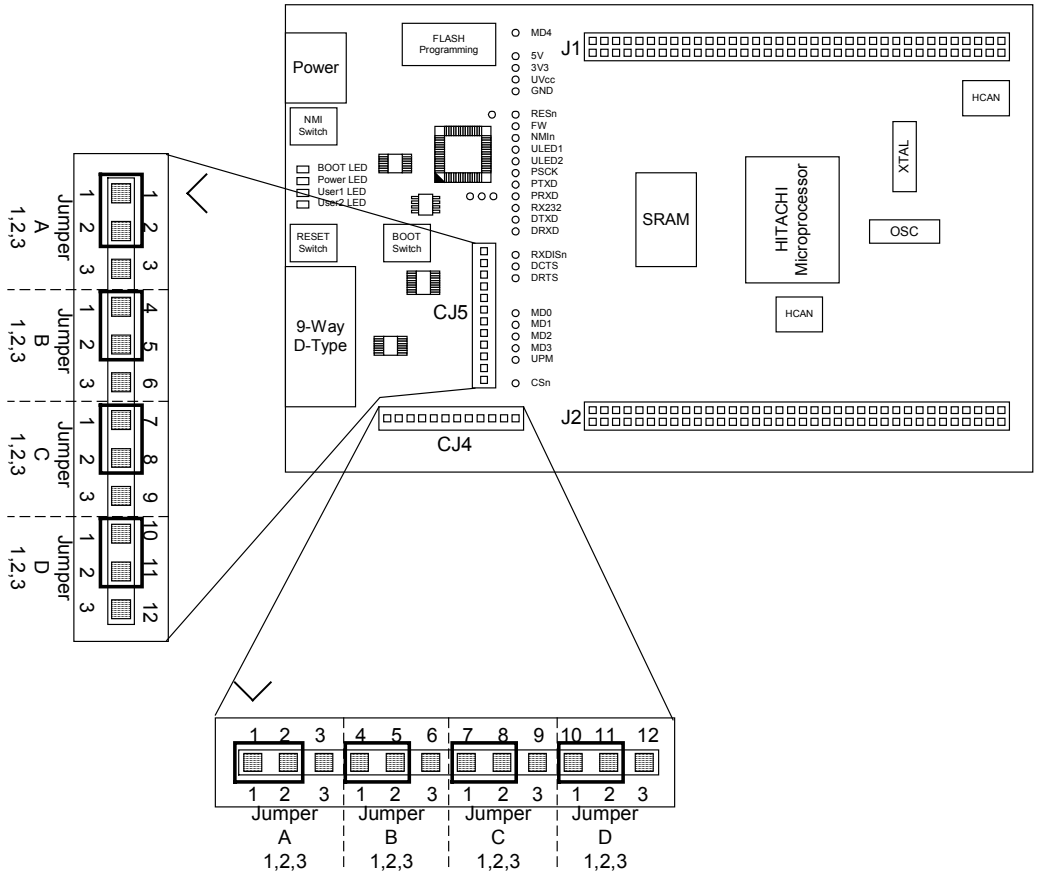


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. USER MODE SETTINGS – CJ5

CJ5 is used to set the operating mode of the microcontroller.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 5-A Default 2-3	User Mode Setting Bit 0	MD0 pulled High	**MD0 pulled Low**
CJ 5-B Default 1-2	User Mode Setting Bit 1	**MD1 pulled High**	MD1 pulled Low
CJ 5-C Default 1-2	User Mode Setting Bit 2	**MD2 pulled High**	MD2 pulled Low
CJ 5-D Default 1-2	User Mode Setting Bit 3	**MD3 pulled High**	MD3 pulled Low

TABLE 5-1: USER MODE: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

The default settings indicated in bold text place the microcontroller into Mode 2 and specify a 4x multiplier applied to the external clock frequency for both the peripheral devices and the CPU.

5.3. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 4-A Default 2-3	Serial Receive Source	Disables the RS232 receive signal to enable the use of the Flash Programming Header	**Enables the RS232 receive signal. The Flash Programming Header* must not be used in this state.**
CJ 4-B Default 2-3	User Programming Mode	Disables the Flash write hardware protection. The flash can be overwritten in User Mode.	**Enables the Flash write hardware protection. The flash can not be overwritten in User Mode.**
CJ 4-C Default 2-3	Not Used	Not Used	Not Used
CJ 4-D Default 1-2	Lower Byte Select Enable	**Connects the Lower Byte select line of the SRAM to the Glue-logic**	Disconnects the Lower Byte select line of the SRAM from the Glue-logic and pulls it high

TABLE 5-1: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.5

The following table lists the connections to each jumper pin.

Pin	Net Name	Description
1	UVCC	Microcontroller Supply Voltage
2	RXDISn	Disable Flash Header functions. Pulled low. (Enables RX232)
3	No Connection	No Connection
4	UVCC	Microcontroller Supply Voltage
5	UPM	CPLD Controlled option to set Flash Write (FW). Pulled low.
6	No Connection	No Connection
7	No Connection	No Connection
8	CSn	Chip Select of the SRAM, may be pulled-up to Uvcc by fitting R8
9	No Connection	No Connection
10	LBnLOGIC	Low Byte Select from the Glue logic
11	LBn	Low Byte Select of the SRAM, pulled high via R7 (4K7)
12	No Connection	No Connection

5.4. SERIAL PORT SELECTION

The programming serial port is connected to the RS232 connector by default. This allows direct programming of the EDK using the supplied software tools. A secondary serial port is available on the microcontroller and can be connected to the RS232 connector by changing some board option links. The additional port option allows the user to write messages or connect to other devices via the serial port while programming support is provided by the Flash programming header.

The following surface mount, zero-ohm link settings are fitted by default and connect the RS232 header to the programming serial port of the microcontroller.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Fitted	Transmit data from EDK	P33
CR23	Fitted	Receive data to EDK	P34
CR19	Not Fitted	Alternate Transmit data from EDK	P30
CR22	Not Fitted	Alternate Receive data to EDK	P31

TABLE 5-1: OPTION LINKS – DEFAULT SETTINGS

To enable the use of this alternate port the user must change the settings to those in the following table.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Not Fitted	Transmit data from EDK	P33
CR23	Not Fitted	Receive data to EDK	P34
CR19	Fitted	Alternate Transmit data from EDK	P30
CR22	Fitted	Alternate Receive data to EDK	P31

TABLE 5-2: OPTION LINKS – ALTERNATE SERIAL PORT

The user may implement a handshaking protocol on the EDK. This is not supported with the software tools supplied. To support this option two spare port pins have been allocated on the microcontroller. Using these port pins the CTS and RTS lines of the host serial interface can be controlled.

The user may also control the operation of the board via the same handshaking lines. This is not supported with the software tools supplied but may be written by the user. Using the CTS line the user may simulate pressing the boot button, see section:5.6. This will cause the EDK to swap into and out of Boot mode on each low-level activation of CTS. Feedback of the current mode is provided on the RTS line. A high level indicates boot mode and a low level indicates user mode.

The following settings are made by default, and ensure that there are no conflicts on unnecessary microcontroller pins.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR12	Not Fitted	Mode State out from EDK	N/A (From CPLD*)
CR7	Not Fitted	Change Mode request to EDK	N/A (From CPLD*)
CR16	Not Fitted	Alternate RTS232 – Ready to send – from EDK	P16
CR13	Not Fitted	Alternate CTS232 – Clear to send – to EDK	P17

TABLE 5-3: OPTION LINKS – SERIAL PORT CONTROL

* See section 5.6

Note: These setting pairs are exclusive:
If CR12 and CR7 are fitted; CR16 and CR13 must not be fitted.
If CR16 and CR13 are fitted; CR12 and CR7 must not be fitted.

5.5. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Hitachi Flash Debug Board (FDB). The FDB is a USB based programming tool for control and programming of Hitachi microcontrollers, available separately from Hitachi. This header provides direct access for the FDB to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Disable the RX232 signal from the RS232 transceiver.
   Jumper link CJ4-A is provided for this purpose. Please refer to section5.3.
2. Disable User Program Mode using jumper CJ4-B. Please refer to section5.3.

Caution: Do not operate the board with the user mode jumpers removed and the FDB disconnected, as the microcontroller mode pins will float to an indeterminate state. This may damage the microcontroller device.

5.6. BOOT CONTROL

The method for placing the microcontroller device in to Boot mode for reprogramming has been incorporated into a complex programmable logic device (CPLD). This is not necessary for most user designs but allows a measure of increased flexibility for the EDK designs. Mode transitions including boot mode transitions only require the reset to be held active while the mode settings are presented. On releasing reset the microcontroller will be in the required mode.

The logic design detects a power up event and provides a timed reset pulse to guarantee the reset of the device. At the end of the rest pulse the processor will be placed in user mode and any code in the device will execute.

During user mode the NMI button can be pressed at any time. This will provide a single de-bounced NMI interrupt to the device.

Pressing the boot button will cause the boot mode controller to reset the device and, during the reset period, present the required mode settings to start the device in boot mode. At the end of the reset period the boot mode settings will have been latched into the device, which will then be ready to accept a boot mode connection via the RS232 interface or the flash programming header. Pressing the boot button during a normal reset will not cause the EDK to enter boot mode.

The boot mode settings are fixed at mode 2. The required mode settings are made using a tri-state capable buffer.

Note: The boot control device is programmed to support all possible EDK products.
For this reason the reset pulse is over 500ms. Repetitive activation of either the Boot or Reset buttons will restart the reset timer and extend the reset period. Pressing the boot button within the 500mS period of a reset will not cause the board to enter boot mode.

5.6.1. CPLD CODE

The code is based upon a four state machine providing a guaranteed reset period, which can be extended by holding the relevant control input in the active state. When released the timer will extend the reset for approximately 500mS.

The states are split into two functions, one for User mode and one for Boot mode. The first state of each is used to hold the reset line active. When the timer expires then the second state is used to hold the device in the selected mode and wait for an external control signal to either move back into the user reset state or into the boot reset state.

5.6.2. STATE DIAGRAM

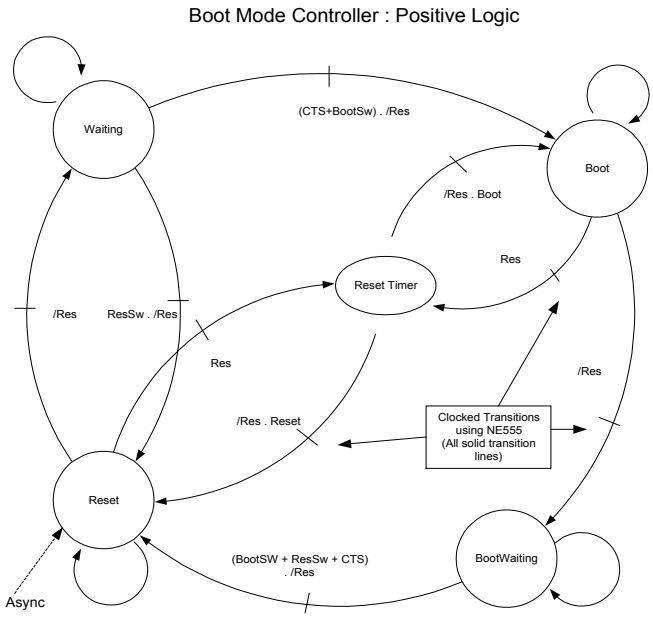


FIGURE 5-1: CPLD STATE DIAGRAM

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each or the headers on the board.

6.1. HEADER J1

Pin No	Function (mode6)	EDK Symbol	Device pin	Pin No	Function (mode6)	EDK Symbol	Device pin
1	D15	PD7	17	2	D14	PD6	18
3	PC1/A1	PC1	15	4	PC0/A0	PC0	16
5	PC3/A3	PC3	13	6	PC2/A2	PC2	14
7	PC5/A5	PC5	11	8	PC4/A4	PC4	12
9	PC7/A7	PC7	9	10	PC6/A6	PC6	10
11	PA2/A18/RxD2	PA2	7	12	PA3/A19/SCK2	PA3	8
13	PA0/A16	PA0	5	14	PA1/A17/TxD2	PA1	6
15	NC	NC3	3	16	NC	NC4	4
17	VCC	UVcc	1	18	VCC	UVcc	2
19	VSS	Ground	127	20	PB0/A8/TIOCA3	PB0	128
21	PB2/A10/TIOCC3	PB2	125	22	PB1/A9/TIOCB3	PB1	126
23	PB4/A12/TIOCA4	PB4	123	24	PB3/A11/TIOCD3	PB3	124
25	PB6/A14/TIOCA5	PB6	121	26	PB5/A13/TIOCB4	PB5	122
27	PF0/IRQ2	PF0	119	28	PB7/A15/TIOCB5	PB7	120
29	MD1	MD1	117	30	MD2	MD2	118
31	AVSS	CON_AVSS	115	32	MD0	MD0	116
33	P92/AN10	P92	113	34	P93/AN11	P93	114
35	P90/AN8	P90	111	36	P91/AN9	P91	112
37	P46/AN6/DA0	P46	109	38	P47/AN7/DA1	P47	110
39	P44/AN4	P44	107	40	P45/AN5	P45	108
41	P42/AN2	P42	105	42	P43/AN3	P43	106
43	P40/AN0	P40	103	44	P41/AN1	P41	104
45	AVCC	CON_AVCC	101	46	VREF	CON_VREF	102
47	VSS	VSS	99	48	NC	NC100	100
49	HTxD0	HTxD0	97	50	HRxD0	HRxD0	98
51	P16/PO14/TIOCA2/ IRQ1	DRTS	95	52	P17/PO15/TIOCB2/ TCLKD	DCTS	96
53	P14/PO12/TIOCA1/ IRQ0	ULED1	93	54	P15/PO13/TIOCB1/ TCLKC	ULED2	94
55	P12/PO10/TIOCC0/ TCLKA/A22	P12	91	56	P13/PO11/TIOCD0/ TCLKB/A23	P13	92
57	P10/PO8/TIOCA0/A20	P10	89	58	P11/PO9/TIOCB0/A21	P11	90
59	STBY	STBYn	87	60	PF7/ø	PF7/ø	88
61	EXTAL	CON_EXTAL	85	62	FWE	FWE	86
63	XTAL	CON_XTAL	83	64	VSS	VSS	84

6.2. HEADER J2

Pin No	Function (mode6)	EDK Symbol	Device pin	Pin No	Function (mode6)	EDK Symbol	Device pin
1	D13	PD5	19	2	D12	PD4	20
3	D11	PD3	21	4	D10	PD2	22
5	D9	PD1	23	6	VCC	VCC	24
7	D8	PD0	25	8	VSS	VSS	26
9	PE7/D7	PE7	27	10	PE6/D6	PE6	28
11	PE5/D5	PE5	29	12	PE4/D4	PE4	30
13	PE3/D3	PE3	31	14	PE2/D2	PE2	32
15	PE1/D1	PE1	33	16	PE0/D0	PE0	34
17	VSS	UVcc	35	18	VSS	Ground	36
19	HRxD1	HRxD1	37	20	HTxD1	HTxD1	38
21	AS	CSn	39	22	RD	RD	40
23	HWR	HWR	41	24	PF3/LWR/ADTRG/IRQ3	PF3	42
25	VSS	VSS	43	26	PWMVSS	PWMVSS	44
27	PH0/PWM1A	PH0	45	28	PH1/PWM1B	PH1	46
29	PH2/PWM1C	PH2	47	30	PH3/PWM1D	PH3	48
31	PWMVCC	PWMVCC	49	32	PH4/PWM1E	PH4	50
33	PH5/PWM1F	PH5	51	34	PH6/PWM1G	PH6	52
35	PH7/PWM1H	PH7	53	36	PWMVSS	PWMVSS	54
37	PJ0/PWM2A	PJ0	55	38	PJ1/PWM2B	PJ1/	56
39	PJ2/PWM2C	PJ2	57	40	PJ3/PWM2D	PJ3/	58
41	PWMVCC	PWMVCC	59	42	PJ4/PWM2E	PJ4/	60
43	PJ5/PWM2F	PJ5	61	44	PJ6/PWM2G	PJ6	62
45	PJ7/PWM2H	PJ7	63	46	PWMVSS	PWMVSS	64
47	P30/TxD0	DTXD	65	48	P31/RxD0	DRXD	66
49	VSS	Ground	67	50	VSS	Ground	68
51	P32/SCK0/SDA1/ IRQ4	P32	69	52	P33/TxD1/SCL1	PTXD	70
53	P34/RxD1/SDA0	PRXD	71	54	P35/SCK1/SCL0/ IRQ5	PSCK	72
55	RES	RESn	73	56	NMI	NMIn	74
57	PLLCAP	NC75	75	58	VSS	Ground	76
59	PLLVSS	PLLVSS	77	60	OSC2	CON_OSC2	78
61	OSC1	CON_OSC1	79	62	VCC	UVcc	80
63	VCC	UVcc	81	64	VCL	NC82	82

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support Advanced Expanded Mode only. HMON supports Modes 6 and 7.

7.1.2. BREAKPOINT SUPPORT

The monitor utilises the PC Break Controller for code located in ROM, allowing a single breakpoint to be set in the code. Code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

7.1.2.1. CODE LOCATED IN FLASH / ROM

Double clicking in the breakpoint column in the code sets the breakpoint. Adding a further breakpoint elsewhere in the code removes the previous one.

7.1.2.2. CODE LOCATED IN RAM

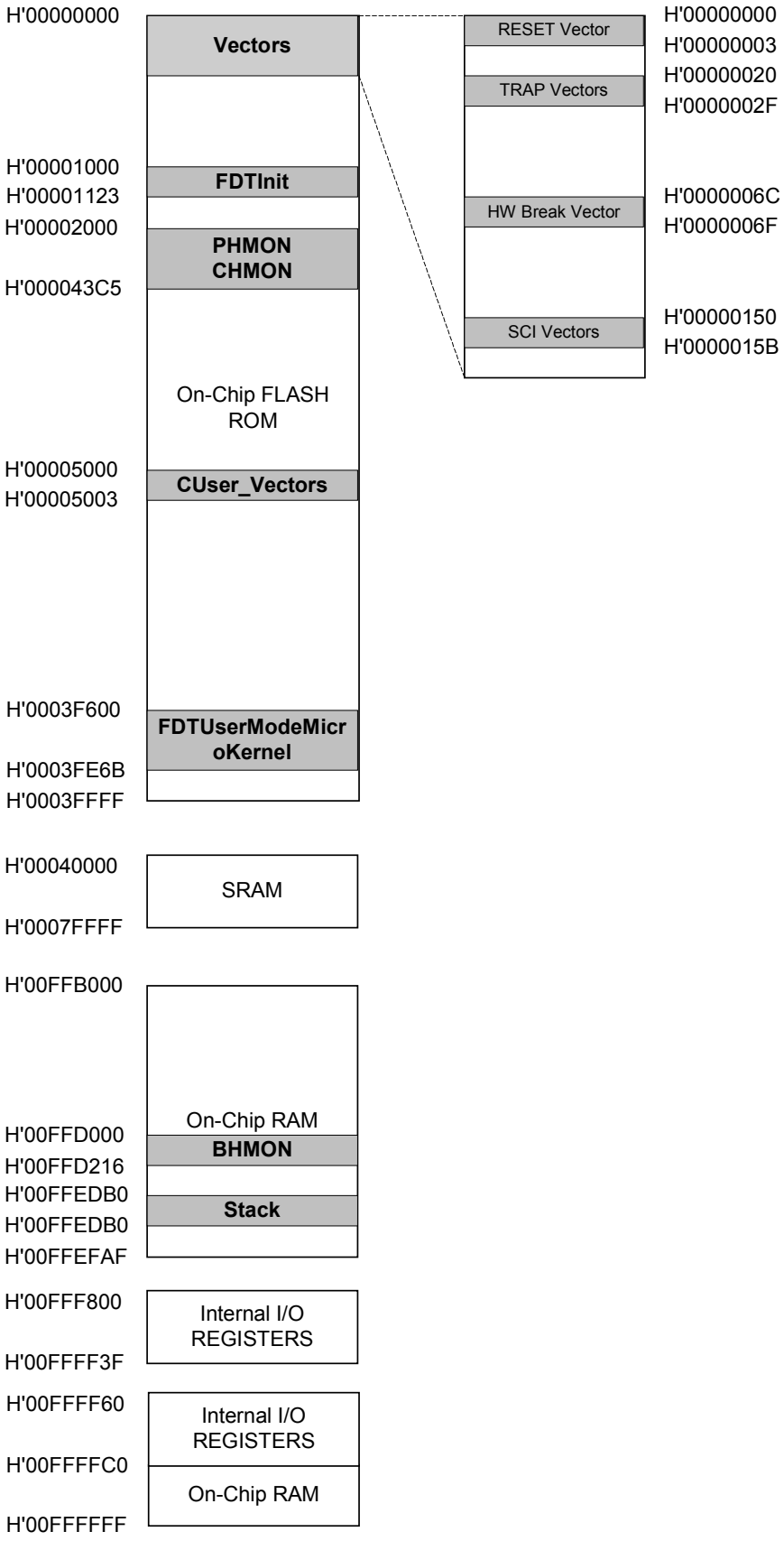
Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 000000000	4
TRAP_VECTORS	Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM	H' 00000020	10
HW_BREAK_VECTORS	HMON Break Controller (Vector 27) Required by HMON to create Breakpoints in ROM	H' 0000006C	4
SCI_VECTORS	HMON Serial Port Vectors (Vector 84, 85, 86, 87) Used by HMON when EDK is configured to connect to the default serial port.	H' 00000150	C
PHMON	HMON Code	H' 00002000	2288
CHMON	HMON Constant Data	H' 00004288	13e
BHMON	HMON Uninitialised data	H' 00FFD000	217
FDTInit	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 00001000	124
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0003F600	86C
CUser_Vectors	Pointer used by HMON to point to the start of user code.	H' 00005000	4

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

HMON has an interrupt priority of 6. The serial port has an interrupt priority of 7. Modules using interrupts should be set to lower than this value (6 or below), so that serial communications and debugging capability is maintained.

7.2. ADDITIONAL INFORMATION

For details on how to use Hitachi Embedded Workshop (HEW), with HMON, `refer to the HEW manual and the HMON User Manual, available on the CD or from the web site.

For information about the H8S/2638 series microcontrollers refer to the H8S/2638 *Series Hardware Manual*

For information about the H8S/2638 assembly language, refer to the H8S *Series Programming Manual*

Further information available for this product can be found on the HMSE web site at:

http://www.hmse.com/products/support.htm

General information on Hitachi Microcontrollers can be found at the following URLs.

Global: http://www.hitachisemiconductor.com

Europe: http://www.hmse.com