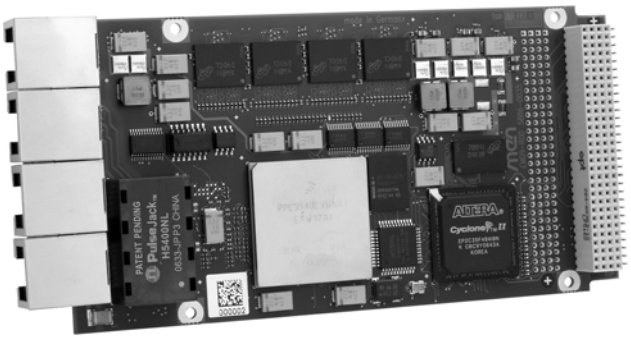
Embedded Solutions

EM9/EM9A – Embedded System Modules with MPC8548



EM9

Configuration example
(shown without heat sink)

EM9A

Configuration example
(shown without heat sink)

User Manual

mikro elektronik
gmbh · nürnberg

EM9/EM9A – Embedded System Modules with MPC8548

The EM9/EM9A is a complete embedded SBC for use on any carrier board in different industrial environments. The final application consists of a stand-alone EM9/EM9A, an EM9/EM9A with an application-specific carrier card and/or with additional PCI-104 modules (EM9).

The EM9/EM9A is controlled by an integrated PowerPC® MPC8548 or MPC8543 processor (optionally with encryption unit) running at clock frequencies between 800 MHz and 1.5 GHz.

The EM9/EM9A is equipped with soldered DDR2 SDRAM for data and with NAND Flash for program storage. The EM9 provides front-panel access for three Gigabit Ethernet channels and one COM port via four RJ45 connectors, while the EM9A provides access for three Gigabit Ethernet channels and two COM ports via its I/O connector J3.

Additional functionality such as graphics, touch, CAN bus, protocol converters etc. can be realized in an FPGA for the needs of the individual application. The corresponding connectors are available on a carrier board. Application software dynamically loads the functions of the FPGA.

The EM9/EM9A comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

The EM9/EM9A is a communication engine ideal for use in embedded applications, for instance as an embedded Linux server, but also for high-end automation and robot control under a real-time operating system.

For a first evaluation of the functions of the EM9/EM9A we strongly recommend to use the EK9 ESM™ starter kit. The kit consists of the standard EM9 module, an FPGA loaded with additional I/O functions, the carrier card with I/O connectors, an external PSU, cables, and an adapter for mounting a PCI-104 module.

ESM™ modules consist of the hardware (CPU, chip set, memory, I/O) which is not fixed to any application-specific function, and an FPGA programmed in VHDL code, which provides I/O that is also still independent of a specific application. ESM™ modules are based on PCI. They have two or three system connectors: J1 has a fixed signal assignment, while J2 is variable depending on the final application-specific configuration of the ESM™ and the carrier board. J2 also feeds the I/O signals of the functions programmed in the FPGA to the carrier card. Some ESM™ modules have an additional J3 connector that is used to replace the front I/O connectors to route the signals to the carrier board or to the backplane of a CPCI or VME system.

Technical Data

EM9

CPU

- PowerPC® PowerQUICC™ III MPC8548, MPC8548E, MPC8543 or MPC8543E
  - 800MHz up to 1.5GHz
  - For more information on available standard versions see online data sheet.
  - See also Configuration Options.
  - e500 PowerPC® core with MMU and double-precision embedded scalar and vector floating-point APU
  - Integrated Northbridge and Southbridge

Memory

- 2x32KB L1 data and instruction cache, 512KB/256KB L2 cache integrated in MPC8548/MPC8543
- Up to 2GB SDRAM system memory
  - Soldered
  - DDR2
  - Up to 300 MHz memory bus frequency, depending on CPU
- Up to 1GB soldered NAND Flash (and more), FPGA-controlled
- 32MB additional DDR2 SDRAM, FPGA-controlled, e.g. for video data and NAND Flash firmware
- 16MB boot Flash
- 128KB non-volatile FRAM
- Serial EEPROM 4kbits for factory settings

Mass Storage

- Parallel IDE (PATA)
  - One port for hard-disk drives
  - Available via I/O connector
  - FPGA-controlled
  - PIO mode 0 and UDMA mode 5 (UDMA100) support
- Up to 1GB soldered ATA NAND Flash (and more), FPGA-controlled

Graphics

- Available via I/O connector
- FPGA-controlled
- 800 x 600, 60Hz/75Hz, 6-bit RGB

I/O

- Three Ethernet channels
  - Three 10/100/1000Base-T Ethernet channels with MPC8548/E
  - Two 10/100/1000Base-T Ethernet channels with MPC8543/E
  - Three RJ45 connectors at front panel
  - Six onboard LEDs to signal LAN Link and Activity
- One RS232 UART (COM1)
  - One RJ45 connector at front panel
  - Data rates up to 115.2kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS; or: COM2, without any COM handshake lines
- Further I/O depending on FPGA configuration

Front Connections

- Three Ethernet (RJ45)
- One RS232 UART COM1 (RJ45)

FPGA

- Standard factory FPGA configuration:
  - Main bus interface
  - Interrupt controller, reset controller
  - 16Z070_IDEDISK – IDE controller for NAND Flash
  - 16Z043_SDRAM – Additional SDRAM controller (32MB DDR2)
  - 16Z016_IDE – IDE controller (PIO mode 0 and UDMA mode 5)
  - 16Z044_DISP – Display controller (800 x 600, 60Hz/75Hz, 6-bit RGB)
  - 16Z031_SPI – SPI touch panel controller
  - 16Z125_UART – UART controller (controls COM10..COM12)
  - 16Z034_GPIO – GPIO controller (8 I/O lines, system control signals)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

PCI Interface

- 32-bit, 33/66-MHz PCI interface at PCI-104 connectors J1 and J2
- Compliant with PCI Specification 2.2
- Support of four external masters

Miscellaneous

- Real-time clock
- Temperature sensor, power supervision and watchdog

Electrical Specifications

- Supply voltage/power consumption:
  - +5V (-2%/+5%), 2A typ.
  - +3.3V (-2%/+5%), 0.5A typ.

Mechanical Specifications

- Dimensions: conforming to ESM™ specification (PCB: 149mm x 71mm), Type I-S, except height: approx. 1mm higher than standard
- Weight: 108g (w/o heat sink); standard heat sink: 142g

Environmental Specifications

- Temperature range (operation):
  - -40..+85°C (screened)
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 1g/10..150Hz
- Conformal coating on request

MTBF

- 245,671h @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

BIOS

- MENMON™

Software Support

- Linux
- VxWorks®
- QNX®
- INTEGRITY® (Green Hills® Software)
- OS-9® (on request)
- For more information on supported operating system versions and drivers see online data sheet.

EM9A

CPU

- PowerPC® PowerQUICC™ III MPC8548, MPC8548E, MPC8543 or MPC8543E
  - 800MHz up to 1.5GHz
  - For more information on available standard versions see online data sheet.
  - See also Configuration Options.
  - e500 PowerPC® core with MMU and double-precision embedded scalar and vector floating-point APU
  - Integrated Northbridge and Southbridge

Memory

- 2x32KB L1 data and instruction cache, 512KB/256KB L2 cache integrated in MPC8548/MPC8543
- Up to 2GB SDRAM system memory
  - Soldered
  - DDR2
  - Up to 300 MHz memory bus frequency, depending on CPU
- Up to 1GB soldered NAND Flash, FPGA-controlled
- 32MB additional DDR2 SDRAM, FPGA-controlled, e.g. for video data and NAND Flash firmware
- 16MB boot Flash
- 128KB non-volatile FRAM
- Serial EEPROM 4kbits for factory settings

Mass Storage

- Parallel IDE (PATA)
  - One port for hard-disk drives
  - Available via I/O connector J2
  - FPGA-controlled
  - PIO mode 0 and UDMA mode 5 (UDMA100) support
- Up to 1GB soldered ATA NAND Flash, FPGA-controlled

Graphics

- Available via I/O connector J2
- FPGA-controlled
- 800 x 600, 60Hz/75Hz, 6-bit RGB

I/O

- Three Ethernet channels
  - Three 10/100/1000Base-T Ethernet channels with MPC8548/E
  - Two 10/100/1000Base-T Ethernet channels with MPC8543/E
  - On board-to-board connector J3

- Two RS232 UARTs (COM1/COM2)
  - On board-to-board connector J3
  - Data rates up to 115.2kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS
- Further I/O depending on FPGA configuration

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- Real-time clock
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Electrical Specifications

- Supply voltage/power consumption:
  - +5V (-2%/+5%), 2A typ.
  - +3.3V (-2%/+5%), 0.5A typ.

Mechanical Specifications

- Dimensions: conforming to ESM™ specification (PCB: 149mm x 71mm), Type II-N, except height: approx. 1mm higher than standard
- Heat sink is always tailor-made to the customer's needs (no heat sink included in standard version)
- Weight: 90g (w/o heat sink)

Environmental Specifications

- Temperature range (operation):
  - -40..+85°C (screened), with appropriate heat sink
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
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- Vibration (sinusoidal): 1g/10..150Hz
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BIOS

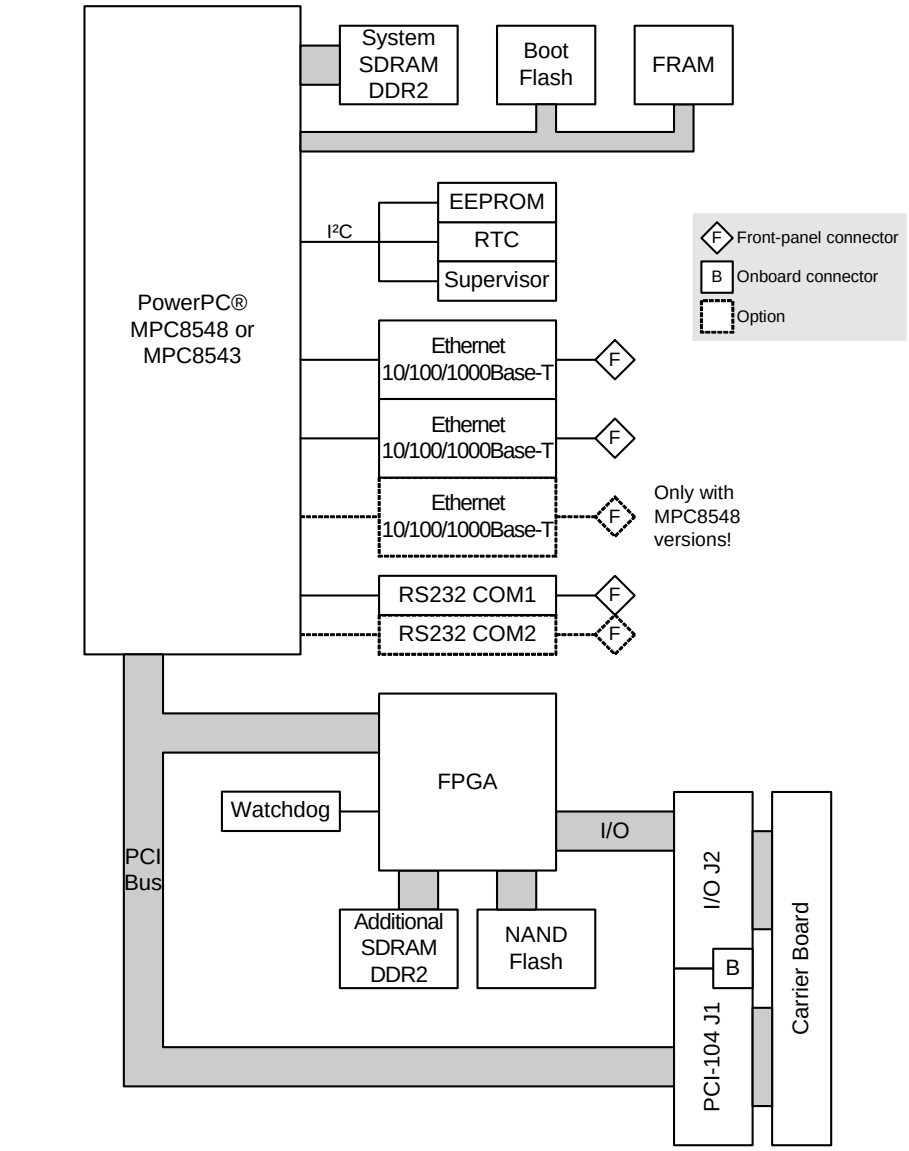
- MENMON™

Software Support

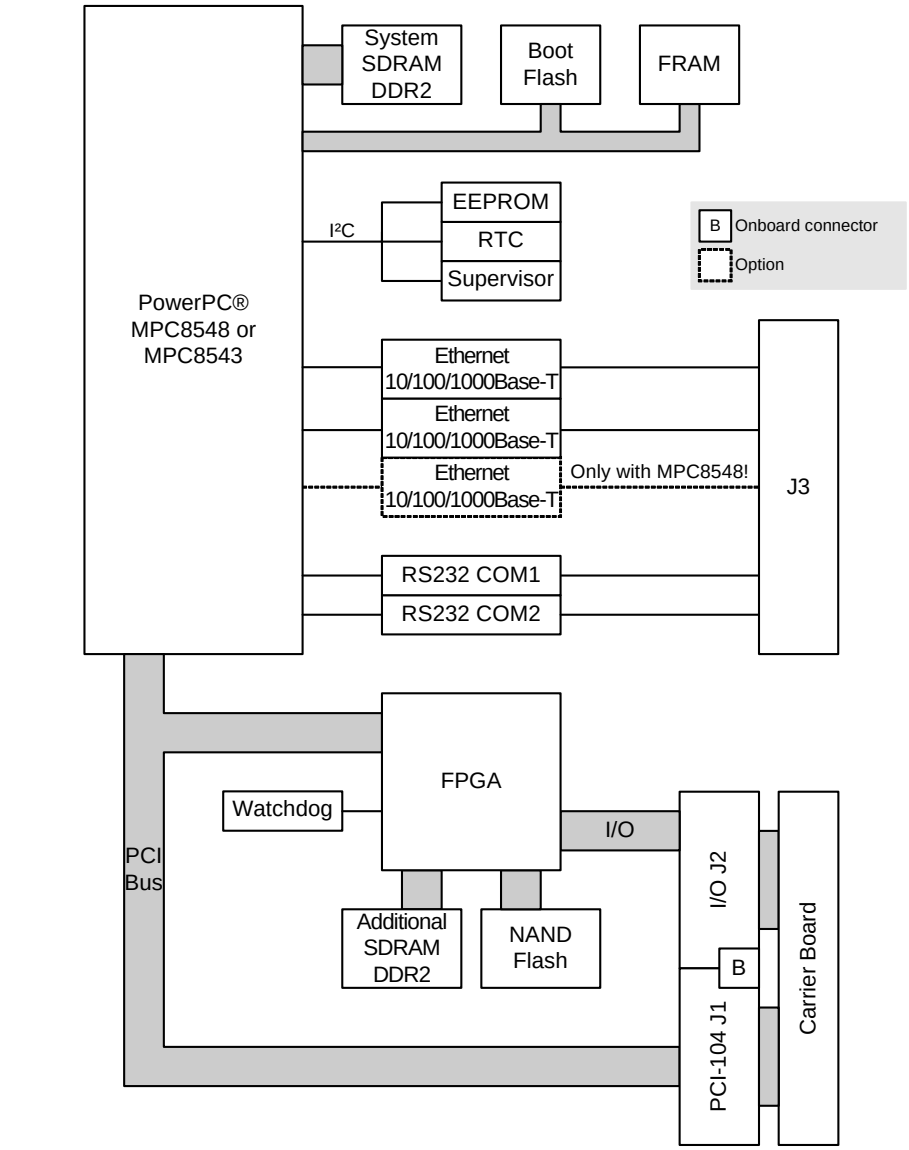
- Linux
- VxWorks®
- QNX® (on request)
- INTEGRITY® (Green Hills® Software) (on request)
- OS-9® (on request)
- For more information on supported operating system versions and drivers see online data sheet.

Block Diagram

EM9



EM9A


System SDRAM DDR2
Boot Flash
FRAM
EEPROM
RTC
Supervisor
I²C
B Onboard connector
Option
PowerPC® MPC8548 or MPC8543
Ethernet 10/100/1000Base-T
Ethernet 10/100/1000Base-T
Ethernet 10/100/1000Base-T
Only with MPC8548!
J3
RS232 COM1
RS232 COM2
FPGA
Watchdog
I/O
I/O J2
PCI Bus
Additional SDRAM DDR2
NAND Flash
B
PCI-104 J1
Carrier Board

Configuration Options

CPU

- Several PowerQUICC™ III types with different clock frequencies
- MPC8548 or MPC8548E
  - 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz
- MPC8543 or MPC8543E
  - 800 MHz or 1 GHz

Memory

- System RAM
  - 512 MB, 1 GB or 2 GB
- NAND Flash
  - 0 MB up to maximum available
- FRAM
  - 0 KB or 128 KB
- Boot Flash
  - 8 MB or 16 MB

I/O EM9

- Front Connections
  - D-Sub connectors for Ethernet and COM
  - LAN1 and LAN2 via one 9-pin D-Sub connector with 10/100Base-T support
  - LAN3 and COM1 via one 9-pin D-Sub connector (LAN3 with 10/100Base-T)
- Ethernet
  - Only two channels instead of three with MPC8543
- COM2
  - Additional COM2 RS232 interface
  - COM1 and COM2 sharing front connector
  - Both COMs without handshake lines

I/O EM9A

- Ethernet
  - Only two channels instead of three with MPC8543

FPGA Type

- Altera® Cyclone® II EP2C20 instead of EP2C35
  - 18,752 logic elements
  - 239,616 total RAM bits

Thermal Characteristics EM9A

- The ESM™ module's heat sink is always tailor-made to the customer's thermal requirements.

Power Supply

- Single +5V power supply (instead of +5V and +3.3V)

Mechanical

- EM9: PCI and I/O connectors can also be placed for face-to-face assembly (ESM™ Type N)
- EM9A: PCI and I/O connectors can also be placed for face-up assembly (ESM™ Type S)

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

For available standard configurations see online data sheets:

- EM9
- EM9A

FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® II EP2C35
  - 33,216 logic elements
  - 483,840 total RAM bits
- Connection
  - Total available pin count: 81 pins
  - Functions available via I/O connector J2
- MEN offers a starter kit for a computer-on-module of the same product family (version with front I/O). The kit includes a suitable carrier board with different I/O connectors for FPGA signals. An FPGA development package for this hardware kit is also available for download.

Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

Unless otherwise stated, all information in this manual is valid for the EM9 and EM9A. For reasons of simplicity, we generally refer to "ESM" in the text.

History

Issue	Comments	Date
E1	First edition	2007-09-10
E2	Chapters on MENMON and board organization added	2007-10-29
E3	UDMA support added, addition to MENMON	2008-03-20
E4	Description of EM9A added, minor errors corrected	2010-02-01

Conventions

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ# /IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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Contents

Figures

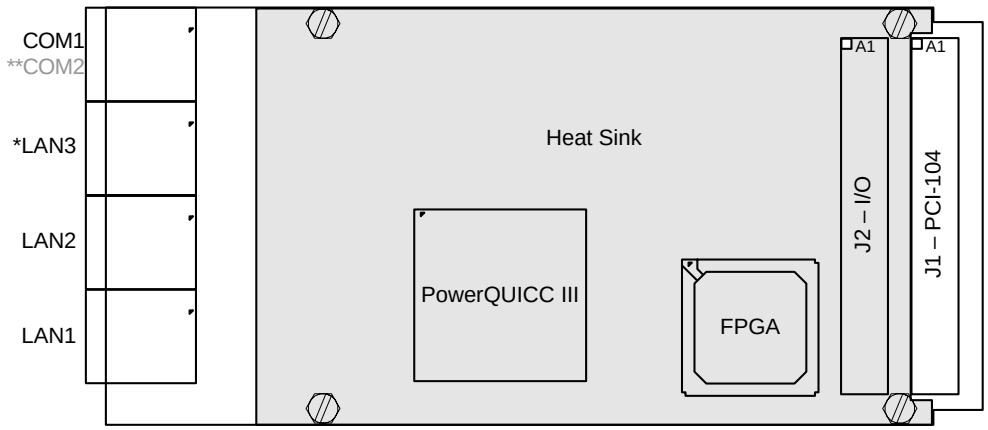
Tables

1 Getting Started

This chapter will give an overview of the board and some hints for first installation in a system as a "check list".

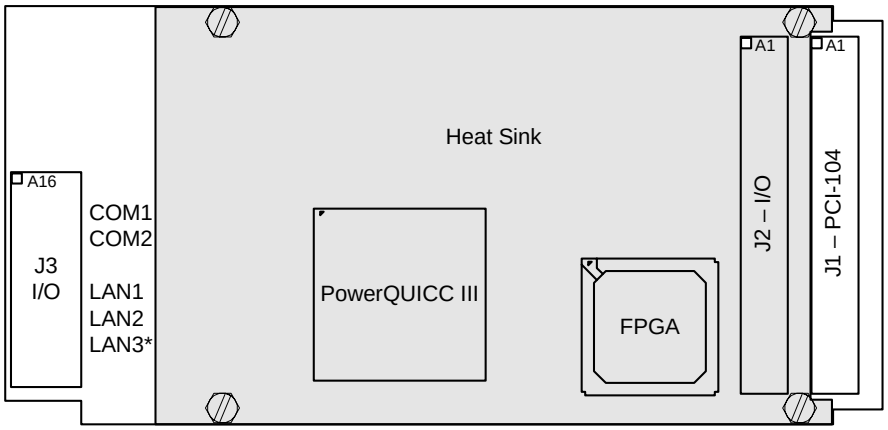
1.1 Map of the Board

Figure 1. *Map of the board – EM9 – top view*



* Connector LAN3 is only assembled on board versions with MPC8548(E).
** COM2 is available as an option.

Figure 2. *Map of the board – EM9A – top view*



* LAN3 is only available on board versions with MPC8548(E).

1.2 Integrating the Board into a System

You can use the following check list when installing the board in a system for the first time and with minimum configuration.

The board is completely trimmed on delivery.

- ☑ Power-down the system.
- ☑ Install the ESM on your carrier card.
- ☑ Insert the assembly into your system.
- ☑ Connect a terminal to the standard RS232 interface COM1.
- ☑ Set your terminal to the following protocol:
  - 9600 baud data transmission rate
  - 8 data bits
  - 1 stop bit
  - No parity
- ☑ Power-up the system.
- ☑ The terminal displays a message similar to the following:

```
 ____________________ Secondary MENMON for MEN EM9 Family 0.21 ____________________
|                                                                                   |
|          (c) 2007 - 2007 MEN Mikro Elektronik GmbH Nuremberg                      |
|         MENMON 2nd Edition, Created  Oct 12 2007     11:35:09                     |
|___________________________________________________________________________________|
|    CPU Board: EM09-00                |            CPU: MPC8548E                   |
|Serial Number: 24                     |    CPU/MEM Clk:   1386 / 198 MHz           |
|  HW Revision: 00.02.01               |    CCB/LBC Clk:    396 /  50 MHz           |
|                                      |            PCI: 32 Bit /  33 MHz           |
|   DDR2 SDRAM: 512 MB ECC off 3.0/3/8|           FRAM:    0 kB                    |
|     Produced:                        |          FLASH:   16 MB                    |
|  Last repair:                        |    Reset Cause: Power On                   |
|___________________________________________________________________________________|
|  Carrier Board: EC01-11, Rev 01.02.00, Serial 736                                 |
 \_________________________________________________________________________________/
Setting speed of NETIF 0 to AUTO
Setting speed of NETIF 1 to AUTO
Setting speed of NETIF 2 to AUTO

press 'ESC' for MENMON, 's' for setup
Test SDRAM                    : OK
Test FPGA                     : OK
Test ETHER0                   : OK
Test ETHER1                   : OK
Test ETHER2                   : OK
Test EEPROM                   : OK
Test RTC                      : OK
Test IDE0-NAND                : OK
Test TOUCH                    : OK

NOW AUTOEXECUTING: B0
No default start address configured. Stop.
Setup network interface CLUN 0x02, 00:c0:3a:62:00:18 AUTO
Searching for server (BOOTP) in background
 Telnet daemon started on port 23
 HTTP daemon started on port 80
MenMon>
```

☑ Now you can use the MENMON BIOS/firmware (see detailed description in Chapter 4 MENMON on page 46).

☑ Observe the installation instructions for the respective software.

1.3 Installing Operating System Software

The board supports Linux, VxWorks, QNX, and INTEGRITY.

By standard, no operating system is installed on the board. Please refer to the operating system installation documentation on how to install the software!

You can find any software available on MEN's website:

» EM9

» EM9A

1.4 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software available on MEN's website:

» EM9

» EM9A

2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned (Chapter 6.1 Literature and Web Resources on page 74).

2.1 Power Supply

The board is supplied with +5V and ±3.3V via PCI-104 connectors J1/J2.

The onboard power supply generates the 1.1V core voltage for the CPU, 1.8V for memory, 2.5V for Ethernet, and the 1.2V core voltage for the FPGA.

2.2 Board Supervision

The board features a temperature sensor and voltage monitor.

The temperature sensor and voltage monitor cause a reset when the temperature reaches a critical point or the voltages are not in the specified range.

A voltage monitor supervises 5V, 3.3V, 2.5V, 1.8V, 1.2V and 1.1V and holds the CPU in reset condition until all supply voltages are within their nominal values. In addition this device contains a watchdog that must be triggered. The watchdog timeout switches automatically from 56 s after reset to 1.6 s after the first trigger pulse. This allows a longer watchdog timeout period during the start-up phase.

After power-up the CPU loads the FPGA. The configuration file depends on the application. After configuration the FPGA serves the external hardware watchdog without further action by the CPU. If there is any problem loading the FPGA, the external watchdog causes a reset.

An additional watchdog is implemented in the FPGA.

2.3 Clock Supply

The CPU is supplied with one copy of the onboard PCI clocks. This is internally multiplied to generate the core clock and the memory clock.

By default the ESM runs at 66 MHz (PCI), 266 MHz (SDRAM memory) and 1.33 GHz (core).

2.4 Real-Time Clock

The board includes an RA8581 real-time clock. Interrupt generation of the RTC is not supported. For data retention during power off the RTC must be supplied with 3.3V from an external battery via J2 pin *+3.3V_STBY* (B30).

A control flag indicates a back-up power fail condition. In this case the contents of the RTC cannot be expected to be valid. A message will be displayed on the MENMON console in this case.

2.5 PowerPC CPU

The board is equipped with the MPC8548 or MPC8543 processor, which includes a 32-bit PowerPC e500 core, the integrated host-to-PCI bridge, Ethernet controllers and UARTs.

2.5.1 General

The MPC8548/3 family of processors integrates an e500v2 processor core built on Power Architecture technology with system logic required for networking, telecommunications, and wireless infrastructure applications. The MPC8548/3 is a member of the PowerQUICC III family of devices that combine system-level support for industry-standard interfaces with processors that implement the embedded category of the Power Architecture technology.

The MPC8548/3 offers a double-precision floating-point auxiliary processing unit (APU), up to 512 KB of level-2 cache, up to four integrated 10/100/1Gbits/s enhanced three-speed Ethernet controllers with TCP/IP acceleration and classification capabilities, a DDR/DDR2 SDRAM memory controller, a programmable interrupt controller, two I²C controllers, a four-channel DMA controller, a general-purpose I/O port, and dual universal asynchronous receiver/transmitters (DUART).

The MPC8548/3 is available with (MPC8548/3E) or without an integrated security engine with XOR acceleration.

Table 1. *Processor core options on EM9/EM9A*

Processor Type	Core Frequency	L2 Cache	Encryption Unit	Ethernet Ports
MPC8548	1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz	512 KB	No	3
MPC8548E	1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz	512 KB	Yes	3
MPC8543	800 MHz or 1 GHz	256 KB	No	2
MPC8543E	800 MHz or 1 GHz	256 KB	Yes	2

2.5.2 Thermal Considerations

The CPU generates around 8 W of power dissipation when operated at 1.33 GHz.

To meet thermal requirements a suitable heat sink must be attached to the CPU and sufficient airflow must be provided.

MEN provides suitable heat sinks to meet thermal requirements for different board versions and ESM carrier cards.

Please note that if you use any other heat sink than that supplied by MEN, or no heat sink at all, warranty on functionality and reliability of the ESM may cease. If you have any questions or problems regarding thermal behavior, please contact MEN.

2.6 Bus Structure

2.6.1 Host-to-PCI Bridge

The integrated host-to-PCI bridge is used as host bridge and memory controller for the PowerPC processor. All transactions of the PowerPC to the PCI bus are controlled by the host bridge. The FRAM and boot Flash are connected to the local memory bus of the integrated host-to-PCI bridge.

The PCI interface is PCI bus Rev. 2.2 compliant and supports all bus commands and transactions. Master and target operations are possible. Only big-endian operation is supported.

2.6.2 Local PCI Bus

The local PCI bus is controlled by the integrated host-to-PCI bridge. It runs at 66/ 33 MHz.

The I/O voltage is fixed to 3.3V. The data width is 32 bits.

The FPGA is connected to the local PCI bus.

2.7 Memory

2.7.1 DRAM System Memory

The board provides up to 2 GB onboard, soldered DDR2 (double data rate) SDRAM on eight memory components. The memory bus is 8 bits wide and operates at up to 300 MHz (physical), depending on the processor type.

2.7.2 Boot Flash

The board has 16 MB of onboard Flash. It is controlled by the CPU.

Flash memory contains the boot software for the MENMON/operating system bootstrapper and application software. The MENMON sectors are software-protected against illegal write transactions through a password in the serial download function of MENMON (cf. Chapter 4.5.1 Update via the Serial Console using SERDL on page 51).

2.7.3 NAND Flash

The board includes up to 1 GB soldered NAND Flash memory controlled by the FPGA. The data bus is 8 bits wide.

MEN's NAND-ATA controller provides wear leveling without user interaction. Using the NAND-ATA controller the NAND Flash is seen as an ATA disk.

NAND Flash provides 100,000 erase cycles minimum and 10 years data retention.

See also Chapter 4.5 Updating Boot Flash, NAND Flash, SDRAM and EEPROM on page 51.

2.7.4 FRAM

The board has 128 KB non-volatile FRAM memory connected to the local bus of the CPU.

The FRAM does not need a back-up voltage for data retention.

2.7.5 Additional SDRAM

The board can be supplied with up to 32 MB additional DDR2 SDRAM. It is controlled by the FPGA and a part of it is used for the NAND Flash firmware. It can also be used for graphics, for instance.

2.7.6 EEPROM

The board has a 4-kbit serial EEPROM for factory data, MENMON parameters and for the VxWorks bootline.

2.8 Ethernet Interfaces

The ESM has three Ethernet interfaces. All the channels are controlled by the CPU, LAN1 to LAN3. They support up to 1000 Mbits/s and full-duplex operation. Board versions with the MPC8543(E) processor only have two Ethernet channels.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The MAC addresses on the ESMs are as follows:

EM9

- LAN1: `0x 00 C0 3A 62 xx xx`
- LAN2: `0x 00 C0 3A 63 xx xx`
- LAN3: `0x 00 C0 3A 64 xx xx`

where "`00 C0 3A`" is the MEN vendor code, "`62`", "`63`" and "`64`" are the MEN channel-related codes, and "xx xx" is the hexadecimal serial number of the product, which depends on your board, e. g. "... `00 2A`" for serial number "000042".

EM9A

- LAN1: `0x 00 C0 3A 9E 1x xx`
- LAN2: `0x 00 C0 3A 9E 2x xx`
- LAN3: `0x 00 C0 3A 9E 3x xx`

where "`00 C0 3A`" is the MEN vendor code, and "`9E 1`", "`9E 2`", and "`9E 3`" are the MEN channel-related codes, and "x xx" is the hexadecimal serial number of the product, which depends on your board, e. g. "... `0 2A`" for serial number "000042".

(See also Chapter 6.2 Finding out the Board's Article Number, Revision and Serial Number on page 75.)

2.8.1 Connection

On EM9, three standard RJ45 connectors or two D-Sub connectors are available at the front panel for connection to network environments. Two status LEDs for each connector are accommodated on the bottom side of the PCB, right next to the connectors, so as to be visible at the front.

EM9A has no front connectors. The Ethernet signals are available on the J3 I/O connector.

The pin assignments correspond to the Ethernet specification IEEE802.3.

Table 2. *Signal mnemonics of Ethernet interface*

Signal	Direction	Function
BI_Dx+/-	in/out	Differential pairs of data lines for 1000Base-T
RX+/-	in	Differential pair of receive data lines for 10/100Base-T
TX+/-	out	Differential pair of transmit data lines for 10/100Base-T

Connection via RJ45 Connectors (EM9)

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

Table 3. *Pin assignment and status LEDs of RJ45 Ethernet connectors (LAN1..3) (EM9)*

			1000Base-T	10/100Base-T
Lights up whenever there is receive activity	A	1	BI_DA+	TX+
		2	BI_DA-	TX-
		3	BI_DB+	RX+
		4	BI_DC+	-
Lights up as soon as a 1000-Gbit link is established	L	5	BI_DC-	-
		6	BI_DB-	RX-
		7	BI_DD+	-
		8	BI_DD-	-

Connection via 9-pin D-Sub Connectors (EM9)

D-Sub connectors can be implemented as an option. **In this case, only 10Base-T and 100Base-TX are supported, no Gigabit Ethernet connection**. In addition, the D-Sub connector for LAN3 replaces not only the LAN3 RJ45 but also the COM1 RJ45 connector. These two interfaces are routed to one D-Sub connector.

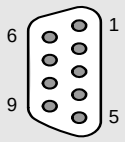
Connector types:

- 9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  9-pin D-Sub receptacle according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

Table 4. *Pin assignment of 9-pin D-Sub Ethernet plug connector (LAN1..2) (EM9)*

			1	LAN1_TX+
	6	LAN1_TX-	2	LAN2_TX+
	7	LAN2_TX-	3	-
	8	LAN2_RX-	4	LAN2_RX+
	9	LAN1_RX-	5	LAN1_RX+

Table 5. *Pin assignment of 9-pin D-Sub Ethernet plug connector (LAN3/COM1) (EM9)*



		1	LAN3_TX+
6	LAN3_TX-	2	COM1_RXD
7	COM1_RTS#	3	COM1_TXD
8	COM1_CTS#	4	LAN3_RX+
9	LAN3_RX-	5	GND

Connection via J3 Onboard I/O Connector (EM9A)

See Chapter 2.10 I/O Connector J3 (EM9A) on page 35.

2.8.2 General

Ethernet is a local-area network (LAN) protocol that uses a bus or star topology and supports data transfer rates of 100 Mbits/s and more. The Ethernet specification served as the basis for the IEEE 802.3 standard, which specifies the physical and lower software layers. Ethernet is one of the most widely implemented LAN standards.

Ethernet networks provide high-speed data exchange in areas that require economical connection to a local communication medium carrying bursty traffic at high-peak data rates.

A classic Ethernet system consists of a backbone cable and connecting hardware (e.g. transceivers), which links the controllers of the individual stations via transceiver (transmitter-receiver) cables to this backbone cable and thus permits communication between the stations.

2.8.3 10Base-T

10Base-T is one of several adaptations of the Ethernet (IEEE 802.3) standard for Local Area Networks (LANs). The 10Base-T standard (also called Twisted Pair Ethernet) uses a twisted-pair cable with maximum lengths of 100 meters. The cable is thinner and more flexible than the coaxial cable used for the 10Base-2 or 10Base-5 standards. Since it is also cheaper, it is the preferable solution for cost-sensitive applications.

Cables in the 10Base-T system connect with RJ45 connectors. A star topology is common with 12 or more computers connected directly to a hub or concentrator.

The 10Base-T system operates at 10 Mbits/s and uses baseband transmission methods.

2.8.4 100Base-T

The 100Base-T networking standard supports data transfer rates up to 100 Mbits/s. 100Base-T is actually based on the older Ethernet standard. Because it is 10 times faster than Ethernet, it is often referred to as Fast Ethernet. Officially, the 100Base-T standard is IEEE 802.3u.

There are several different cabling schemes that can be used with 100Base-T, e.g. 100Base-TX, with two pairs of high-quality twisted-pair wires.

2.8.5 1000Base-T

1000Base-T is a specification for Gigabit Ethernet over copper wire (IEEE 802.3ab). The standard defines 1 Gbit/s data transfer over distances of up to 100 meters using four pairs of CAT-5 balanced copper cabling and a 5-level coding scheme.

Because many companies already use CAT-5 cabling, 1000Base-T can be easily implemented.

Other 1000Base-T benefits include compatibility with existing network protocols (i.e. IP, IPX, AppleTalk), existing applications, Network Operating Systems, network management platforms and applications.

2.9 UART Interfaces

COM1/COM2 are standard RS232 interfaces. On EM9A they are both led to the J3 onboard I/O connector. On EM9, by standard, only COM1 is available via an RJ45 or D-Sub connector at the front panel. As an option, the CTS/RTS handshaking signals can be replaced by the RXD/TXD signals of COM2.

COM1 is controlled by the MPC854X UART 0, COM2 is controlled by the MPC854X UART 1.

Table 6. *Signal mnemonics of UART interfaces*

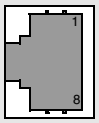
Signal	Direction	Function
CTS#	in	Clear to send
GND	-	Ground
RTS#	out	Request to send
RXD	in	Receive data
TXD	out	Transmit data

Connection via RJ45 Connector (EM9)

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

Table 7. *Pin assignment of RJ45 UART connector (EM9)*

		Standard version: COM1	Option: with COM2
	1	-	-
	2	-	-
	3	-	-
	4	GND	GND
	5	RXD1	RXD1
	6	TXD1	TXD1
	7	CTS1#	RXD2
	8	RTS1#	TXD2

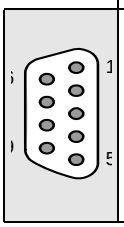
Connection via 9-pin D-Sub Connector (EM9)

A D-Sub connector can be implemented as an option. This connector replaces not only the COM1 RJ45 but also the LAN3 RJ45 connector. These two interfaces are routed to one D-Sub connector.

Connector types:

- 9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  9-pin D-Sub receptacle according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

Table 8. *Pin assignment of 9-pin D-Sub COM1/LAN3 plug connector (EM9)*



Standard version: COM1				Option: with COM2			
		1	LAN3_TX+			1	LAN3_TX+
6	LAN3_TX-	2	COM1_RXD	6	LAN3_TX-	2	COM1_RXD
7	COM1_RTS#	3	COM1_TXD	7	COM2_TXD	3	COM1_TXD
8	COM1_CTS#	4	LAN3_RX+	8	COM2_RXD	4	LAN3_RX+
9	LAN3_RX-	5	GND	9	LAN3_RX-	5	GND

Connection via J3 Onboard I/O Connector (EM9A)

See Chapter 2.10 I/O Connector J3 (EM9A) on page 35.

2.10 I/O Connector J3 (EM9A)

EM9A has no front connectors. Instead, the serial interfaces COM1/COM2 and the physical Ethernet lines for LAN1 to LAN3 are led to onboard connector J3.

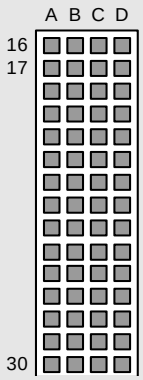
J3 is a board-to-board connector that directly leads the interfaces to the carrier board. Its pin assignment complies with the ESM Embedded System Module Specification.

Connector types:

- 4-row, 60-pin PCI-104 receptacle connector, 2mm pitch, e.g., Samtec SQT-115-01-F-Q
- Mating connector:
  4-row, 60-pin PCI-104 plug connector, 2mm pitch

For the position of connector J3 on the board see Chapter 1.1 Map of the Board on page 22.

Table 9. *Pin assignment of onboard I/O connector J3 (EM9A)*



	A	B	C	D
16	GND	GND	GND	GND
17	COM1_TXD	COM1_RTS	COM2_TXD	COM2_RTS
18	COM1_RXD	COM1_CTS	COM2_RXD	COM2_CTS
19	GND	GND	GND	GND
20	-	-	-	-
21	SHIELD	SHIELD	SHIELD	SHIELD
22	L3_MD[0]+	L3_MD[2]+	L3_MD[1]+	L3_MD[3]+
23	L3_MD[0]-	L3_MD[2]-	L3_MD[1]-	L3_MD[3]-
24	SHIELD	SHIELD	SHIELD	SHIELD
25	L1_MD[0]+	L1_MD[1]+	L2_MD[0]+	L2_MD[1]+
26	L1_MD[0]-	L1_MD[1]-	L2_MD[0]-	L2_MD[1]-
27	SHIELD	SHIELD	SHIELD	SHIELD
28	L1_MD[2]+	L1_MD[3]+	L2_MD[2]+	L2_MD[3]+
29	L1_MD[2]-	L1_MD[3]-	L2_MD[2]-	L2_MD[3]-
30	SHIELD	SHIELD	SHIELD	SHIELD

Table 10. *Signal mnemonics of onboard I/O connector J3 (EM9A)*

	Signal	Direction	Function
Power	GND	-	Digital ground
UARTs COM1/COM2	COM*x*_CTS	in	COM1/2 clear to send
	COM*x*_RTS	out	COM1/2 request to send
	COMx_RXD	in	COM1/2 receive data
	COM*x*_TXD	out	COM1/2 transmit data
Ethernet LAN1..LAN3	L*x*_MD[3:0]+/-	in/out	Differential pairs of data lines for LAN1/2/3

2.11 I/O Connector J2

The board features a second 120-pin PCI-104-standard connector that implements additional I/O. The type of I/O depends on the FPGA configuration of the ESM, which is very flexible and can contain a number of FPGA IP cores. For more information, please refer to Chapter 3 FPGA on page 44.

To illustrate the possibilities, this manual shows the standard factory FPGA configuration that is used on models 15EM09-00 and 15EM09A00.

It provides the following interfaces via J2:
(See Chapter 3.2 Standard Factory FPGA Configuration on page 45.)

- IDE
- SRAM
- Serial interfaces COM10..12
- Display
- SPI touch panel
- GPIO (8 lines)
- Miscellaneous functions

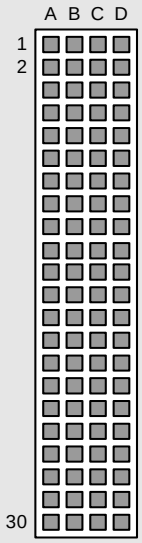
The following tables give the pinouts of the raw J2 connector (FPGA-independent) and of its signals in conjunction with the above-mentioned FPGA configuration.

Connector types:

- 4-row, 120-pin PCI-104 receptacle connector, 2mm pitch
- Mating connector:
  4-row, 120-pin PCI-104 plug connector, 2mm pitch

For the position of connector J2 on the board see Chapter 1.1 Map of the Board on page 22.

Table 11. *Pin assignment of I/O connector J2 – general pinout*

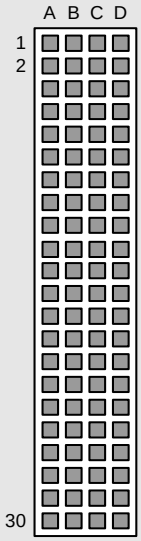


	A	B	C	D
1	PA1	PB1	+5V	PD1
2	GND	PB2	PC2	+5V
3	PA3	GND	PC3	PD3
4	PA4	PB4	GND	PD4
5	+3.3V	PB5	PC5	GND
6	PA6	+3.3V	PC6	PD6
7	PA7	PB7	+3.3V	PD7
8	GND	PB8	PC8	+3.3V
9	PA9	GND	PC9	PD9
10	PA10	PB10	GND	PD10
11	+5V	PB11	PC11	GND
12	PA12	+5V	PC12	PD12
13	PA13	PB13	+5V	PD13
14	GND	PB14	PC14	+5V
15	PA15	GND	PC15	PD15
16	PA16	PB16	GND	PD16
17	+3.3V	PB17	PC17	GND
18	PA18	+3.3V	PC18	PD18
19	PA19	PB19	+3.3V	PD19
20	GND	PB20	PC20	+3.3V
21	PA21	GND	PC21	PD21
22	PA22	PB22	GND	PD22
23	+5V	PB23	PC23	GND
24	PA24	+5V	PC24	PD24
25	PA25	PB25	+5V	PD25
26	GND	PB26	PC26	+5V
27	PA27	GND	PC27	PD27
28	PA28	PB28	GND	PD28
29	+5V	SDA	PC29	GND
30	SCL	+3.3V_STBY	PC30	PD30

Table 12. *Signal mnemonics of I/O connector J2 – general pinout*

	Signal	Direction	Function
Power	+3.3V	-	+3.3V power supply
	+3.3V_STBY	in	Power supply for real-time clock
	+5V	-	+5V power supply
	GND	-	Digital ground
FPGA I/O	PA*xx*..PD*xx*	in/out	FPGA general-purpose I/O lines
I²C EEPROM	SCL	out	I²C bus
	SDA	in/out	I²C bus

Table 13. *Pin assignment of I/O connector J2 – factory standard FPGA configuration*



	A	B	C	D
1	IDE_RST#	SCLK	+5V	BLUE[2]
2	GND	SDI	RXD10	+5V
3	IDE_D7	GND	RTS10#	BLUE[3]
4	IDE_D6	IDE_D8	GND	BLUE[4]
5	+3.3V	IDE_D9	CTS10#	GND
6	IDE_D5	+3.3V	TXD12	BLUE[5]
7	IDE_D4	IDE_D10	+3.3V	GREEN[0]
8	GND	IDE_D11	RXD12	+3.3V
9	IDE_D3	GND	RTS12#	GREEN[1]
10	IDE_D2	IDE_D12	GND	GREEN[2]
11	+5V	IDE_D13	CTS12#	GND
12	IDE_D1	+5V	TXD11	GREEN[3]
13	IDE_D0	IDE_D14	+5V	GREEN[4]
14	GND	IDE_D15	RXD11	+5V
15	IDE_DRQ	GND	GPIO_0.3	GREEN[5]
16	IDE_WR#	SDO	GND	RED[0]
17	+3.3V	SCS#	GPIO_0.4	GND
18	IDE_RD#	+3.3V	GPIO_0.5	RED[1]
19	IDE_RDY	IDE_EN#	+3.3V	RED[2]
20	GND	PENIRQ#	COM10_SW	+3.3V
21	IDE_DAK#	GND	IDE_R/W#	RED[3]
22	IDE_IRQ	GPIO_0.0	GND	RED[4]
23	+5V	PWR_FAIL	PBRST#	GND
24	IDE_A1	+5V	GPIO_0.6	RED[5]
25	IDE_A0	TXD10	+5V	DOTCLK
26	GND	IDE_A2	GPIO_0.1	+5V
27	IDE_CS1#	GND	GPIO_0.2	DTMG
28	GPIO_0.7	IDE_CS3#	GND	HSYNC
29	+5V	SDA	BLUE[0]	GND
30	SCL	+3.3V_STBY	BLUE[1]	VSYNC

Table 14. *Signal mnemonics of I/O connector J2 – factory standard FPGA configuration*

	Signal	Direction	Function
Power	+3.3V	-	+3.3V power supply
	+3.3V_STBY	in	Power supply for real-time clock
	+5V	-	+5V power supply
	GND	-	Digital ground of respective interface
I²C EEPROM	SCL	out	I²C bus
	SDA	in/out	I²C bus
IDE/SRAM	IDE_A[2:0]	out	IDE/SRAM address [2:0]
	IDE_CS1#	out	IDE chip select 1
	IDE_CS3#	out	IDE chip select 3
	IDE_D[15:0]	in/out	IDE/SRAM data [15:0]
	IDE_DAK#	out	IDE DMA acknowledge
	IDE_DRQ	in	IDE DMA request
	IDE_EN#	out	IDE/SRAM enable (0 = IDE, 1 = SRAM)
	IDE_IRQ	in	IDE interrupt request
	IDE_RD#	out	IDE/SRAM read strobe
	IDE_RDY	in	IDE ready
	IDE_RST#	out	IDE reset
	IDE_R/W#	out	SRAM address latch enable
	IDE_WR#	out	IDE/SRAM write strobe
UARTs	COM10_SW	out	COM10 mode 0 = COM10 operates in RS422/485 mode 1 = COM10 operates in RS232 mode
	CTS10#	in	COM10 clear to send
	RTS10#	out	COM10 request to send
	RXD10	in	COM10 receive data
	TXD10	out	COM10 transmit data
	RXD11	in	COM11 receive data
	TXD11	out	COM11 transmit data
	CTS12#	in	COM12 clear to send
	RTS12#	out	COM12 request to send
	RXD12	in	COM12 receive data
	TXD12	out	COM12 transmit data

	Signal	Direction	Function
Display	DOTCLK	out	Dot clock
	DTMG	out	Display data valid/invalid
	HSYNC	out	Horizontal synchronization
	RED[5:0], GREEN[5:0], BLUE[5:0]	out	Monitor interface (red, green, blue)
	VSYNC	out	Vertical synchronization
SPI Touch Control	PENIRQ#	in	Touch controller interrupt
	SCLK	out	SPI clock
	SDI	in	SPI data in
	SDO	out	SPI data out
	SCS#	out	SPI chip select
Other	GPIO_x	in/out	GPIO lines
	LED[4:1]	out	LEDs, controlled through GPIO
	PBRST#	in	Push button reset, controlled through GPIO
	PWR_FAIL	in	Power supply fail, controlled through GPIO

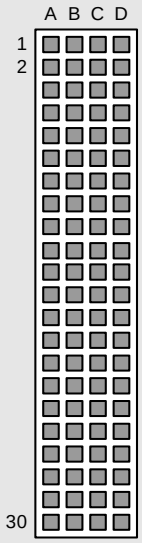
2.12 PCI-104 Interface J1

The ESM provides a 32-bit PCI interface at the PCI-104 connector J1. The ESM is always the system controller of the PCI-104 bus and supports four external masters.

Connector types:

- 4-row, 120-pin PCI-104 receptacle connector, 2mm pitch, e.g., Samtec ESQT-130-02-G-Q-368
- Mating connector:
  4-row, 120-pin PCI-104 plug connector, 2mm pitch

Table 15. *Pin assignment of PCI J1*



	A	B	C	D
1	GND	Reserved	+5V	AD00
2	VI/O +3.3V	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O +3.3V	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	SB0#	PAR
10	GND	PERR#	+3.3V	SDONE
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O +3.3V	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O +3.3V
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O +3.3V	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	Reserved	INTA#	INTB#	INTC#
30	Reserved	REQ3#	GNT3#	GND

For a description of signals please refer to the PCI-104 specification see Chapter 6.1 Literature and Web Resources on page 74.

3 FPGA

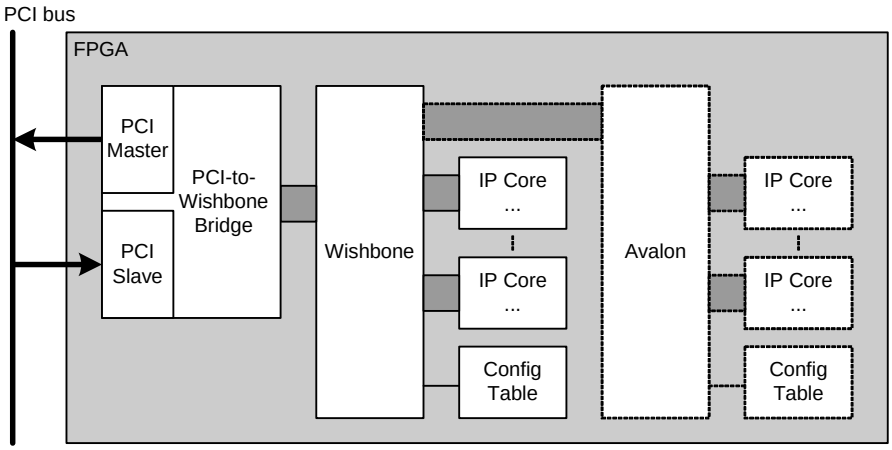
3.1 General

The FPGA – as a part of the ESM – represents an interface between a user-selectable configuration of I/O modules (IP cores) and the PCI bus. The PCI core included in the FPGA can be a PCI target or master. It can be accessed via memory single/burst read/write cycles.

The Wishbone bus is the uniform interface to the PCI bus. However, the FPGA may have multiple internal buses, so that IP cores can be connected to one of several internal buses, e.g. Wishbone or Avalon. This guarantees the highest possible flexibility for different configurations of the FPGA.

Typically each implementation contains basic system functions such as reset and interrupt control etc. and the system library, which are also IP cores.

Figure 3. *FPGA – Block diagram (exemplary)*



A configuration table provides the information which modules are implemented in the current configuration. Furthermore the revision, the instance number (one module can be instantiated more than one time), the interrupt routing and the base address of the module are stored. At initialization time, the CPU has to read the configuration table to get the information of the base addresses of the included modules.

Note that with regard to the FPGA resources such as available logic elements or pins it is not possible to grant all possible combinations of the FPGA IP cores. The following chapter describes one possible configuration of the FPGA. Please ask our sales staff for other configurations.

You can find an overview and descriptions of all available FPGA IP cores on MEN's website.

3.2 Standard Factory FPGA Configuration

3.2.1 IP Cores

The factory FPGA configuration for standard boards comprises the following FPGA IP cores:

- Main bus interface
- 16Z024-01_Chameleon – Chameleon V2 table
- 16Z069_RST – Reset controller
- 16Z052_GIRQ – Interrupt controller
- 16Z070_IDEDISK – IDE controller for NAND Flash
- 16Z043_SDRAM – Additional SDRAM controller (32 MB DDR2, 8 MB used as NAND Flash main memory, 8 MB used as graphics RAM, 16 MB unused)
- 16Z016_IDE – IDE controller (PIO mode 0 and UDMA mode 5 / UDMA100)
- 16Z044_DISP – Display controller (800 x 600, 60Hz/75Hz, 6-bit RGB)
- 16Z031_SPI – SPI touch panel controller
- 16Z125_UART – UART controller (controls COM10..COM12)
- 16Z034_GPIO – GPIO controller (2 cores; 8 general I/O lines; *PWR_FAIL*, LEDs and other system control signals)

3.2.2 FPGA Configuration Table

The resulting configuration table of the standard FPGA is as follows:

Note: 16Z070_IDEDISK consists of three cores:

- 16Z053_IDEATA
- 16Z068_IDETGT
- 16Z063_NANDRAW

Table 16. *FPGA – Factory standard configuration table for ESM*

IP Core	Device	Variant	Revision	Interrupt	Group	Instance	BAR	Offset	Size
Chameleon Table	24	1	5	3F	0	0	0	0	200
16Z069_RST	69	0	2	3F	0	0	0	200	100
16Z052_GIRQ	52	0	2	3F	0	0	0	300	100
16Z016_IDE	116	0	1	1	0	0	0	400	100
16Z031_SPI	31	0	4	4	0	0	0	500	100
16Z044_DISP	44	1	1	3F	1	0	0	600	100
16Z034_GPIO	34	0	3	2	0	0	0	700	100
16Z034_GPIO	34	0	3	2	0	1	0	800	100
16Z125_UART	125	0	7	3	0	0	0	900	10
16Z125_UART	125	0	7	3	0	1	0	910	10
16Z125_UART	125	0	7	3	0	2	0	920	10
16Z063_NANDRAW	63	0	7	3F	2	0	0	4600	100
16Z068_IDETGT	68	0	F	5	2	0	0	6000	800
16Z053_IDEATA	53	0	F	5	2	0	0	A000	400
16Z043_SDRAM	43	1	1	3F	1	0	1	0	1E+06
16Z043_SDRAM	43	1	1	3F	2	1	1	1E+06	1E+06
Usermodule_0	900	0	0	6	0	0	0	8000	1000
Usermodule_1	900	0	0	7	0	0	0	9000	1000

All values in the tables are given in hexadecimal notation.

4 MENMON

4.1 General

MENMON is the CPU board firmware that is invoked when the system is powered on.

The basic tasks of MENMON are:

- Initialize the CPU and its peripherals.
- Load the FPGA code.
- PCI auto configuration.
- Perform self-test.
- Provide debug/diagnostic features on MENMON command line.
- Interaction with the user via touch panel/TFT display.
- Boot operating system.
- Update firmware or operating system.

The following description only includes board-specific features. For a general description and in-depth details on MENMON, please refer to the MENMON 2nd Edition User Manual.

4.1.1 State Diagram

Figure 4. *MENMON – State diagram, Degraded Mode/Full Mode*

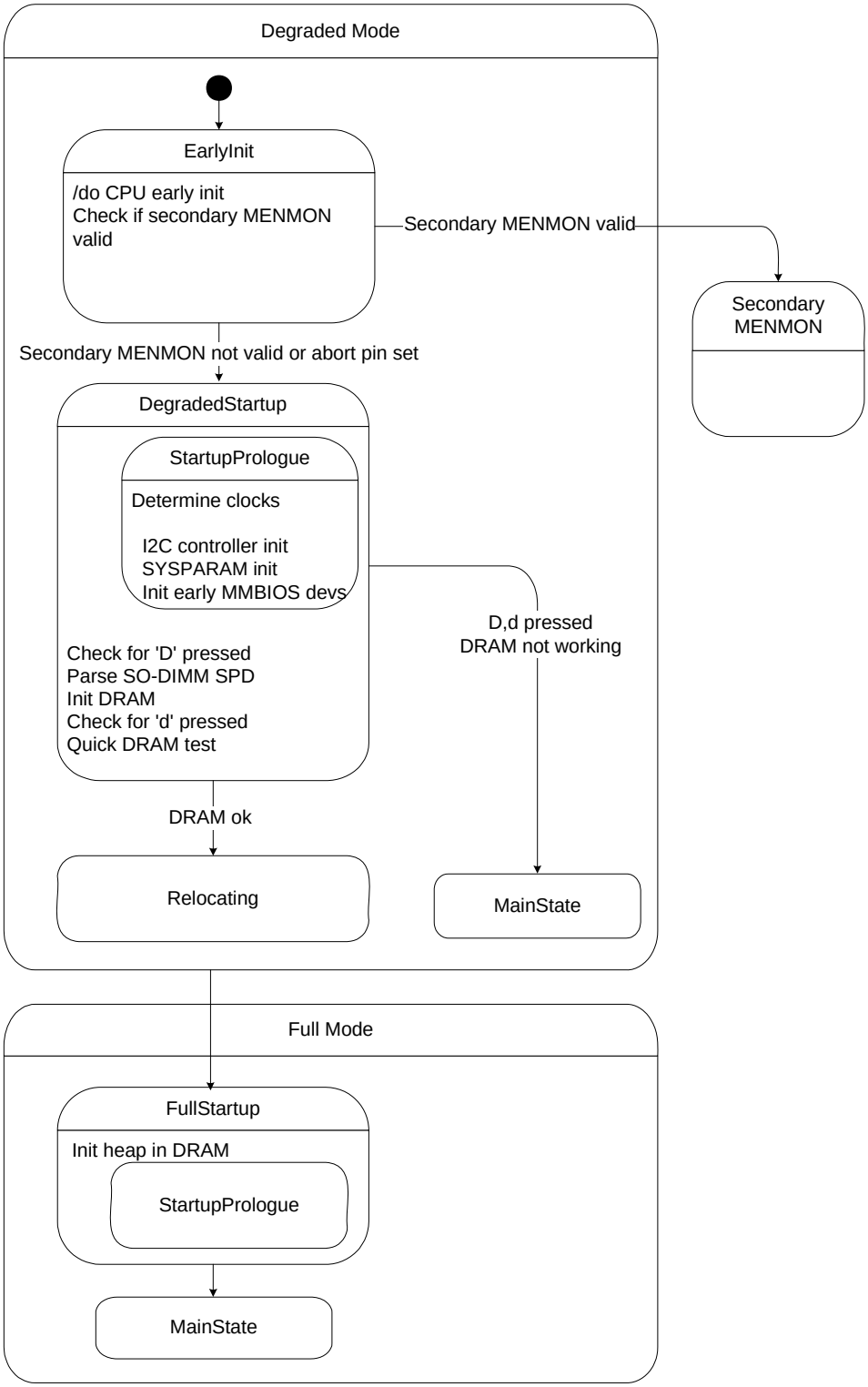
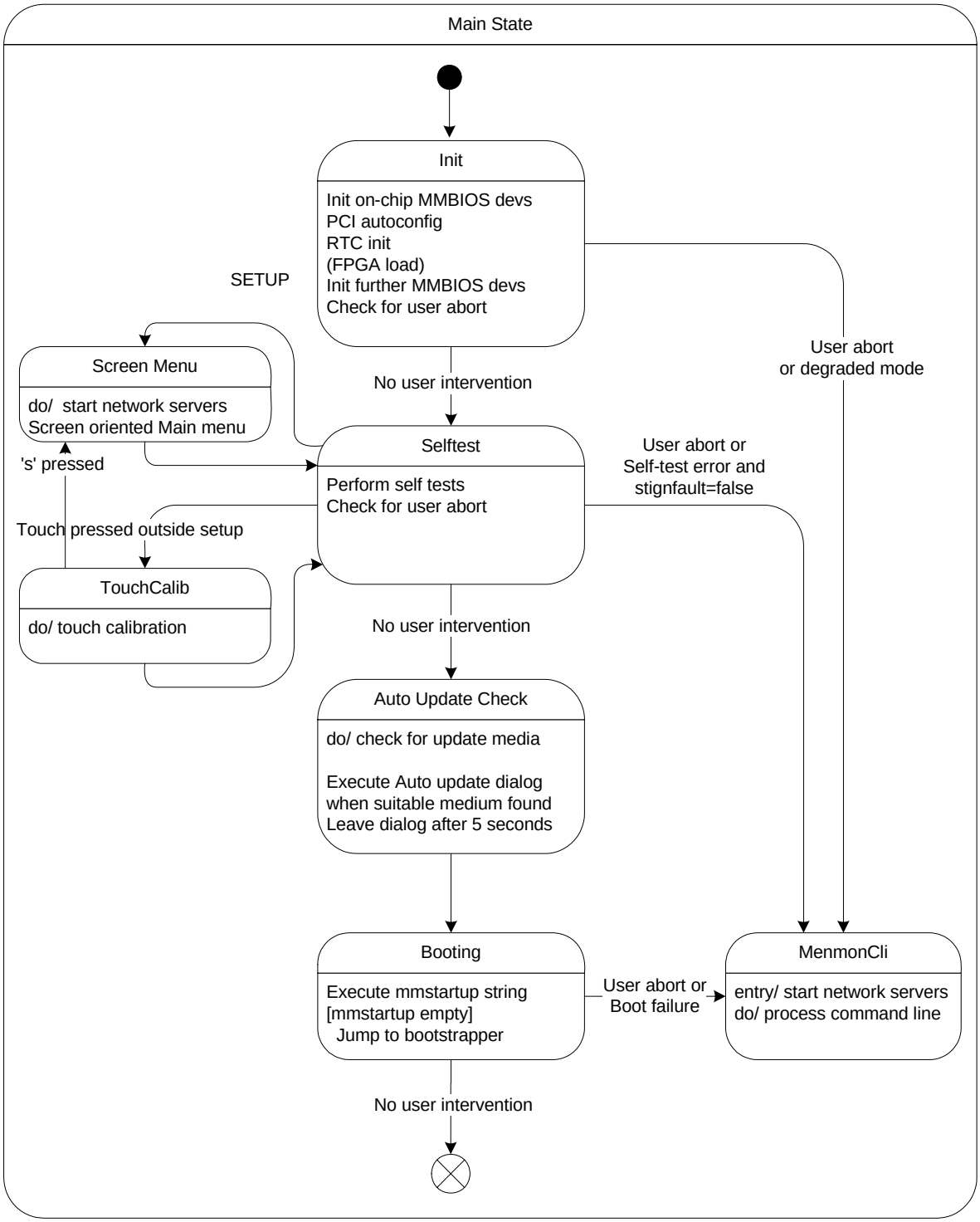


Figure 5. *MENMON – State diagram, main state*



4.2 Interacting with MENMON

To interact with MENMON, you can use the following consoles:

- UARTs COM1..2 (RS232)
- UARTs COM10..12 (FPGA)
- Touch panel / TFT interface (if present)
- Telnet via network connection
- HTTP */monpage* via network connection

The default setting of the COM ports is 9600 baud, 8 data bits, no parity, and one stop bit.

4.2.1 Entering the Setup Menu/Command Line

During normal boot, you can abort the booting process in different ways during the self-test, depending on your console:

- With a touch panel press the "Setup" button to enter the Setup Menu.
- With a text console press the "s" key to enter the Setup Menu.
- With a text console press "ESC" to enter the command line.

By default, the self-test is not left until 3 seconds have elapsed (measured from the beginning of the self-test), even if the actual test has finished earlier, to give the user a chance to abort booting and enter the Setup Menu.

You can modify the self-test wait time through MENMON system parameter *stwait* (see page 66).

4.3 Configuring MENMON for Automatic Boot

You can configure how MENMON boots the operating system either through the Setup Menu or through the command line.

In the Basic Setup Menu you can select the boot sequence for the bootable devices on the ESM. The selected sequence is stored in system parameter *mmstartup* as a string of MENMON commands. For example, if the user selects: "Int. CF (NAND), Ether, (None)", the *mmstartup* string will be set to "DBOOT 0; NBOOT TFTP".

You can view and modify this string directly, using the Expert Setup Menu, option *Startup string*, or through the command-line command *EE-MMSTARTUP*.

(See also MENMON 2nd Edition User Manual for further details.)

4.4 Calibrating the Touch Screen

You can enter the touch-panel calibration function through the Setup Main Menu.

This function is also entered automatically during the self-test, if you hit the touch screen at any position outside the "Setup" button. You may have missed the "Setup" button because the touch panel was incorrectly calibrated.

Follow the instructions on the screen to complete calibration.

(See also MENMON 2nd Edition User Manual for further details.)

4.5 Updating Boot Flash, NAND Flash, SDRAM and EEPROM

Primary MENMON is hardware protected.

4.5.1 Update via the Serial Console using *SERDL*

You can use command *SERDL* to update program data using the serial console.

The following table shows the ESM locations:

Table 17. *MENMON – Program update files and locations*

File Name Extension	Typical File Name	Password for *SERDL*	Location
.SMM	*MENMON_EM09.SMM*	MENMON	Secondary MENMON
.FP0	*EM09-00IC005B1.FP0*	FPGA0	FPGA0 code (33 MHz PCI clock)
.FP1	*EM09-00IC005B1.FP1*	FPGA1	FPGA1 code (backup)
.FP2	*EM09-00IC005A1.FP2*	FPGA2	FPGA2 code (66 MHz PCI clock)
.FP3	*EM09-00IC005A1.FP3*	FPGA3	FPGA3 code (backup)
.Bxx	*DSKIMG.B00*	DISK	Starting at sector *xx* in second disk
.Cxx	*DSKIMG.C00*	DISK	Starting at sector *xx* in first disk (NAND Flash)
.Dxx	*MYFILE.D00*	-	Starting at 0x200000 + xx in SDRAM
.Exx	*MYFILE.E00*	-	Starting at byte *xx* in EEPROM
.Fxxx	*MYFILE.F000*	-	Starting at sector *xxx* in boot Flash (Flash has 128 sectors with 0x20000 bytes each)

4.5.2 Update from Network using *NDL*

You can use the network download command *NDL* to download the update files from a TFTP server in network. The file name extensions, locations and passwords are the same as for the *SERDL* command.

4.5.3 Update via Program Update Menu

The following Program Update Menu is implemented in the ESM MENMON:

```
Program Update Menu

  >Copy external CF -> internal CF (1:1)

   Copy external CF:IMAGE.C00 -> internal CF

   Copy external CF:IMAGE.FP0 -> boot flash FPGA code

   Copy external CF:IMAGE.FP1 -> boot flash fallback FPGA code

   Copy external CF:IMAGE.SMM -> boot flash sec. MENMON

   Copy internal CF -> external CF (1:1)
```

"internal CF" stands for the onboard NAND Flash, "external CF" stands for the first external IDE storage device.

4.5.4 Automatic Update Check

MENMON's automatic update check looks for some special files on an external IDE device (if present on carrier card).

The files that are searched for are:

- Name stored in system parameter *bf* or *bootfile*, or – if this is empty – *BOOTFILE*[1].
- *IMAGE.C00* (see also Table 17, MENMON – Program update files and locations, on page 51.)

To allow MENMON to locate these files, they must be in the root directory of a DOS FS. This works on unpartitioned media or on drives with one partition.

MENMON does not automatically start the copying process. Depending on the type of file found, it presents different menus to the user:

In case *BOOTFILE* was found:

```
Detected an update capable external Disk

  >Ignore, continue boot

   Boot from this medium
```

In case *IMAGE.C00* was found:

```
Detected an update capable external Disk

  >Ignore, continue boot

   Copy external CF:IMAGE.C00 -> internal CF
```

The copying process is then performed in the same way as a standard sector-by-sector media copy program update (see MENMON 2nd Edition User Manual).

If there is no user input for 5 seconds after the menu appears, booting continues.

[1] MENMON versions < 3.4 only search for *bootfile*.

4.5.5 Updating MENMON Code

Updates of MENMON are available for download from MEN's website. MENMON's integrated Flash update functions allow you to do updates yourself. However, you need to take care and follow the instructions given here. Otherwise, you may make your board inoperable!

In any case, read the following instructions carefully!

Please be aware that you do MENMON updates at your own risk. After an incorrect update your CPU board may not be able to boot.

WARNING: After a MENMON update, the hardware revision displayed by MENMON will most probably be different from the actual hardware revision of your CPU board, because MENMON follows MEN's hardware revision updates.

Do the following to update MENMON:

- ☑ Unzip the downloaded file, e.g., *14EM09-00_01_02.zip*, into a temporary directory.
- ☑ Connect a terminal emulation program with the COM 1 port of your ESM and set the terminal emulation program to 9600 baud, 8 data bits, 1 stop bit, no parity, no handshaking (if you haven't changed the target baud rate on your own).
- ☑ Power on your ESM, and press "ESC" immediately.
- ☑ In your terminal emulation program, you should see the "MenMon>" prompt.
- ☑ Enter "SERDL MENMON" to update the secondary MENMON. You should now see a "C" character appear every 3 seconds.
- ☑ In your terminal emulation program, start a "YModem" download of file *14EM09-00_01_02.smm* (for example, with Windows Hyperterm, select *Transfer > Send File* with protocol "YModem").
- ☑ When the download is completed, reset the ESM.

4.6 Diagnostic Tests

Note: MENMON may include further tests for COM or other interfaces depending on the ESM functionality and carrier board. The standard carrier board tests are:

- TOUCH
- IDE
- COM_CB

4.6.1 Ethernet

Table 18. *MENMON – Diagnostic tests: Ethernet*

Test Name	Description	Availability
ETHER0 *ETHER1* *ETHER2*	Ethernet 0/1/2 (LAN1/2/3) internal loopback test Groups: POST AUTO	Always (except ETHER2 with an MPC8543 processor)
ETHER0_X *ETHER1_X* *ETHER2_X*	Ethernet 0/1/2 (LAN1/2/3) external loopback test Groups: NONAUTO ENDLESS	Always (except ETHER2 with an MPC8543 processor)

4.6.1.1 Ethernet Internal Loopback Test

The test

- configures the network interface for loopback mode (on PHY)
- verifies that the interface's ROM has a good checksum
- verifies that the MAC address is valid (not `0xFFFFFF`…)
- sends 10 frames with `0x400` bytes payload each
- verifies that frames are correctly received on the same interface.

If the network interface to test is the currently activated interface for the MENMON network stack, the interface is detached from the network stack during test and reactivated after test.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY

Does not check:

- Connection between PHY and physical connector
- Interrupt line
- All LAN speeds

4.6.1.2 Ethernet External Loopback Test

This test is the same as the Ethernet Internal Loopback Test, but requires an external loopback connector. Before sending frames, the link state is monitored. If it is not ok within 2 seconds, the test fails.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY
- Connection between PHY and physical connector

Does not check:

- Interrupt line
- All LAN speeds

4.6.2 SDRAM and FRAM

Table 19. *MENMON – Diagnostic tests: SDRAM and FRAM*

Test Name	Description	Availability
SDRAM	Quick SDRAM connection test Groups: POST AUTO	Always
SDRAM_X	Full SDRAM test Groups: NONAUTO ENDLESS	Always
FRAM	Quick FRAM test Groups: POST AUTO	ESM is known to have FRAM (Tests available as of EM9 hardware revision 01.xx)
FRAM_X	Full FRAM test Groups: NONAUTO ENDLESS	

4.6.2.1 Quick RAM Test

This quick test checks most of the connections to the RAM chips but does not test all RAM cells. It executes very quickly (within milliseconds).

This test is non-destructive (saves/restores original RAM content).

Checks:

- All address lines
- All data lines
- Byte enable signals
- Indirectly, checks clock and other control signals

Does not check:

- SDRAM cells
- Burst mode

4.6.2.2 Extended RAM Test

This full-featured memory test allows to test all RAM cells. Depending on the size of the SDRAM, this test can take up to one minute.

It tests 8-, 16- or 32-bit access, each with random pattern, and single and burst access.

On each pass, this test first fills the entire memory (starting with the lowest address) with the selected pattern, using the selected access mode, and then verifies the entire block.

This test is destructive.

Checks:

- All address lines
- All data lines
- All control signals
- All SDRAM cells

4.6.3 FPGA

Table 20. *MENMON – Diagnostic tests: FPGA*

Test Name	Description	Availability
FPGA	FPGA presence test Groups: POST AUTO	Always

4.6.4 EEPROM

Table 21. *MENMON – Diagnostic tests: EEPROM*

Test Name	Description	Availability
EEPROM	I²C access/Magic nibble check Groups: POST AUTO ENDLESS	Always

This test reads the first EEPROM cell over SMB and checks if bits 3..0 of this cell contain the magic nibble `0xE`.

4.6.5 IDE/NAND Flash

Table 22. *MENMON – Diagnostic tests: IDE/NAND Flash*

Test Name	Description	Availability
IDE	External IDE master access / sector 0 access Groups: NONAUTO ENDLESS	MENMON BIOS device 1/0 present and carrier board is known to have external IDE (e.g., hard disk or Compact-Flash)
IDE0-NAND	Check if IDE NAND Flash device ("disk") is present Groups: POST	If SDRAM and IDE-NAND devices are present in FPGA

The test first performs an ATA register test, then reads sector 0 from the Flash disk without verifying the content of the sector.

Checks:

- Most ATA control lines
- Basic ATA transfer

Does not check:

- ATA signals IRQ, DAK, DRQ
- Partition table or file system on disk

4.6.6 COM1/COM2

Table 23. *MENMON – Diagnostic tests: COM1/COM2*

Test Name	Description	Availability
COM1	External loopback test RxD/TxD/ RTS/CTS Groups: NONAUTO ENDLESS Note: Test will be skipped when COM1 is currently used as a console	Always
COM2	External loopback test RxD/TxD Groups: NONAUTO ENDLESS	Only if implemented
*COM*x	External loopback test RxD/TxD/ *handshake lines* Groups: NONAUTO ENDLESS	Depending on FPGA-programmed UARTs

This test requires an external test adapter connecting:

- TXD and RXD
  To test TXD/RXD, a test string is sent through the UART.
- RTS and CTS

To test TXD/RXD, a test string is sent through the UART.

To test handshake lines, the lines are toggled and it is checked whether input lines follow.

4.6.7 Touch

Table 24. *MENMON – Diagnostic tests: touch*

Test Name	Description	Availability
TOUCH	Touch controller communication test Groups: POST AUTO ENDLESS	Carrier board is known to have a touch controller

This test tries to communicate over the SPI bus with the touch controller on the carrier board by sending an Identify command to the controller.

Checks:

- SPI connection to touch controller

Does not check:

- Connection between touch controller and touch panel

4.6.8 RTC

Table 25. *MENMON – Diagnostic tests: RTC*

Test Name	Description	Availability
RTC	Quick presence test of RTC Groups: POST AUTO	Always
RTC_X	Extended test of RTC Groups: NONAUTO ENDLESS	Always

4.6.8.1 RTC Test

This is a quick presence test of the real-time clock (RTC) and is executed on POST.

Checks:

- Presence of RTC (I2C access)

Does not check:

- If RTC is running
- RTC backup voltage

4.6.8.2 Extended RTC Test

Checks:

- Presence (e.g., I²C access)
- RTC is running

Does not check:

- RTC backup voltage

4.7 MENMON Configuration and Organization

4.7.1 Consoles

You can select the active consoles by means of system parameters *con0..con3* and configure the console through parameters *ecl*, *gcon*, *hdp* and *tdp*. MENMON commands *CONS(-xxx)* also give access to the console settings (see Chapter 4.8 MENMON Commands (page 69)).

Table 26. *MENMON – System parameters for console selection and configuration*

Parameter (alias)	Description	Default	User Access
cbr (baud)	Baud rate of all UART consoles (decimal) (default: 9600 baud, 8n1)	9600	Read/write
con0..con3	CLUN of console 0..3 CLUN=0x00: disable CLUN=0xFF: autoselect next available console *con0* is implicitly the debug console	*con0*: 08 (COM1) *con1*: 0A (Touch) *con2*: 00 (none) *con3*: 00 (none)	Read/write
ecl	CLUN of attached network interface (hex) CLUN=0x00: none CLUN=0xFF: first available Ethernet	0xFF	Read/write
gcon	CLUN of graphics device to display boot logo CLUN=0x00: disable CLUN=0xFF: Autoselect first available graphics console	0xFF (AUTO)	Read/write
hdp	HTTP server TCP port (decimal) 0: don't start telnet server -1: use default port 23 else: TCP port for telnet server	-1	Read/write
tdp	Telnet server TCP port (decimal) 0: don't start HTTP server -1: use default port 80 else: TCP port for HTTP server	-1	Read/write

4.7.2 Video Modes

None of the included drivers allows to change the video mode.

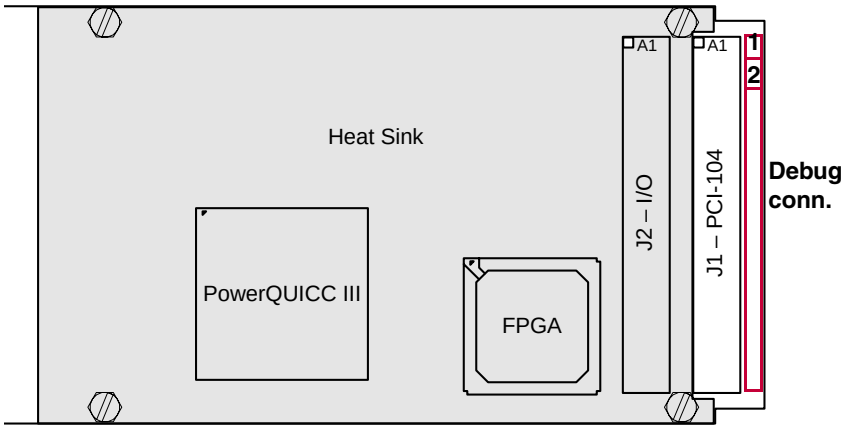
4.7.3 Abort Pin

Since the ESM has no real "abort" button, it is simulated by connecting pin 1 to pin 2 on the debug connector (TDI pin of debugger with GND).

If the abort pin is detected asserted, the secondary MENMON is not invoked, the fallback FPGA image is loaded, MENMON uses default parameters (such as baud rate, console port), deactivates the FPGA watchdog and enters the command-line interface. This is useful if a secondary MENMON has been programmed that does not work or if you have misconfigured a system parameter.

Note that when a JTAG debugger is connected, the abort pin is always read as active.

Figure 6. *MENMON – Position of abort pins on debug connector*



4.7.4 MENMON Memory Map

4.7.4.1 MENMON Memory Address Mapping

Table 27. *MENMON – Address map (full-featured mode)*

Address Space	Size	Description
0x 0000 0000 .. 0000 1400	5 KB	Exception vectors
0x 0000 3000 .. 0000 3FFF	4 KB	MENMON parameter string
0x 0000 4200 .. 0000 42FF	256 bytes	VxWorks bootline
0x 0000 4300 .. 00FF FFFF	Nearly 16 MB	Free
0x 01D0 0000 .. 01DF FFFF	2 MB	Heap2
0x 01E0 0000 .. 01EF FFFF	1 MB	Text + Reloc
0x 01F0 0000 .. 01F1 FFFF	128 KB	Stack
0x 01F2 0000 .. 01F4 FFFF	128 KB	Stack for user programs and operating system boot
0x 01F5 0000 .. 01FE FFFF	640 KB	Heap
0x 01FF 0000 .. 01FF FFFF	64 KB	Not touched for OS post mortem buffer i.e. VxWorks WindView or MDIS debugs (requires ECC to be turned off!)
0x 0200 0000 .. End of RAM		Free or download area

4.7.4.2 Boot Flash Memory Map

Table 28. *MENMON – Boot Flash memory map*

Flash Offset	CPU Address	Size	Description
0x 00 0000	0x FF00 0000	10 MB	Available to user
0x A0 0000	0x FFA0 0000	1 MB	Fallback FPGA code (FPGA1) (66 MHz)
0x B0 0000	0x FFB0 0000	1 MB	Initial FPGA code (FPGA0) (66 MHz)
0x C0 0000	0x FFC0 0000	1 MB	Fallback FPGA code (FPGA1) (33 MHz)
0x D0 0000	0x FFD0 0000	896 KB	Initial FPGA code (FPGA0) (33 MHz)
0x DE 0000	0x FFDE 0000	128 KB	System parameter section in boot Flash (if *useflpar* system parameter is set to 1)
0x E0 0000	0x FFE0 0000	1 MB	Secondary MENMON
0x F0 0000	0x FFF0 0000	1 MB	Primary MENMON

4.7.5 MENMON BIOS Logical Units

The following table shows fixed assigned CLUNs. All other CLUNs are used dynamically.

Table 29. *MENMON – Controller Logical Units (CLUNs)*

CLUN	MENMON BIOS Name	Description
0x00	IDE0	NAND Flash IDE (primary IDE)
0x01	IDE1	IDE devices controlled by onboard FPGA
0x02	ETHER0	Ethernet #0 (LAN 1)
0x03	ETHER1	Ethernet #1 (LAN 2)
0x04	ETHER2	Ethernet #2 (LAN 3)
0x08	COM1	MPC854X UART channel #0
0x09	COM2	MPC854X UART channel #1 (optional on EM9)
0x0A	TOUCH	Touch console (if 16Z031_SPI found in onboard FPGA and can communicate with touch controller)
0x0B	COM10	UART #0 of onboard FPGA UART
0x0C	COM11	UART #1 of onboard FPGA UART
0x0D	COM12	UART #2 of onboard FPGA UART
0x20		All other devices dynamically detected on PCI or FPGA devices
0x40		Telnet console
0x41		HTTP monitor console

Table 30. *MENMON – Device Logical Units (DLUNs)*

CLUN/DLUN	MENMON BIOS Name	Description
0x00/0x00	NAND(Int.CF)	Internal NAND Flash
0x01/0x00	IDE1-M(Ext.CF)	External IDE Master
0x01/0x01	IDE1-S	External IDE Slave

4.7.6 System Parameters

System parameters are parameters stored in EEPROM. Some parameters are automatically detected by MENMON (such as CPU type and frequency). The parameters can be modified through the *EE-xxx* command via the command line.

4.7.6.1 Physical Storage of Parameters

Most parameters are stored in the 512-byte serial EEPROM on the ESM. Carrier-board specific parameters are stored in the serial EEPROM on the carrier board.

If required, you can configure MENMON to store some strings in boot Flash rather than in EEPROM.

4.7.6.2 Start-up with Faulty EEPROM

If a faulty EEPROM is detected (i.e. the checksum of the EEPROM section is wrong), the system parameters will use defaults. The behavior is the same if the EEPROM is blank. The default baud rate is 9600.

4.7.6.3 ESM System Parameters

Note: Parameters marked by "Yes" in section "Parameter String" are part of the MENMON parameter string.

Note: Parameters for production data of carrier boards will use prefixed parameter names, e.g., *c-brd*.

Table 31. *MENMON – ESM system parameters – Autodetected parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
ccbclkhz	CCB clock frequency (decimal, Hz)		Yes	Read-only
clun	MENMON controller unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
cons	Selected console. Set to name of first selected console		Yes	Read-only
cpu	CPU type as ASCII string (e.g., "MPC8548E")		Yes	Read-only
cpuclkhz	CPU core clock frequency (decimal, Hz)		Yes	Read-only
dlun	MENMON device unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
flash0	Flash size (decimal, kilobytes)		Yes	Read-only
fram0	FRAM size (decimal, kilobytes)		Yes	Read-only
immr	Physical address of CCSR register block		Yes	Read-only
mem0	RAM size (decimal, kilobytes)		Yes	Read-only
mem1	Size of SRAM[1] (decimal, kilobytes)		Yes	Read-only

Parameter (alias)	Description	Standard Default	Parameter String	User Access
memclkhz	Memory clock frequency (decimal, Hz)		Yes	Read-only
mm	Info whether primary or secondary MENMON has been used for booting, either "smm" or "pmm"		Yes	Read-only
mmst	Status of diagnostic tests, as a string		Yes	Read-only
nmac0/1/2	MAC address of Ethernet interface x (0..n). Format e.g., "00112233445566". Set automatically according to serial number of the board		Yes	Read-only
pciclkhz	PCI bus clock frequency = system input clock (decimal, Hz)		Yes	Read-only
rststat	Reset status code as a string, see Chapter 4.7.6.4 Reset Cause – Parameter rststat on page 68		Yes	Read-only

[1] If implemented.

Table 32. *MENMON – ESM system parameters – Production data*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
brd	Board name	-	Yes	Read-only
brdmod	Board model "mm"	-	Yes	Read-only
brdrev	Board revision "xx.yy.zz"	-	Yes	Read-only
prodat	Board production date MM/DD/YYYY	-	Yes	Read-only
repdat	Board last repair date MM/DD/YYYY	-	Yes	Read-only
sernbr	Board serial number	-	Yes	Read-only

Table 33. *MENMON – ESM system parameters – MENMON persistent parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
bsadr (bs)	Bootstrapper address. Used when BO command was called without arguments. (hexadecimal, 32 bits)	0	No	Read/write
cbr (baud)	Baudrate of all UART consoles (dec)	9600	Yes	Read/write
con0..con3	CLUN of console 0..3. (hex) (see Chapter 4.7.1 Consoles on page 59)	0xFF = auto	No	Read/write
eccsth	ECC single-bit error threshold	32	No	Read/write
ecl	CLUN of attached network interface (hex)	0xFF	No	Read/write
gcon	CLUN of graphics screen (hex) (see Chapter 4.7.1 Consoles on page 59)	0xFF = auto	No	Read/write
hdp	HTTP server TCP port (decimal)	-1	No	Read/write
kerpar	Linux Kernel Parameters (399 chars max). Part of VxWorks bootline if *useflpar*=0. (400 chars max if *useflpar*=1)	Empty string	No	Read/write
ldlogodis	Disable load of boot logo (bool)	0	No	Read/write
mmstartup (startup)	Start-up string 144 chars max if *useflpar*=0 512 chars max if *useflpar*=1	Empty string	No	Read/write
nobanner	Disable ASCII banner on start-up	0	No	Read/write
noecc	Do not use ECC even if board supports it (bool)	0	No	Read/write
nspeed0/1/2	Speed setting for Ethernet interface 0..2. Possible values: *AUTO*, *10HD*, *10FD*, *100HD*, *100FD*, *1000*	AUTO	Yes	Read/write
stdis	Disable POST (bool)	0	No	Read/write
stdis_XXX	Disable POST test with name XXX (bool) *stdis_ether* – Internal ETHER0/1/2 loopback *stdis_nand* – NAND Flash test *stdis_fpga* – FPGA test *stdis_fram* – FRAM test *stdis_sram* – SRAM test[1] *stdis_touch* – Touch controller test	0	No	Read/write
stignfault	Ignore POST failure, continue boot (bool)	1	No	Read/write

Parameter (alias)	Description	Standard Default	Parameter String	User Access
stwait	Time in 1/10 seconds to stay at least in SELFTEST state (decimal) 0 = Continue as soon as POST has finished	30	No	Read/write
tdp	Telnet server TCP port (decimal)	-1	No	Read/write
tries	Number of network tries	20	No	Read/write
tto	Minimum timeout between network retries (decimal, in seconds)	0	No	Read/write
u00..u15	User parameters (hex, 16 bits)	0x0000	No	Read/write
updcdis	Disable auto update check (bool)	0	No	Read/write
useflpar	Store *kerpar* and *mmstartup* parameters in boot Flash rather than in EEPROM (bool)	0	No	Read/write
vmode	Vesa Video Mode for graphics console (hex) (see Chapter 4.7.2 Video Modes on page 59)	0x0101	No	Read/write
wdt	Time after which watchdog timer shall reset the system after MENMON has passed control to operating system (decimal, in 1/10 s) If 0, MENMON disables the watchdog timer before starting the operating system.	0 (disabled)	No	Read/write

[1] If SRAM is implemented.

Table 34. *MENMON – ESM system parameters – VxWorks bootline parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
bf (bootfile)	Boot file name (127 chars max)	Empty string	No	Read/write
bootdev	VxWorks boot device name	Empty string	No	Read/write
e (netip)	IP address, subnet mask, e.g., 192.1.1.28:ffffff00	Empty string	No	Read/write
g (netgw)	IP address of default gateway	Empty string	No	Read/write
h (nethost)	Host IP address (used when booting over *NBOOT TFTP*)	Empty string	No	Read/write
hostname	VxWorks name of boot host	Empty string	No	Read/write
netaddr	Access the IP address part of *netip* parameter		No	Read/write
netsm	Access the subnet mask part of *netip* parameter		No	Read/write
procnum	VxWorks processor number (decimal)	0	No	Read/write
s	VxWorks start-up script	Empty string	No	Read/write
tn (netname)	Host name of this machine	Empty string	No	Read/write
unitnum	VxWorks boot device unit number (decimal)	0	No	Read/write

4.7.6.4 Reset Cause – Parameter *rststat*

The following *rststat* values are possible:

When MENMON starts up, it determines the reset cause and sets system parameter *rststat* accordingly:

Table 35. *MENMON – Reset causes through system parameter* rststat

***rststat* Value**	**Description**
hrst	Board was reset due to activation of HRESET line
pwon	Power On
pdrop	Power error
swrst	Board was reset by software (by means of the board's reset controller).
wdog	Board was reset by FPGA watchdog time-out (reset controller)
rbut	Board was reset by an external reset pin (e.g., reset button)

4.8 MENMON Commands

The following table gives all MENMON commands that can be entered on the ESM MENMON prompt. You can fork up this list also using the *H* command.

A green background marks commands different to the global specification.

Table 36. *MENMON – Command reference*

Command	Description
.[<reg>] [<val>]	Display/modify registers in debugger model
ACT [<addr>] [<size>]	Execute a HWACT script
ARP	Dump network stack ARP table
B[DC<no>] [<addr>]	Set/display/clear breakpoints
BIOS_DBG <mask> [net] | cons <clun>	Set MENMON BIOS or network debug level, set debug console
BO [<addr>] [<opts>]	Call OS bootstrapper
BOOTP [<opts>]	Obtain IP config via BOOTP
C[BWLLNAX#] <addr> [<val> ...]	Change memory
CHAM-LOAD [<addr>]	Load FPGA
CHAM [<clun>]	Dump FPGA Chameleon table
CONS	Show active consoles
CONS-ACT <clun1> [<clun2>] ...	Test console configuration
CONS-GX <clun>	Test graphics console
D [<addr>] [<cnt>]	Dump memory
DBOOT [<clun>] [<dlun>] [<opts>]	Boot from disk
DCACHE ON | OFF	Enable/disable L1 data cache
DIAG [<which>] [VTF]	Run diagnostic tests
DSKRD <args>	Read blocks from RAW disk
DSKWR <args>	Write blocks to RAW disk
EER[-xxx] [<arg>]	Raw serial EEPROM commands
EE[-xxx] [<arg>]	Persistent system parameter commands
ERASE <D> [<O>] [<S>]	Erase Flash sectors
ESMCB-xxx	ESM carrier commands
FI <from> <to> <val>	Fill memory (byte)
GO [<addr>]	Jump to user program
H HELP	Print help (list commands)
I [<D>]	List board information
ICACHE ON | OFF	Enable/disable L1 instruction cache
IOI	Scan for BIOS devices
LM81	Show monitor values

Command	Description
LOGO	Display MENMON start-up text screen
LS <clun> <dlun> [<opts>]	List files/partitions on device
MC <addr1> <addr2> <cnt>	Compare memory
MII <clun> [<reg>] [<val>]	Ethernet MII register command
MO <from> <to> <cnt>	Move (copy) memory
MS <from> <to> <val>	Search pattern in memory
MT [<opts>] <start> <end> [<runs>]	Memory test
NBOOT [<opts>]	Boot from Network
NDL [<opts>]	Update Flash from network
NETSTAT	Show current state of networking parameters
PCI-VPD[-] <devNo> [<busNo>] [<capId>]	PCI Vital Product Data dump
PCIC <dev> <addr> [<bus>] [<func>]	PCI config register change
PCID[+] <dev> [<bus>] [<func>]	PCI config register dump
PCI	PCI probe
PCIR	List PCI resources
PCI-VPD[-] <devNo> [<busNo>] [<capId>]	PCI Vital Product Data dump
PFLASH <D> <O> <S> [<A>]	Program Flash
PGM-XXX <args>	Media copy tool
PING <host> [<opts>]	Network connectivity test
RELOC	Relocate MM to RAM
RST	Cause an instant system reset
RTC[-xxx] [<arg>]	Real time clock commands
S [<addr>]	Single step user program
SERDL [<passwd>]	Update Flash using YModem protocol
SETUP	Open interactive Setup menu

5 Organization of the Board

To install software on the board or to develop low-level software it is essential to be familiar with the board's address and interrupt organization.

5.1 Memory Mappings

Table 37. *Memory map – processor view*

CPU Address Range	Size	Description
0x 0000 0000..End of RAM	512/1024/ 2048 MB	SDRAM
0x 8000 0000..EFFF FFFF	1792 MB	PCI Memory Space
0x F000 0000..F00F 0000	64 MB	CCSR
0x F200 0000..F200 3FFF		Config PLD
0x F300 0000..F301 FFFF		FRAM (opt.)
0x FB00 0000..FBFF FFFF	16 MB	PCI I/O / ISA Space
0x FF00 0000..FFFF FFFF	16 MB	Boot Flash

Table 38. *Address mapping for PCI*

CPU Address Range	Mapped to PCI Space	Description
0x 8000 0000..83FF FFFF	0x 8000 0000..83FF FFFF (MEM)	Prefetchable BARs of onboard FPGA
0x 8400 0000..8FFF FFFF	0x 8400 0000..8FFF FFFF (MEM)	Prefetchable BARs of all other PCI devices
0x 9000 0000..EFFF FFFF	0x 9000 0000..EFFF FFFF (MEM)	Non-prefetch-able BARs
0x FB00 0000..FBFE FFFF	0x 0000 0000..00FE FFFF (MEM)	PCI ISA mem-ory
0x FBFF 0000..FBFF 0FFF	0x 0000..0FFF (I/O)	PCI I/O space of onboard FPGA
0x FBFF 1000..FBFF FFFF	0x 1000..FFFF (I/O)	PCI I/O space of all other PCI devices

5.2 Interrupt Handling

Interrupt handling between the FPGA and the CPU is done via the 12 external interrupt lines of the CPU (IRQ[0..11]). While the IRQ lines 8 to 11 are used as the four PCI interrupt lines (see Table 40, Interrupt numbering assigned by MENMON, on page 72), each FPGA unit interrupt is routed to a dedicated interrupt line. The mapping is as follows:

Table 39. *Dedicated interrupt line assignment*

MPC854X External Interrupt Line	FPGA Function
IRQ[1]	IDE (UDMA capable)
IRQ[2]	GPIOs
IRQ[3]	UARTs
IRQ[4]	SPI (Touch controller)
IRQ[5]	NAND Flash IDE
IRQ[6]	User module 1
IRQ[7]	User module 2

Table 40. *Interrupt numbering assigned by MENMON*

MPC854X IRQ Input	PCI Interrupt Line	Assigned Number (MENMON)
IRQ8	INTA	0x8
IRQ9	INTB	0x9
IRQ10	INTC	0xA
IRQ11	INTD	0xB

5.3 SMB Devices

Table 41. *SMB devices*

Address	Function
0x5E	LM81 hardware monitor
0xA0	Reserved
0xA2	Real-time clock
0xA8	CPU EEPROM (512 bytes)
0xAC	Carrier board EEPROM (if present and supported)

5.4 PCI Devices on Bus 0

Table 42. *PCI devices on bus 0*

Device Number	Vendor ID	Device ID	Function	Interrupt
0x00	0x1057	0x0012	PCI host bridge in MPC854X	-
0x13	0x1A88	0x4D45	FPGA	
0x14			PCI-104 slot 1	INTA
0x15			PCI-104 slot 2	INTB
0x16			PCI-104 slot 3	INTC
0x17			PCI-104 slot 4	INTD

6 Appendix

6.1 Literature and Web Resources

- EM9 data sheet with up-to-date information and documentation:
  www.men.de/products/15em09-.html
- EM9A data sheet with up-to-date information and documentation:
  www.men.de/products/15em09a.html

6.1.1 PowerPC

- MPC8548:
  MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual
  MPC8548ERM; 2007; Freescale Semiconductor, Inc.
  www.freescale.com

6.1.2 PCI-104

- PCI-104:
  PCI-104 Specification; PC/104 Embedded Consortium
  www.pc104.org

6.1.3 Ethernet

- Ethernet in general:
  - The Ethernet, A Local Area Network, Data Link Layer and Physical Layer Specifications, Version 2.0; 1982; Digital Equipment Corporation, Intel Corp., Xerox Corp.
  - ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE
    www.ieee.org
- www.ethermanage.com/ethernet/
  links to documents describing Ethernet, components, media, the Auto-Negotiation system, multi-segment configuration guidelines, and information on the Ethernet Configuration Guidelines book
- www.iol.unh.edu/training/ethernet.html
  collection of links to Ethernet information, including tutorials, FAQs, and guides
- ckp.made-it.com/ieee8023.html
  Connectivity Knowledge Platform at Made IT technology information service, with lots of general information on Ethernet

6.1.4 EIDE

- EIDE:
  Information Technology - AT Attachment-3 Interface (ATA-3), Revision 6, working draft; 1995; Accredited Standards Committee X3T10

6.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the ESM. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 7. *Labels giving the board's article number, revision and serial number*