iVPI™

Integrated Vital Processor Interlocking Control System

Product Overview

Product Overview Manual
P2521A

iVPI™

Integrated Vital Processor Interlocking Control System

Product Overview

Product Overview Manual
Alstom Signaling Inc.

P2521A, Rev. G, November 2013, Printed in U.S.A.

LIST OF EFFECTIVE PAGES

P2521A, iVPI Integrated Vital Processor Interlocking Control System Product Overview Manual

ORIGINAL ISSUE DATE:	October 2008
CURRENT REVISION AND DATE:	Rev G, November 2013
PAGE	CHANGE OR REVISION LEVEL
Cover	Nov/13
Title page	Nov/13
Preface	Nov/13
i through viii	Nov/13
1–1 through 1–6	Nov/13
2–1 through 2–18	Nov/13
3–1 through 3–4	Nov/13
4–1 through 4–32	Nov/13
5–1 through 5–8	Nov/13
6–1 through 6–14	Nov/13
7–1 through 7–6	Nov/13
8–1 through 8–2	Nov/13
9–1 through 9–2	Nov/13
10–1 through 10–2	Nov/13
A–1 through A–4	Nov/13

THIS PAGE INTENTIONALLY LEFT BLANK.

PREFACE

NOTICE OF CONFIDENTIAL INFORMATION

Information contained herein is confidential and is the property of Alstom Signaling Inc. Where furnished with a proposal, the recipient shall use it solely to evaluate the proposal. Where furnished to customer, it shall be used solely for the purposes of inspection, installation, or maintenance. Where furnished to a supplier, it shall be used solely in the performance of the contract. The information shall not be used or disclosed by the recipient for any other purposes whatsoever.

FOR QUESTIONS AND INQUIRIES, CONTACT CUSTOMER SERVICE AT
1–800–717–4477
OR
WWW.ALSTOMSIGNALINGSOLUTIONS.COM

ALSTOM SIGNALING INC.
1025 JOHN STREET
WEST HENRIETTA, NY 14586

REVISION LOG

Revision	Date	Description	By	Checked	Approved
1(A)	October 2008	Original issue	MAS	NI	NI
2(B)	April 2010	Added board Part Numbers, BEX, and PTC	MAS	RH	CZ
3(C)	March 2011	Updated configuration and subracks	MAS	RH	NI
4(D)	May 2011	Updated to reflect current product	JF	RH	NI
5(E)	March 2012	Updated to support new BEX boards, cables, and chassis	JF	RH	NI
6(F)	February 2013	Updated	LR	KW	NI
G	November 2013	Updated to include additional warnings	SG	KW	MS

ABOUT THE MANUAL

This manual is intended to introduce the Alstom Integrated Vital Processor Interlocking Control System (iVPI).

The information in this manual is arranged into sections. The title and a brief description of each section follow:

Section 1 – GENERAL DESCRIPTION: This section describes the manual organization, introduces the topics covered, and provides a glossary of terms used in this manual.

Section 2 – SYSTEM ORGANIZATION: This section gives general information on function and organization of the iVPI System.

Section 3 – SUBRACK CONFIGURATION: This section describes the Subrack used for the iVPI System.

Section 4 – VITAL SUBSYSTEM: This section describes the Vital boards and assemblies used in the iVPI System.

Section 5 – NON VITAL SUBSYSTEM: This section describes the non-vital boards and assemblies used in the iVPI System.

Section 6 – DESIGN, TEST AND VALIDATION TOOLS: This section describes the design, test, and validation tools used for the iVPI System.

Section 7 – NON-VITAL SYSTEM AND COMMUNICATIONS SOFTWARE: This section describes the non-vital System and communications software used in the iVPI System.

Section 8 – MIGRATION STRATEGIES: This section describes the migration strategies for migrating existing VPI® Systems to iVPI Systems.

Section 9 – REDUNDANCY, AVAILABILITY AND ISOLATION: This section describes the iVPI System redundancy, availability and isolation.

Section 10 – SUMMARY: This section summarizes the benefits of using the iVPI System.

Appendix A – HISTORY OF THE VPI PRODUCT LINE: This section describes the history and evolution of the VPI® product line.

THIS PAGE INTENTIONALLY LEFT BLANK.

MANUAL SPECIAL NOTATIONS

In the Alstom manuals, three methods are used to convey special informational notations. These notations are warnings, cautions, and notes. Both warnings and cautions are readily noticeable by boldface type and a box around the entire informational statement.

Warning

A warning is the most important notation to heed. A warning is used to tell the reader that special attention needs to be paid to the message because if the instructions or advice is not followed when working on the equipment then the result could be either serious harm or death. The sudden, unexpected operation of a switch machine, for example, or the technician contacting the third rail could lead to personal injury or death. An example of a typical warning notice follows:

> **WARNING**
>
> Disconnect motor energy whenever working on switch layout or switch machine. Unexpected operation of machine could cause injury from open gears, electrical shock, or moving switch points.

Caution

A caution statement is used when an operating or maintenance procedure, practice, condition, or statement, which if not strictly adhered to, could result in damage to or destruction of equipment. A typical caution found in a manual is as follows:

> **CAUTION**
>
> Turn power off before attempting to remove or insert circuit boards into a module. Boards can be damaged if power is not turned off.

Note

A note is normally used to provide minor additional information to the reader to explain the reason for a given step in a test procedure or to just provide a background detail. An example of the use of a note follows:

> Note: This step should be done first to validate the correct information is used.

THIS PAGE INTENTIONALLY LEFT BLANK.

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 1 – GENERAL DESCRIPTION

1.1 GENERAL

This document contains a general description of the Alstom iVPI Vital Processor Interlocking Control System. It contains basic, system level information, and hardware descriptions and is intended to be used to estimate the items required to satisfy a specific interlocking's control requirements.

CAUTION

Be aware this manual is not intended as an Application or Operation and Maintenance manual.

Detailed information for applying and configuring an iVPI System is available in the following Alstom publications:

P2521B V1	iVPI Gen Install., Operation and Theory
P2521B V2	iVPI Subrack Configuration
P2521B V3	iVPI Vital Subsystem
P2521B V4	iVPI Non-Vital Subsystem
P2521B V5	iVPI Maintenance and Troubleshooting
P2512A	Computer-Aided Application Programming Environment Software Package CAAPE User Manual
P2512F	iVPI Computer Aided Application (CAA) Reference Manual

1.2 SYSTEM TERMS

The iVPI System is highly modular in design, implemented in a 19-inch rack mounted card cage (Subrack) with a set of plug-in printed circuit boards (boards) that are applied in varying quantities to meet the needs of specific applications.

The terminology used to define the Subrack and its components is as follows:

- A Subrack is a Chassis with Motherboard
- A System is one or more Subracks filled with the appropriate boards for the application
- When a System is configured with more than one Subrack populated with boards, the individual populated Subracks are Subsystems

1.3 ACRONYMS AND ABBREVIATIONS

Terms and abbreviations used throughout this manual are provided in Table 1–1.

Table 1–1. Glossary

Term	Definition
ACO	Vital AC Output board
ADV	Application Data Verifier
AF	Audio Frequency
AlsDload	A tool for programming application and system software on VPI, iVPI, PGK, PGK2, GK3, and AFTC boards
AOCD	Absence Of Current Detector
AREMA	American Railway Engineering and Maintenance-of-Way Association
ARES	Advanced Railroad Electronic System
ATC	Automatic Train Control
ATCS	Automatic Train Control System
ATO	Automatic Train Operation
ATP	Automatic Train Protection
BEX	Bus Expansion board
CAA	Computer-Aided Application
CAAPE	Computer-Aided Application Programming Environment
Chassis	The hardware case; it becomes a Subrack when the Motherboard is installed and a System or Subsystem when populated with boards
CIC	Cable Integrity Check
CMOS	Complementary Metal-Oxide-Semiconductor, a major class of integrated circuits; CMOS devices use little power and do not produce as much heat as other forms of logic
COF	Cycle of Forgiveness
Compiler	Program that translates a high-level computer language into machine language
CPU	Central Processing Unit – the computer section that handles the actual processing of data into information
CRC	Cyclical Redundancy Checks
CRG	Code Rate Generator board

Table 1–1. Glossary (Cont.)

Term	Definition
DBO	Double Break Output board
Diagnostic	The process of detection and isolation of either a malfunction or a mistake
Diagnostic Routine	A routine designed specifically to locate a malfunction in the computer
DI	Direct Input board
EIA	Electronic Industries Alliance
EMI	Electromagnetic Interference
EPROM	A programmable read-only memory device that is erasable using high intensity ultra-violet light
Fail-safe	The concept that if a system fails only a safe result will occur
Firmware	Instructions stored on a ROM chip
FLASH	A form of electrically erasable programmable read only memory used with embedded processors
FPGA	Field Programmable Gate Array
FRA	Federal Railroad Administration
GTP	Genrakode Track Processor
Hardware	The electronic section of the computer that stores and manipulates symbols under the direction of the computer
HMI	Human Machine Interface
I^2C	Inter-Integrated Circuit
I/O	Input/Output
iVPI	Alstom's integrated Vital Processor Interlocking product
Interface	The equipment that enables one kind of hardware to be recognized and processed by another kind of hardware
Latch	A mode of operation for a circuit in which an output's state is maintained
LCP	Local Control Panel
LDO	Lamp Driver Output board
LRT	Light Rail Transit
MAC	Maintenance Access connection point in a system. This enables the connection of a VT100-compatible terminal to examine system diagnostics and internal operation of the system

Table 1–1. Glossary (Cont.)

Term	Definition
MMS	Maintenance Management System
Modem	A piece of equipment that connects data terminal equipment to a communication line
MODBUS	A messaging structure used to establish master-slave/MODBUS/TCP communication between intelligent devices
MUX	Multiplexer
NISAL	Numerically Integrated Safety Assurance Logic
Non-Vital	A component or function that is not critical to safety, its failure is not considered critical to the safe operation of a railroad but may be significant operationally
NVI	Non-Vital Input board
NVO	Non-Vital Output board
NVSP	Non-Vital System Processor board
PCB	Printed Circuit Board (board)
POR	Power On Reset
Program	A series of instructions for the computer to follow
PROM	Programmable Read-Only Memory – programmable memory devices that store firmware
PTC	Positive Train Control
RAM	Random Access Memory – this part of memory temporarily stores information that is constantly being changed in the computer; here, words may be stored (written) or read (retrieved) in any order at random
Reset	The act of changing a bit value to zero or an output to an inactive condition. Also refers to the startup or restart of a processor-based system
RF	Radio Frequency
ROM	Read-Only Memory – this part of memory is built in during the integrated circuit fabrication process; ROM content cannot be altered after the chip is produced
RTU	Relay Test Unit
SBO	Single Break Output board
SCADA	Supervisory Control And Data Acquisition
Simulator	A special program that represents the behavior of a system

Table 1–1. Glossary (Cont.)

Term	Definition
SMT	Surface Mount Technology
Software	Programs that direct the activity of the computer
Subrack	Chassis with Motherboard; it becomes a System or Subsystem when populated with boards
Main Subrack	The Subrack housing the VSP
Expansion Subrack	One of up to three additional Subracks that house a Bus Expansion board in place of a VSP
Subroutine	A section of a program that carries out a specific operation
Subsystem	Used to summarize the Vital or non-vital functions of an iVPI System, as in Vital Subsystem and non-vital Subsystem
Subsystem (iVPI)	One of multiple Subracks populated with boards in a System configuration composed of more than one Subrack
System (iVPI)	One or more Subracks populated with boards
Task	A program that is run as an independent unit
TTL	Transistor-Transistor Logic
TWC	Train-to-Wayside Communications
Vital Component or Circuit	Any device, circuit or software module used to implement a Vital function; a Vital circuit is so named because its function is critical to the operation of certain signals and track equipment
Vital Function	A system, subsystem, equipment or component that provides a function critical to safety; its failure is considered critical to the safe operation of a railroad; it is implemented using fail-safe design principals, hardware, software and/or relays
VRD	Vital Relay Driver board
VSC	Vital Serial Controller board that provides a means for exchanging the states of Vital interlocking functions between interlocking systems in a Vital manner
VSOE	Vital Serial Over Ethernet
VSP	Vital System Processor board
w/o	Without

.

SECTION 2 – SYSTEM ORGANIZATION

2.1 GENERAL

This section describes the organization of the iVPI System.

2.2 EVOLUTION TO IVPI

First introduced in 2007, the iVPI version of the VPI family offers the newest upgrades in electronics packaging and the latest in surface mount technology (SMT). iVPI Systems maintain the usage of the same Vital hardware designs and Vital software algorithms as the earlier generations of the VPI family. Like the previous generations of the VPI family, iVPI is functionally compatible with previous versions of the family and is designed for long life cycle support and upgrades.

2.3 IVPI INTERNAL ARCHITECTURE

Alstom's integrated Vital Processor Interlocking (iVPI) System seamlessly integrates Vital and non-vital functions, including Vital and non-vital communications. Adding in the Ethernet networking capability, iVPI can communicate with a large number of Vital and non-vital devices (see Section 2.6 for details). See Figure 2–1 for general iVPI product architecture.

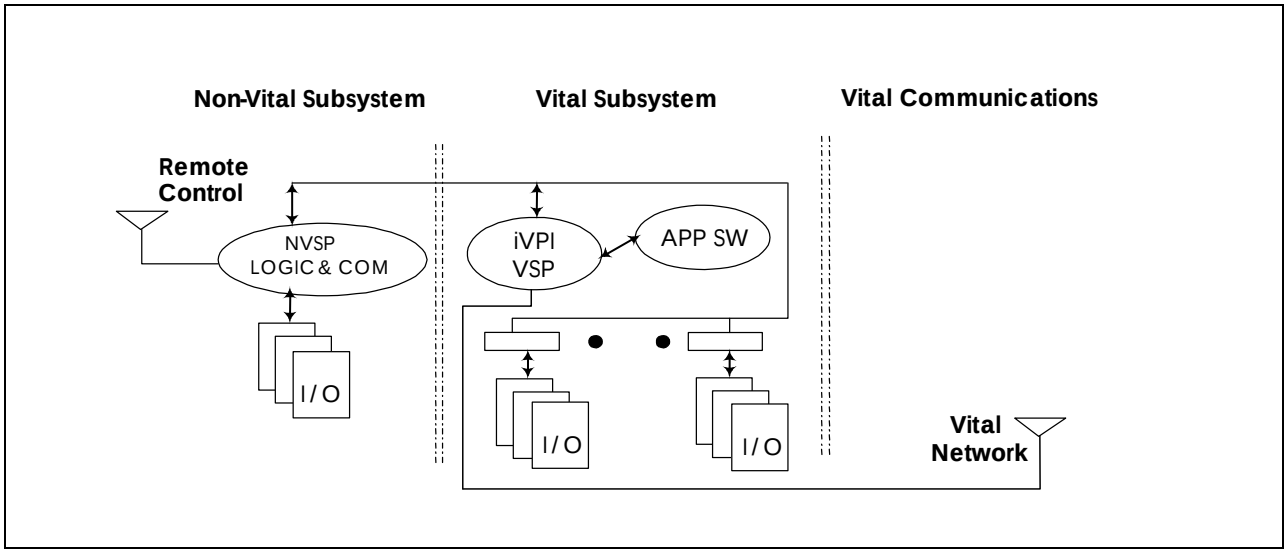

Figure 2–1. Overall Architecture, IVPI-Based Interlocking

2.4 IVPI GENERAL FUNCTIONS

The Interlocking subsystem provides the Vital fail-safe interface with the signaling Field Equipment. The electronic interlocking is Alstom's integrated Vital Processing Interlocking (iVPI) control system.

The iVPI System comprises Vital and non-vital subsystems, both of which are optional. Normally, both are present, although both Vital-only and non-vital-only systems may be configured. An iVPI System may have no more than one Vital subsystem but up to four non-vital subsystems.

The iVPI Vital subsystem consists of:

- A single fail-safe Vital System Processor (VSP) with integrated Vital communications protocols over Ethernet UDP/IP and non-vital communications over Ethernet TCP/IP to the Alstom Maintenance Management System (MMS).
- Family of fail-safe Vital I/O to/from remote signaling devices and Vital field apparatus such as switch machines, train stops, track circuits, signal lamps and LED arrays, highway crossing equipment, cab signaling equipment, and more.
- Integrated Genrakode Track Processor (GTP) where required for direct interface at control points to the coded track circuits. Other integrated Track Circuit functions are possible.
- Integrated Code Rate Generator (CRG) for generating the speed command pulses used to modulate the carrier frequency (for example, 60 Hz) for track circuits within the interlocking plant and at the interlocking end of the approach track circuits.
- Bus Expansion (BEX) modules that facilitate the expansion of the iVPI System into multiple Subracks (see Section 3).

The iVPI non-vital subsystem consists of:

- A single Non-Vital System Processor (NVSP) with integrated Ethernet TCP/IP, synchronous and asynchronous communication channels capable of simultaneously supporting multiple communication protocols and MMS.
- Family of Non-Vital I/O to interface with non-vital signaling apparatus such as Local Control Panels (LCP), intrusion alarms, non-vital train inspection equipment, and more.

The Vital and non-vital subsystems generally operate independently with the exception of an Application Data exchange channel that may be configured between the VSP and each NVSP.

2.5 COMPETITIVE BENEFITS OF IVPI SYSTEMS

- Scalability/Modularity – iVPI Systems can be arranged in many user-programmable system configurations ranging from:
  - Fully centralized logic and I/O; to
  - Centralized logic with remote I/O and object controllers; to
  - Fully distributed self-standing systems
- Network Interfaces – the iVPI platform provides improved integration with transparent interface-to-radio offerings, providing Vital and non-vital communications to fit the need of the application. Included in the networking improvements is the addition of Ethernet connectivity, which is described in greater detail in Section 2.8.
- System Maintainability – iVPI supports more cost-effective maintenance than other systems, including the:
  - “Health status” monitors on the front panel of each board, simplifying and reducing maintenance time,
  - Elimination of wire wraps eliminates potential rewiring expense, Vital I/O headers and Signature PROMS,
  - Eurocard 9U Subrack and surface mount boards reduce potential future obsolescence issues, and
  - Electronic revision configuration control simplifies the new FRA compliance rules
- Plug & Play Capability – Built-in slot definitions automatically configure I/O boards with unique signature and header assignments. Moving a board to a different slot reconfigures the board without changing any board devices. Intelligent software tools and hardware decrease system complexity, yet allow the system to be highly configurable.
- Compatibility – the new iVPI platform is compatible with previous versions of the VPI family, and is designed for long life cycle support and upgrades.
- Redundant vs. Non-Redundant – iVPI Systems can operate with no redundancy, while providing extremely high reliability and availability, as well as in system and subsystem arrangements with redundant pairs to provide hot standby and automatic failover.
- System Testing – the iVPI VSP board has both a Communications processor as well as a Main processor with separate application programming that minimizes retesting. Minimal retesting results in lower system serviceability and maintainability requirements, which equate to lower system costs.

- System Safety – the iVPI platform is based on the proven VPI and Genrakode safety design case that utilizes Numerically Integrate Safety Assurance Logic (NISAL™) to ensure system safety.
- Spares – smaller systems with fewer boards result in lower spares requirements. Reducing the costly rack-mounted power supplies (by moving the power supplies directly to each system board) results in further reductions to spares inventory.

  Further spares reductions occur when a system uses the Genrakode Track Processor (GTP) board for track circuit control. iVPI integrates this functionality into one system, alleviating the previously required Genrakode module and boards.
- Application Software Changes – through use of the CAAPE tool, the engineer or maintainer can download software directly to the VSP and NVSP boards and verify CRCs. There is no need for external PROM burners or PC RS232 converter devices.

2.6 IVPI GENERAL SPECIFICATIONS

Table 2–1 lists the nominal specifications for the iVPI System (Subrack(s) and boards). Additional board voltages can be supported as required by specific applications. It is to be understood that iVPI represents a generic platform that can be used in Freight, Commuter, Light Rail, and Heavy Rail Transit applications. Table 2–2 lists the boards used in the iVPI System. Not all maximum board configurations can be arranged in a single application. For example, the number of allowable GTP boards decreases by the number of CRG boards configured in a system.

See Alstom publication P2521B for specification details for each board.

Table 2–1. iVPI Specifications

Product Characteristics	Alstom iVPI (Typical per System)
Number of Track Circuits Supported by GTP	Up to 20 track circuits per system, 2 track circuits per GTP, maximum 10 GTP boards per system
Maximum Track Circuit Length Supported by GTP	24,000 feet @ 3 ohms per 1,000 feet ballast non-electrified territory
Lamp Control	8 outputs per board
Cab Signal Generator Controls	8 outputs per board; maximum 3 CRG boards per system
Operating Voltages	9–16 VDC (RR and Transit)
Networking Capability	VSP has 2 Ethernet Device Interfaces for connectivity of up to 32* nodes using the VSOE protocol plus MMS NVSP has 2 Ethernet Device Interfaces that support up to 10 TCP/IP connections plus MMS (* dependent on system configuration)
Scalability	Control of a single switch point to a complex interlocking
Recorder Logging Capability	Approximately 50,000 events; unlimited when coupled with periodic log data retrieval via MMS.
Graceful Degradation	Achievable between interlocking control and track circuits through system partitioning

Table 2–1. iVPI Specifications (Cont.)

Product Characteristics	Alstom iVPI (Typical per System)
Vital Inputs/Outputs	8 outputs per board; maximum 40 boards per system, 320 ports 16 inputs per board; maximum 20 boards per system, 320 ports
Non-Vital Inputs/Outputs	32 inputs per board 32 outputs per board 19 boards per subrack

WARNING

iVPI contains special safety circuit components which must only be replaced by components specified by the Alstom part number.

These original-design replacement parts are manufactured to the same standards as the original parts; their performance being verified. The use of replacement parts that are not of the same Alstom part number could potentially impair the safe performance of the system.

The railroad or transit system authority and the manufacturer of an aftermarket (i.e., non-Alstom designated) part assume the responsibility that the part will not adversely affect the safe performance of the system. The authority and the manufacturer of the aftermarket part must analyze and certify in writing that use of the part will not result in a failure of the system to comply with safety regulations and safety performance. Completion of such an analysis and certification is considered due diligence and standard practice, will not be reviewed or approved by Alstom, and neither absolves the authority and aftermarket part manufacturer of responsibility nor implies approval by Alstom to use such an aftermarket part. The responsibility of any consequences resulting from using such a part remains with the authority and part manufacturer.

Table 2–2. iVPI Board Part Numbers

Board Type	Drawing Number	Comments
Vital System Processor (VSP)	31166-427-01	386 Processor, 2 Ethernet Ports, I-O Bus Interface, Vital Relay Driver Operate 9–16 VDC
Direct Input (DI)	31166-429-01	Low Pass Filter, In 9–16 VDC, Differential 16-High/Low True
Direct Input (DI)	31166-429-02	DI, Momentary In-Hold DCAP, In 9–16 VDC, Differential, 16-High/Low True
Direct Input (DI)	31166-429-03	Low Pass Filter, In 24–34 VDC, Differential 16-High/Low True
Single Break Output (SBO)	31166-430-01	Supply 9–30 VDC, 8-Ports
Double Break Output (DBO)	31166-433-01	Supply 10–16 VDC, Output 9–16 VDC, 8-Ports
Double Break Output (DBO)	31166-433-02	Supply 10–15 VDC, Output 18–32 VDC, 8-Ports
Lamp Driver Output (LDO)	31166-431-01	Supply 8–16 VDC, Hot & Cold Check, Cable Integrity Check, Over/Low Current Monitor, 8-Ports
Vital AC Output (ACO)	31166-432-01	Supply 90–130 VAC, 40–150 Hz, 8-Ports, High Current Output
Vital AC Output (ACO)	31166-432-02	Supply 90–130 VAC, 40–150 Hz, 8-Ports, Low Current Output
Code Rate Generator (CRG)	31166-459-01	Code Rates: 0, 50, 75, 120, 180, 270, 420, Steady-On, Solid State Driver
Code Rate Generator (CRG)	31166-459-02	Code Rates: 0, 50, 75, 120, 180, 270, 420, Steady-On, Relay Driver
Bus Expansion (BEX)	31166-460-01	BEX, Bus Expansion Board

Table 2–2. iVPI Board Part Numbers (Cont.)

Board Type	Drawing Number	Comments
Genrakode Track Processor (GTP)	31166-434-01	2-Genrakode DC Track Circuits w/o Ethernet Software, up to 24,000 feet @ 3 ohms per 1,000 feet ballast non-electrified territory
VSP System ID	31166-472-01	Vital Application Revision and Site ID
VSP/BEX Interface	31166-485-01	Expansion Chassis connections
VSP P3 Interface	31166-473-01	2 Ethernet ports, VRD Relay connections
Non-Vital System Processor (NVSP)	31166-428-01	386 Processor, 3 Comm Ports, 2 Ethernet ports
Non-Vital Input (NVI)	31166-457-01	32 inputs, 18–36 VDC
Non-Vital Input (NVI)	31166-457-02	32 inputs, 9–18 VDC
Non-Vital Output (NVO)	31166-458-01	32 Form A mechanical relay outputs, 0–35 V AC/DC, 1 A, Power On Reset
Non-Vital Output (NVO)	31166-458-02	32 Form A solid state outputs, 0–35 V AC/DC, 1 A, Power On Reset
NVSP P1 Interface	31166-474-01	2 Ethernet ports
NVSP P3 Interface	31166-475-01	3 Serial ports

2.7 VERSATILE APPLICATION SCENARIOS FOR IVPI

Compared to other solutions, iVPI's wide range of scalability and interconnectivity provides greater flexibility to deploy signaling components in a way that facilitates more savings. This ranges from smaller room arrangements, to use of small cases where larger rooms were once required, to the placing of the control functions closer to the device being controlled, saving on cable costs.

This new approach, made possible by reducing the form factor of the Vital and non-vital hardware and the use of network connectivity, makes it possible to provide a "best fit" solution to all types of signaling applications. Actual hardware and software elements are described in detail later in the document.

Figure 2–2 is block diagram of an example iVPI application using every board type available for the iVPI System. Figure 2–3 is an example iVPI using the expansion system.

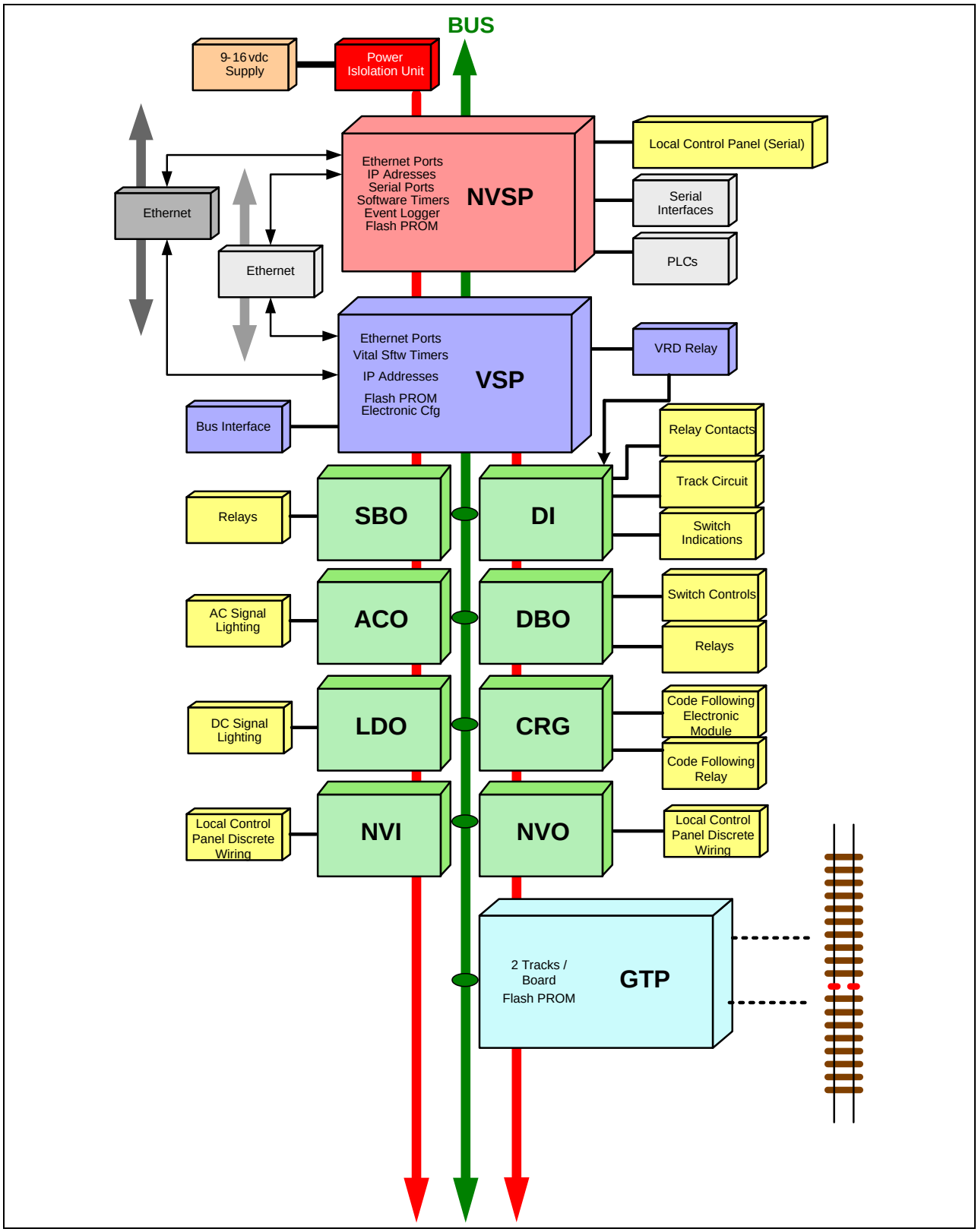

Figure 2–2. Example iVPI Vital/Non-Vital System Application

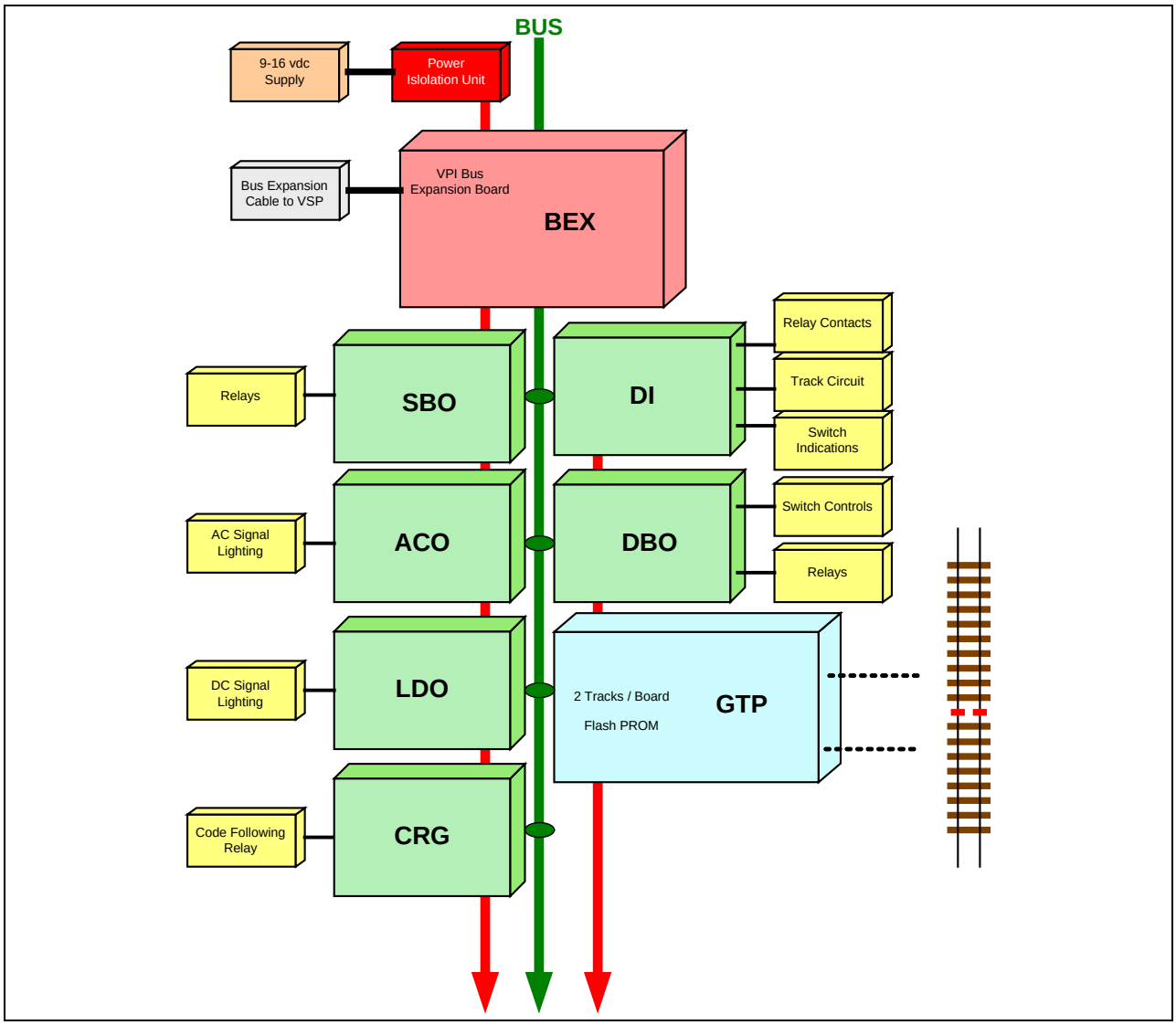

Figure 2–3. Example iVPI Expansion System Application

2.7.1 Freight Railroads

The interlocking function for traditional block signaling applications generally requires a combination of:

- Power supply for interlocking
- Signaling logic (Vital and non-vital)
- Local emergency control
- Communications to a central office with an industry standard protocol
- Local signal and switch machine interfaces
- Local track occupancies and approach track circuits using DC Coded track circuits
- Vital disconnect of load power in case of a safety critical failure

With iVPI, this is accomplished by the use of one electronics system containing:

- A Vital interlocking processor with signaling logic and network connections (Ethernet) to other Systems and MMS diagnostics for 24/7 troubleshooting
- A non-vital processor (if required) for non-vital logic, event recording, local emergency control, interface to CTC, or other, including network interfaces for intra-system communications, MMS diagnostics for 24/7 monitoring, and event log uploads
- A Vital I/O to drive switch and signal and other Vital equipment
- An integrated track circuit for providing full track circuit functionality
- Non-Vital I/O as needed through the use of third-party I/O systems with a serial link and/or Ethernet to the non-vital processor or non-vital I/O boards
- Power from the local signaling batteries is provided directly to the iVPI System with no intermediate power supply elements
- A Vital “B” relay is provided to deliver energy feeds for Vital output circuits in absence of any safety critical failures; backs of the relay are used to light red aspects should a failure occur

The system is capable of providing the status of all interlocking inputs to the Positive Train Control (PTC) network, and optionally receiving code line (non-vital office request) inputs from the PTC network.

This hardware configuration can be easily contained in small rack or case (one control system), supplied with customer pre-engineered application logic rules and ordered with one part number.

2.7.2 Commuter Rail Applications

In North America Commuter Rail Lines, equipment used is that of Freight lines with added cab signaling equipment. For this application, the incremental requirements for the interlocking are:

- Cab signal rate codes assigned per track within the interlocking as well as on approach track circuits
- Freight requirements as noted previously

For iVPI, Commuter Rail use, the incremental functions to be included within the electronics system are:

- An integrated track circuit for providing full track circuit functionality
- A rate code generator which has outputs that can be coded at any of the standard NA and Freight rates
- For Full Commuter Rail applications including intermediate/adjacent track circuits, the same track circuit function as integrated within iVPI electronic system is used in a standalone mode along with a cab signal system to deliver coded rates to the rails

2.7.3 Light Rail Applications

Light Rail applications can take two forms: one where trains run on traditional Freight lines, and others that are more like street-level trams. For Freight-based lines, the requirements are still fulfilled and may or may not include cab signaling or other ATP functions. The requirements represent a superset of those items generally required and provided for with iVPI.

For Systems that mimic a transit orientation, iVPI can integrate many different functions depending on the requirements and type of system desired. This includes functionality for:

- Interfaces to Automatic Train Protection (ATP) Systems, both for train detection and including several levels of cab signaling. ATP logic is resident within the same processor as the signaling logic for the interlocking
- Formation of small Vital control elements using the same hardware and software that can be located centrally to a wayside control room (or case) or distributed along the right of way
- Ease of integration with supplier specified non-vital control systems where required to perform local supervisory control, routing functions, or Train-to-Wayside Communication (TWC) functions

2.7.3.1 ATP or No ATP

iVPI has the interfaces identified previously as well as an interface through the network to Audio Frequency and Digital track circuits where another form of ATP is required. The network interface allows the track circuits to be located in the main equipment room or distributed along the right of way to minimize the use of extended and costly-to-add cable runs.

2.7.3.2 Place Equipment Where It Makes Sense

Also along this line of interconnect, iVPI can be architected to place the location logic resident within the Vital and/or non-vital processors in an equipment house or case and the I/O can be located within the same room or placed at the location of the device to be controlled. This also provides the benefits of cable savings as well as having the remote functions be self-sufficient from a safety perspective. That is, the remote functions have their own Vital checking function. This provides a very high level of availability, as a failure to a remote function does not affect the overall location.

2.7.3.3 Pass Information Any Way Necessary

Along with the Light Rail Transit (LRT) application of iVPI come software and hardware interfaces to support Vital and non-vital communications via network over fiber, radio, or direct wire. An iVPI unit can communicate location-to-location, location-to-control center, or location-to-train in a bidirectional manner.

2.7.3.4 Integrate with Other LRT Specific Control Systems

For applications that require the use of a third party non-vital control system for local emergency control or train routing, iVPI has standard interfaces to communicate status and control data using industry standard protocols such as Modbus and Modbus/TCP or TWC for routing.

2.7.4 Heavy Rail Transit Applications

Based on a wide portfolio of processing and I/O functions (boards), iVPI can be easily applied to NA Metro/Transit applications. Capacity is no issue as one iVPI System can manage an interlocking from 1 to 40[1] switch machines for example while at the same time processing all non-vital logic and communications and interfaces to ATC subsystems.

Available tools and hardware portfolio permit the ability to apply iVPI to:

- Fixed block signaling for interlockings including integrated ATC (Cab Signaling) Logic
- Extensive wayside ATS functions such as driving local hard-wired panels, ATO functions such as station stopping and dwell, SCADA-type functions, and HMI workstations
- Vital and non-vital communications over wire, fiber, or radio
- Local or remote diagnostics and event recording
- Network interface with AF Track circuits or Digital Track Circuits to provide speed commands or temporary speed commands to the vehicle through the rails

2.7.4.1 Large Interlockings

The iVPI portfolio of hardware, software, and tools (design and maintenance) is well suited to manage:

- A small Vital or non-vital control function with one or two boards
- A medium location with up to 20[1] switch machines and associated signals controlled by a single iVPI System
- A large location with hundreds of switch machines and associated signals controlled by multiple iVPI Systems or with a control logic processor

The scalability of iVPI allows this simply by adding the necessary I/O, Serial and/or Ethernet interfaces. An iVPI System can expand from one control Subrack to four Subracks as required for centralized equipment rooms or simply partition into a standalone System as needed. A total of 640 I/O points can be managed directly under the control of each Vital and non-vital processor (when configured as one complete System) or expanded greater with interconnected systems using Ethernet for a distributed approach.

[1] The maximum number of switch machines is application-dependent.

2.8 IVPI ETHERNET CONNECTIVITY OVERVIEW

Each of the iVPI processor boards (both Vital and non-vital) contains two Ethernet devices (media types10/100 BaseT, IEEE 802.3i and 802.3u, respectively) that can be configured in independent or redundant networks. This allows Vital and non-vital messages to be mixed on the same network or to be kept independent from each other on a separate network. The iVPI redundant network configuration is designed to support hot-standby network medium redundancy that facilitates no delay or disruption in the event of a single point network failure (e.g., Ethernet port, cable, network switch, or router).

Each device also supports multiple node connections and protocols. Using the Vital Serial over Ethernet (VSOE) Communications, the two devices on the Vital Serial Processor (VSP) board can handle up to 32[2] VSOE connections to other iVPI, microWIU and track circuit Systems. These can be split as redundant connections with half the total on one device, the other half on another device. One PC-based Maintenance Management System (MMS) connection is also provided.

The Non-Vital Serial Processor (NVSP) board has similar capabilities that service office communications protocols (serially and/or Ethernet) and MMS connections. Both boards could share the same network if there is sufficient bandwidth.

An example of independent and redundant Ethernet backbones can be seen in Figure 2–4 and Figure 2–5.

[2] The maximum number of connections is application-dependent.

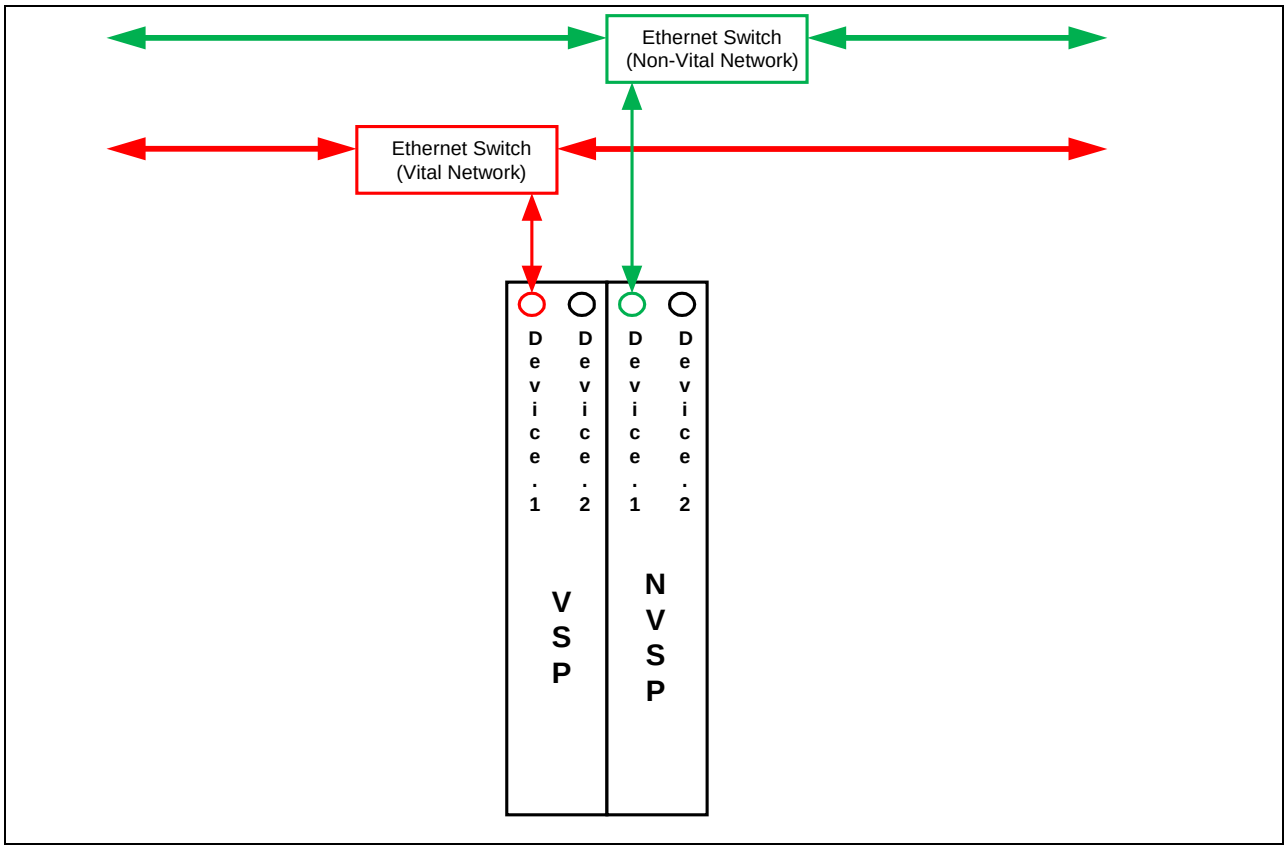

Figure 2–4. Independent Ethernet Backbones Vital Devices Separate from Non-Vital Devices

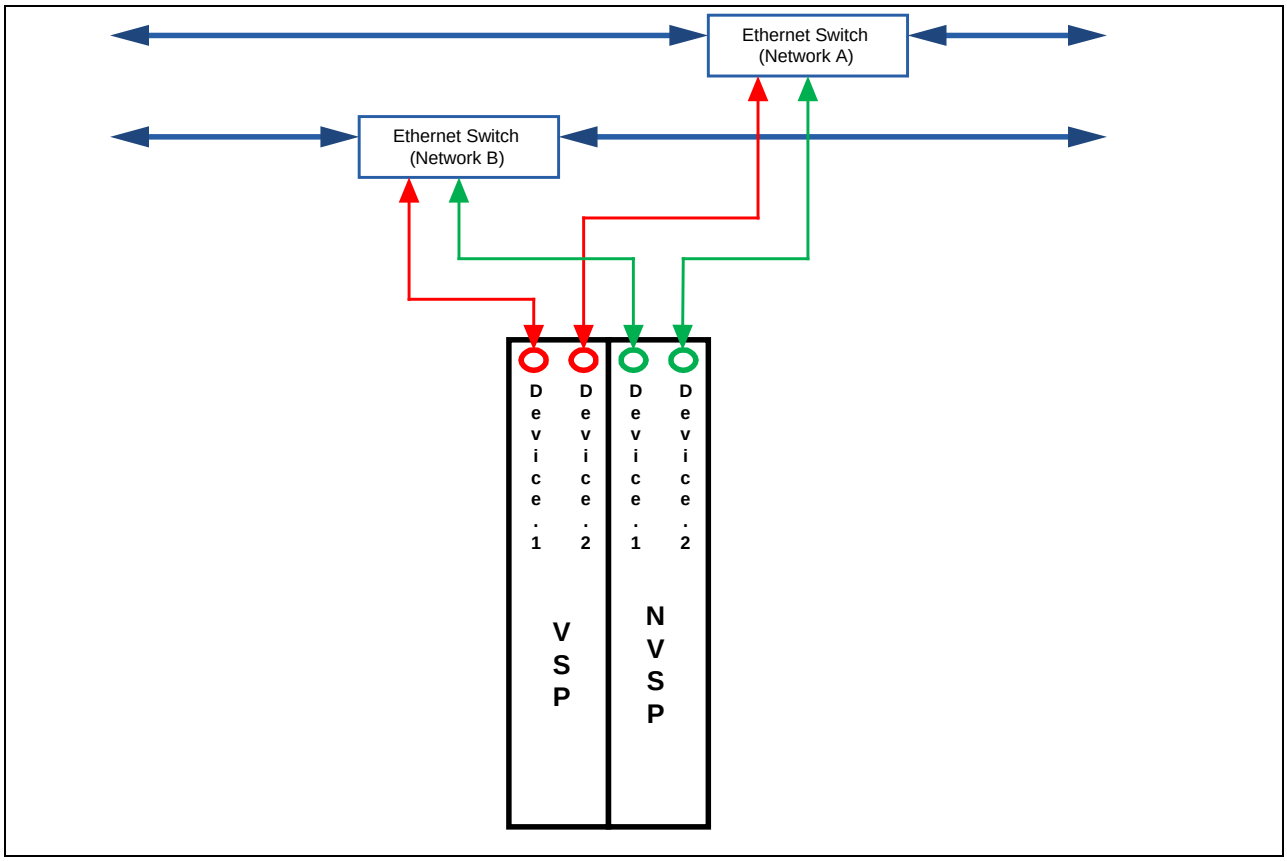

Figure 2–5. Redundant Ethernet Backbones Supporting Vital and Non-Vital Devices

SECTION 3 – SUBRACK CONFIGURATIONS

3.1 GENERAL

This section describes the Subrack configurations of the iVPI System.

3.2 IVPI SUBRACK DESCRIPTION

The iVPI System is highly modular in design, implemented in a 19 inch rack mounted card cage (Subrack) with a set of plug-in printed circuit boards (boards) that are applied in varying quantities to meet the needs of specific applications. iVPI Systems meet and/or exceed all the applicable “AREMA Communication and Signal Manual of Recommended Practices” requirements.

A single iVPI System is housed in one to four Subracks. Each Subrack has space for twenty-one (21) printed circuit boards. The VSP board must occupy slots 1 and 2 of the Main Subrack. Slot 1 of each Expansion Subrack must contain a Bus Expansion (BEX) board to facilitate communications between the VSP and the boards contained in the Subrack.

A single-slot NVSP board may be assigned to any of the slots 3–8 in the Main Subrack or in an Expansion Subrack. Multiple NVSP boards may be assigned to the same Subrack, but only one NVSP in each Subrack may control NVI and NVO boards.

The iVPI Subrack allows for any other board to be inserted into any slot other than 1 or 2, reducing both setup and maintenance time. Figure 3–1 is an illustration showing an example of a full 21-slot Subrack. In smaller systems, any unused board slots may be covered with blank panels.

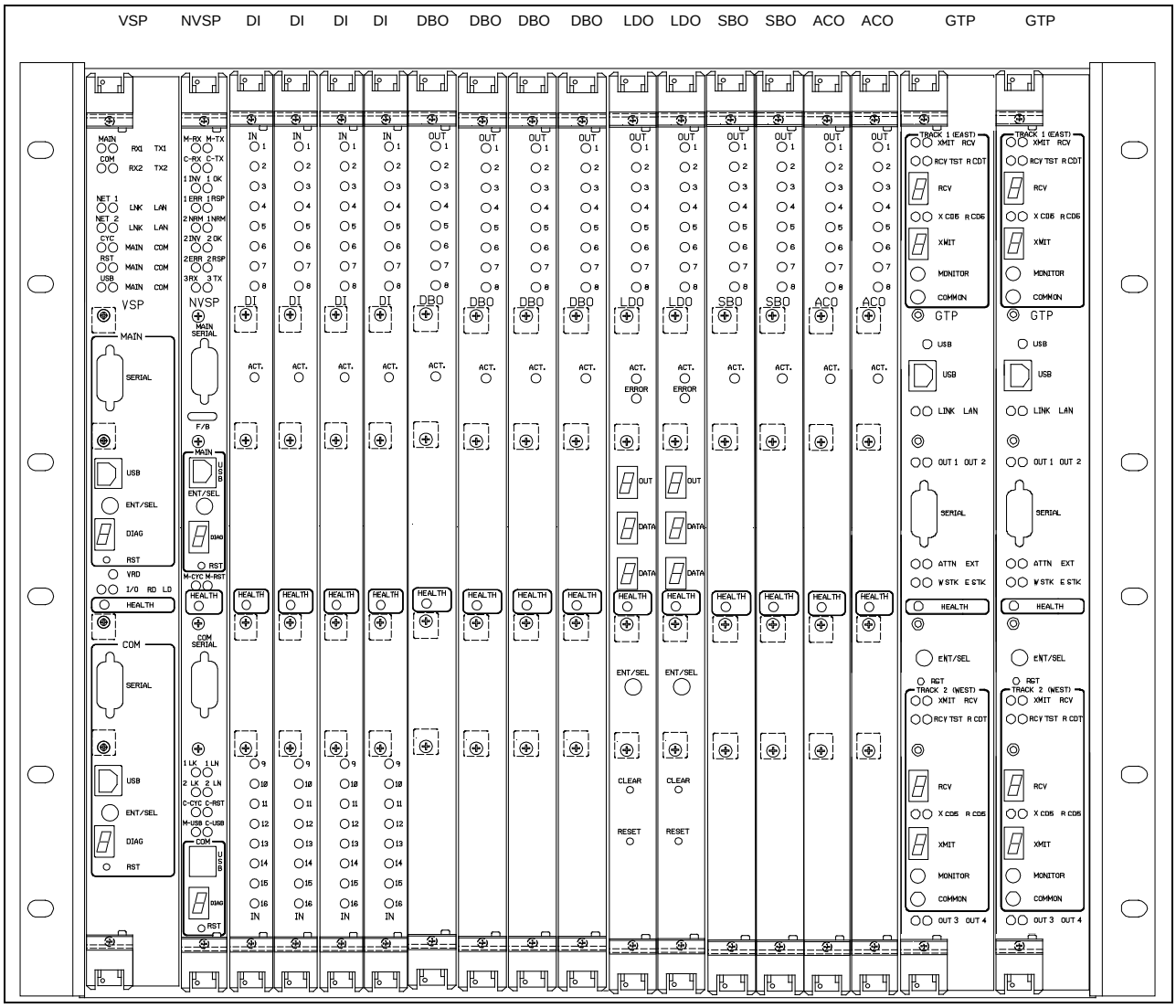

Figure 3–1. 21-Slot iVPI Subrack Filled

All iVPI printed circuit boards:

- Are mechanically keyed to prevent placement of boards in the Subrack in the wrong card slot,
- Contain LED indicators along the front edge of the board that display the operating status of the board to assist in maintenance, and
- Display I/O functions with individual LED indicators to indicate the status of each I/O point.

Vital iVPI printed circuit boards are also electrically keyed. All Vital input/output lines have built-in secondary transient protection to prevent disruption of service from external interference.

Table 3–1. Subrack Part Numbers

Description	Part Number
21-Slot 9U w/P2 Motherboard Main Module VSP slot 1–2, 12 VDC Pwr Isolation Unit, Supply 9–16 VDC, Expansion Interface, for Direct Wired I/O	31038-823-01
21-Slot 9U w/P2 Motherboard Main Module VSP slot 1–2, 12 VDC Pwr Isolation Unit, Supply 9–16 VDC, for Direct Wired I/O	31038-823-02
21-Slot 9U w/P2 Motherboard Expansion 1 Module BEX slot 1, 12 VDC Pwr Isolation Unit, Supply 9–16 VDC, Expansion Interface, for Direct Wired I/O	31038-823-03
21-Slot 9U w/P2 Motherboard Expansion 2 Module BEX slot 1, 12 VDC Pwr Isolation Unit, Supply 9–16 VDC, Expansion Interface, for Direct Wired I/O	31038-823-04
21-Slot 9U w/P2 Motherboard Expansion 3 Module BEX slot 1, 12 VDC Pwr Isolation Unit, Supply 9–16 VDC, Expansion Interface, for Direct Wired I/O	31038-823-05
21-Slot 9U w/Split 10/10 P2 Motherboards Main Modules VSPs slot 1–2, 2–12 VDC Pwr Isolation Units, Supply 9–16 VDC, for Direct Wired I/O	31038-833-01
4-Feet Ribbon Cable, 64-COND, Bus Expansion, BEX	38216-581-04

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 4 – VITAL SUBSYSTEM

4.1 GENERAL

This section describes the Vital Subsystem of the iVPI System.

4.2 INTRODUCTION

iVPI Systems are explicitly designed for operation in the extremely harsh environments seen in railroad and transit properties. The iVPI product line is designed, validated and verified for operation per the AREMA Communication and Signal Manual, Part 11.5.1 for Class C (Wayside Signal Enclosures) and Class D (Wayside Control Rooms) environments without the need for any special environmental conditioning. In practice, each iVPI System for Vital application is comprised of System boards and the appropriate quantity and type of input and output boards required for the particular location.

iVPI System boards for a typical North American Rail application are:

- Vital System Processor (VSP)

The iVPI Vital input and output boards are the following:

- Direct Input (DI)
- Single Break Output (SBO)
- Double Break Output (DBO)
- Lamp Driver Output (LDO)
- AC Output (ACO)

In addition to the system boards listed above, the Vital system may be configured with one or more optional VSP Interface boards to simplify the physical and electrical connections to the VSP board:

- VSP P2 System ID board
- VSP and BEX P1 Interface board
- VSP P3 Interface board

For typical Freight Rail, Commuter Rail, and Light Rail applications, the following iVPI system boards may also be used:

- Code Rate Generator (CRG)
- Genrakode Track Processor (GTP)

4.3 INDIVIDUAL VITAL BOARD DESCRIPTIONS

4.3.1 Vital System Processor (VSP)

The Vital System Processor (VSP) board is the Vital processing unit of the iVPI System. The VSP board can process thousands of Vital expressions, read up to 320 Vital inputs (20 DI boards), set up to 320 Vital outputs (40 Vital output boards, such as SBO, DBO, LDO, ACO), interface to up to 10 GTP boards (20 GENRAKODE III Track Circuits) and 3 CRG boards (8 coded outputs per board), process up to 332 Vital timers (32 of which are programmable without recompiling the application program), receive and transmit Vital network data, and receive and transmit non-vital controls and indications, all within iVPI's fixed Vital 1-second cycle time.

Through the use of VPI application tools, an engineer defines the logic, I/O functionalities, and communications to implement the interlocking control functions. Application software is compiled using the application tools and downloaded directly to the VSP via a USB type connection interface.

4.3.1.1 System Vital Communications

The VSP board includes an integrated two channel Ethernet network interface that supports the Vital Serial over Ethernet (VSOE) protocol for communicating Vital parameters to other iVPI Systems on a network. The Vital message is constructed using Vital techniques for the Vital parameter states and other Vital data in the message. To survive possible message corruption due to the harsh EMI environment VPI Systems operate within, each Vital message is transmitted two times during the cycle with the receiver requiring only one good reception for proper Vital decoding.

Using patented NISAL™ techniques, the Vital communication messages have Vital security to protect against an iVPI System receiving and decoding messages not intended for it (misrouted messages), or messages that may have been stuck in some communication system memory device and re-transmitted, or to reject messages that have been significantly delayed by the communication system and are too old to be processed vitally. These techniques permit iVPI to successfully utilize non-vital communication networks and equipment to transport Vital messages between iVPI Systems.

4.3.1.2 CBTC Vital Communications

The VSP board utilizes the integrated two channel Ethernet network interface for Vital communications to external zone controllers for a CBTC interface using the Digisafe protocol. This protocol allows the iVPI to communicate Vital parameters with zone controllers on the network. The Vital message is constructed using Vital techniques for the Vital parameter states and other Vital data in the message. For availability, the communications with the zone controller are configured in a redundant configuration with the two network interfaces interfacing to redundant units in the zone controller.

Using patented NISAL™ techniques and Numerical Assurance for Arithmetic, the Vital communication messages have Vital security to protect against an iVPI System receiving and decoding messages not intended for it (misrouted messages) or messages that may have been stuck in some communication system memory device and re-transmitted, or to reject messages that have been significantly delayed by the communication system and are too old to be processed vitally. These techniques permit iVPI to successfully utilize non-vital communication networks and equipment to transport Vital messages between iVPI and the zone controller.

4.3.1.3 Logic Processor

All Vital expressions are processed every cycle by the VSP board, and, as such, many inputs from multiple sources may change at the beginning of the cycle and all are processed during that cycle without lengthening the processing cycle. This is a very key performance feature of iVPI Systems that are deployed into large, complex interlocking plants that have a large number of simultaneous train movements. For Vital configuration control, the VSP board directly supports 16 inputs that can be used to set more than 62,000 unique combinations to vitally identify iVPI Site Identification and Revision version.

These inputs are vitally interlocked to the Application Software and to the Executive Software versions at a specific site. This feature fulfills, at the iVPI run-time system level, the requirements of the USDOT FRA Regulation on Configuration Management, which is defined in Regulation 49 CFR 236.18 for ensuring the correct software is installed at the intended version level at the intended site and is uniquely identifiable.

4.3.1.4 System Verification

The VSP board includes an integrated Vital Relay Driver function. This function vitally monitors the Vital outputs for permissive Vital output status verification every 50 ms to generate a dynamic output signal that controls power to the Vital outputs. iVPI checks the state of its Vital outputs using a continuous verification data stream on each Vital output during more than 95% of each 50 ms cycle. Using this method, the iVPI System can detect any Vital output failure and vitally remove its power via the VRD relay within a maximum of 140 ms (typically within 100 ms).

4.3.1.5 Vital Timing

The VSP board supports up to 32 field-settable software Vital application timers and up to 300 permanently programmed Vital application timers. The Vital time base is the Vital iVPI main cycle which is vitally accurate to ±0.002 seconds. This time base is verified by a NISAL™ process, forcing the VRD to drop if the time base ever goes out of tolerance.

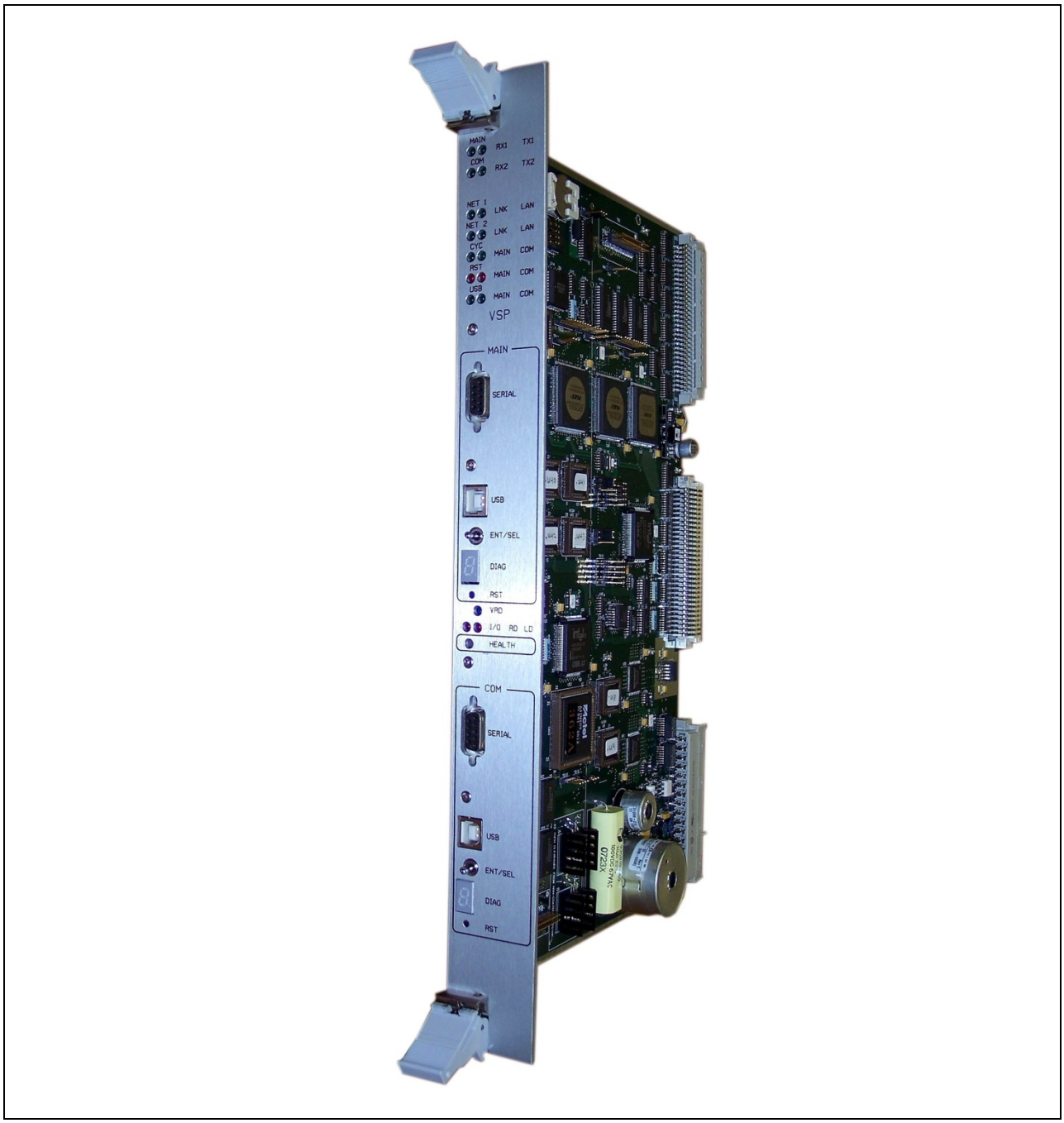

Figure 4–1. VSP Board

4.3.2 Genrakode Track Processor (GTP)

The Genrakode Track Processor (GTP) board is for Commuter, Freight, and LRT applications. It plugs into the iVPI Subrack in any slot other than slots 1 and 2, which are reserved for the VSP board. The GTP board is typically used for driving DC Coded Approach Track Circuits. Provided on the board front edge are connections for downloading the Genrakode programs as well as indicators for Codes In/Codes Out, and other maintenance indicators. The GTP communicates over the System Bus portion of the iVPI Motherboard to the VSP, passing Vital and non-vital codes to be transmitted and received.

Through the use of the iVPI and Genrakode application tools, an engineer defines the logic and I/O functionalities to implement the train detection function. Application software is compiled by the tools and downloaded directly to the GTP via a USB-type communication interface.

Figure 4–2. Genrakode Track Processor Board

4.3.3 Bus Expansion (BEX)

The BEX board is used to enable a single VSP board to control both Vital and non-vital boards in up to three iVPI expansion chassis. Each expansion chassis can contain up to 20 boards in addition to the BEX board. The BEX board resides in slot 1 of each iVPI expansion chassis in place of the VSP board.

Status LEDs on the front panel provide a visual indication of onboard and I/O bus activity as well as the presence of chassis power.

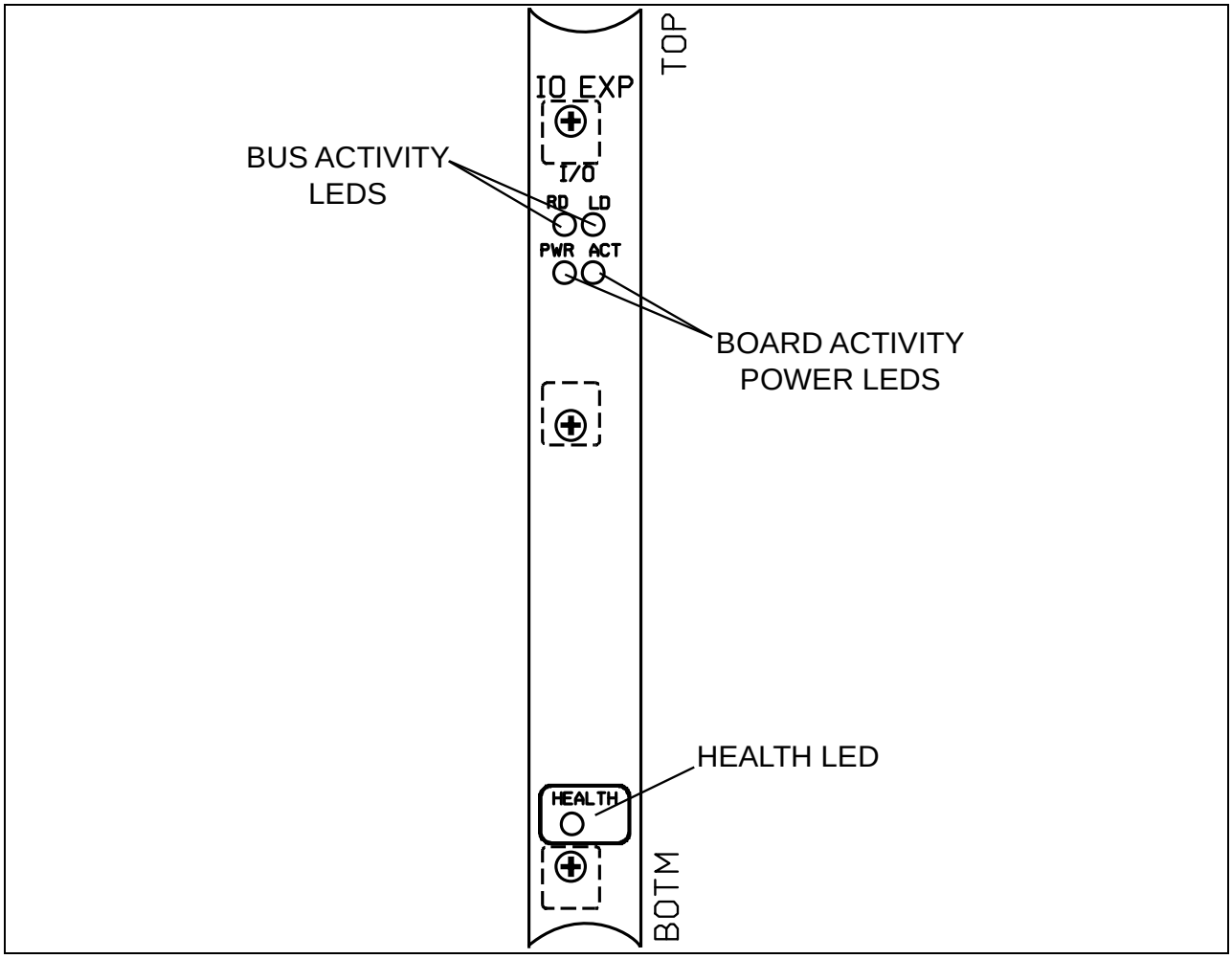

Figure 4–3. BEX Board LEDs

4.3.4 Direct Input

Direct Input (DI) boards are used to vitally input the status of devices such as switch machines, track circuits, line circuits, and a multitude of other Vital signal apparatus. The DI boards contain 16 isolated Vital inputs for DC input current sensing. Each input port has two connections to the field equipment (+IN and –IN), and two inputs may be connected in parallel with opposite polarity to form a bipolar input circuit. Each input circuit is vitally isolated from each other, from ground, and from power using techniques that meet or exceed AREMA isolation requirements (2000 Vrms). Using a unique Vital time interval sampling technique, Vital inputs are immune from false readings due to induced AC frequencies in the range of 25 to 360 Hz. Appropriate transient protection devices are included in the input circuit on the PC board.

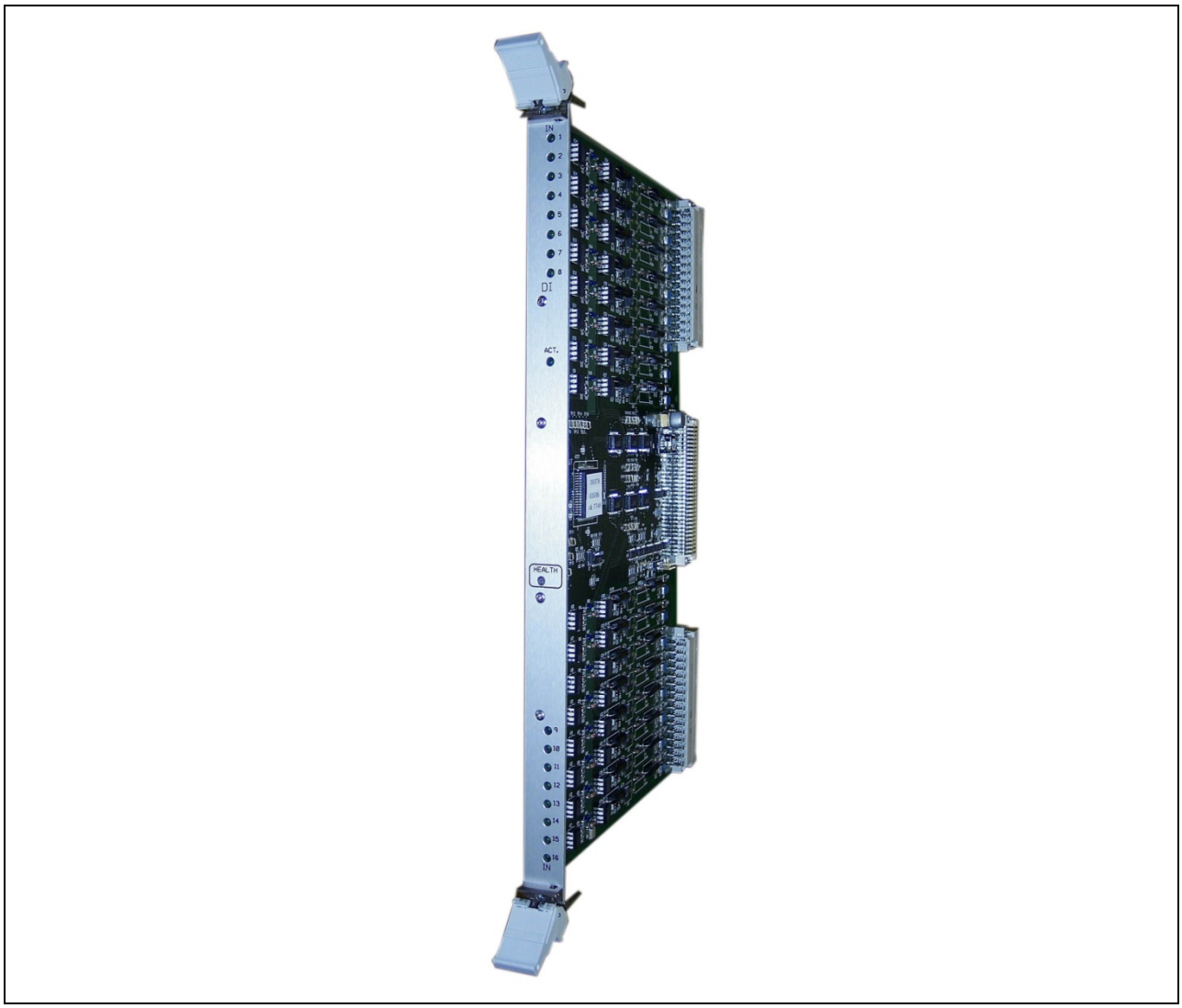

Figure 4–4. Direct Input Board

4.3.5 iVPI Vital Output Board Descriptions

These boards are used to control a wide variety of Vital devices such as switch machines, line circuits, signal lamps and a multitude of other Vital signal apparatus. Vital outputs are available in four distinct types: Single Break Outputs (SBO), Double Break Outputs (DBO), Lamp Drive Outputs (LDO), and AC Outputs (ACO).

These boards have 8 outputs divided into two groups of four. Outputs 1 through 4 are connected to one power supply input while outputs 5 through 8 are connected to a second power supply input.

In Vital applications, these power supply inputs are connected to a source that can be vitally turned off (usually a contact of the VRD relay or one of its repeaters).

4.3.5.1 Single Break Output

Single Break Output (SBO) boards contain eight vitally isolated outputs per board. Each output has one connection to field equipment (+OUT). The negative side of each group of four outputs is connected in common. This group reference is available at the board connector and each group of four outputs may be connected to a different reference. The output port on an SBO board is analogous to a relay circuit with a contact in the feed side of a circuit only. Supply voltage to the output board can be in the range of 9 to 30 VDC with loads up to 0.5 amps.

Appropriate points in the Vital output circuit have RF Bypass capacitors to ground to eliminate RF interference. Appropriate transient protection devices are also included in the output circuits on each PC board.

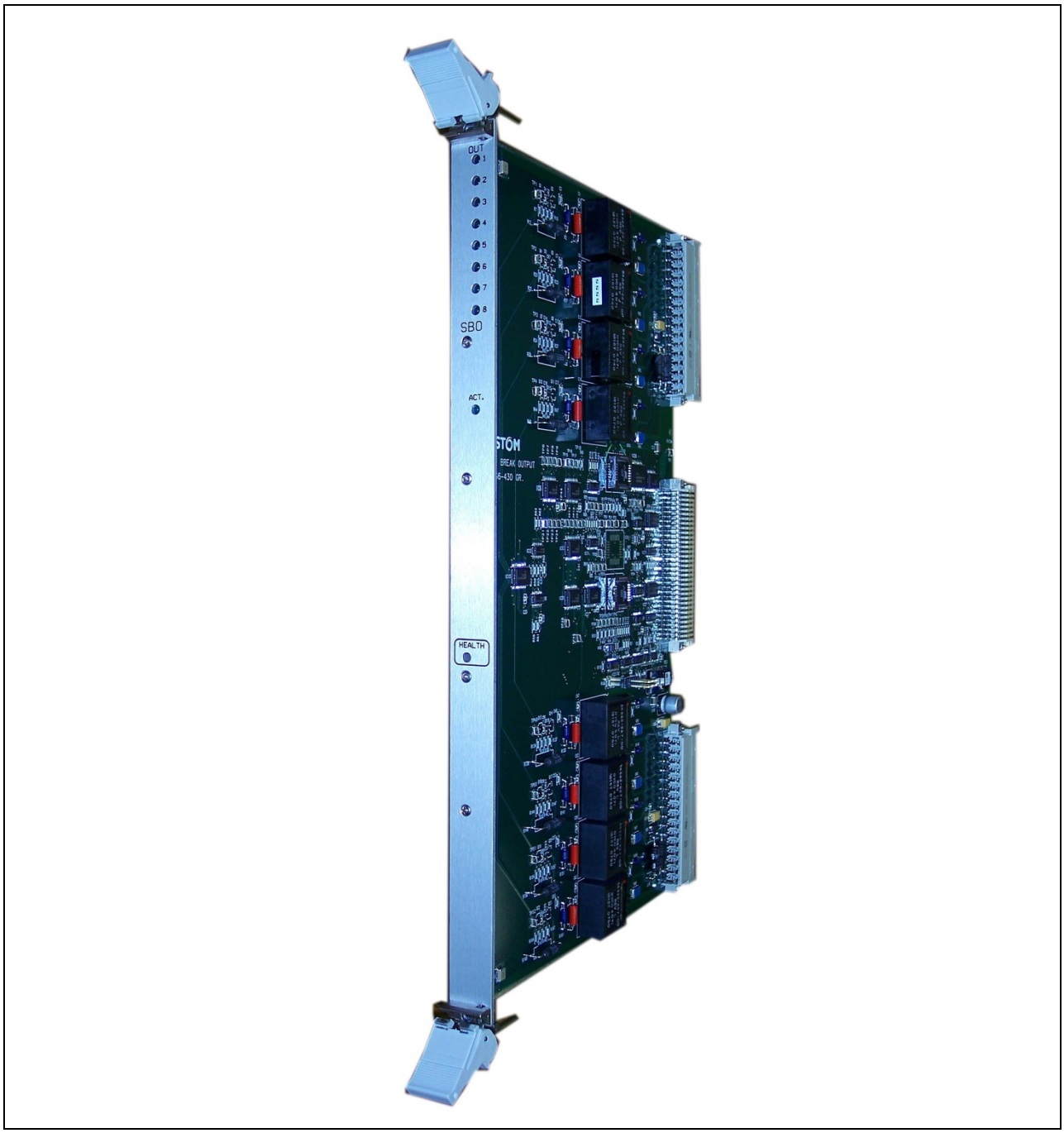

Figure 4–5. Single Break Output Board

4.3.5.2 Double Break Output

Double Break Output (DBO) boards contain eight vitally isolated outputs per board. Each output has two connections to field equipment (+OUT and –OUT) and two outputs may be connected with opposite polarity to form a Bipolar output circuit without requiring a separate external isolator interface for either the Double Break or the Bipolar mode of field connection. The output port on a DBO board is analogous to a relay circuit with contacts in both the feed and return sides of the circuit.

Each output circuit is vitally isolated from each other, from power and from ground. Supply voltage to the board can be in the range of 9 to 16 VDC with loads down to 250 ohms. Being a fully isolated double break output circuit arrangement, this output can tolerate a single point failure to ground or to power without any damage.

Appropriate points in the Vital output circuit have RF Bypass capacitors to ground to eliminate RF interference. Appropriate transient protection devices are also included in the output circuits on each PC board.

Figure 4–6. Double Break Output Board

4.3.5.3 Lamp Driver Output

Lamp Driver Output (LDO) boards contain eight Vital outputs per board that directly drive incandescent signal lamps or directly drive signal lamp LED assemblies. Each output has a Sourcing Drive (positive side switch) capable of providing a maximum output current of 3.3 amps per port. The supply voltage to the board can be adjusted externally to account for line losses to the bulb/LED signal assembly in order to get the desired voltage at the bulb/LED Signal Assembly (provided the 3.3 amps per port is not exceeded). Each port has over-current protection and over-current detection with an appropriate diagnostic.

The LDO board includes hot and cold filament check for incandescent bulbs and for approved LED Signal Assemblies as well as an adjustable low level current detection threshold range for LED signal assemblies. Each group of four output ports shares a common reference signal. The positive side of each output circuit is vitally isolated from each other, from power and as a group of four outputs from ground.

Appropriate points in the Vital output circuit have RF Bypass capacitors to ground to eliminate RF interference. Appropriate transient protection devices are included in the output circuits on each PC board.

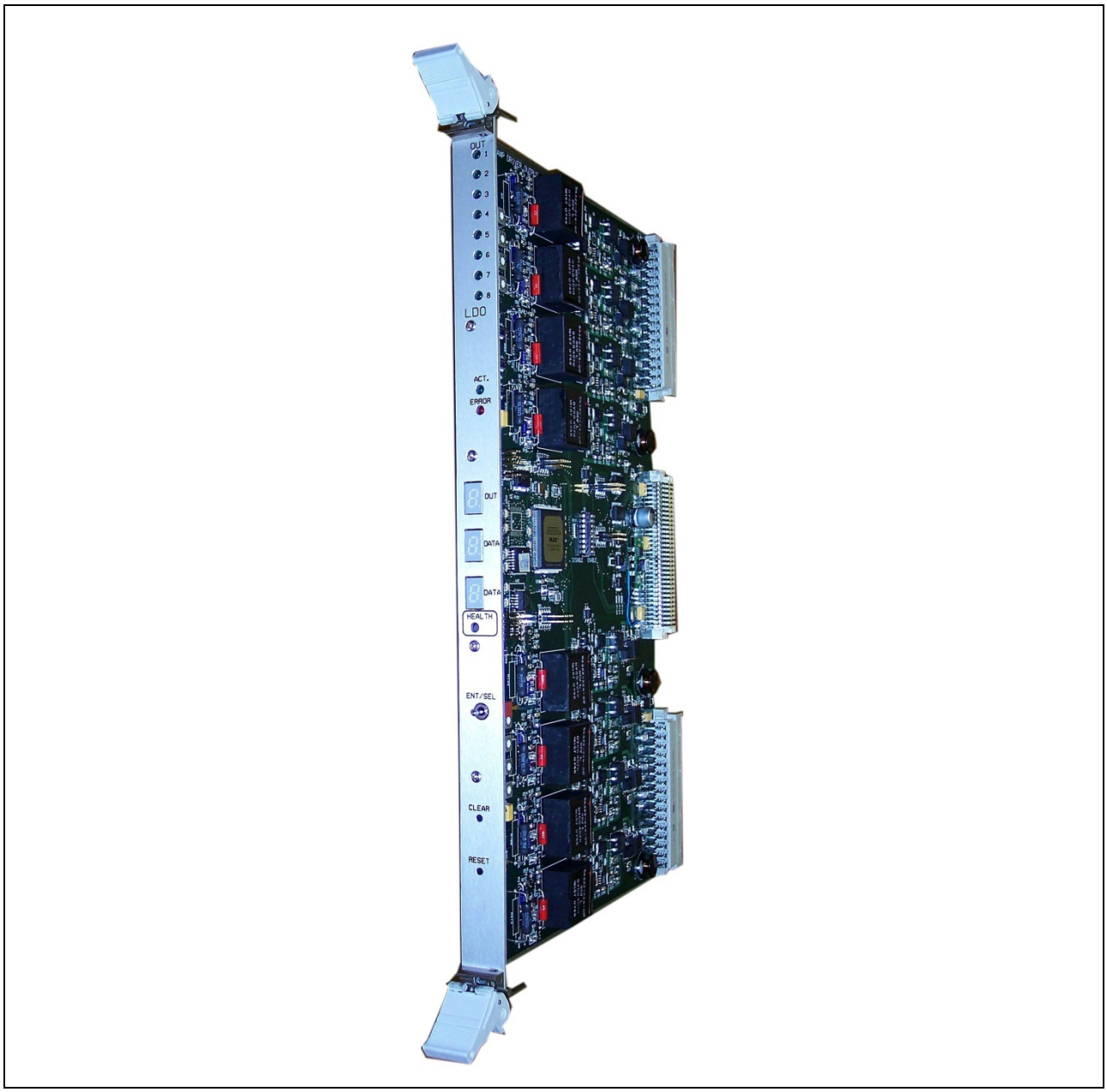

Figure 4–7. Lamp Driver Output Board

4.3.5.4 AC Output

The Vital AC Output (ACO) Boards are used for lighting signal lamps or for operating other AC loads. The 31166-431-01 ACO board is capable of driving loads up to 0.8 amps and includes a high current output threshold. The 31166-431-02 ACO board is capable of driving loads up to 0.5 amps and includes a low output current threshold.

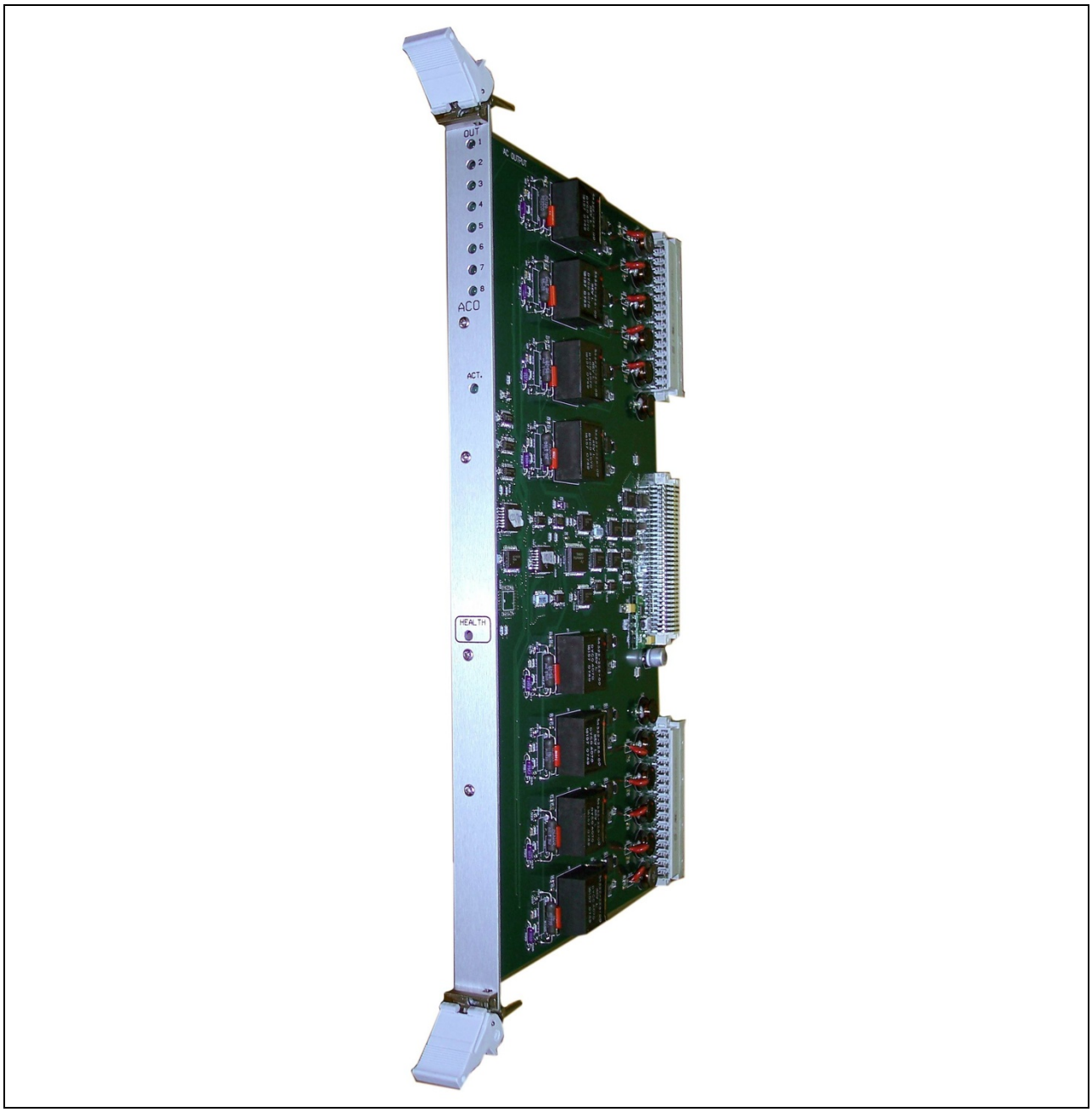

Figure 4–8. AC Output Board

4.3.5.5 Code Rate Generator

The Code Rate Generator (CRG) board contains eight vitally isolated outputs per board. The CRG board has its own Vital processor engine for generating and proving the pulsed outputs typically used to generate cab signal outputs. Each output has two connections to field equipment (+OUT and –OUT). The output port on a CRG board is analogous to a relay circuit with contacts in both the feed and return sides of the circuit.

The CRG communicates over the system Bus portion of the iVPI Motherboard to the VSP passing Vital code to be transmitted.

Each output circuit is vitally isolated from each other, from power and from ground. Appropriate points in the Vital output circuit have RF Bypass capacitors to ground to eliminate RF interference.

Figure 4–9. Code Rate Generator Board

4.3.6 System ID Board And Vital Interface Boards

An iVPI may be configured to use various types of optional Interface boards to provide additional connectivity to the VSP board:

- VSP System ID Board
- VSP/BEX Interface Board
- VSP P3 Interface Board

4.3.6.1 VSP System ID Board Operation

The VSP System ID board (P/N 31166-472-01) is located at P2 on the VSP board.

This board assembly provides a means to set the System ID (revision and site ID) for the VSP board assembly in an iVPI subrack. Four thumbwheel switches are rotated into position to match the revision and site ID produced by the application tool, CAAPE, when the application is compiled. Each thumbwheel switch has 16 positions that are marked 0–9 and A–F. The iVPI Main Subrack System ID Configuration Procedure located in Section 2 of Alstom publication P2521B, Volume 1, describes how to configure the System ID Interface board.

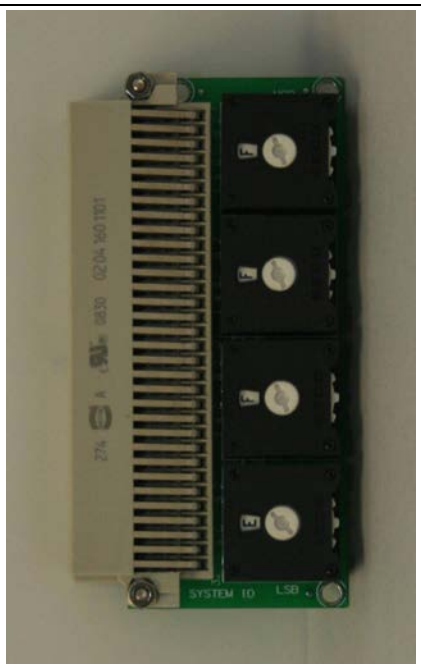

Figure 4–10. VSP P2 System ID Interface Board

4.3.6.2 VSP/BEX Interface Board

The VSP/BEX Interface Board (P/N 31166-485-01) is located at P1 on the VSP board or P3 on the BEX board. This along with Bus Expansion Cable (P/N 38216-581-04) provides a method to connect up to three expansion modules to the main module.

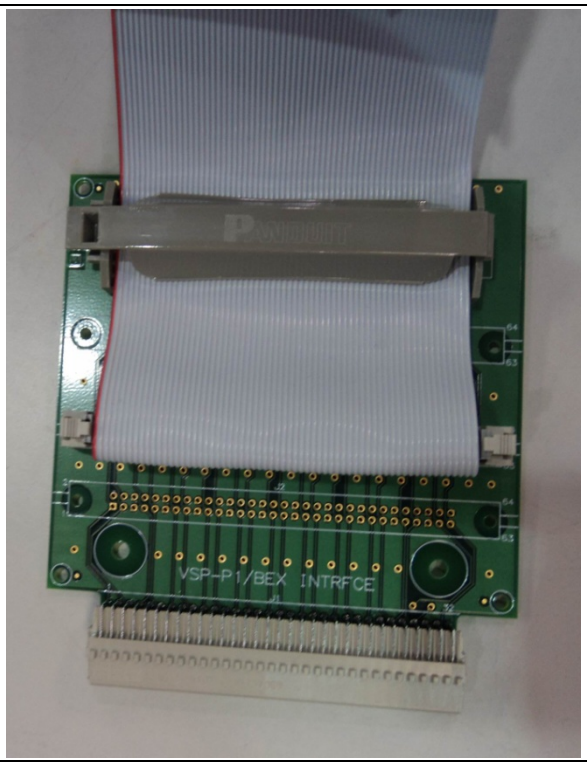

Figure 4–11. VSP/BEX Interface Board

4.3.6.3 VSP P3 Interface Board

The VSP P3 Interface board (P/N 31166-473-01) is located at P3 on the VSP board to provide additional connectivity to the VSP board:

- Two RJ45 modular jacks connect to the VSP board's Ethernet Ports
- One RJ45 modular jack connects to the VSP board's MAC Port
- One RJ12 modular jack connects to the VSP board's Health Monitor Interface
- Four cage clamp type terminals (that accept wire sizes from #14 AWG to #20 AWG) to support loose wire connections for the VSP board's VRD relay interface:
  - Two terminals are used for battery power ("B12" and "N12")
  - Two terminals are used for VRD coil connections ("COIL+" and "COIL–")

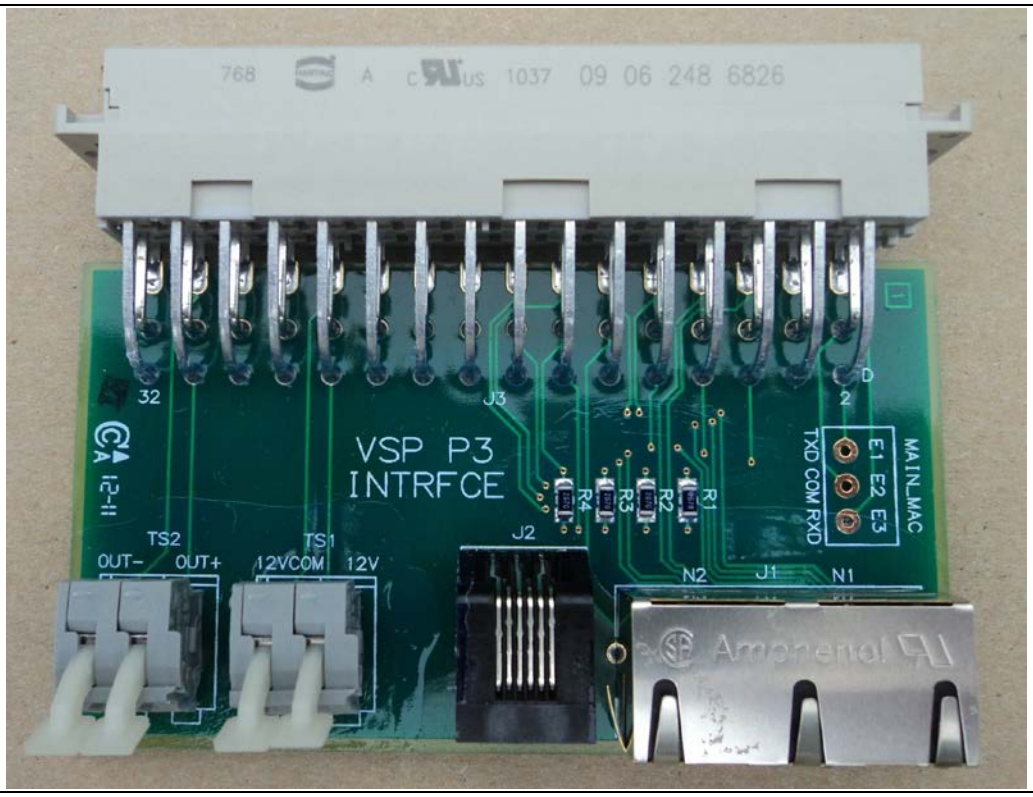

Figure 4–12. VSP P3 Interface Board

4.4 APPLICATION ASSUMPTIONS AND CONSTRAINTS

Several assumptions have been defined to be used in the application of the generic product and are included here along with any associated product constraints.

4.4.1 Application Assumption/Requirements

4.4.1.1 System Cycle

iVPI is based on a defined and vitally verified one-second cycle where all inputs, evaluations, and outputs are provided.

4.4.1.2 Vital Timing

Application timing is provided based on increments of the vitally ensured iVPI one-second system cycle.

4.4.1.3 System Grounding

iVPI's internal logic power supply is internally connected to a ground plane, subsequently to the electronics chassis, and, finally, through an external connection to "earth" through proper RFI friendly cables. Typically this is performed by connecting a shielded cable from the equipment rack in which iVPI is mounted to the earth common reference in the equipment room. This grounding is maintained to "shunt" induced RFI away from critical I/O circuits and prevent disruption to system processing. This "earth ground" must be considered when providing connections between iVPI I/O and field devices in order to insure that the earth ground remains isolated from the signaling battery.

4.4.1.4 Vital Inputs

Inputs that are considered Vital are expected to be provided by a Vital source such that:

- permissive inputs (ON) will be presented as DC signals at the level of the Vital signaling battery (with some tolerance), or
- restrictive inputs (OFF) will be presented as no voltage (0 volts)
- there is no defined threshold for OFF beyond the assumption that no energy is applied (0 VDC, no connection) or there is no presence of voltage signifying ON at signal battery + voltage level
- while iVPI performs input scanning with detection of induced AC (25–250 Hz), proper care must be taken in the installation layout of wiring so that no differentially induced AC signal can be presented to a Vital input where the level of this input could be inappropriately sensed as a permissive state (>3 VDC)

4.4.1.5 Response Time to a Safety Critical Failure

iVPI has been designed to remove output energy when a failure is detected prior to the period required to have a switch (point) machine begin to move from its intended position (normal or reverse) or to energize a traditional B-Relay (<200 ms). This is considered the worst case safety failure. iVPI's design maintains a failure detection to energy removal period of 140 ms.

Switch machines or other signaling devices that complete state change in less than 200 ms, such as air operated switch machines, must not be directly interfaced to an iVPI system without a Vital relay between the iVPI and the machine to introduce a sufficiently delayed response.

4.4.1.6 Signaling Logic Ordering

iVPI evaluates logic in a sequential manner from first expression to last each system cycle. When implementing signaling rules, this fact must be considered to insure proper order of output states and proper sequences of rules implementation.

4.4.1.7 Vital Output Verification

iVPI's detection of failures on outputs is accomplished through the detection of current flow in an output that has been otherwise directed to be in the OFF state. Absence of current in an OFF output is positive proof that no failure has occurred to falsely drive that output. The detection threshold on the absence of current detector is any current over 3 ma for DC non-signal output types and 100 ma for signal lamp drivers. Therefore, when designing an interlocking application, it must be guaranteed that iVPI output loads will draw more than 5 ma (150 ma) of current during normal operation when the output is turned ON to provide safe operating margin.

4.4.1.8 Preventing Potential Output Circuit Run-Around Paths (Vital Outputs)

iVPI outputs have been designed for single break (SBO, ACO, LDO) and double break (DBO) application. When designing equipment room and field wiring, care must be taken when using single break outputs so that external failures such as shorted wires cannot introduce a run-around path for output current that could energize an output that should be in the OFF state.

4.4.1.9 Safety Checks Outputs

In order to achieve required response time, physical output states (for OFF outputs) and Logic expression results (for ON outputs) are verified every 50 ms.

4.4.1.10 Safety Checks System Processing

Verification of system processing checks such as memory integrity, Vital timing, etc., is accomplished once each system's one-second cycle.

4.4.1.11 Application Verification

The basis of the application of iVPI is to use a tool to configure the system hardware and software as well as create the signaling logic for the Vital application. The independent Application Data Verifier Tool, as well as associated procedures, must be run and performed prior to any iVPI application program being tested in field commissioning tests.

4.4.1.12 Output Current Check for Output Ports

iVPI has the ability to vitally determine current flow in an output port. This parameter can be used as an internal parameter in the building of the signaling logic rules. This feature is only available for DC-based outputs. AC outputs that are turned ON cannot take advantage of the Vital current check feature, as the check mechanism cannot produce an expected result due to the unsynchronized nature of the output check and the positive voltage peak of the AC cycle. A non-vital current check feature is available for ACO output ports to determine if the port is conducting current or not.

4.4.1.13 Cycles of Forgiveness

Vital inputs, because they are not synchronized to the system cycle, can be sensed to be in an unknown state during transition from ON to OFF, or due to spurious interference to an ON input. This is not a safety-critical issue. A feature termed "cycle of forgiveness" (COF) can be applied to inputs to prevent either of the two input sensing situations from having an undesirable ripple effect on signaling logic. The COF can be used to delay response to a transitional input for a given system cycle. Care must be taken to analyze the overall system response time when COF are assigned to inputs.

4.4.1.14 Proof of Logic (Primordial Logic Review)

The application of iVPI depends on application engineers defining configurations and logic to be implemented for the interlocking application. While iVPI guarantees that logic and outputs, etc., are managed vitally, there is no intrinsic check on the correctness or completeness of the signaling logic as it is intended to meet the requirements of the railroad application. It is a primary safety requirement that the logic produced for iVPI execution be independently verified as correct and complete through a "circuit check" type process. The check process must be performed by engineers knowledgeable in the requirements of the signaling rules that govern railroad operation and independent from the engineering staff that produced the logic.

4.4.1.15 Short Cycle Timer Protection

All iVPI timer equations should include a Vital input energized from a front contact of the VRD relay, such as a VRDFRNT-DI parameter to ensure that the timing cannot be "short-timed." Protection of system timing is provided by check results each one-second timing cycle. Failure of a timer, runs short, would be detected and drop the VRD. However, timing equations continue to evaluate, and therefore a timer equation could prematurely complete. By inserting the VRDFRNT-DI input into a timer equation this situation can be prevented.

4.4.1.16 VRD Relay and VRD Repeaters

WARNING

iVPI contains special safety circuit components which must only be replaced by components specified by the Alstom part number.

These original-design replacement parts are manufactured to the same standards as the original parts; their performance being verified. The use of replacement parts that are not of the same Alstom part number could potentially impair the safe performance of the system.

The railroad or transit system authority and the manufacturer of an aftermarket (i.e., non-Alstom designated) part assume the responsibility that the part will not adversely affect the safe performance of the system. The authority and the manufacturer of the aftermarket part must analyze and certify in writing that use of the part will not result in a failure of the system to comply with safety regulations and safety performance. Completion of such an analysis and certification is considered due diligence and standard practice, will not be reviewed or approved by Alstom, and neither absolves the authority and aftermarket part manufacturer of responsibility nor implies approval by Alstom to use such an aftermarket part. The responsibility of any consequences resulting from using such a part remains with the authority and part manufacturer.

WARNING

Only Alstom VRD relay (P/N 56001-787-05) is to be used with the Alstom iVPI system. Alstom products are designed to function within all-Alstom systems. The introduction of non-Alstom products into an Alstom iVPI system could have unintended and unforeseeable safety consequences

The iVPI VRD relay is a specific type as it forms the final stage of the Vital circuit residing on the iVPI VSP circuit board. Its pick time and pick-up and drop-away currents are critical parameters in guaranteeing a quick response to a detected failure.

The VRD relay is used to disconnect output energy should iVPI encounter a failure in a Vital process, result, or output state. Back contacts of the VRD relay are typically used to drive the Red Aspect of signals to show a positive Stop aspect rather than a dark signal. In large locations, it may be necessary to use a repeater in order to take advantage of the additional contacts for signal lighting.

VRD repeaters may also be used to distinguish between feeding output groups from different signaling supply sources.

Where either of these situations requiring repeater relays is considered, a response time review should be performed to insure that the added drop times of the repeater relays do not delay the response to a failure detected by iVPI. Depending on repeaters used and arrangement, response time greater than 140 ms will likely be observed.

4.4.1.17 Simultaneous Failures

Two or more independent self-revealing component failures will not occur simultaneously. This assumption has been traditionally accepted in the train signaling industry. There are three aspects of the assumption, however, which should be emphasized.

- The first is the aspect of “independent failures.” Failure modes of individual components may be interrelated in such a way that one failure may precipitate others. These interrelated failures would then constitute one “independent” failure.
- The second aspect is that of simultaneity. “Simultaneously” in this context means “during the period bounded by the occurrence of the first independent self-revealing failure and the occurrence of the event which reveals that failure.”
- The third aspect is that the maximum component failure rate should be low enough to preclude “simultaneous” failures.

4.4.1.18 FMEA Provides Adequate Failure Coverage

The Failure Modes and Effects Criticality Analysis technique, correctly and comprehensively applied, is adequate to reveal all potential unsafe effects of component failure. Justification of this assumption is again based on accepted industry practice (i.e., AREMA).

4.4.1.19 Security of Installation

In order to maintain security from physical tampering, iVPI is required to be installed within either an enclosed case (under lock and key) or a locked equipment house where only those trained in the line maintenance or designated members of the rail authority have necessary means of access.

4.4.1.20 FSSVT Operations

WARNING

All FSSVT modifications are safety-critical and must be verified, using the AlsDload program or the Application Data Verifier program within CAAPE, to determine whether the application PROM code data has been encoded as specified by the AlsDload FSSVT compiler. Refer to Section 4.4.1.11 Application Verification and 4.4.1.14 Proof of Logic (Primordial Logic Review) for additional information.

WARNING

All changes made to the FSSVT must be field tested to validate the intended timer values of any modified timers are observed to be correct in actual operation prior to the return of revenue service.

WARNING

FSSVT passwords shall be provided only to responsible personnel that have been properly trained in the FSSVT modification, verification, and validation process.

WARNING

Verify through Vital signatures that FSSVT values that were not intentionally changed retain their original signature values.

4.4.2 Maintenance Assumption

4.4.2.1 External Input/Output Integrity

iVPI vitally insures that any safety critical failure that occurs internal to the system (inboard side of the electrical boundaries of its input and output circuit boards) is detected with the system attaining a more restrictive state should a failure occur. iVPI does not have the capability to determine if an erroneously applied energy (positive Vital signal battery voltage) has been applied to its input. In a similar manner, iVPI cannot detect if energy has been erroneously applied to an output drive circuit external to the system thereby supplying a potentially more permissive output state than iVPI has calculated. It is assumed that proper maintenance is being provided by the rail authority to prevent instances of signal circuit shorts which could produce such an occurrence.

4.4.2.2 Site Version/Revision Configuration Control

One hazard condition that needs to be considered with regard to software-based interlocking control is the potential of installing an old and incorrect release or that of a similar application program other than the one required. This could occur through improper maintenance activities following system failure. One of the mitigations of this class of failure has been to institute location (site) and revision control features into iVPI. The site and revision ID must be uniquely assigned by the Application Engineer with each interlocking program change that will be installed in a field location.

4.4.3 Production Assumptions

4.4.3.1 System Manufacturing

iVPI has been designed with the latest state of the art surface mount components and has been fully qualified to international rail industry standards as well as quality standards for complete system component manufacture. It is assumed that the manufacturer of printed circuit boards continues to follow recommended production standards for printed circuit boards and that it is periodically verified though quality inspection that proper production and handling best practices have been performed.

It is further assumed that Alstom will be made aware of any change to components, or manufacturing processes of Vital printed circuit boards prior to authorization being given to proceed with the changes. This includes first run production as well as printed circuit boards being cycled through a repair cycle.

4.4.4 External Interface Assumptions

4.4.4.1 I/O Interface

It needs to be considered that iVPI inputs must not be connected to any external device that can act to rectify an induced AC signal. Inputs that are not static in nature (i.e., ON/OFF), such as dynamic signals, must be reviewed for Vital application.

4.4.4.2 Vital Serial Links

iVPI provides a network-based interface capability called Vital Serial Over Ethernet (VSOE2). It must be understood that the Vital protocol established has taken into account all known hazards associated with the medium of communications, as well as the interconnection of various adjacent iVPI systems that reside on the network. The protocol requires that the receiving system must perform the final verification of the message Vital integrity. Connection to other than iVPI systems requires a thorough review of safety methods used on both sides of the interface to insure that all protections provided for in the VSOE2 protocol are maintained.

4.4.4.2.1 Vital Serial Link Message Identification

The VSOE2 messages defined for the network must be unique in order to assure safe communications; supported by the assignment of link and block/sub-block numbers. The message link and block/sub-block values must be assigned such that the combination of these values is unique throughout the network.

The VSOE2 protocol does not protect against spoofing and the user must either maintain a private communications network or implement a lower-layer (relative to OSI model) network encryption.

4.4.4.3 Digisafe® (Siemens) Protocol for CBTC Interface Assumption

Table 4–1. Digisafe (Siemens) Protocol for CBTC Interface Assumption

iVPI Product: Digisafe Safety Assumptions	**System Integration/Application Project Acknowledgment**
The following is a summary of the general safety requirements for Vital data of Siemens Digisafe protocols and safety-related functional and operational requirements for the Digisafe protocol implemented for the iVPI product that need to be reviewed and endorsed by System Integrator/Application Project: 1. A message shall not be valid beyond a pre-defined data freshness threshold (defined in time between current receiver time and the Time Stamp Destination value in the received message – currently fixed at 5 seconds). 2. Message indications (parameters) at a destination shall maintain a permissive state for no more than a pre-defined data freshness threshold before they must revert to their most restrictive states or be refreshed by a subsequent message. 3. Messages that originate from an unexpected node shall not yield permissive values. 4. Message errors introduced during transmission/reception shall not yield falsely permissive values when message is decoded. 5. Calculation errors that corrupt message contents shall not yield falsely permissive values when message is decoded. 6. Vital parameter values for permissive states must be calculated from current, valid received Digisafe messages and not stored in fixed data structures (ROM). When Vital parameter values are calculated, they will be used only in the current cycle then vitally cleared. 7. Any execution failure of required steps of the message encoding and/or decoding algorithm shall not yield permissive values on the receiving end.	

Table 4–1. Digisafe (Siemens) Protocol for CBTC Interface Assumption (Cont.)

iVPI Product: Digisafe Safety Assumptions	**System Integration/Application Project Acknowledgment**
The following is a summary of the specific assumptions from safety Hazard Analysis due to safety critical design details on the Siemens Digisafe protocol implementation in iVPI that need to be reviewed and endorsed by System Integrator/Application Project: 1. The timestamp enforcement method is accepted as sufficient to mitigate hazards due to message loss (Deletion) or out-of-order messages (Resequence). It is assumed, for a zone controller cycle time less than that for iVPI, that every two or three consecutive zone controller – iVPI messages will have the identical Time Stamp Destination value due to the ratio between system cycle rates, and iVPI will process the most recently received zone controller message during each iVPI system cycle. 2. The achievable MTTHE performance with 48-bit SDC protection will be sufficient to meet project requirements. 3. No additional hazards are created by the difference between iVPI (1 s) and zone controller (sub-1-second) cycle periods. 4. Sufficient communications network bandwidth will be provided for all iVPI – zone controller links to prevent Digisafe message dropouts under normal operating conditions (worst case network configuration with all nodes operational and communicating at nominal rates) to a high reliability (for example, 99.999% or one message lost every approximately 28 hours at iVPI cycle rate). 5. Processing re-sequenced messages from a zone controller that are still valid in time (relative to the message freshness threshold) cannot result in a hazardous condition.	

The following hazard table identifies risks that are mitigated by proper application configuration, analysis, and test.

Table 4–2. iVPI Product: Digisafe Transferred Hazards

Description of Hazard	Cause of Hazard	Mitigating Action	System Integration/ Application Project Acknowledgment
Possible collision or derailment due to incorrect user configuration of Digisafe message interface causing unsafe operation.	User application error in assignment of node IDs and/or message bits for Digisafe messages results in falsely permissive parameters at receiver.	1. Circuit check function to provide independent safety check at Application. 2. Project to include assignments of unique IDs to each Digisafe node. 3. Pre-cutover testing of all Digisafe links prior to revenue service to validate all links and message bit assignment.	

Table 4–2. iVPI Product: Digisafe Transferred Hazards (Cont.)

Description of Hazard	Cause of Hazard	Mitigating Action	System Integration/ Application Project Acknowledgment
Possible collision or derailment due to falsely permissive Digisafe message from malicious action.	Undetectable falsely permissive messages intentionally injected into network (spoofing) accepted by receiver. Note: This hazard addresses the EN 50159 “Masquerading” threat.	The Digisafe protocol does not explicitly mitigate this hazard, although the safety coding (SDC) incorporating moving timestamps provides inherent protection. This represents an exported constraint to inform user that the Digisafe protocol does not protect against spoofing and the user must: 1. Maintain a private communications network to mitigate this hazard, 2. Implement lower-layer (relative to OSI model) network encryption to mitigate this hazard, or 3. Accept this hazard or other mitigation.	

4.4.5 Miscellaneous Assumptions

4.4.5.1 O&SHA

O&SHA. This is a project-specific task that is outside the scope of the product, however the Documentation and Operating Manuals and Procedures that are developed for the product provide direct input to the project-level O&SHA development.

4.4.5.2 EMC-EMI

The nature of the modifications for iVPI in comparison to VPI, are not subject to downgrade original EMC / EMI characteristics. iVPI rack as an incremental evolution of the mature VPI has been tested and qualified to AREMA 11.5.1 Class C Standard. However, this document refers to the executed test on the generic VPI-VPI2-iVPI Products, i.e., VPI-VPI2-iVPI rack, EMC-EMI shall be verified in the frame of each Application Project with:

- specific control room power supply characteristics, protection and filter where the VPI-VPI2-iVPI rack in installed
- specific cubicle project configuration
- specific cubicle wiring
- specific cubicle and grounding
- etc.

SECTION 5 – NON-VITAL SUBSYSTEM

5.1 GENERAL

This section describes the non-vital subsystem of the iVPI system.

5.2 INTRODUCTION

For non-vital applications, the iVPI system consists of one or more Non-Vital System Processor (NVSP) board(s), and the quantity of Non-Vital Input (NVI) and Non-Vital Output (NVO) boards required for a particular application. The non-vital iVPI system is contained either in a subrack identical to the iVPI Vital system or within a section of a Vital iVPI subrack. Communications between the non-vital system and the Vital system is via the motherboard (within the system when non-vital and Vital subsystems share the same system or an expansion cable when the two subsystems are in different subracks).

An iVPI system can include up to four NVSP boards on the system bus, thus allowing many arrangements for load sharing, if required. The NVSP board can also operate in a completely standalone mode independent of being connected via the system bus to a Vital processor. In either the standalone or in the connected arrangement, a NVSP board can interface with up to 20 non-vital I/O boards (housed in the same subrack as the NVSP) of 32 I/O points each for a total of 640 non-vital I/O points per NVSP board.

The iVPI non-vital system board and the non-vital input/output boards are:

- NVSP – Non-Vital System Processor
- NVI – Non-Vital Input

  Note: Non-vital input boards must be grouped together and not interleaved with non-vital output boards.

- NVO – Non-Vital Output

  Note: Non-vital output boards must be grouped together and not interleaved with non-vital input boards.

In addition to the system boards listed above, the non-vital system may be configured with one or more optional NVSP Interface boards to simplify the physical and electrical connections to the NVSP board:

- NVSP P1 Interface board
- NVSP P3 Interface board

  Note: An NVSP board with a P3 Interface (P/N 31166-475-01) requires two slots.

Through the use of the VPI application tools, an engineer defines the logic, I/O functionalities, and communications to implement interlocking non-vital control functions. Application software is compiled by the tools and downloaded directly to the NVSP via a use type communication interface.

5.3 INDIVIDUAL NON-VITAL BOARD DESCRIPTIONS

5.3.1 Non-Vital System Processor

The Non-Vital System Processor (NVSP) board has two Ethernet communication channels and four serial ports (three ports which are programmable, one port is always the MAC – Maintenance ACcess) available with each serial port being capable of operating up to 57.6 KBPS. The NVSP board can be interfaced directly to standard communication equipment such as Fiber Optic Modems, Multiplexers, and Network Adapters.

The NVSP board can be application programmed with non-vital logic to perform Human Machine Interfaces (HMI), entrance-exit logic, and a multitude of other non-vital functions. The NVSP board can be used to interface with communications based Local Control Panel and/or HMI computers; or by using the NVI and NVO boards it can directly interface to discrete wired Local Control Panels and non-vital support functions.

The NVSP board also contains a battery backed-up memory section and clock/calendar to support the onboard DATALOGGER™ software used for logging both Vital and non-vital variables. Three of the communication ports in addition to the two Ethernet ports can be utilized for external non-vital communications. Each port may be configured with the same or with a different communication protocol. The choice of protocols is assigned and configured in the Computer Aided Application tools by the signal engineer.

A library of communication protocols common to the railroad and transit industry is included in the Computer Aided Application package. See Section 4 of Alstom publication P2521B, Volume 1, for Alstom’s library of communications protocols.

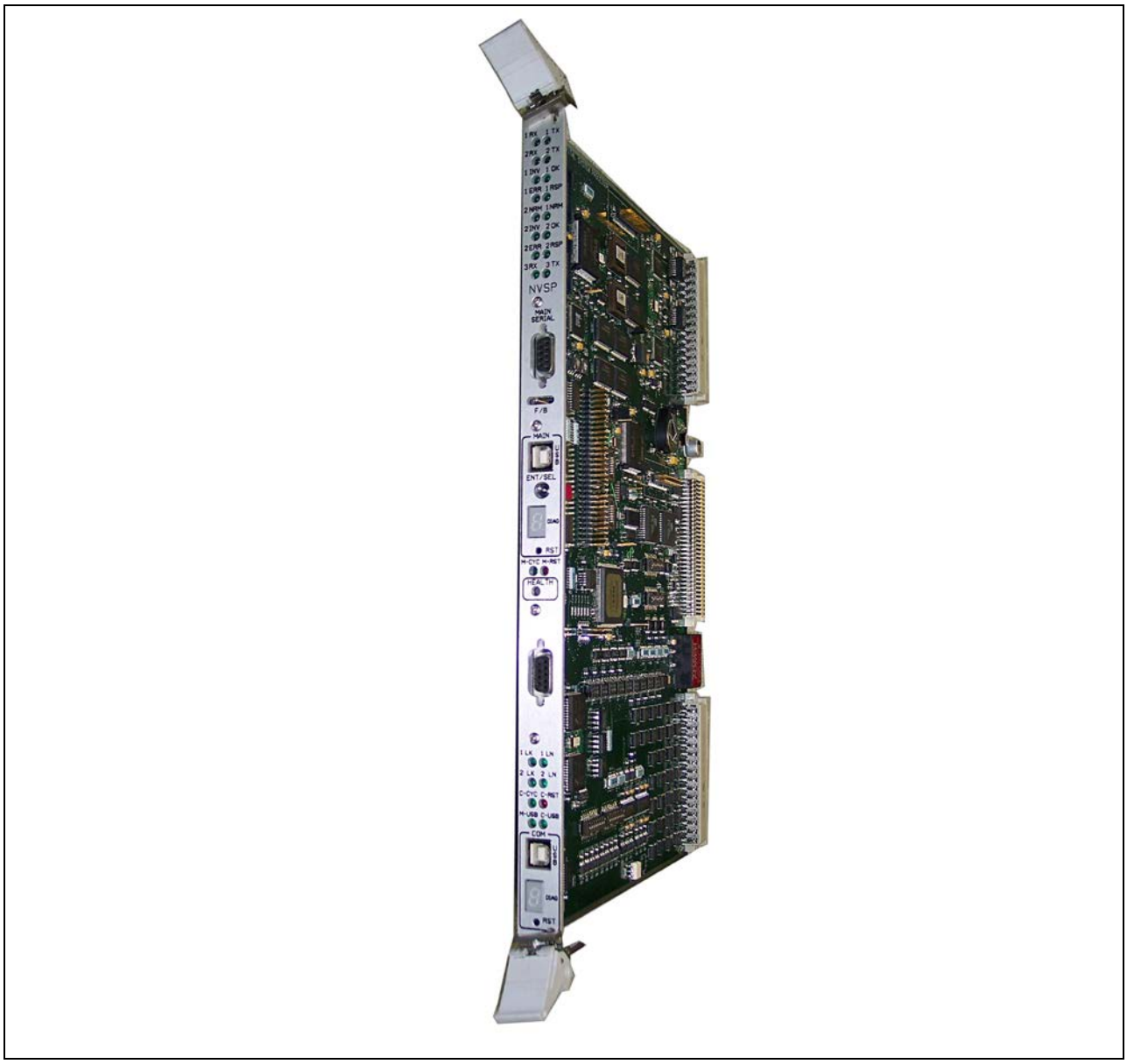

Figure 5–1. NVSP Board

5.3.2 Non-Vital Input

Non-Vital Input (NVI) boards provide 32 optical isolated inputs, which are read every 25 ms by the NVSP board. Each of four groups of eight inputs shares a common signal return.

Transient protection devices are included in the input circuits.

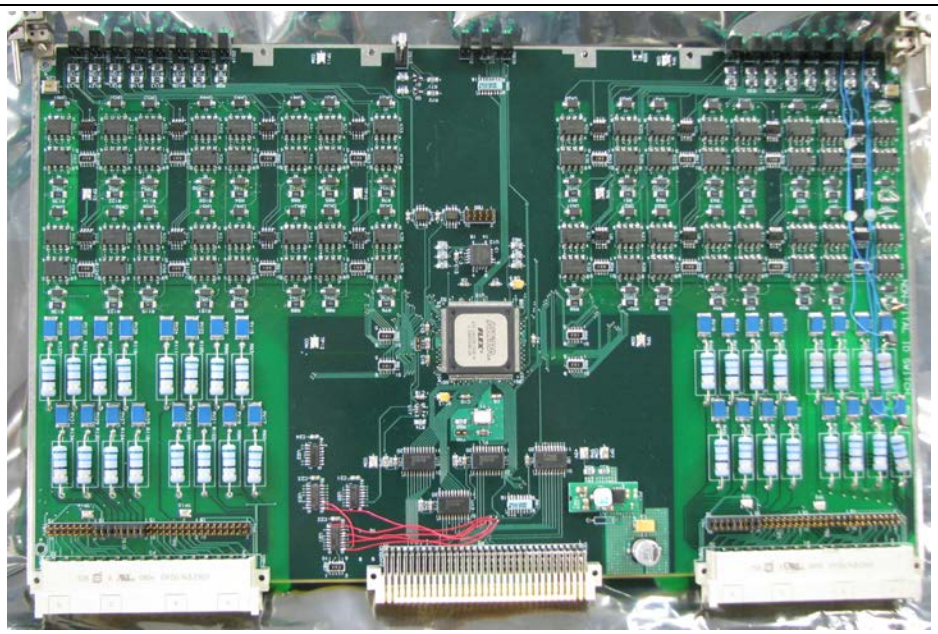

Figure 5–2. NVI Board

5.3.3 Non-Vital Output

Non-Vital Output (NVO) boards provide 32 optical isolated outputs, which are controlled by the NVSP board.

Transient protection devices are included in the output circuits.

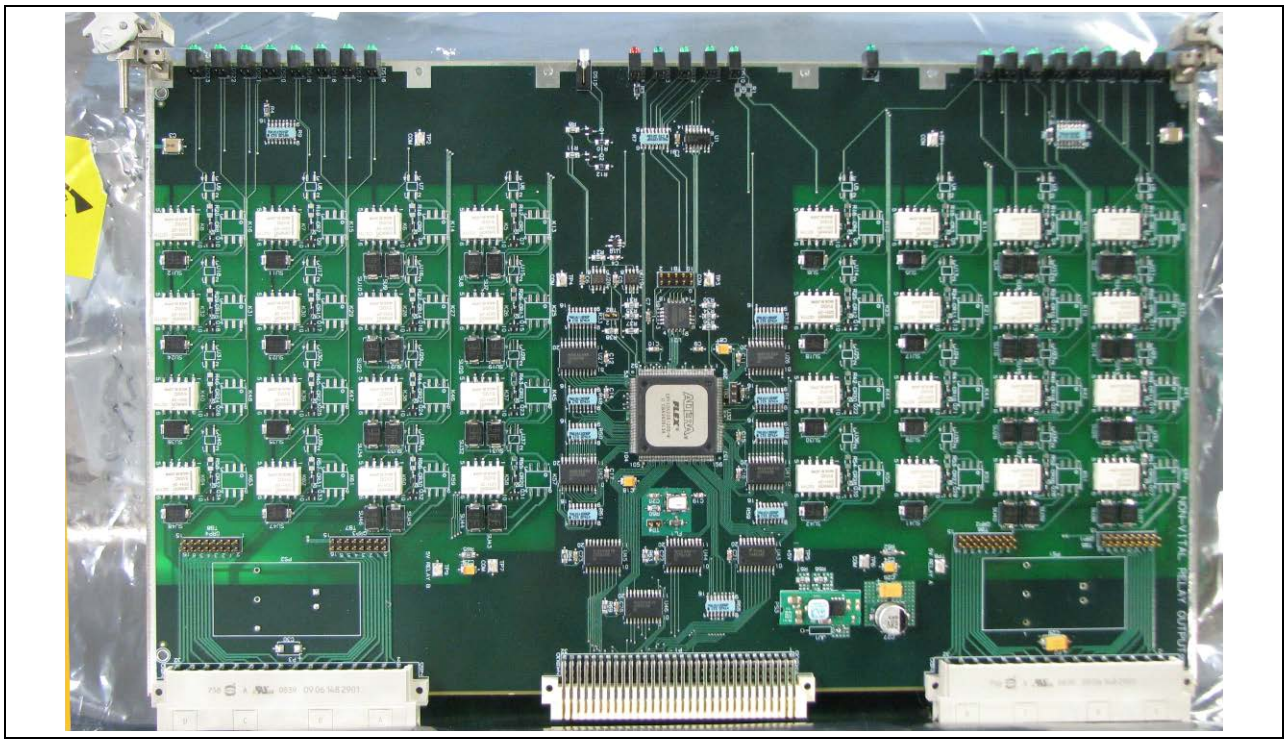

Figure 5–3. NVO Board

5.3.4 NVSP Interface Boards

An iVPI may be configured to use two NVSP Interface boards to provide additional connectivity to the NVSP board:

- NVSP P1 Interface Board
- NVSP P3 Interface Board

5.3.4.1 NVSP P1 Interface Board Operation

The NVSP P1 Interface board (P/N 31166-474-01) is located at P1 on the NVSP board to provide additional connectivity to the NVSP board:

- Two RJ45 modular jacks connect to the NVSP board's Ethernet Ports

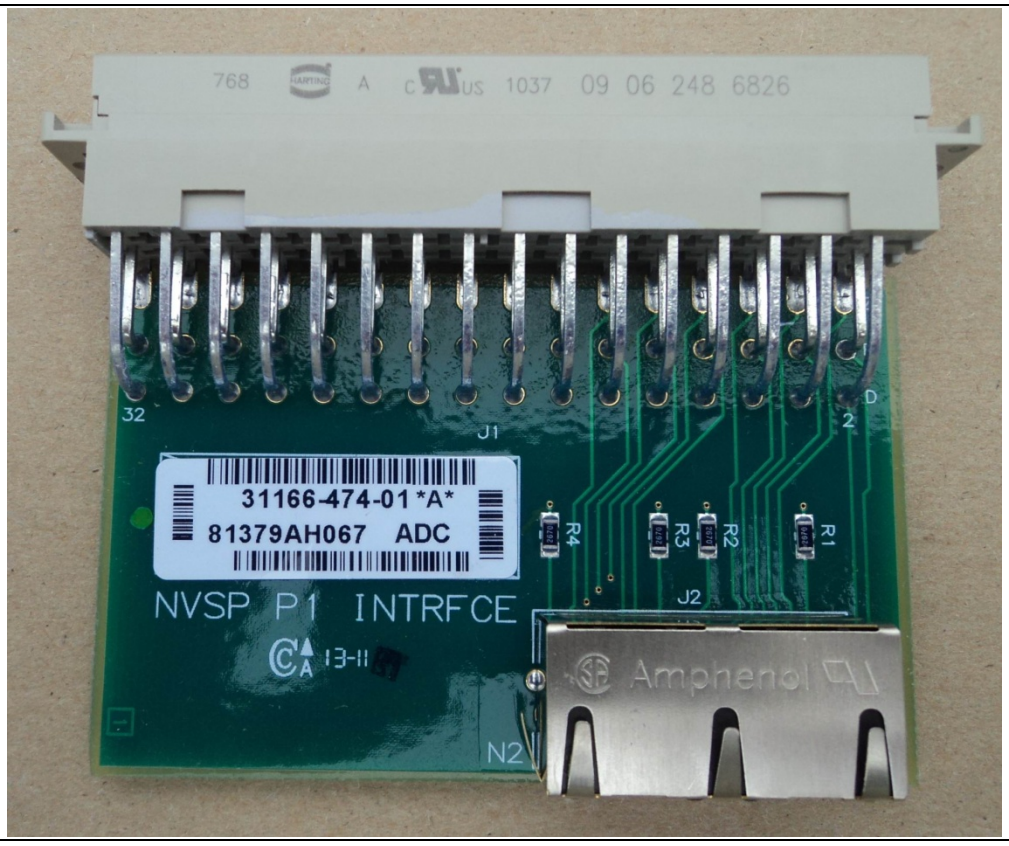

Figure 5–4. NVSP P1 Interface Board

5.3.4.2 NVSP P3 Interface Board Operation

The NVSP P3 Interface board (P/N 31166-475-01) is located at P3 on the NVSP board to provide additional connectivity to the VSP board:

- Two EIA RS-232 DB-25 connectors that connect to the NVSP board's serial ports 1 and 2:
  - One connector is labeled Port 1
  - One connector is labeled Port 2
- One RJ45 modular jack connects to the NVSP board's MAC Port
- One RJ45 modular jack connects to the NVSP board's serial port 3, labeled Port 3
- One RJ12 modular jack for use with the NVSP board's Health Status

Note: An NVSP board with a P3 Interface (P/N 31166-475-01) requires two slots.

Note: The NVSP P3 Interface board is wider than a single slot; therefore, adjacent NVSP boards that utilize P3 Interface boards must not be placed in immediately adjacent slots in a subrack.

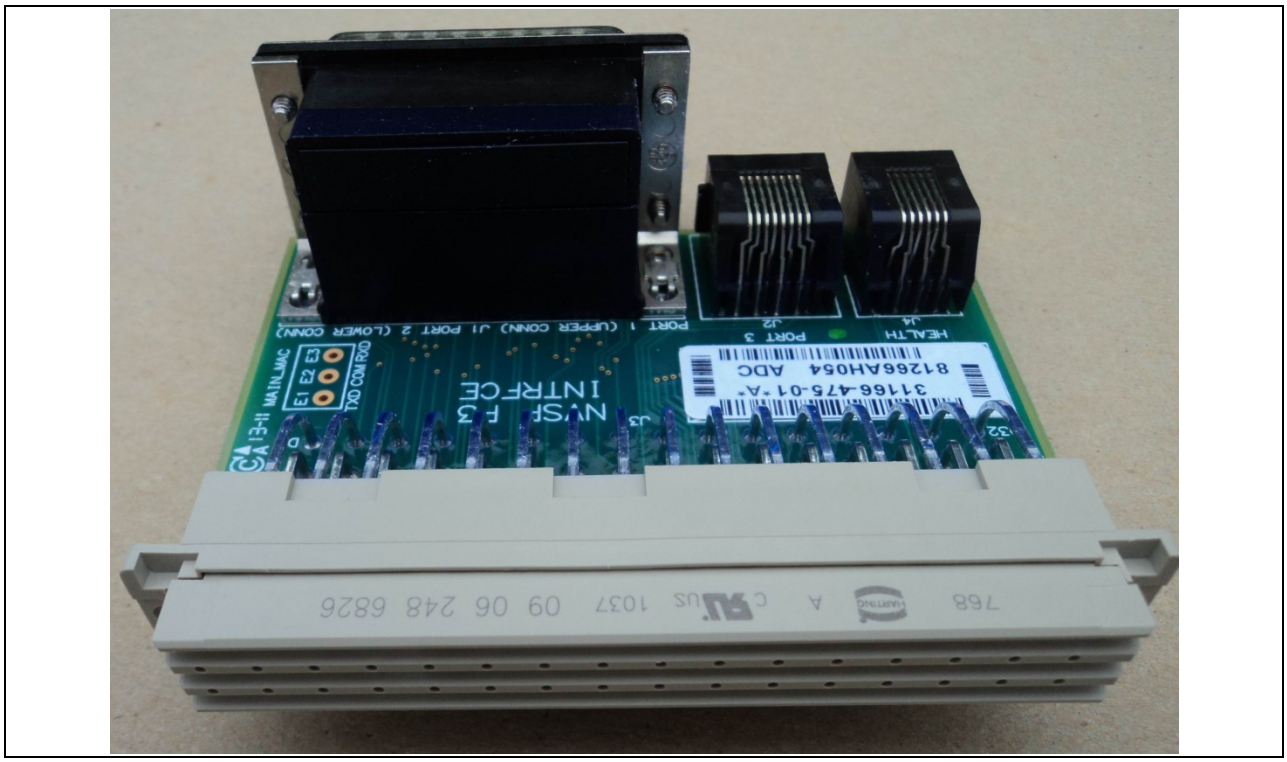

Figure 5–5. NVSP P3 Interface Board

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 6 – DESIGN, TEST, AND VALIDATION TOOLS

6.1 GENERAL

This section describes the design, test and validation tools available for the iVPI System.

6.2 INTRODUCTION

The Vital system performs all Vital logic associated with interlocking control (switch control, locking, and signal control). At the user's option, this logic can be written in the form of Boolean equations or drawn as relay circuits in AREMA Drop-Line format, AREMA Straight Line format or as commercial PLC format that emulate traditional relay logic. No special programming language is used in the application thus allowing the source file(s) to be easily understood by a signal engineer.

After the Boolean equations or relay diagrams have been created by the Signal Engineer, the Computer Aided Application (CAA) software package is used to compile the equations into machine readable code. Through the use of AlsDload, the VSP application is written to the appropriate system's VSP board.

The non-vital system performs similar functions on all non-vital logic associated with interlocking control (switch position requests, signal clear requests, Local Control interface, remote control communications, local data logging). Through the use of AlsDload, the NVSP application is written to the appropriate system's NVSP board.

Table 6–1. Design Test and Validation Tool Part Numbers

Description	Part Number
CAAPE CD-ROM ("XX" in part number = customer ID)	31754-015-XX
MMS Server/Editor, Maintenance Management System (Windows XP, Windows 7 Professional, 32 bit)	51795-081-00
MMS Client, Maintenance Management System (Windows XP, Windows 7 Professional, 32 bit)	51795-082-00
AlsDload CD-ROM	51795-085-02

6.3 APPLICATION DEVELOPMENT TOOL

The Computer-Aided Application Programming Environment (CAAPE) is a comprehensive set of development tools for creating iVPI Vital and non-vital applications. These tools are integrated together within a Windows®-based development environment for easy access.

The CAAPE package is intended for use by Alstom signal engineers, by railroad and transit signal engineers, and by third-party signal engineering consultants. The iVPI CAAPE toolset is built on the same stable foundation that has become an industry-accepted favorite, and is backward compatible to all previous versions.

The top-level CAAPE program provides access to available tools and manages application data through the use of projects. A project is a collection of files describing one or more applications. Some of these files, such as report and prom files are meant to be directly accessible by the user; others are for internal use and are readable only by CAAPE. Typically, a CAAPE project describes all the applications in a particular iVPI System.

All the files for a given project are contained in a single directory. A single main project file acts as a directory to the rest of the files in the project and specifies the CAAPE options selected by the user for the project. When the CAAPE opens a project it reads the main file to determine the full list of files and options in the project. Tools to assist in software configuration control are included within the CAAPE package.

The lower-level tools such as compilers and application data verifiers, which are tied to a particular version of iVPI System software, comprise a CAA package. The CAAPE can provide access to the tools in multiple CAA packages (Windows versions only). The user can select which set of compiler and data verifier tools to use for a particular application by selecting a specific compiler version based on which version of Vital system software is used. This allows support of older versions of the VPI product line as well as newer versions in the same development environment.

WARNING

Field testing of an Application is required before placing the location into revenue service. The customer's testing plan and safety plan define the testing requirements for the Application.

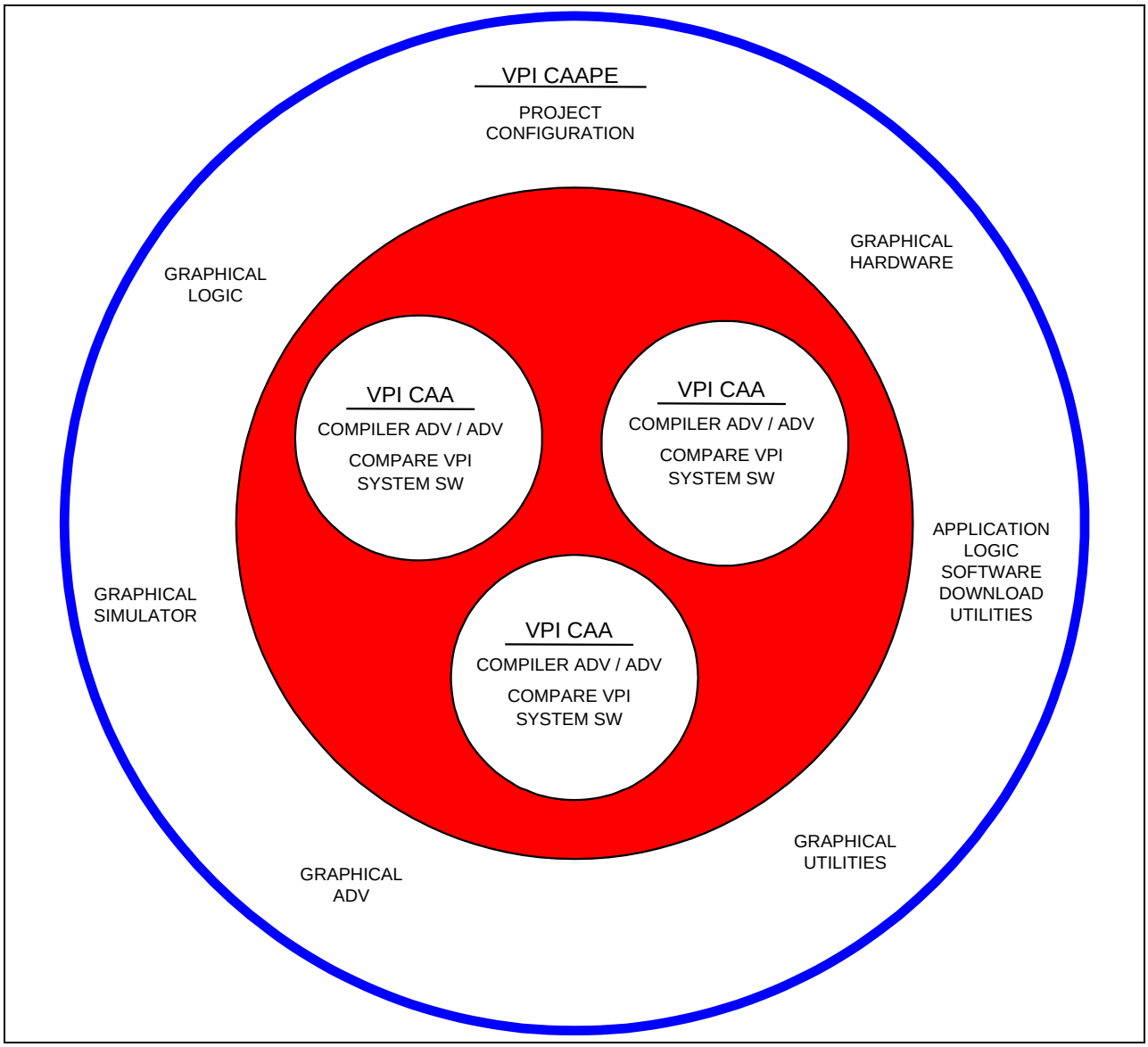

Figure 6–1. iVPI/VPI CAAPE/CAA Typical Arrangement

CAAPE includes the following utilities:

- Compilers for iVPI Vital and non-vital applications
- Application Data Verifier (ADV) for iVPI
- ADV Comparison for iVPI for identifying differences between two VPI Application Programs
- Graphical Simulators for both iVPI Vital and non-vital logic
- AlsDload – a FLASH program with a software configuration checker
- Utilities such as:
  - PROM file generation
  - I/O Label generation for printer/plotters
  - Consolidation report for iVPI ADV
  - Relay equivalent circuits for final documentation
  - System Hardware and Software Configuration Reports for Configuration Management
  - Utilities to convert to/from Text format (Boolean Equations) and Graphic Format (Relay/Ladder Logic Graphics)

The CAAPE package uses a project-based architecture that allows the user to create projects containing any number of iVPI applications. Computer programming experience is not required; applications can be built using either graphical or textual methods. The graphical methods include form entry, pull-down lists, extensive prompts, online documentation, and a HELP facility to guide the designer through the process. An extensive, stand-alone tutorial is also provided for easy training and reference.

The CAAPE package can be used for both Vital and non-vital applications, and includes a database function to store and organize all relevant data. An extensive documentation section makes it easy to track applications through various stages of development and provides enhanced revision control.

Online, context-sensitive assistance is available through the HELP facility in the form of a SEARCH window. Also accessible from the HELP menu, the comprehensive tutorial provides an easy reference guide and training tool for the CAAPE package. The program allows the viewer to follow the creation of a typical new application from the beginning to end, and also contains an index for handy access to the main control topics and a full set of user manuals.

6.3.1 CAAPE Operation

The CAAPE design tool shows project contents, graphical logic editing and compile results in a message window to illustrate the integrated nature of CAAPE.

CAAPE provides:

- Integrated project-oriented environment for developing, compiling, and verifying applications and for managing input, output and report files
- Graphical entry of application data, including graphical logic with AREMA Straight Line or Drop Line symbols, or PLC Ladder Logic symbols. The user can switch from any symbol set to another at any time
- Traditional text-based (Boolean equations) application data entry is supported as well
- Compiler configuration reports include date/time of input and output files, system software versions, calculated checksums, and CRCs

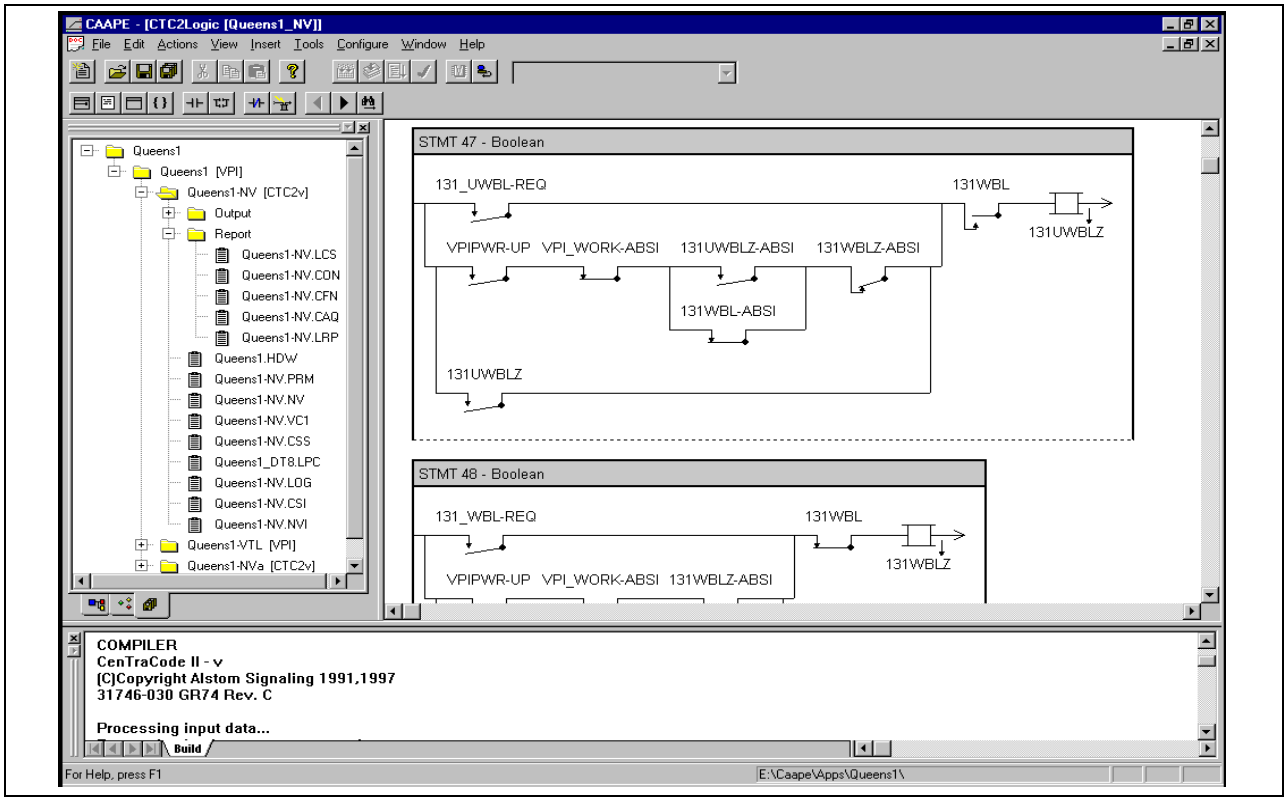

Figure 6–2. CAAPE Relay Application Logic Display
(Depicting AREMA Drop Line Symbols)

6.3.2 Application Data Verification and ADV Comparison

WARNING

The Application Data Verification (ADV) procedure output listing provides a means to compare and verify equivalence between the input and the output data.

However, the Application Data Verification process neither determines the safety suitability of the Boolean expression list nor determines the validity of certain encoded application data. The input data to the ADV process must be verified for safety separately, prior to the ADV process, and the safety and suitability of the input data is the responsibility of the user.

The ADV does, however, issue warnings and error messages as a result of non-vital data checking to alert the user to possible discrepancies.

The ADV is a CAAPE utility that is used to verify a compiled design, as it is resident in iVPI System Memory. This feature has been an integral component of the VPI tool set since the first VPI entered revenue service in 1986 and has continued to evolve through all feature enhancements to the VPI and iVPI product line.

The ADV Comparison program highlights the differences between two versions of an iVPI Vital application. This feature was added in the early 1990s to support large multi phased distributed VPI installations and is a core component of the “incremental” (“reduced”) retest philosophy.

In general, the ADV:

- Reconstructs Application Design from Flash EPROM
- Generates Reports for Circuit Check
- Used to Reconstruct Entire Application from the Application .Hex File
- Creates the Equivalent of an Electronic Book Of Plans
- Provides for a Difference Utility that Highlights Changes
- Provides Security Far Beyond Simple Checksums
- Validates Configuration Management

Specifically:

- ADV helps verify that application prom data matches intended user input. New Consolidation Reports simplify analysis of ADV data
- “Graphical ADV” helps verify that graphically entered logic matches prom data. ADV Compare program compares ADV reports to highlight differences between applications in their Vital logic, symbols, messages and I/O
- ADV Compare program compares ADV reports to highlight differences between applications in their Vital logic, symbols, messages and I/O

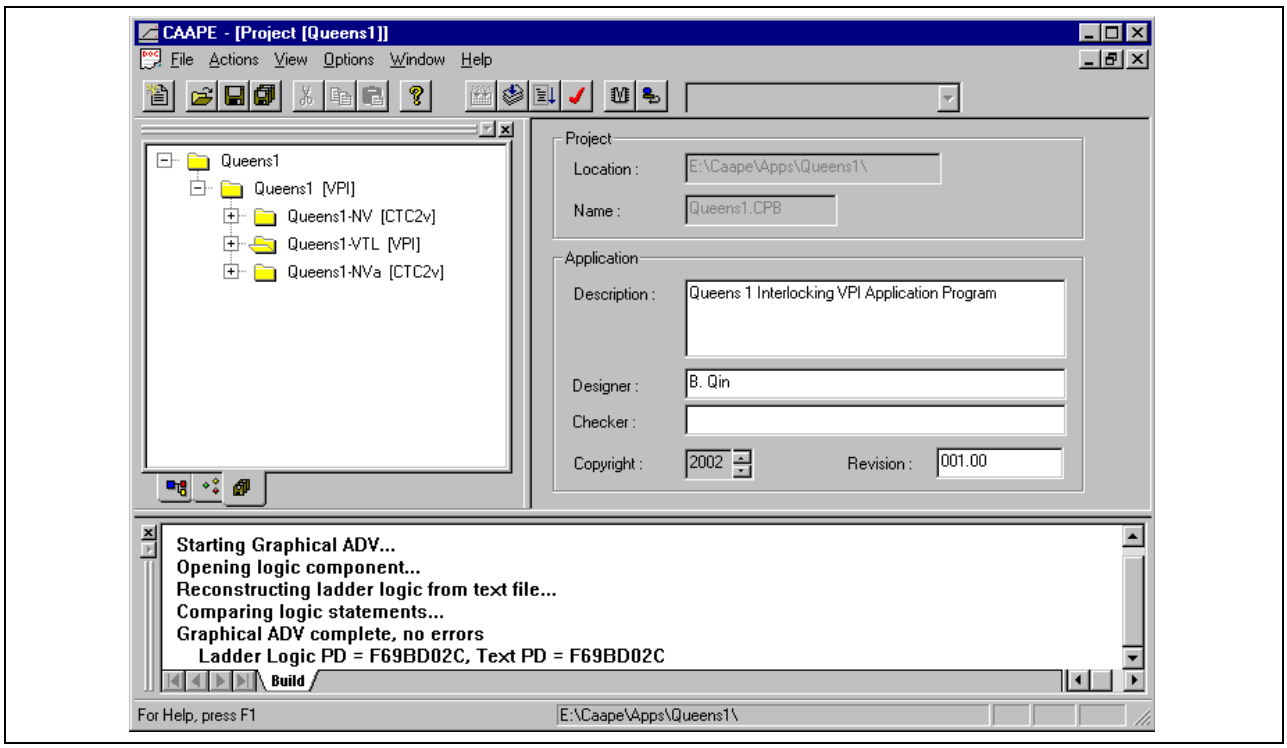

Figure 6–3. Graphical ADV – Compares Logic Input to Output Files with CRCs

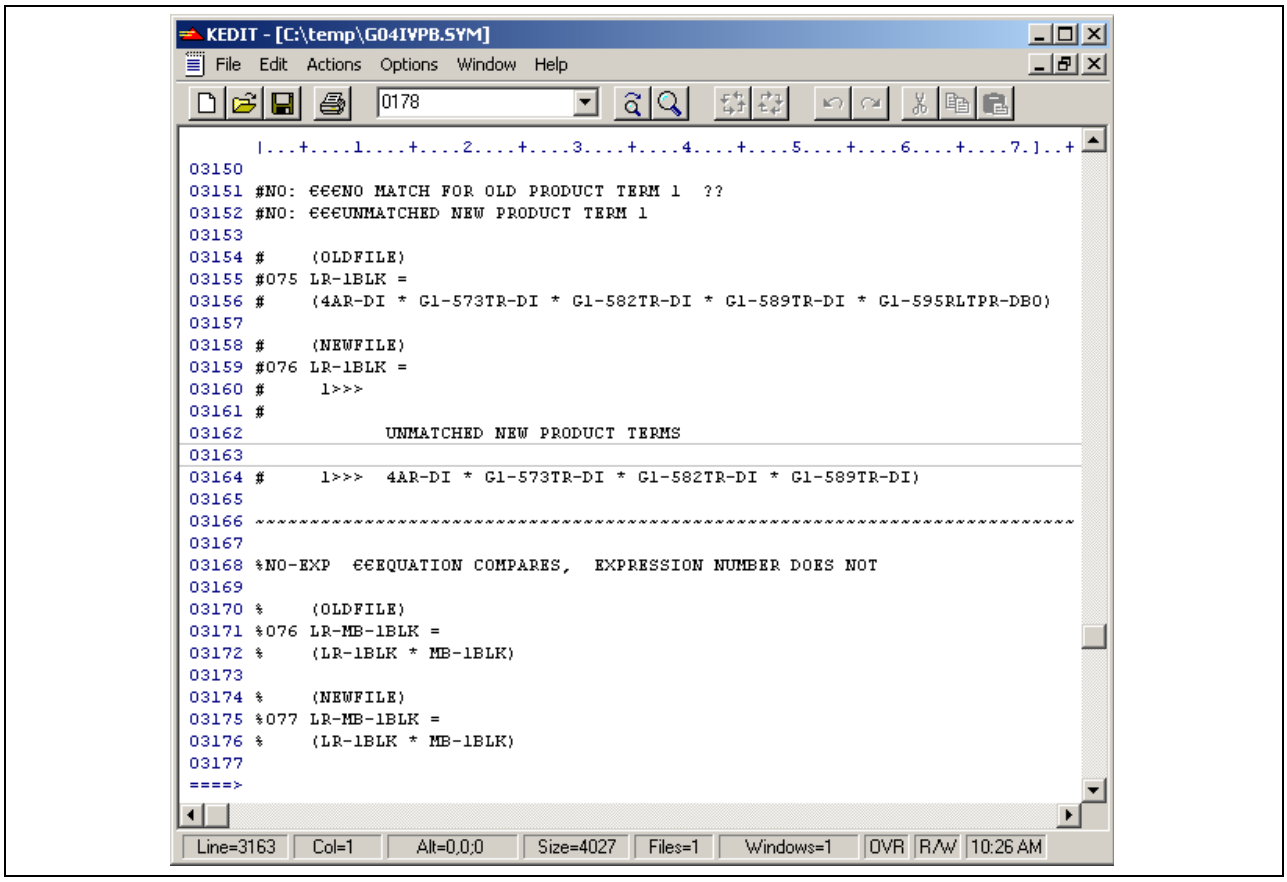

Figure 6–4. ADV Comparison Report Depicting Expression Changes on a Boolean Expression

6.3.3 Graphical Simulator – Integrated and Provided With The CAAPE Package

The Graphical Simulator shows project contents, watch window and track plan display (refer to Figure 6–5 and Figure 6–6). It is used to:

- Simulate multiple Vital and non-vital applications simultaneously; large distributed iVPI System arrangements can be simulated at one time with both discrete I/O and communication links simulated between systems as well as to field apparatus and control offices
- Provide timing data to analyze iVPI System response time to the various operations
- Inject many types of failures (broken filaments, blocked switch points, failed communication links)
- Easily manipulate and observe system behavior
- Model many types of field apparatus. The user can add additional simulated apparatus
- Utilize a user-defined track plan display to simulate operation of field devices
- View status of application logic in graphical format, set breakpoints to stop simulation at specific points in the logic
- Monitor and record the states of selected variables
- Provide a project-oriented interface similar to CAAPE
- Provide a Watch Window
- Test scripts and user-defined command sequences
- Support multiple physical and multiple virtual screens for large systems and large interlocking plant simulations
- Function as an engineering aid to debug new designs, to investigate reported field problems, and as a training tool for new operators and engineers

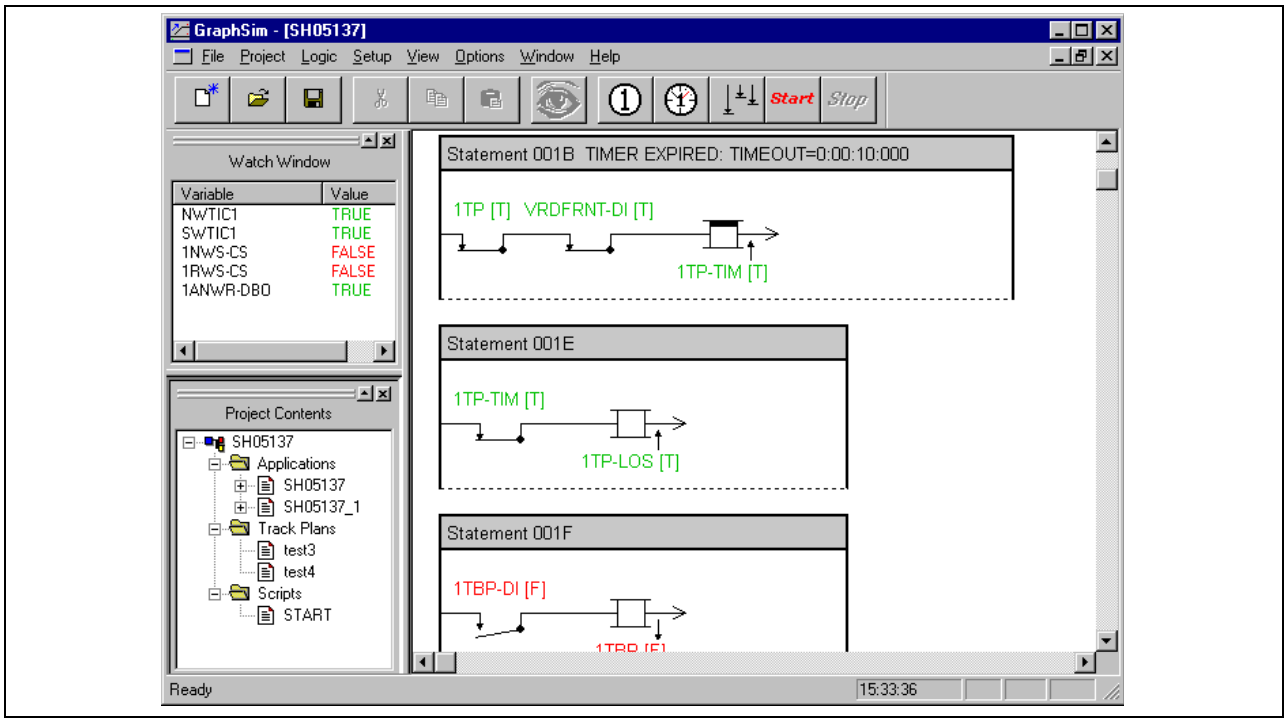

Figure 6–5. Graphical Simulator Application Logic Display

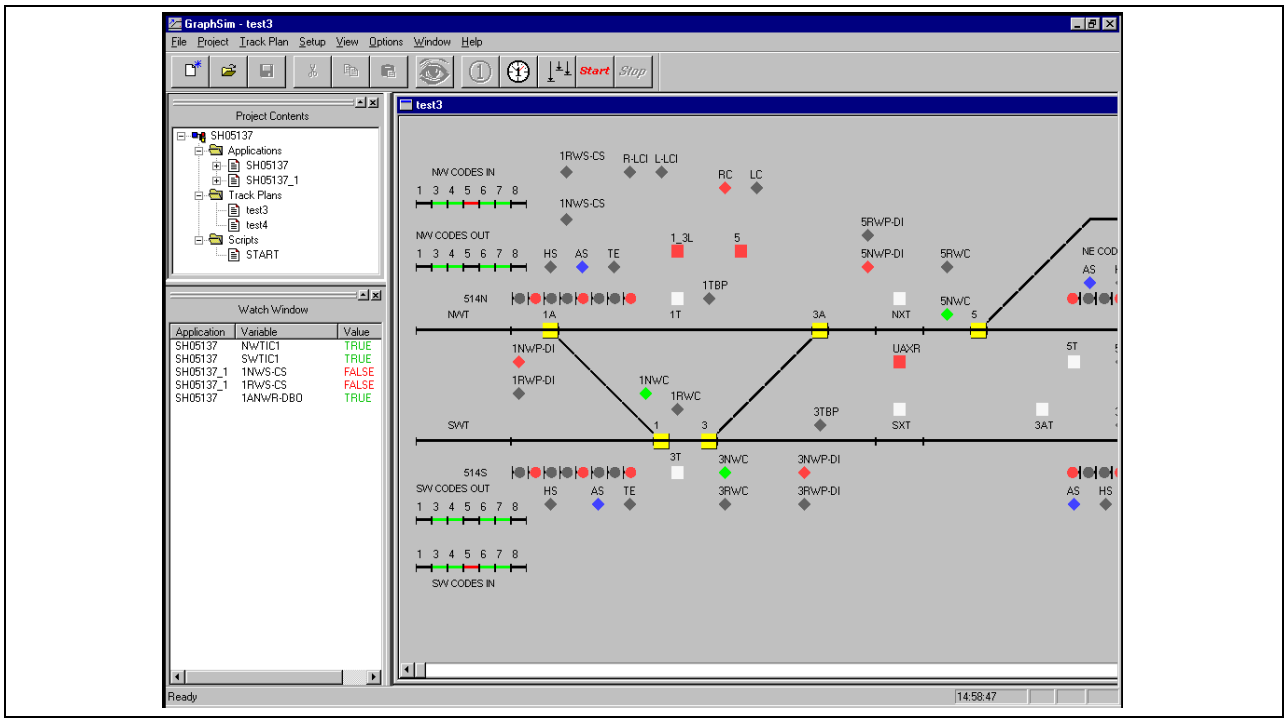

Figure 6–6. Graphical Simulator Track Plan Display
(Depicting Interlocking Control and GENRAKODE Codes)

6.3.4 AlsDload

AlsDload is a tool for programming application and system software on VPI, iVPI, PGK, PGK2, GK3, and AFTC boards.

AlsDload provides the following capabilities:

- Download of application and/or system software from files on the PC to the programmable memory on the board
- Upload of application and/or system software from the programmable memory on the board to files on the PC (available with iVPI VSP boards)
- Report or change values of field-settable software Vital application timers (available with iVPI VSP boards)
- Verification that board configuration data is identical to that in selected files
- Access to board diagnostics
- Basic VT100 terminal emulation

6.3.5 CAAPE System Benefits

The exclusive and incomparable benefits that are offered as a result of implementing iVPI with the CAA tools package include:

- The CAAPE is a Computer Aided Application Programming Environment allowing for configuring, compiling, and simulating VPI Systems.
- Overall test time is decreased, and application hardware can be tested without hardware. The “Application Data Verifier” (ADV) validates changes that are made to the Vital application software ensuring that only the desired changes are incorporated. This system generates configuration comparison reports automatically and compares then to the original program.

> **WARNING**
>
> No trains may be put into revenue service until ALL of the file outputs are verified to be identical.

- The Vital processor supports future interfaces and in doing so has the aggregate capacity of processing up to 4,000 Boolean logic equations per second without any change in cycle time dependent upon the number of changed inputs. Programming can be either Boolean equations or relay equivalent circuits drawn in AREMA Drop Line, AREMA Straight Line or commercial PLC Ladder Logic format. The user can switch from any format to any other format as desired. Any format can be used to generate hard copy drawings of the equivalent circuits as a final system output for documentation.
- The CAAPE package for the iVPI Control System contains a tool called the Graphical Simulator that allows the user to generate control and indication panels, the field apparatus, and simulators to exercise the Vital and non-vital logic on a standard PC screen(s). The logic equations and variables can be viewed graphically with the corresponding states during the simulation run-time. Multiple iVPI Systems can be simulated simultaneously and the states of selected equations can be monitored and recorded.

6.3.6 CAAPE System Requirements

Table 6–2 shows the computer and operating system requirements for CAAPE P/N 31754-005J and later.

Table 6–2. Computer and Minimum Operating System Requirements

Description	Requirement
Operating System	Windows 95/98, NT 4.0 SP 6, 2000, XP SP3
RAM	64 Meg
CPU	Pentium or compatible
Hard Disk	200 Meg available
Input Device	Keyboard and mouse
Display	SVGA (800 x 600)
Other	CD-ROM

6.4 MAINTENANCE MANAGEMENT SYSTEM

The Maintenance Management System (MMS) is an Alstom diagnostic tool that can remotely monitor each iVPI Vital and non-vital networked system.

MMS is a graphical diagnostic and maintenance application that uses a graphical track layout to dynamically record and display the iVPI diagnostic status, the status of linked iVPI variables and play back recorded data.

Additional tools are available to manage diagnostics, configuration, event and data logs, schedule maintenance tasks, and view, record and play back iVPI application variable data.

For more information on this Alstom tool, refer to Alstom publication *P2509 Maintenance Management System for Alstom Vital Processor Interlocking Systems (VPI, VPI II, iVPI)* or *P2528 MMS Client/Server for Alstom Vital Processor Interlocking Systems (VPI II/iVPI).*

SECTION 7 – NON-VITAL SYSTEM AND COMMUNICATIONS SOFTWARE

7.1 GENERAL

This section describes the non-vital subsystem and communications software used in the iVPI System.

7.2 INTRODUCTION

The non-vital subsystem can support multiple communication/code system protocols simultaneously while performing non-vital input/output operations, application logic functions, train-to-wayside and wayside-to-train communications and data logging within the iVPI System. The data logged information is time-stamped and can be viewed real-time, can be selected by the user by run-time, or downloaded for off-line examination. The logic may be written using a combination of Boolean and higher-level programming techniques to control the communications and input/output functions.

7.3 APPLICATION

7.3.1 I/O

Non-vital inputs and outputs can interface to external equipment in order to provide indications to a remote office or to an adjacent location. Outputs are capable of flashing at 60 cycles per minute or 120 cycles per minute. Examples of inputs and outputs include the following:

- Local Control Panel
  - Switch Machine Normal and Reverse Request Controls
  - Switch Machine Normal and Reverse Position and Lock
  - Indications
  - Signal Request, Fleet, and Cancel Controls
  - Signal Aspect and Fleeting Indications
  - Traffic Indications
  - Snowmelter
  - Controls and Indications
- Maintainer Calls
- Battery Power Alarms
- Ground Detection
- Fire Alarm
- Intrusion Alarm
- Room Temperature Monitor
- Track Indications
- System Health
- Redundancy Transfer

7.3.2 Logic

The non-vital logic can be written to perform a wide array of functions, including the following:

- N/X (Entrance/Exit) Interlocking Control
  - Controls provided from a local panel and/or a remote office
- Unilever Interlocking Control
- Remote Office Controls and Indications
- Train-to-Wayside and Wayside-to-Train Communications
  - Train Dwell Control
  - Train Identification
  - Train Berthing
- Automatic Train Operation
- Automatic Route Generation
- Auxiliary Train Tracking
- Interface to Vital Logic

7.3.2.1 Logic Statement Types

- Boolean Equations
- Timer Equations - delays the setting of an equation
- Integer Equations - arithmetic using variables and constants
- Program Flow Control: IF/ELSE, WHILE, GOTO
- User-Defined Subroutines: SUBROUTINE, CALL
- Predefined Subroutines: timer control, format conversion (e.g., Integer-Binary)
- Arrays

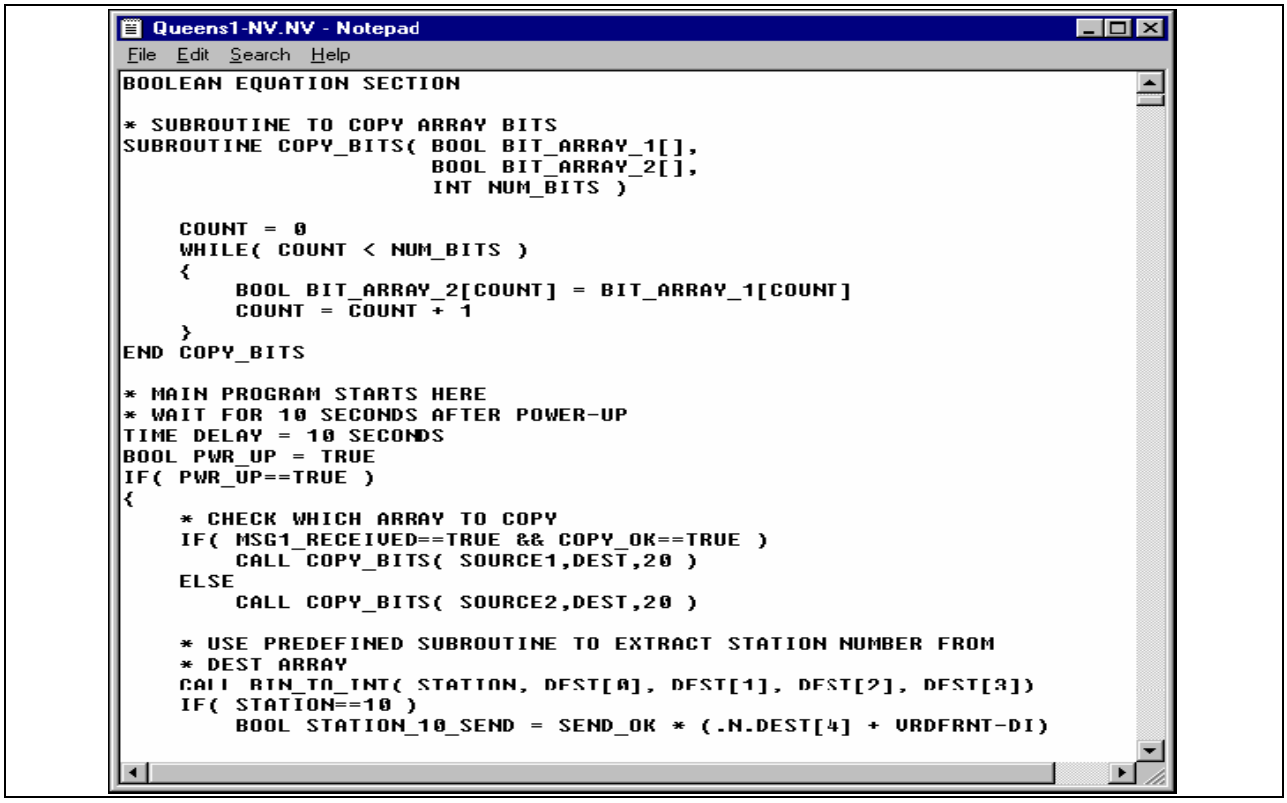

Figure 7–1. Logic Programming Sample

7.3.3 Communications

iVPI communications include:

- Office - provides local or interlocking information to a remote office for display while allowing the office to control routing through the interlocking
- Remote Access Terminal
- Automatic Train Dispatch
- Platform Signs
- Intra- or Inter-system Communications - allows expansion of the system or partitioning of the non-vital subsystem into multiple processors; also allows neighboring locations to exchange interlocking information

The communications protocols are distributed with the CAAPE software package.

7.4 SYSTEM SOFTWARE INTERFACE MATRIX

See Section 4 in Alstom publication P2521B, Volume 1, for Alstom's library of communications protocols.

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 8 – MIGRATION STRATEGIES

8.1 GENERAL

This section describes iVPI System migration strategies.

8.2 MIGRATION

Because of the nature of the iVPI architecture, installation in the field can accommodate any phased alternative that best suits the need of the customer. A simple non-vital subsystem, to a subsystem with Vital I/O, to a system with full non-vital and Vital I/O and Logic capability can be achieved.

Upgrading legacy installations on Transit applications can be performed as follows:

- Start with installing networking communications to replace older generation line wire carrier based communications systems which operated at much lower baud rates
- Add NV Logic to replace older electronic or relay cabinets
- Make provisions for Vital add-on by defining the configuration of the boards populating a subrack
- Add Vital communications or I/O Interfaces
- Add Vital Logic

For Commuter, Freight, or LRT, follow a similar progression including the addition of train detection and cab signaling as required.

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 9 – REDUNDANCY, AVAILABILITY, AND ISOLATION

9.1 GENERAL

This section describes iVPI System redundancy, availability, and isolation.

9.2 REDUNDANCY

The iVPI product is constructed to allow for Hot, Warm, or Cold standby redundancy. The very high reliability of the electronics permits many applications to be implemented with only one controlling System in many cases.

Historically, failures encountered have been those effecting I/O circuitry. Therefore, full System redundancy is suggested, in line with a high availability System requirement. iVPI insures that all software and hardware is strictly configured and controlled internally, so proof (between the Systems) that the Systems are of the same version and revision is not required. Any change that influences the safety elements of the System is revealed to the user both in reports from the System tools and from the on-line System itself. Any configurability issue results in the effected System functioning in a more restrictive operating state until the failure is repaired.

9.3 AVAILABILITY

Hot Standby configurations can be implemented through the passing of active application parameters indicating the current state of the interlocking. During a transfer initiated due to failure(s) of one System, the standby System seamlessly transitions to control field elements as long as the application parameters are appropriate.

With iVPI's superior diagnostics capability, failures are identified quickly and repaired (MTTR <30 min) without affecting the online System.

9.4 ISOLATION

The network capability of iVPI permits I/O to be isolated from the central interlocking logic based on customer preference or in unique harsh environments. The I/O Systems need only provide I/O interface functions. If an I/O System should fail, only that System is affected. This provides a higher level of availability for the interlocking.

The use of isolated Systems is a tradeoff between the amount of hardware and engineering and the installation logistics.

THIS PAGE INTENTIONALLY LEFT BLANK.

SECTION 10 – SUMMARY

10.1 GENERAL

This section summarizes the iVPI system.

10.2 SUMMARY

The new iVPI system represents a significant movement to a modular, scalable microprocessor control unit that can handle applications as small as a single control point or end of siding to large, complex interlockings. Built on the solid and safe foundation of its predecessor, VPI, the iVPI solution combines the power of Ethernet networking capability with industry standard diagnostic tools to form a powerful new control package offering.

iVPI presents a lower initial investment in material outlay, as well as installation and testing expenses. When combining this with the many value-added after sale savings in serviceability and maintainability, the iVPI platform presents significant cost reductions for both railroad and transit interlocking and wayside applications.

For additional information on this or any other Alstom Signaling Inc. product, including product manuals, contact our Customer Service Line at 800-717-4477 or visit our website at:

www.alstomsignalingsolutions.com

THIS PAGE INTENTIONALLY LEFT BLANK.

APPENDIX A – HISTORY OF THE VPI PRODUCT LINE

A.1 GENERAL

This appendix describes the history of the VPI product line.

A.2 INTRODUCTION

Since its introduction in 1986, the VPI product line has undergone continuous evolution and improvement. At its initial introduction, VPI Systems were primarily designed to interface with the traditional Vital 12 VDC systems that had become standard in North American Railroads. Families of Vital and non-vital AC I/O boards were also developed for interfacing to AC signals and AC equipment found in North American transit as well as in the international railroad and transit markets. For transit systems with higher degrees of automation, integrated families of Vital cab signal and non-vital train-wayside communication boards were also developed as integral features of the VPI product line.

With the advances over the last two decades in processor and communications technology, VPI Vital and non-vital processor boards have been updated at key points in time for more processing capacity, higher speed communications and protocols, more advanced diagnostics, and more sophisticated man-machine interfaces. VPI point-to-point Vital serial communications was introduced in 1990 and expanded to point-to-multipoint in 1994. VPI Vital communications can be transported over non-vital communication systems including fiber optic systems, both dedicated and multiplexed channels.

All of these updates have been performed in an upward compatible manner. In recent years, some of the original VPI installations of the 1980s have been upgraded by customers by just a Vital and/or a non-vital processor board upgrade. These upgrades to existing installations incrementally bought these systems up to date with the latest communications technology, the latest advanced diagnostics, and the latest man-machine interfaces that did not exist at the time of the original installation the without necessity of a total system replacement.

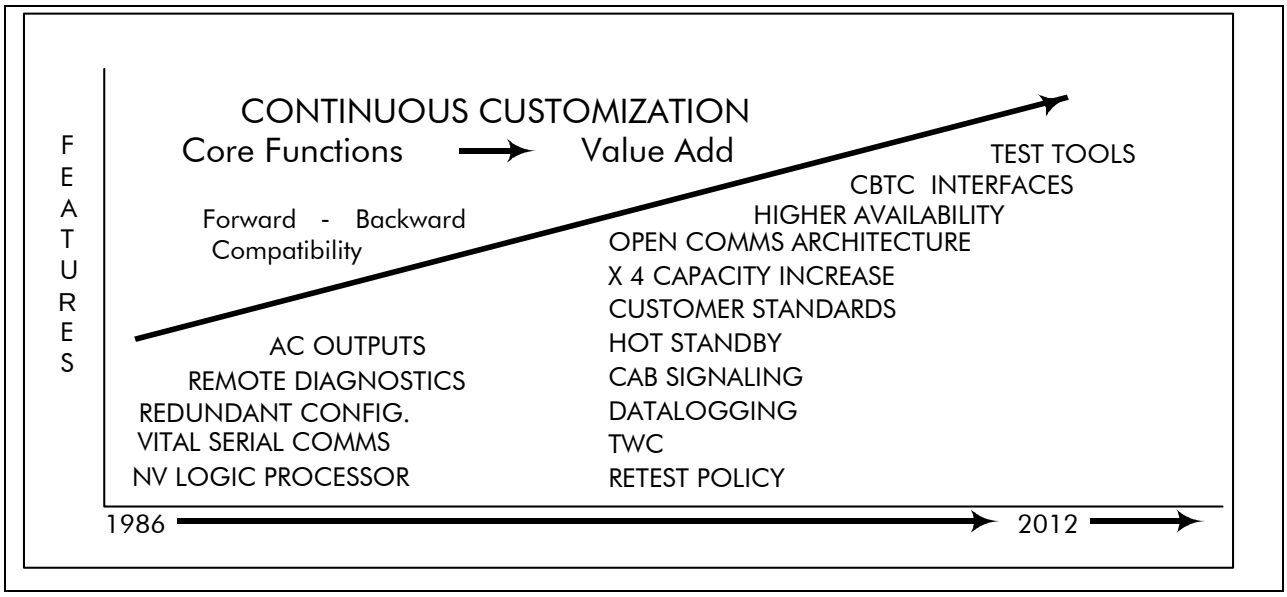

Figure A–1. Continuous Evolution of VPI®

In recent years, the VPI product line has undergone a series of major product upgrades known as VPI II. VPI II upgrades was a five-year development plan that brought a number of advanced product enhancements, all of which are upward compatible with the existing installed base to the VPI product line. Several of the early products of this upgrade plan including the LDO board, the VPI II Maintenance Management System [described in Section 6.4 Maintenance Management System

] and the VSC board which offers increased performance and an integrated network adapter while maintaining the same Vital software algorithms. The current iVPI System is the latest addition to this continuous product improvement program.

A.3 VPI OPERATING CONDITIONS

VPI Systems have seen years of successful operation in the northern reaches of Canada with winter temperatures frequently in the range of –40 °C, in the hot, dry deserts of western Colorado and northern Queensland, Australia, with summer temperatures in the bungalows approaching +70 °C and in the hot, humid climates in the rain forests of Indonesia and Sri Lanka.

VPI Systems have been extensively tested and operated in the extremely harsh EMI environments including lightning that are generally seen within railroad and rail transit systems and especially within electrified railroad transit systems. VPI Systems are designed to operate within the guidelines for systems installed per AREMA Communication and Signal Manual Parts 11.1 to 11.4 regarding Electrical Surge Protection and Lightning Protection. VPI Systems are designed to operate with the traditional lightning protection equipment and proper wiring techniques utilized in the railroad and transit system environments.

More than half of the more than 1500 VPI Systems have been installed on rail and transit properties with electric traction power. These traction power systems have run the gamut of 25 Hz, 50 Hz, and 60 Hz primary power converted to traction power for 600 VDC, 750 VDC, and 1000 VDC third rail and for 12.5 KVAC, 25 KVAC high voltage catenaries. VPI Systems have been successfully installed and operated on many properties using radio communications for normal operations and for maintenance operations in the 160 MHz, 450 MHz, and in the 900 MHz bands. VPI System neither interferes with nor is interfered with by equipment in these bands with normal installation arrangements.

THIS PAGE INTENTIONALLY LEFT BLANK.

FOR QUESTIONS AND INQUIRIES, CONTACT CUSTOMER SERVICE AT
1-800-717-4477
OR
WWW.ALSTOMSIGNALINGSOLUTIONS.COM

ALSTOM SIGNALING INC.
1025 JOHN STREET
WEST HENRIETTA, NY 14586