FMC-MCM-1000

Evaluation and Product Development Platform

User Manual

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
1/10/2013	SOC initial Release	
20/10/2013	Version 1.00	Rev. 1
10/01/2014	Version 1.10	Rev. 2
20/07/2014	Version 2.00	Rev. 3
30/07/2014	Version 2.10	Rev. 4

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Preface

About This User Manual

This User Manual describes the features and operations of the FMC-MCM-1000 Evaluation and Product Development Platform. Details on the I/O interfaces and the corresponding components are provided.

Related Documents

- H.264 Video/Audio Encoder Datasheet
- H.264 Video/Audio Decoder Datasheet
- MPEG2 Video/Audio Encoder Datasheet
- MPEG2 Video/Audio Decoder Datasheet
- MPEG2-to-H.264 Transcoder Datasheet
- H.264-to-MPEG2 Transcoder Datasheet
- H.264 Video/Audio Encoder Module Product Brief
- H.264 Video/Audio Decoder Module Product Brief
- MPEG-2 Video/Audio Encoder Module Product Brief
- MPEG-2 Video/Audio Decoder Module Product Brief
- MPEG2-to-H.264 Transcoder Module Product Brief
- H.264-to-MPEG2 Transcoder Module Product Brief
- SOC Generic System-on-Module (G-SoM) Product Brief

FMC-MCM-1000 Evaluation and Product Development Platform

1. Overview

The SOC FMC-MCM-1000 Evaluation and FPGA Development Platform is designed for four major functions:

1. As an evaluation board for the SOC MPEG codec modules (the MCM-1000 series) and SOC MPEG Codec IP Cores (encoders, decoders, and transcoders).

2. As a product development platform for systems that uses the SOC MPEG codec modules or IP cores.

3. As a development board for product development based on the SOC Generic System-on-Module (G-SoM) Modules.

4. As a general FPGA and DSP development board.

A unique feature of the FMC-MCM-1000 is that it has a DDR3 connector that is used to connect the SOC MPEG codec modules (the MCM-1000 series) and the SOC G-SoM modules (FPGA/DSP-SoM-1000 series). Users can use the FMC-MCM-1000 to evaluate the SOC MPEG codec modules or IP cores, and then use it to do product development.

The FMC-MCM-1000 has its own FPGA chip which controls the I/Os and can be combined with the FPGA on the G-SoM module for multiple FPGA based system development. The FMC-MCM-1000 also has two FMC connectors, one male and one female, which allow it to connect FMC I/O daughter cards for large selection of I/O ports and to connect off-the-shelf FPGA boards to access FPGA types and resources.

The FMC-MCM-1000 is assembled with one of the four possible FPGAs, which are:
1. Spartant-6, LX45
2. Spartant-6, LX75
3. Spartant-6, LX100
4. Spartant-6, LX150

Development boards of other type of FPGAs can be connected to the FMC-MCM-1000 via one of the FMC connectors.

The FMC-MCM-1000 Evaluation Board and FPGA Development Platform is shown in Fig. 1 (top view) and Fig. 2 (bottom view). A block diagram of the system is provided in Fig. 3. *Fig. 4* shows a SOC MPEG Codec module (MCM-1000) is plugged on to the DDR3 connector on the FMC-MCM-1000.

Key Features

- Xilinx / LX150/LX100/LX75/LX45 FPGA
- 2 GB DDR3 RAM
- FMC male connector
- FMC female connector
- DDR3 connector for SOC MPEG Codec Modules or SOC SOM-1000 modules
- HDMI input
- HDMI output
- Ethernet
- Power rails for SOC MPEG Codec Modules or SOC SOM-1000 modules

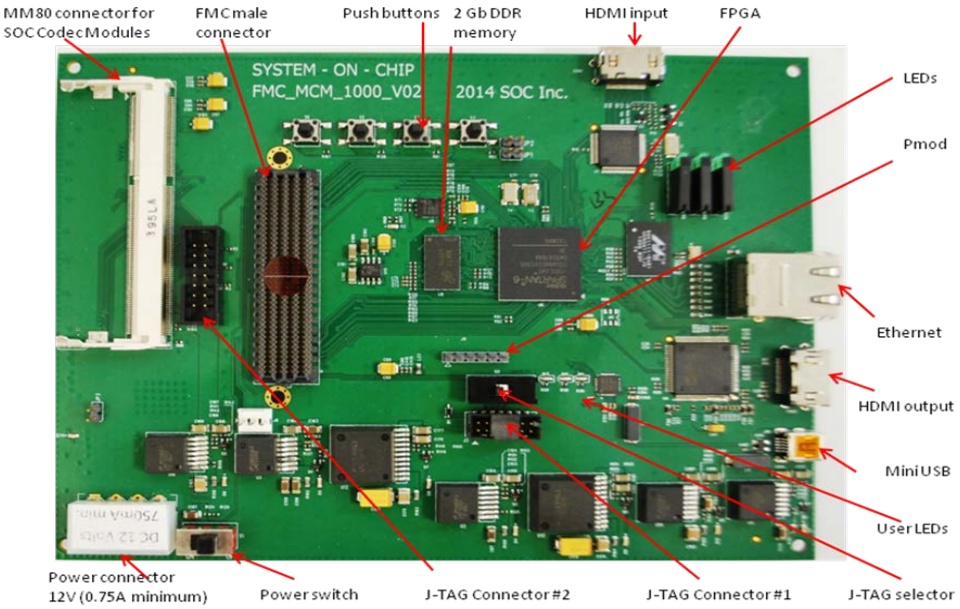

Fig. 1. FMC-MCM-1000 Top View

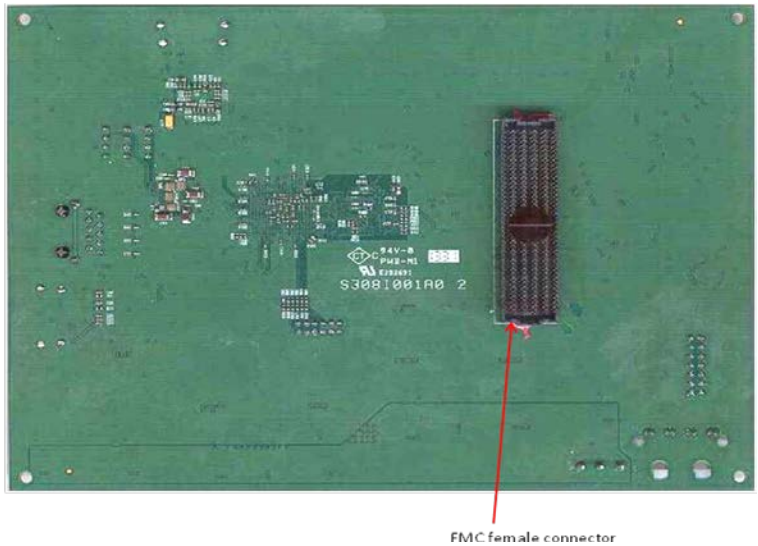

Fig. 2. FMC-MCM-1000 Bottom View

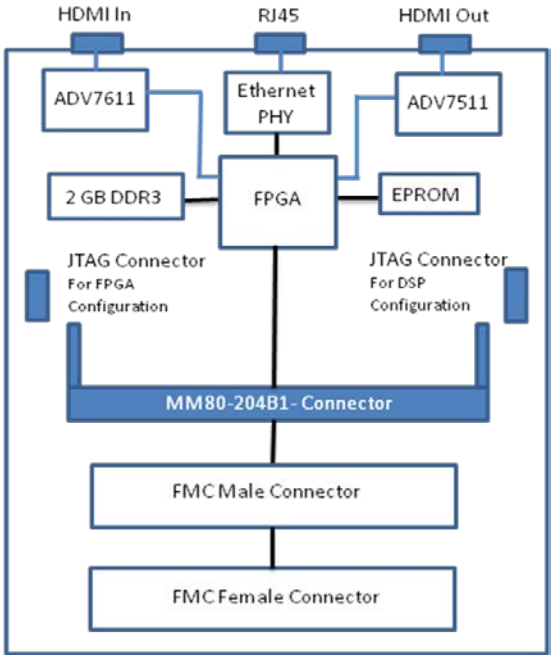

Fig. 3. FMC-MCM-1000 Block Diagram

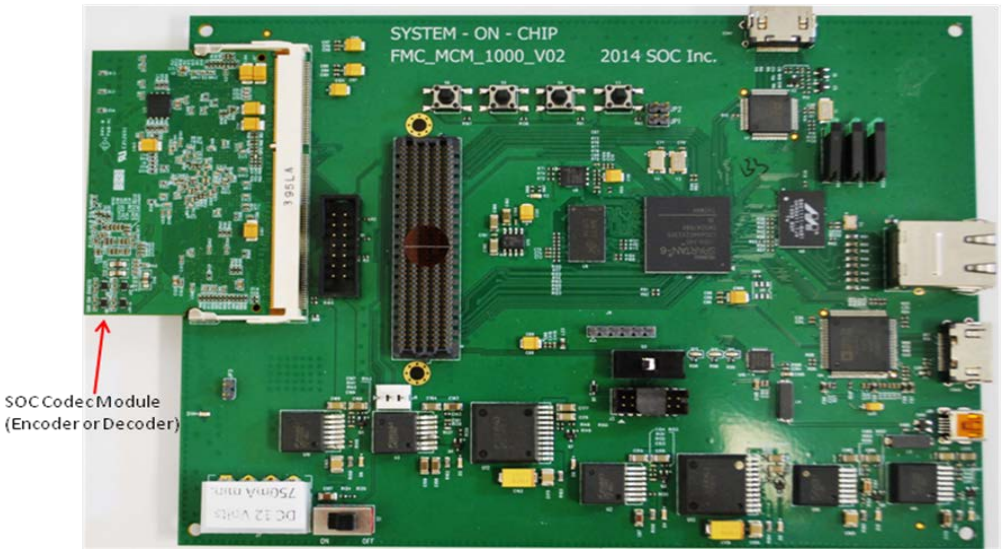

Fig. 4. FMC-MCM-1000 with a codec module plugged on the DDR3 connector

2. Use the FMC-MCM-1000

2.1 Use the FMC-MCM-1000 for Evaluating the SOC MPEG Codec Modules

The FMC-MCM-1000 is preloaded with the firmware for evaluating the SOC MCM-1000 MPEG codec modules. It is a plug-and-play system that allows the user to insert the selected module (encoder, decoder, or transcoder), and connect the I/O devices to start the evaluation.

For encoder evaluation, the input video source is sent into the FMC-MCM-1000 via the HDMI input port; the encoded stream will be sent to a computer through the Ethernet port. Users can decode the encoded streams by using standard software decoders.

For decoder evaluation, the compressed streams are sent into the FMC-MCM-1000 through the Ethernet port by a computer. The software for sending the streams is provided within the FMC-MCM-1000 package. The decoded video and audio are sent to the HDMI output port for display.

Two FMC-MCM-1000 boards can be connected back-to-back through the Ethernet ports, which can evaluate the encoder and decoder together at the same time.

For transcoder evaluation, both the input stream and transcoded stream go through the Ethernet port from/to a personal computer.

Detailed instructions for evaluating the SOC encoders and decoders using the FMC-MCM-1000 are provided in Appendix-A.

2.2 Use the FMC-MCM-1000 for Product Development

The FMC-MCM-1000 is a versatile platform for product development, especially when the SOC MPEG codecs (the MCM-1000 series) are used in the design.

SOC provides (through a one-time fee licensing) a “netlist” IP core which contains all the I/O drivers for the FMC-MCM-1000, so that the users can drop in their own designs without having to implement the I/O modules. An Ethernet/UDP/IP network stack netlist IP core is also available for one-time-fee licensing.

A design template is also provided to licensees of the I/O drivers and the network stack IP cores, which will accelerate the design process of the users.

The schematics of the FMC-MCM-1000 are attached with this document in Appendix-B, which provides the details information for using the board for product development.

Users can also purchase the design files (e.g. Gerber file) from SOC, which can be used as a reference for the user PCB once the product is developed. Contact SOC sales (sales@soctechnologies.com) for details.

2.3 Use the FMC-MCM-1000 for Product Development based on the SOC G-SoM

The SOC Generic System-on-Module (FPGA/DSP-SoM-1000 series) module is a small card with 204 edge pins compatible with a DDR3 connector. It is equipped with one FPGA, one DSP, and required memories, which allow users to download their own firmware/software to configure the module according to their own design. Once configured, the module can be used as SoM module for user applications. This saves the time and cost for user product development. Refer to the datasheet of the G-SoM-1000 for further details.

3. Detailed Descriptions

Table-1 lists the components on the FMC-MCM-1000 that are important to the users. Refer to the schematics of the FMC-MCM-1000 for the circuit design and the rest of the components. The schematics of the FMC-MCM-1000 come with the board on delivery.

The following Sections describe the components listed in Table-1. Each Section details the corresponding components and their functions. Refer to the datasheets of the components for further details. The Schematics of the FMC-MCM-1000 in Appendix-B provides the circuit information and the pin connections.

Table-1 Major components on the FMC-MCM-1000

Item	Reference	Part Name	Description	Manufacturer
1	U6	XC6SLX45-2FGG484C	FPGA, Spartan-6, LX150/LX100/LX75/LX45	Xilinx
2	U9	MT41J128M16JT-125:K	DDR3 SDRAM 2GBit	Micron Technology Inc
3	U4	ADV7511KSTZ-P	HDMI Transmitter	Analog Devices Inc
4	U1	ADV7611BSWZ-P	HDMI receiver	Analog Devices Inc
5	U5	88E1111_BAB1C000	Gigabit Ethernet Transceiver, 10/100/1000	Marvell
6	U8	N25Q128A13EF740F	128Mb, Serial Flash Memory	MICRON
7	Y3	ASFL1-27.000MHZ-L-T	OSCILLATOR 27.000 MHZ 3.3V	ABRACON
8	Y4	ASFLMB-100.000MHZ-XY-T	OSCILLATOR MEMS 100.000 MHZ	ABRACON
9	Y1	ABM3-28.6363MHZ-B2-T	CRYSTAL 28.6363MHZ 18PF	Abracon Corporation
10	Y2	ABM8-25.000MHZ-B2-T	CRYSTAL 25.000MHZ 18PF	Abracon Corporation
11	J2	MM80-204B1	CONN 204POS DDR3 SDRAM SODIMM	JAE Electronics
12	J5	ASP-134486-01	FMC Connector, FEMALE, 400POS	Samtec Inc
13	J1	ASP-134488-01	FMC Connector, MALE 400POS	Samtec Inc
14	U7	DS28E01P-100+	1Kb PROTECTED 1-WIRE EEPROM	MAXIM

3.1 FPGA Selection

The SOC product code and the corresponding FPGA on board are listed in *Table-2* below. Refer to the schematics of the FMC-MCM-1000 and Data Sheet of the FPGAs for further details.

Table-2 List of FMC-MCM-1000 Models and corresponding FPGAs

Model Number	FPGA
FMC-MCM-1000-LX150	XC6SLX150-2CSG484C
FMC-MCM-1000-LX100	XC6SLX100-2CSG484C
FMC-MCM-1000-LX75	XC6SLX75-2CSG484C
FMC-MCM-1000-LX45	XC6SLX45-2CSG484C

3.2 DDR3 RAM

The FMC-MCM-1000 is equipped with an off-chip DDR3 RAM of 2Gbit, which can be used for systems that require off-the-chips memories. Refer to the datasheet of MT41J128M16JT-125:K for the specs and used of this memory.

The SOC FMC-MCM-1000 Reference Design provides an example of using this DDR3 RAM.

3.3 HDMI Transmitter

The HDMI Transmitter is the ADV7511KSTZ-P by Analog Devices. Refer to the Datasheet of ADV7511KSTZ-P for details.

SOC provides the configuration file for ADV7511KSTZ-P which is a part of the I/O driver package. For evaluations, the ADV7511KSTZ-P is preconfigured for plug-and-play.

The SOC FMC-MCM-1000 Reference Design provides an example of using ADV7511KSTZ-P.

3.4 HDMI Receiver

The HDMI Receiver is the ADV7611BSWZ-P by Analog Devices. Refer to the Datasheet of ADV7611BSWZ-P for details.

SOC provides the configuration file for ADV7611BSWZ-P which is a part of the I/O driver package. For evaluations, the ADV7611BSWZ-P is preconfigured for plug-and-play.

The SOC FMC-MCM-1000 Reference Design provides an example of using ADV7611BSWZ-P.

3.5 Gigabit Ethernet

The Ethernet PHY is the 88E1111_BAB1C000 by Marvel. It can be used for 10Mbps/100Mbps/1000Mbps. The configuration file is included in the I/O package. An Ethernet MAC core is a part of the Ethernet/UDP/IP network stack which can be licensed. For evaluations, the networks stack is preloaded to allow a plug-and-play system.

The SOC FMC-MCM-1000 Reference Design provides an example of using M88E1111_BAB1C000.

3.6 Serial Flash Memory

The serial flash memory, N25Q128A13EF740F, is used to store the firmware of the FPGA. For evaluation, the I/O drivers and the Ethernet/UDP/IP network stack are pre-stored in the N25Q128A13EF740F. When the FMC-MCM-1000 is booted, the firmware stored in the N25Q128A13EF740F will configure the FPGA and make the board a plug-and-play device for evaluations of the SOC MPEG codec modules.

After the evaluation, users can store their own firmware into the N25Q128A13EF740F for product development. Users can license the I/O driver and the Ethernet/UDP/IP network stack IP core in "netlist" format for product development uses.

The method of downloading the firmware into the N25Q128A13EF740F is detailed in Appendix-C.

4. Ordering Information

The FMC-MCM-1000 can be ordered from SOC directly or through the distributors of SOC. Refer to the SOC web site, www.soctechnologies.com , for distributor locations and contact information.

SOC contacts:
E-mail: sale@soctechnologies.com
Telephone: 1-519-880-8609

Appendix A

Using the FMC-MCM-1000 to Evaluate the SOC Encoder or Decoder Modules

Preloaded Evaluation Cores

SOC provides the FMC-MCM-1000 with a configuration image programmed in the SPI Flash for either Encoder or Decoder evaluation. Upon powering the flash will program the FPGA on the FMC-MCM-1000 in approximately 5 seconds (Spartan6 LX45).

Decoder Evaluation Image

The decoder evaluation image configures the HDMI Output Chip by Analog Devices and configures the Network MAC. SOC has integrated a fully operational UDP/IP stack capable of DHCP. The network core can be configured to 100Mbps or 1Gbps operation. The USB UART is connected to API registers within the system. The API can also be forwarded to the module cards.

Encoder Evaluation Image

The encoder evaluation image configures the HDMI Input and Output Chip by Analog Devices. The Network MAC is configured and SOC has integrated a fully operational UDP/IP stack capable of DHCP within the FPGA. The network core can be configured to 100Mbps or 1Gbps operation. The USB UART is connected to API registers within the system. The API can also be forwarded to the module cards.

Source Code

Source code for the FMC-MCM-1000 is available for purchase, however specific modules may be limited to Encrypted Netlists. SOC also provides a wide range of other IP cores that can be used to speed up product development. For any inquiries please contact sales@soctechnologies.com

SOC API Interface

The API interface is a critical component to properly setting up and running the evaluation platforms. It is used to set up the network stack, read status registers, and customized cores running on the module cards.

Connect a Mini-USB cable from a PC to the FMC-MCM-1000. Open a terminal/serial program and connect to the UART using the following settings:

- baud rate : 115200
- Data Bit: 8
- Parity: None
- Stop bits: 1
- Flow Control: None

On power-up or reset the terminal window will display the prompt shown in Figure A-1.

```
--------------------------------------
|| SOC Technologies UART Interface ||
--------------------------------------

Note: Changing Register Values may cause unintended/unexpected
results. Please make sure you are using the correct register
programming guide for your system.
Remember you may press 'Esc' when asked for a new Data Value
to keep the current setting.

Enter a HEX Address (00-FF) to Modify:
```

Figure A-1. UART Startup Prompt

When entering an address to modify or read, the address must be entered in Hexadecimal. 0X00 – 0xFF. When changing the Data value of the register, the value may be entered in decimal, or it may be entered in hexadecimal by starting the number with an 'h'.

```
Enter a HEX Address (00-FF) to Modify: a4
Current Value(HEX): 000004D2 | New Value(DEC): 100

Enter a HEX Address (00-FF) to Modify: a4
Current Value(HEX): 00000064 | New Value(DEC): hABC

Enter a HEX Address (00-FF) to Modify: a4
Current Value(HEX): 00000ABC | New Value(DEC): |
```

Figure A-2. UART Data Entry

Figure A-2 shows an example of reading and changing register 0xA4. On the first line 0xA4 is entered as the address to read/write. After entering the address the current value of the register is returned (0x4D2=1234). The new value 100 is then written to the register.

In the next line 0xA4 is read again and the new value '100' can be seen in the register. Next a Hexadecimal value of 0xABC is written to the register using 'hABC' to specify ABC as Hexadecimal. The successful write can be seen when reading the register in the third line.

The Module and FMC-MCM-1000 board share the same UART interface. Thus to communicate with the module cards the FMC-MCM-1000 has to forward the UART signals to the module. In the example systems this is toggled by pressing Pushbutton 'S6' and checking the status of LED 'D11'.

LED 'D11' STATUS	MEANING
OFF	Network Stack Running Initialization
Blinking – 1 Second Interval	FMC_MCM_1000 UART Interface Active
Blinking – 3 Second Interval	MCM_1000 UART Interface Active

For more information on API registers that can be read or modified please request the corresponding API register document for your IP Core / Module / Interface Board.

Setting up the Network

The most critical part of setting up the evaluation platform is correctly configuring the network core. When both an Encoder and Decoder platform is purchased the boards will be set up to directly communicate with one another on power up.

Network Speed

The FMC-MCM-1000 is capable of both 100Mbps and 1Gbps operation. Note that the board will negotiate to the fastest available link speed.

The link speed should be known prior to powering on the FPGA. SOC provides a jumper on the PMOD connector (J9) to select the network speed for the logic on power up or reset. This mode must match the link speed for proper operation. Figure A-3 Shows the Power-up configuration mode.

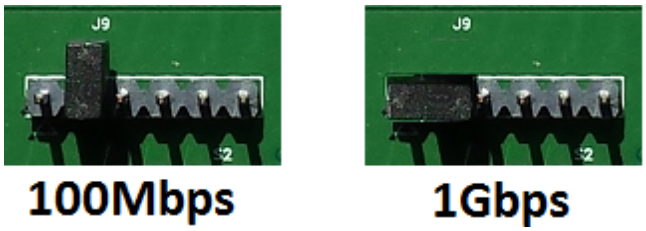

Figure A-3. Network Power-up Configuration

The link speed can also be changed during run-time by changing the API register 0xAF. By writing '1' to 0xAF the network will reconfigure to 100Mbps. By writing '2' to 0xAF the network will reconfigure to 1Gbps operation.

Board IP Address / DHCP

On power-up and the presence of an active network, SOC's network IP core will attempt to obtain an IP address via DHCP. If DHCP is not available the network core will assign itself an initial IP address. The board's IP address can be read via the API register 0xAA. If the board is currently attempting to obtain an IP address via DHCP the boards IP address will not be readable and will return 0xFFFFFFFF via the API when read.

When DHCP is not present the FMC-MCM-1000 will initialize to an IP address such as 192.168.xxx.xxx. This IP address is customizable upon request, and to the discretion of SOC.

At any time the boards IP address may be changed via the API. To change the IP address 4 API registers must be change; one for each byte of the IP.

- 0xAA – First Byte
- 0xAB – Second Byte

- 0xAC – Third Byte
- 0xAD – Fourth Byte

For the IP address to take effect the last byte (register 0xAD) must be written to. Once all bytes have been update the IP address can be read back using register 0xAA to confirm the change is correct.

Network RX

The network is capable of receiving user UDP packets. In the default configuration these packets are only for the Decoder Module. The decoder module expects Transport Stream data transmitted via UDP on port 1234. The network core is capable of receiving UDP packets on all ports from any IP address, however for demo applications the UDP Port is locked to 1234.

Network TX

The network is capable of sending user UDP packets. The default application for network transmission is the Encoder Modules. The default transmission UDP port is 1234, however this can be changed via the API (0xA4). The default Target/Transmission IP can be read from API Register 0xA0. Typically this IP will be 192.168.x.xxx. The target IP is changed in the same way the boards IP address is changed using the following registers:

- 0xA0 – First Byte
- 0xA1 – Second Byte
- 0xA2 – Third Byte
- 0xA3 – Fourth Byte

The target address is readable using any of the above registers. The target computer or device must be capable of sending IP ARP replies to be connectable. The determine if the target IP is reachable bit 10 of register 0xAF can be check. When it is '1' the target can be reached. When '0' the target has not responded or can not be found.

Sending / Receiving Transport Streams

Receiving Transport Streams (Encoder)

Encoder modules are capable of sending transport stream via UDP. Once the Network stack has been configured correctly, the target IP has been discovered, and the Encoder has a valid input (Video), the transport stream will be transmitted.

To receive the transport stream SOC suggests two possible methods, however others are possible as well.

VLC Media Player

The simplest Method for playing the received transport stream is via VLC media player.

- Open VLC media player
- Media → Open Network Stream
- Enter the following the field 'udp://@:1234'
- Click Play

If the board is set up properly VLC will begin playing the transport stream.

SOC's UDP Receiver

SOC's UDP receiver is capable of receiving UDP data on any specified port. By default the receiver will save the file as a transport stream file (.ts). Once the receiver is closed the file may be played back using many populate media players such as VLC. The UDP receiver is a single Windows executable (.exe) file which is launched via a batch (.bat) file. The receiving port may be changed by editing the .bat file, simply change the number after '-p' to the desired port.

Note that SOC does not provide the UDP receiver with the FMC-MCM-1000. It is intended for more advanced application/debugging and must be requested. Contact support@soctechnologies.com

Sending Transport Streams (Decoder)

SOC Suggest only one method for sending Transport stream files to the FMC-MCM-1000 running a Decoder Module. Upon request SOC will provide a TS_Sender program. This simple program sends the Transport Stream file to the FMC-MCM-1000.

To set up the TS_Sender edit and save the Batch file so that the IP address and Port match the configuration of the FMC-MCM-1000.

To use simply drag the '.ts' file onto the batch file of the program. If the settings are configured and the board is properly connected a window showing the status of the transport stream transmission will look similar to Figure A-4. If the IP address is not reachable the 'Sent Present', 'Sent Size', and 'Stream time' will remain at 0. If this occurs please check the network configuration.

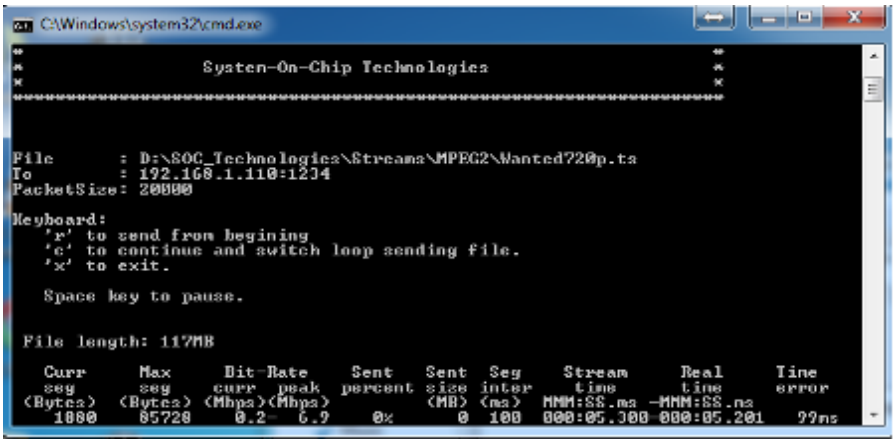

Figure A-4. TS Sending Status Window

Additional Resources

- SOC API H264 Encoder Register MAP
- SOC API MPEG2 Encoder Register MAP
- SOC API H264 Decoder Register MAP
- SOC API MPEG2 Decoder Register MAP
- SOC API Network UDP/IP Register MAP

Appendix B – FMC-MCM-1000 Schematics

This Appendix will come within the FMC-MCM-1000 package shipped to customers.

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