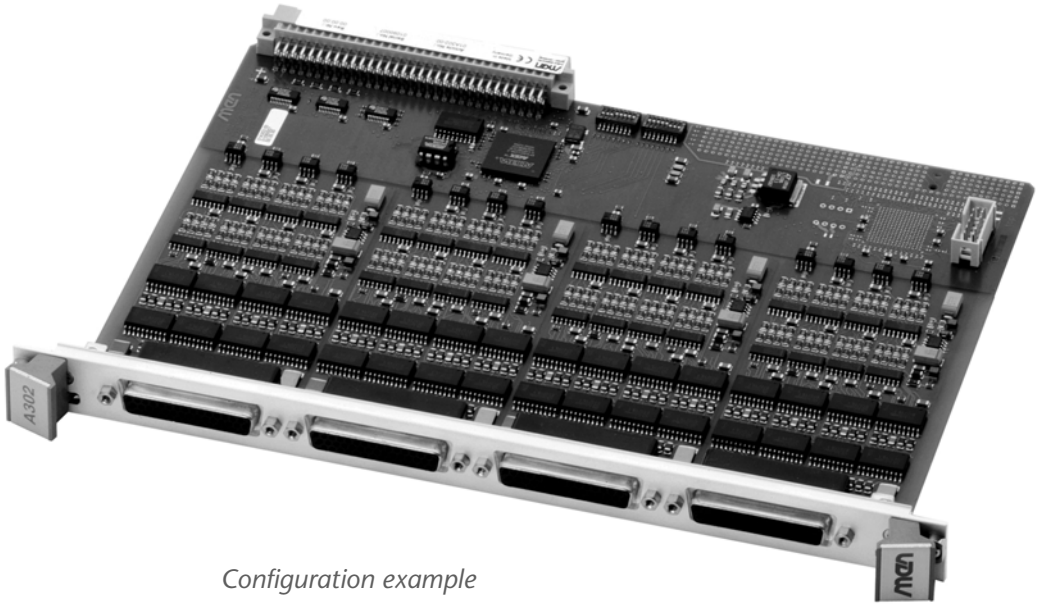
Embedded Solutions

A302 – 6U VMEbus Card with 128 Binary I/Os



Configuration example

User Manual

mikro elektronik
gmbh · nürnberg

A302 – 6U VMEbus Card with 128 Binary I/Os

The A302 is an input/output VMEbus target board for 128 binary process signals. The I/Os are divided into four optically isolated units. The card is used for input/ output of digital signals with different voltage levels and ground references. For each unit 32 channels are driven to a 44-pin D-Sub connector. Each channel can be either input or output.

The binary inputs/outputs can be universally used in industrial systems. They are optically isolated from the system, which is essential for advanced automotive and industrial applications.

Technical Data

Binary I/Os

- 128 binary signals
  - 4 optically isolated units
  - 32 channels for each unit
- Individual use of each channel as input or output
- Individual edge-triggered interrupts
- Input/output load on ground
- High-side output switches
- High output current
  - Max. 1.9A per channel
  - Max. 16A per unit
- Over-current and over-temperature protection

Output Characteristics

- Output voltage range: 12V..32V
- Output current log. 0: max. 10mA
- Output current log. 1: max. 1.9A
- Switching time for output change: < 200µs
- Isolation voltage (optocoupler): 500V DC

Input Characteristics

- Input voltage min.: 0V
- Input voltage max. external supply voltage (12..32V)
- Voltage level log. 0: 0V..6V or open
- Voltage level log. 1: 12V..32V
- Input current log. 1: 2.03mA @ 24V
- Switching threshold: 9.2V @ 0.78mA typ.
- Switching time for input change: min. 33µs, max. 44µs
- Excess voltage protection: max. +47V

Peripheral Connections

- Via front panel on four shielded 44-pin HD-Sub receptacle connectors

VMEbus

- Only one slot required on the VMEbus
- A24/A16/D16/D08(EO) slave
- D08(O) interrupter

Electrical Specifications

- Isolation voltage
  - 500V DC between isolated side and digital side
  - 180V DC between the channels
  - Voltage between the connector shield and isolated ground is limited to 180V using a varistor; AC coupling between connector shield and isolated ground through 47nF capacitor
- Supply voltage/power consumption:
  - +5V (4.85V..5.25V), 106mA
  - +3.3V (3.0V..3.6V), 27mA
  - +24V (external supply voltage 12..32V), 78mA (total for all units)

Mechanical Specifications

- Dimensions: standard double Eurocard, 233.3mm x 160mm
- Weight: 280g

Environmental Specifications

- Temperature range (operation):
  - 0..+60°C or -40..+85°C
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity range (operation): max. 95% without condensation
- Relative humidity range (storage): max. 95% without condensation
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

MTBF

- MTBF: 98,000h @ 50°C (derived from MIL-HDBK-217F)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

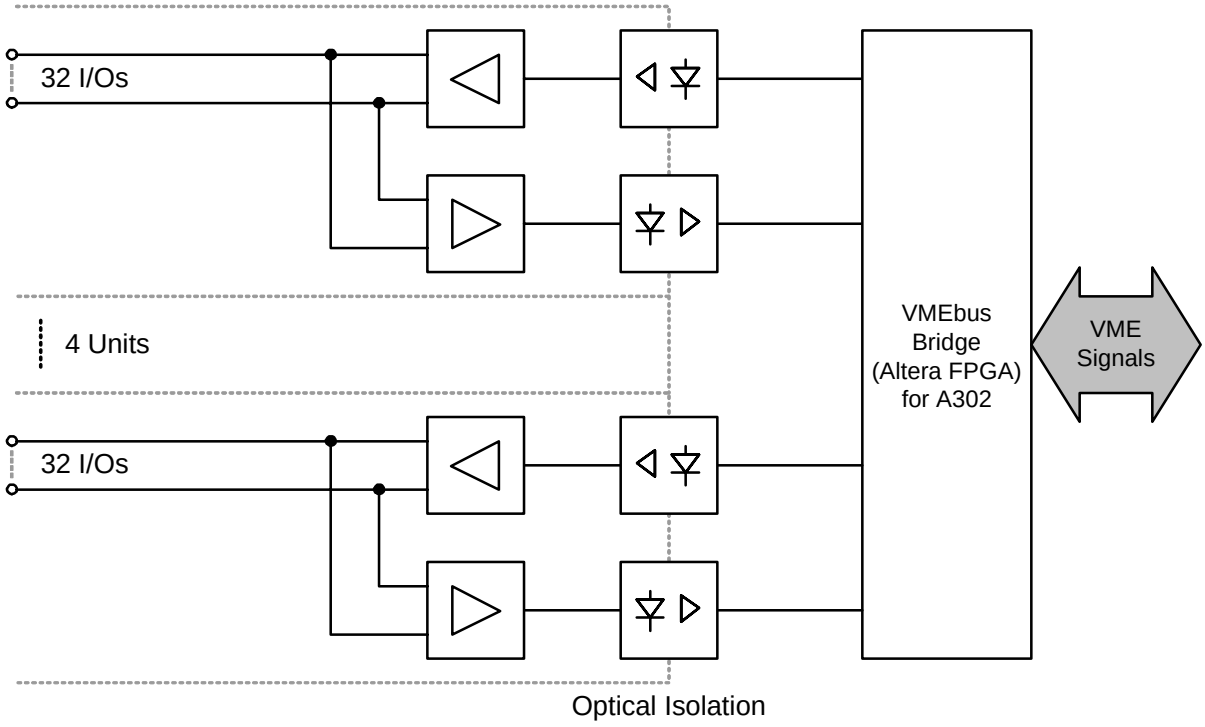
EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst) with regard to CE conformity

Software Support

- MEN Driver Interface System (MDIS™ for Windows®, Linux, VxWorks®, QNX®, OS-9®)
- For more information on supported operating system versions and drivers see online data sheet.

Block Diagram



Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Edition	Comments	Technical Content	Date of Issue
E1	First edition	Michael Himmler, Thomas Eckert	2002-02-08
E2	Updated technical data section Corrected information in Chapter 3.7.2 Interrupter on page 23 Modified Figure 1, Map of the board - top view, on page 13 (removed elements of the similar D302; the original image was used in both user manuals)	T. Eckert	2008-07-22

Conventions

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ# /IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous edition of the document.

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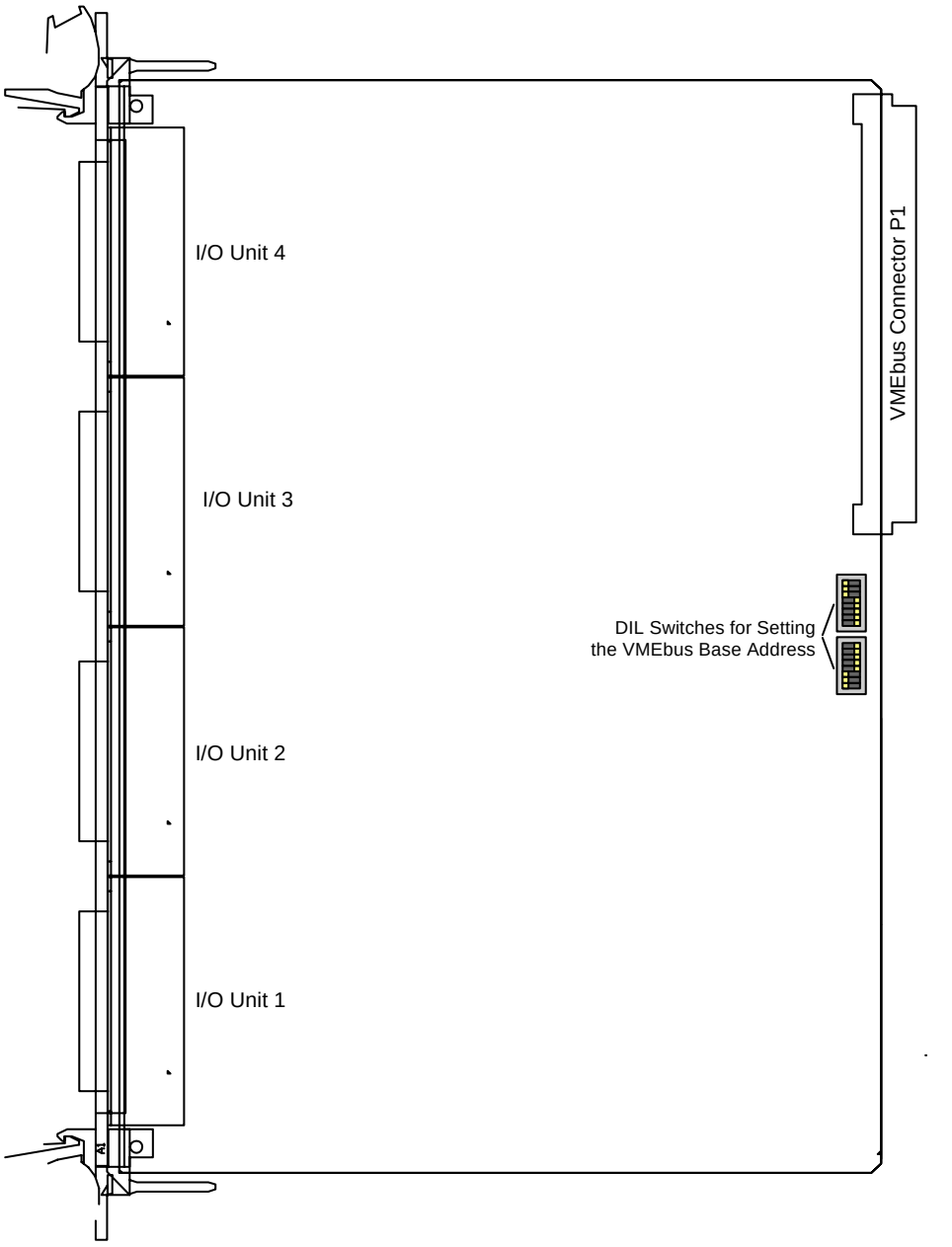
1 Getting Started

This chapter will give an overview of the board and some hints for first installation in a system as a "check list".

1.1 Map of the Board

Figure 1. *Map of the board - top view*



1.2 Integrating the Board into a System

You can use the following "check list" to install the I/O board in a system for the first time and to test proper functioning of the board.

The A302 has an A24/D16 or A16/D16 VMEbus slave interface. This interface only requires the board's upper 96-pin connector (P1) on the board. The A302 has no P2 connector, so that peripherals can only be connected via the front panel.

If it is required for the board to issue an interrupt via the bus, then the daisy chain must be established through to the A302.

- ☑ Power-down the system.
- ☑ The board is set for A24 accesses, the base address being 0xE00000. This base address is set using DIL switches. It may be necessary to set it to an address with which the master can access the board in A24/D16 mode.
  (If you have to change the base address, please refer to Chapter 3.7.1.1 Setting the Base Address on page 21.)
- ☑ Insert the A302 into your VMEbus system, making sure that the VMEbus connectors are properly aligned.
- ☑ Power-up the system.
- ☑ After power-up, load a suitable debugger.
- ☑ First, attempt to perform a read-word access to the base address plus 0x100, (i.e. 0xE00100 if the base address was not altered).
  With 32-bit masters it may be necessary to load a register on the master board to set the access mode. In any case you should be aware of the contents of the high-order byte of the 32-bit address. For instance, access may require using address 0xFFE00100 or 0xFCE00100 or any other address (depends on the master board).
- ☑ If a bus error occurs while you are attempting to read, check if the base address is set correctly and whether it is possible for the master to access the VMEbus at all at the selected address and using the correct mode. Then try again.
- ☑ Now attempt to perform a word access to the base address plus 0x102. Again, no bus error should occur. Write accesses to this memory location should be successful for the right half of the word. For instance, if 0x55 is written to the register it should be possible to read 0x*xx*55.

1.3 Installing Driver Software

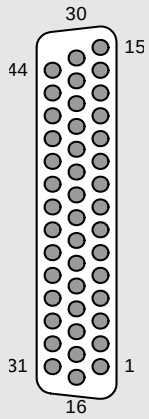
For a detailed description on how to install driver software please refer to the M66 software user manual.

2 Connecting the Board

2.1 Peripheral Interfaces

Peripherals can be connected via four 44-pin HD-Sub connectors at the front panel.

Table 1. *Pin assignment of the 44-pin HD-Sub connectors*



		30	I+24V	15	I+24V
44	IO32	29	IO30	14	IO31
43	IO29	28	IO27	13	IO28
42	IO26	27	IGND	12	IO25
41	I+24V	26	IO24	11	I+24V
40	IO23	25	IO21	10	IO22
39	IO20	24	IO18	9	IO19
38	IO17	23	I+24V	8	IGND
37	I+24V	22	IO15	7	IO16
36	IO14	21	IO12	6	IO13
35	IO11	20	IO9	5	IO10
34	IGND	19	I+24V	4	I+24V
33	IO8	18	IO6	3	IO7
32	IO5	17	IO3	2	IO4
31	IO2	16	IGND	1	IO1

Connector types:

- 44-pin high-density D-Sub receptacle (similar to DIN41652/MIL-C-24308), with thread bolt UNC 4-40
- mating connector:
  44-pin high-density D-Sub plug (similar to DIN41652/MIL-C-24308) available e.g. for hand-soldering connection or crimp connection

Table 2. *Signal mnemonics of peripheral connectors*

Signal	Direction	Function
I+24V	-	external supply voltage (see also Chapter 3.3 Inputs on page 17)
IGND	-	isolated ground
IO1..IO32	in/out	input/output channels 1 to 32

3 Functional Description

3.1 Power Supply

The board is supplied with +5V via the VMEbus bus.

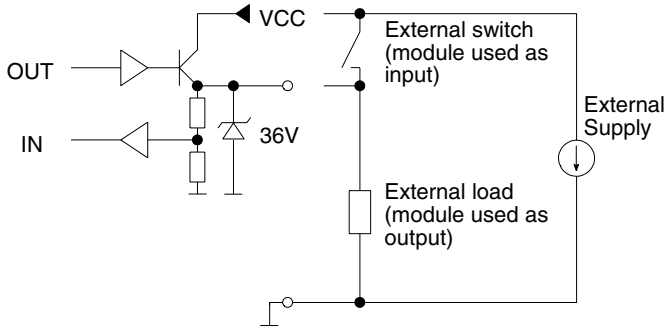
Voltage supply from an external source is +12V..32V at approx. 20mA for each unit. If you do not use all four units, you do not need to supply the unused unit(s) with power.

The external supply voltages are designated I+24V/IGND and must be connected via the peripheral connectors.

3.2 Principle of Operation

Input and output data is transmitted via a serial interface between the controller chip on the host side and the optically isolated part of each of the four I/O units. Data transmission is simultaneous for input and output information. The transfer time for all 32 bits of one unit is 32µs.

Figure 2. *I/O stage*



A monitoring circuit guarantees that no output driver is activated if an external supply but no supply to the respective I/O unit is applied. If an interrupt is triggered for an I/O unit, the circuit also guarantees that all outputs are passive.

3.3 Inputs

The inputs are voltage-sensitive. The nominal switching point is at approx. 8V. The input current is a nominal 2mA at 24V.

The input signals are serially transferred to the digital isolated binary-I/O controller.

The binary-I/O controller checks the input signal state three times in intervals of 32µs. Only if the signal is stable for this period of 120µs will the I/O controller update input bit *IN* in the corresponding data Input/Output Register. The circuit is known as a digital "debouncer".

You must never supply the board "backwards", i.e. the voltage at the input must never exceed the external supply voltage. This may destroy the board. In the ideal case the external supply voltage should be directly connected with the supply of the external device connected.

3.4 Outputs

Eight 4-channel source drivers are used as output drivers. The device is over-current protected and includes thermal shutdown and output transient protection/clamp diodes.

Under normal operating conditions, each of eight outputs will source in excess of 1.9A continuously at an ambient temperature of 25°C and a supply of 35V. The over-current fault circuit will protect the device from short-circuits to ground with supply voltages of up to 35V.

3.5 Input/Output Registers

The board has four Binary Input/Output Controllers (BIOCs)—one per unit. This controls the inputs and outputs on a channel basis. For each channel there is one register—32 registers per unit, 128 registers per board—, which stores the desired value and the actual value. Edge detection and interrupt masking are also handled by this 6-bit register.

One bit of the input/output register is used to specify the state of the power switch. If this bit is 0, then the switch is open. The I/O pin can now be used as an input. If the bit is 1, the switch is closed. In this case, output voltage is applied to the I/O pin. The real output state of the switch can also be read from the same register. Because of the serial transmission, it may take up to 40µs for the switch to assume the desired value. It takes another 120µs before the confirmation is returned, because of the debounce logic. Two bits are used to indicate that the output has changed—from on to off or vice versa. If one of the bits is set, it can be reset by software to be able to detect a new edge. Each of these edges can trigger an interrupt if the corresponding interrupt-enable bit is set.

Data Input/Output Registers (0x000..0x03E) (r/w)

15..8	7..6	5	4	3	2	1	0
-	-	E2	E1	IN	IE2	IE1	OUT

E2 falling edge occurred
0 = no edge
1 = edge occurred

E1 rising edge occurred
0 = no edge
1 = edge occurred

IN value of the I/O pin (read only)

IE2 interrupt enable, falling edge
0 = disable
1 = enable

IE1 interrupt enable, rising edge
0 = disable
1 = enable

OUT output switch
0 = open (used in input mode)
1 = closed (output, switched to supply voltage)

3.6 Interrupts

3.6.1 Configuring Interrupts

If an interrupt occurs, the number of the channel (5 bits) that triggered the interrupt is stored in the Interrupt Register. There are four Interrupt Registers—one per unit.

Interrupt Register (0x0FE) (read only)

15..8	7..6	5..1	0
-	-	CHNL	-

CHNL channel number
0 0 0 0 0 = channel 1
.. ..
1 1 1 1 1 = channel 32

Control Register (0x100) (read/write)

15..6	5	4	3	2..0
-	RES	IRE	IRAC	L

RES reserved, no function

IRE interrupt enable
This bit must be 1 to allow an interrupt to be generated at all. If this bit is 0, no interrupt is triggered on the VMEbus—even though an interrupt from the I/O unit is pending.
0 = disable
1 = enable

IRAC interrupt auto clear
If this bit is 1, the *IRE* bit is cleared during an IACK cycle (in response to this interrupt request) which disables the interrupt. In order to enable the interrupt again, the *IRE* bit must be set again by writing to the Control Register.

L interrupt level
These bits select the line on which the interrupt request is to be generated.
0 0 0 = disable interrupt generation
0 0 1 = generate interrupt request on line /IRQ1
0 1 0 = generate interrupt request on line /IRQ2
0 1 1 = generate interrupt request on line /IRQ3
1 0 0 = generate interrupt request on line /IRQ4
1 0 1 = generate interrupt request on line /IRQ5
1 1 0 = generate interrupt request on line /IRQ6
1 1 1 = generate interrupt request on line /IRQ7

Vector Register (0x102) (read/write)

15..8	7..0
-	*Interrupt Vector*

3.6.2 Interrupt Handling

If an interrupt source is enabled by setting the interrupt-enable bit (*IEx*) in the Data Input/Output Register and if a corresponding edge occurs on the input channel so that the corresponding edge bit is set, then an interrupt is internally triggered. This causes the corresponding interrupt-enable bit in the Data Input/Output Register to be reset. The Interrupt Register indicates the channel that caused the interrupt. Whether the trigger was a rising or falling edge can be ascertained from the appropriate Data Input/Output Register.

If several edges capable of triggering an interrupt occur simultaneously, the first edge detected generates an interrupt. The corresponding edge bit is set for the appropriate edges.

See also Chapter 3.7.2 Interrupter on page 23.

3.7 VMEbus Interface

The A302 has a VMEbus slave interface. It is implemented using an ACEX PLD. The ACEX is loaded and initialized after power-on.

The VMEbus register mapping is 100% compatible to MEN's A201S board.

3.7.1 Slave Interface

The A302 board is equipped with an A16/A24/D16 slave interface, i.e, only cycles with standard (24-bit) addresses and short (16-bit) address range are supported. For accesses from the VMEbus, the slave recognizes this type of cycle on the basis of the address modifier lines. The data bus interface of the A302 complies with the D16 specification. The A302 will operate with masters which support so-called "address pipelining". /DTACK is generated 120ns after /AS at the earliest. The maximum access time is limited to 10µs.

3.7.1.1 Setting the Base Address

The A302 occupies an area of 0x800 in the address space. Identical quarters of this—i.e. 0x200–are reserved for each I/O unit together with the interrupt handler.

The base address of the A302 can be varied in increments of 0x800 within the whole A16 or A24 address range. It is set using DIL switches. There is one switch for each address bit from A11 to A23. If the switch is "on", the corresponding address bit is compared with 0. If the switch is "off", it is compared with 1. If the address is the same as the switch setting (taking address modifiers into account), a "select" signal for the board is generated. In the short address range, the switches corresponding to A16 to A23 are ignored.

The selection between short address range and standard address range is made by the SRT switch. If SRT is switched on, short accesses are possible; if SRT is switched off, standard accesses are allowed.

Figure 3. *Setting the base address - Default (A24)*

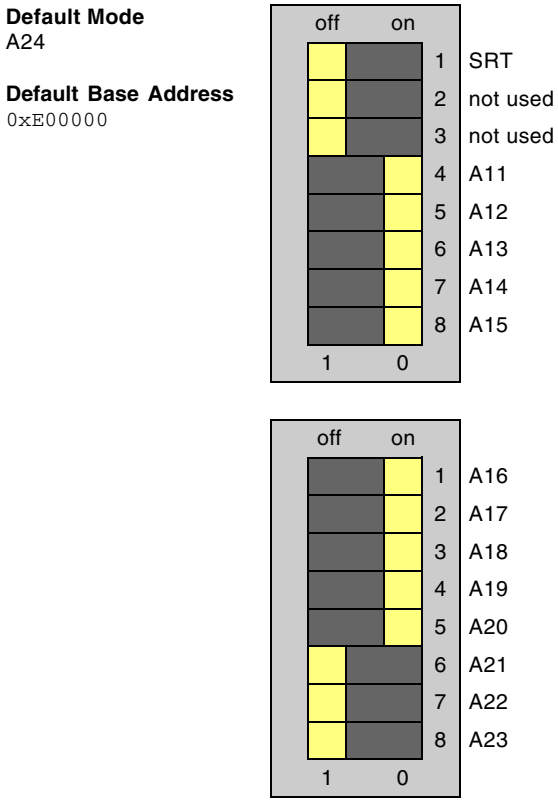
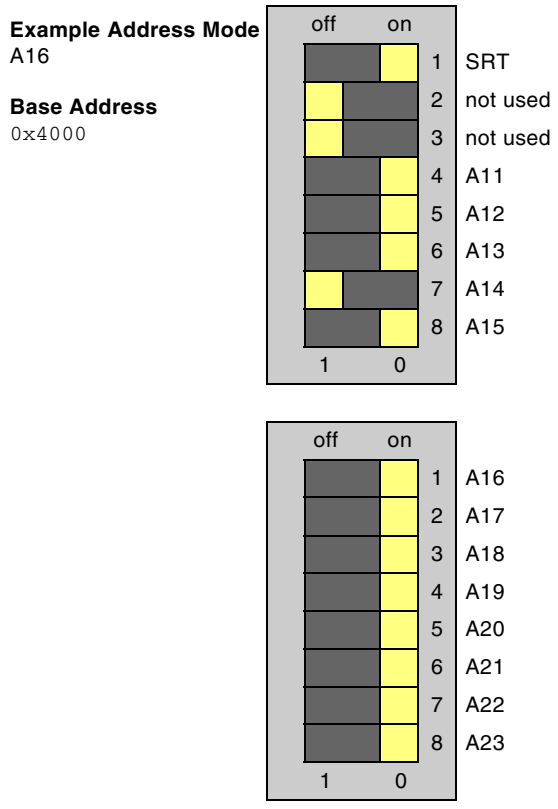


Figure 4. *Setting the base address - Example (A16)*



3.7.1.2 Address Modifiers

The VMEbus has 6 "address modifier" lines. These lines allow the master to transfer additional binary information to the slave during a data transfer cycle. The lines are used to divide the address space of the VMEbus into several classes. The following codes are permitted for the A302:

Table 3. *Address modifier codes permitted on A302*

HEX Code	AM 5	AM 4	AM 3	AM 1	AM 0	Function	SRT
3d, 39	H	H	H	L	H	Standard supervisory and non-privileged data access	off
2d, 29	H	L	H	L	H	Short supervisory and non-privileged data access	on

As mentioned above, SRT specifies standard or short access. The factory setting allows supervisor-mode and nonprivileged-mode access. Other address modes are possible in principle. They are specified in a programmable ACEX component.

3.7.2 Interrupter

The interrupter has been implemented using the ACEX PLD. This chip permits interrupts to be issued at a programmable level independently for each I/O unit. The A302 is a D08(O) interrupter. This means that the interrupter outputs status information on D0..D7 during an interrupt acknowledge cycle. The interrupt is a RORA (= Release On Register Access) interrupt, i.e., the interrupt request is reset by access to a specific register.

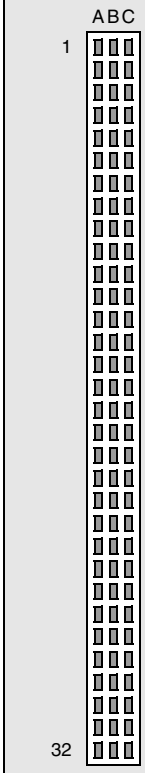
Since the interrupter is fully programmable, it is not necessary to set any jumpers or DIL switches.

3.7.3 VMEbus Connector P1

Connector types:

- 96-pin type-C plug connector according to DIN41612/MIL-C-55302/IEC603-2
- mating connector:
  type-C 96-pin receptacle according to DIN41612/MIL-C-55302/IEC603-2, available with solder/wire-wrap pins, for hand-soldering connection or for insulation piercing connection (IDC)

Table 4. *Pin assignment of the 96-pin VMEbus P1 connector*



A	B	C
D0	-	D8
D1	-	D9
D2	-	D10
D3	-	D11
D4	-	D12
D5	-	D13
D6	-	D14
D7	-	D15
GND	-	GND
SYSCLK	-	-
GND	-	-
/DS1	-	/SYSRST
/DS0	-	/LWORD
/WRITE	-	AM5
GND	-	A23
/DTACK	AM0	A22
GND	AM1	A21
/AS	AM2	A20
GND	AM3	A19
/IACK	GND	A18
/IACKIN	-	A17
/IACKOUT	-	A16
AM4	GND	A15
A7	/IRQ7	A14
A6	/IRQ6	A13
A5	/IRQ5	A12
A4	/IRQ4	A11
A3	/IRQ3	A10
A2	/IRQ2	A9
A1	/IRQ1	A8
-12V	-	+12V
+5V	+5V	+5V

4 Organization of the Board

4.1 Local Address Map

The board's local I/O and control registers occupy an address space of 0x800 bytes. These 0x800 bytes are divided into four identical parts. Each of these 512-byte part is assigned to one I/O unit.

The address map looks like an M-Module carrier board assembled with four M66 M-Modules, forming the four I/O units of the board:

Table 5. *Local address map*

Offset Address	Unit
0x000	Unit 0
0x200	Unit 1
0x400	Unit 2
0x600	Unit 3

Every I/O unit's address space contains the following register set:

Table 6. *Local address map for one I/O unit*

Offset Address	D15..D8	D7..D0
0x000	-	Input/Output Register for I/O line IO1 (r/w)
0x002	-	Input/Output Register for I/O line IO2 (r/w)
0x004	-	Input/Output Register for I/O line IO3 (r/w)
0x006	-	Input/Output Register for I/O line IO4 (r/w)
0x008	-	Input/Output Register for I/O line IO5 (r/w)
0x00A	-	Input/Output Register for I/O line IO6 (r/w)
0x00C	-	Input/Output Register for I/O line IO7 (r/w)
0x00E	-	Input/Output Register for I/O line IO8 (r/w)
. . .	-	...
0x03E	-	Input/Output Register for I/O line IO32 (r/w)
0x0FC	-	I/O unit's Magic Word (0x5346) (r)
0x0FE	-	Interrupt Register (r)
0x100	-	Control Register (r/w) (A302, A201S-compatible)
0x102	-	Vector Register (r/w) (A302, A201S-compatible)
0x104..0x106	-	reserved

All local registers of the board can be accessed using the VMEbus base address as the Local Base Address:

$$LocalBaseAddress = VMEBaseAddress + UnitNo \cdot 0x200$$

5 Appendix

5.1 Literature and Web Resources

- A302 data sheet with up-to-date information and documentation:
  www.men.de
- VMEbus General:
  - The VMEbus Specification, 1989
  - The VMEbus Handbook, Wade D.Peterson, 1989

  VMEbus International Trade Association
  www.vita.com

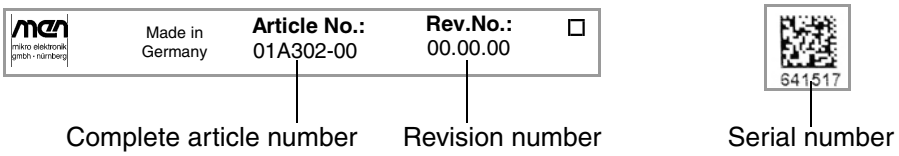
5.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the A302. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 5. *Labels giving the board's article number, revision and serial number*



You can request the circuit diagrams for the current revision of the product described in this manual by completely filling out and signing the following non-disclosure agreement.

Please send the agreement to MEN by mail. We will send you the circuit diagrams along with a copy of the completely signed agreement by return mail.

MEN reserves the right to refuse sending of confidential information for any reason that MEN may consider substantial.

Non-Disclosure Agreement

for Circuit Diagrams provided by MEN Mikro Elektronik GmbH

between

MEN Mikro Elektronik GmbH
Neuwieder Straße 5-7
D-90411 Nürnberg

("**MEN**")

and

_____
_____
_____
_____

("**Recipient**")

We confirm the following Agreement:

MEN		**Recipient**	
Date:	_____	Date:	_____
Name:	_____	Name:	_____
Function:	_____	Function:	_____

Signature: _____

Signature: _____

The following Agreement is valid as of the date of the MEN signature.

MEN Mikro Elektronik GmbH

Neuwieder Straße 5-7
90411 Nürnberg
Deutschland

Tel. +49-911-99 33 5-0
Fax +49-911-99 33 5-901

E-Mail info@men.de
www.men.de

1 Subject

The subject of this Agreement is to protect all information contained in the circuit diagrams of the following product:

Article Number: _____ [filled out by recipient]

MEN provides the recipient with the circuit diagrams requested through this Agreement only for information.

2 Responsibilities of MEN

Information in the circuit diagrams has been carefully checked and is believed to be accurate as of the date of release; however, no responsibility is assumed for inaccuracies. MEN will not be liable for any consequential or incidental damages arising from reliance on the accuracy of the circuit diagrams. The information contained therein is subject to change without notice.

3 Responsibilities of Recipient

The recipient, obtaining confidential information from MEN because of this Agreement, is obliged to protect this information.

The recipient will not pass on the circuit diagrams or parts thereof to third parties, neither to individuals nor to companies or other organizations, without the written permission by MEN. The circuit diagrams may only be passed to employees who need to know their content. The recipient protects the confidential information obtained through the circuit diagrams in the same way as he protects his own confidential information of the same kind.

4 Violation of Agreement

The recipient is liable for any damage arising from violation of one or several sections of this Agreement. MEN has a right to claim damages amounting to the damage caused, at least to €100,000.

5 Other Agreements

MEN reserves the right to pass on its circuit diagrams to other business relations to the extent permitted by the Agreement.

Neither MEN nor the recipient acquire licenses for the right of lectual possession of the other party because of this Agreement.

This Agreement does not result in any obligation of the parties to purchase services or products from the other party.

6 Validity of Agreement

The period after which MEN agrees not to assert claims against the recipient with respect to the confidential information disclosed under this Agreement shall be _____ months [filled out by MEN]. (Not less than twenty-four (24) nor more than sixty (60) months.)

7 General

If any provision of this Agreement is held to be invalid, such decision shall not affect the validity of the remaining provisions and such provision shall be reformed to and only to the extent necessary to make it effective and legal.

This Agreement is only effective if signed by both parties.

Amendments to this Agreement can be adopted only in writing. There are no supplementary oral agreements.

This Agreement shall be governed by German Law.

The court of jurisdiction shall be Nuremberg.

MEN Mikro Elektronik GmbH

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90411 Nürnberg
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