USER MANUAL

Accessory 34DD

64-Bit OPTO I/O Interface Board (20 in 12 out)

4Ax-603433-xUxx

October 16, 2003

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Table of Contents

INTRODUCTION **1**

CONNECTORS **3**
J2 - 34D 3
J2 - 34DD 3
J3 - 34D 3
J3 - 34DD 3
J4A (JTHW) 3
J4B 3
TB1 - pins 1 & 2 3
TB1 - pins 3 & 4 3

MULTIPLEX ADDRESS MAP **5**
SW1 DIP Switch Setting 5
M-Variable Assignments 6

PROCESSING ACC-34DX INPUTS & OUTPUTS **7**
When to Access ACC-34Dx 7
Image Word Variables 7
Location of Image Words 7
Preventing Conflicts in Output Image Words 8
Example 9

POWER SUPPLY AND OPTO-ISOLATION CONSIDERATIONS **11**

WATCHDOG TIMER (ROLE OF JUMPER E2) **13**

BOARD LAYOUT AND CONNECTOR PINOUTS **15**
ACC-34D and ACC-34DD Board Layout 15
ACC-34D - J2 (50 Pin Header) 16
ACC-34D – J3 (50 Pin Header) 17
ACC-34D – J3 (50 Pin Header) 18
ACC-34DD - J2 (50 Pin Header) 18
J4A & J4B (26-PIN Header) 20
TB1 (4-pin Terminal Block) 21

SCHEMATICS **23**

INTRODUCTION

PMAC's Accessory 34D (ACC-34D) and Accessory 34DD (ACC-34DD) are discrete input/output (I/O) boards designed for easy connection to Opto-22 and compatible mounting racks. The board interfaces with several third party opto modules (e.g. Opto-22 Models G4PB32, 70GRQ432 and all PB8, 16, and 24 boards) via standard 50-pin flat cables (see ACC-21 cables). In addition to the third party I/O boards the ACC-34DD interfaces directly to the I/O Pack board (Delta Tau part number 603052). ACC-34 D and DD provide 32 lines of optically isolated inputs and 32 lines of optically isolated outputs. Both the inputs and the outputs are TTL compatible negative logic (low true) types. The actual I/O Reads and Writes are carried out using a special form of M-variables which will be described later.

The ACC-34D differs from the ACC-34DD in only one aspect, the input and output layout on the connectors J2 and J3. The D has 32 inputs on connector J2, while the DD has 20 inputs and 12 outputs. The D has 32 outputs on J3, while the DD has 12 inputs and 20 outputs. If the application only requires 1 I/O board or the I/O boards being used are the I/O Pack (Delta Tau #603052) then the ACC-34DD should be used, otherwise the ACC-34D should be used.

From this point on this document will refer to the ACC-34D and the ACC-34DD as ACC-34DDX when they could be used interchangeably.

ACC-34DDX is part of a series of I/O accessories for PMAC that use the JTHW connector. Others are:

- **ACC-34A** The Opto 32 Bit Input/32 Bit Output board
- **ACC-34B** The Opto 32 Bit Input/32 Bit Output board
- **ACC-34C** The Opto 64 Bit Input/32 Bit Output board
- **ACC-18** The Thumbwheel Multiplexer board
- **ACC-8D-Opt.7** The Resolver to Digital Converter board
- **ACC-8D-Opt.8** The Absolute Encoder Interface board

All of the above accessories use the JTHW multiplex address scheme and several of them may be daisy-chained to a single PMAC. In addition for enhanced noise reduction and long distance installation, accessories 35A and 35B provide differential buffer capability for the JTHW signals. The use of the long distance buffer pair (ACC-35A and ACC-35B) is recommended whenever the required cable length between PMAC and ACC-34Dx is beyond 3 meters (10 feet).

Up to 32 ACC-34Dxs may be connected to a single PMAC, giving the possible total number of 1024 input and 1024 output lines in addition to those available on the PMAC board and those available on the parallel I/O expansion board(s) (ACC-14). Accessory 34Dx communicates to PMAC via its JTHW connector through the supplied flat cable. In situations where the I/O modules are a long distance away from PMAC, ACC-35A & ACC-35B may be used as local and remote buffers between PMAC and ACC-34Dx.

ACC-34Dx also supports a local watchdog timer feature independent of that of PMAC's. The mode of operation of this function is explained at the end of this manual (see also the enclosed schematic).

CONNECTORS

Please refer to the layout diagram of ACC-34Dx for the location of the connectors on the board. A pin definition listing for each connector is provided at the end of this Manual.

J2 - 34D

This is a 50-pin header which provides the connection for the input lines numbered 0 to 31. In addition, this connector has a 5 volt (maximum 0.5 A) power supply outlet is provided for external logic circuits.

J2 - 34DD

This is a 50-pin header which provides the connection for the input lines numbered 0 to 11, 24 to 31 and output lines numbered 0 to 11. In addition, this connector has a 5V (maximum 0.5 A) power supply outlet is provided for external logic circuits.

J3 - 34D

This is a 50-pin header which provides the connection for the output lines numbered 0 to 31. In addition, this connector has a 5V (maximum 0.5 A) power supply outlet is provided for external logic circuits.

J3 - 34DD

This is a 50-pin header which provides the connection for the output lines numbered 12 to 31 and input lines numbered 12 to 23. In addition, this connector has a 5V (maximum 0.5 A) power supply outlet is provided for external logic circuits.

J4A (JTHW)

This is a 26-pin header which provides the link between PMAC's JTHW (J3) and this board. Using the supplied flat cable PMAC's J3 should be connected to J4A. Through this connector PMAC sets the outputs and reads the inputs. In addition, the power for the processor side of the opto-isolation circuitry is provided from the PMAC board through this connector.

J4B

This is a 26-pin header which brings out the JTHW signals for the next accessory board on the JTHW multiplex memory map. This connector is pin-to-pin compatible with J4A.

TB1 - pins 1 & 2

Terminal block through which a 5V power supply may be brought in for the optically isolated side of the digital circuitry on ACC-34Dx (50 mA is required). Remove jumper E1 if the power is supplied to the board via TB1 - pins 1 & 2. Note that with jumper E1 is installed, whenever a 12 to 24V supply is brought in from TB1 - pins 3 & 4, then TB1 - pins 1 & 2 can be used as a 5-volt power source for the logic circuits on the external opto boards (see the enclosed schematic).

TB1 - pins 3 & 4

Terminal block through which a 12 to 24V unregulated power supply may be brought for the optically isolated side of the digital circuitry on ACC-34Dx. The voltage is reduced to 5V via the on board regulator. Install jumper E1 if the required power is supplied via TB1 - pins 3 & 4. Do not supply power through both 1 & 2 and 3 & 4.

MULTIPLEX ADDRESS MAP

Each ACC-34Dx occupies eight bytes of address space on the PMAC JTHW MULTIPLEX memory space. This memory space is 8-bit wide, providing the ability to daisy-chain 32 (256/8) ACC-34Dxs together (or a combination of ACC-34Dxs, ACC-34As, ACC-18s and ACC-8D OPT7s). The 5-bit DIP switch, SW1, determines the address of each ACC-34D board on the allocated memory space. Port A, the input port, occupies the base address (i.e. bytes 0, 8, 16 etc.) and Port B, the output port, occupies the base address plus 4 (i.e. bytes 4, 12, 20 etc.). The table below shows how SW1 should be set for one or more ACC-34D boards connected to the same PMAC.

SW1 DIP Switch Setting

Board #	Byte #	SW1 DIP Switch Setting				
	Port A & Port B	**5**	**4**	**3**	**2**	**1**
#1	0 & 4	ON	ON	ON	ON	ON
#2	8 & 12	ON	ON	ON	ON	OFF
#3	16 & 20	ON	ON	ON	OFF	ON
#4	24 & 28	ON	ON	ON	OFF	OFF
#5	32 & 36	ON	ON	OFF	ON	ON
#6	40 & 44	ON	ON	OFF	ON	OFF
#7	48 & 52	ON	ON	OFF	OFF	ON
#8	56 & 60	ON	ON	OFF	OFF	OFF
#9	64 &68	ON	OFF	ON	ON	ON
#10	72 & 76	ON	OFF	ON	ON	OFF
#11	80 & 84	ON	OFF	ON	OFF	ON
#12	88 &92	ON	OFF	ON	OFF	OFF
#13	96 & 100	ON	OFF	OFF	ON	ON
#14	104 & 108	ON	OFF	OFF	ON	OFF
#15	112 & 116	ON	OFF	OFF	OFF	ON
#16	120 & 124	ON	OFF	OFF	OFF	OFF
#17	128 & 132	OFF	ON	ON	ON	ON
#18	136 & 140	OFF	ON	ON	ON	OFF
#19	144 & 148	OFF	ON	ON	OFF	ON
#20	152 & 156	OFF	ON	ON	OFF	OFF
#21	160 & 164	OFF	ON	OFF	ON	ON
#22	168 & 172	OFF	ON	OFF	ON	OFF
#23	176 & 180	OFF	ON	OFF	OFF	ON
#24	184 &188	OFF	ON	OFF	OFF	OFF
#25	192 & 196	OFF	OFF	ON	ON	ON
#26	200 & 204	OFF	OFF	ON	ON	OFF
#27	208 & 212	OFF	OFF	ON	OFF	ON
#28	216 & 220	OFF	OFF	ON	OFF	OFF
#29	224 & 228	OFF	OFF	OFF	ON	ON
#30	232 & 236	OFF	OFF	OFF	ON	OFF
#31	240 & 244	OFF	OFF	OFF	OFF	ON
#32	248 & 252	OFF	OFF	OFF	OFF	OFF

The daisy-chain board address relationship with respect to the 5-bit (SW1) dip position setting. Note: on=closed, off=open. To turn "off" a switch, push down on the "open" side. To turn "on" a switch, push down on the "numbered" side.

M-Variable Assignments

Port A is always configured as a negative logic input port which can be read through TWS type M-variables (see below). The output lines are driven by writing to port B.

There is a special format 32-bit wide M-variable for reading the data from, and writing the data to, an ACC-34Dx cards, TWS. NOTE: This special M-variable definition is implemented in PMAC's firmware with a version number equal to or higher than 1.13. In version 1.14D, the TWS format was modified in its address designation field to prevent un-intentional reads from an output port or un-intentional writes to an input port. If your PROM version is between 1.13 to 1.14C, you may request for a free PROM update to version 1.14D or above.

The definition format is of the form:

M{constant}->TWS:{m-plex}

For an input port, **{m-plex}** is a legal byte number (from column 2 of Table 1) plus 1. Any attempt to write to a TWS type M-variable defined with bit zero of its address set to 1, is prevented by PMAC's firmware automatically. For an output port, **{m-plex}** is a legal byte number (from column 2 of Table 1) plus 2. An attempt to read a TWS type M-variable defined with bit one of its address set to 1, returns zero and the actual read is prevented by PMAC's firmware (no error is reported). Note that individual bits cannot be directly assigned to an M-variable of this type. Rather banks of 32 bits (ports) can be assigned to M-variables. For example to address Port A (bits 0 to 31) of board #1 as an input using M100, we would use the following definition:

```
M100->TWS:1      ;Port A (AIO 0-31) of an ACC-34Dx with SW1 switches
                 all ON
                 ;assigned for read only (1=0+1)
```

Similarly to address Port B of the same board #1 as an output using M101, we would use the following definition:

```
M101->TWS:6      ;Port B  (BIO 0-31) of an  ACC-34Dx  with SW1 switches
                 all ON
                 ;assigned for write only (6=4+2)
```

Yet another example: to address Port A of board #6 as an input using M300, we would use the following definition:

```
M300->TWS:41     ;Port A (AIO 0-31) of an ACC-34Dx with SW1 switches
                 ;ON,ON,OFF,ON,OFF
                 ;assigned for read only (41=40+1)
```

Note

1. A 32-bit Read or a 32-bit Write to an individual port takes approximately 64 microseconds of time in the PMAC's background time slot. As a result excessive and unnecessary references to TWS type M-variables is not recommended (see below for efficient ACC-34Dx I/O processing).
2. TWS type M-variable definition addresses which point to the base address directly (e.g. **M300->TWS:40**) are still valid (i.e. they do not generate error). However their use is very strongly discouraged. This because both reads and writes are enabled when the least significant and the next least significant addresses bits are both zero (e.g. decimal 40 = 01000000 in binary). In this situation, any accidental read of an output port (say via the Executive programs watch window) will cause all the output to be turned on! It is therefore safer and more predictable when bits 0 & 1 of the M-variable definition are intentionally used to disable either the read function or the write function.

PROCESSING ACC-34DX INPUTS & OUTPUTS

Because the PMAC interface to the Accessory 34 family of I/O boards (ACC-34Dx) is by full 32-bit words transmitted serially, even when access to only a single bit is desired, the user must consider carefully how the interface is done and how frequently. Care must also be taken to work efficiently with the data so that PMAC is not bogged down with slow serial reads and writes, and time-consuming logic to assemble and disassemble I/O words.

The recommended strategy is to keep "images" of each input or output word in PMAC's internal memory, or in the dual-ported RAM. The input words are copied into their image words, and the output words are copied from their image words. Most program operations deal with these image words; much less frequently is the slow transfer to or from an ACC-34Dx board performed. During the act of copying, bit inversion can also be performed with the exclusive-or function.

When to Access ACC-34Dx

The actual reads and writes for an ACC-34Dx board can only be done in a background PLC program (PLC 1-31) or through on-line commands, which are executed between PLC programs. Motion programs and PLC 0 cannot directly access this I/O -- they can work only with the image words. Reading an input word from an ACC-34Dx is simply a question of using the TWS-form M-variable for that word on the right side of an equation. Usually this operation simply copies the input word into its internal image variable. Similarly, writing an output word to an ACC-34Dx just involves using the M-variable for that word on the left side of an equation, typically just copying it from its internal image word.

Most users will treat ACC-34Dx I/O the same way that a traditional PLC treats its I/O; all of the inputs are read at the beginning of a PLC software scan, and all of the outputs are written to at the end of the scan. In between, all the processing of the variables is done working with the internal image words. It is possible to make the write operation to the output word conditional on a change in the image word for the output from the previous scan, but the time involved in making the decision and storing each scan's value is about the same as the actual writing to the output.

Image Word Variables

It is best to use fixed-point M-variables as the internal image variables for the I/O words. When this is done, a single M-variable representing the entire I/O word can be used for the copying operation. Then separate M-variables can be used to access individual bits or segments of the image word. Use of these smaller M-variables allows PMAC's efficient firmware to do the masking and logic necessary to pick out portions of the I/O word, rather than slower user program code.

Location of Image Words

Where should these internal image variables reside in PMAC's memory? If the system has dual-ported RAM, it is probably best to use a 32-bit register in DPRAM. This way, the host computer always has immediate access to the I/O. In fact, it is possible to use PMAC just as a pass-through between the host computer and the ACC-34Dx boards, letting the host computer do all the processing. A 32-bit fixed-point register in DPRAM is defined by the DP format of M-variable (e.g. **M60->DP:$DF00**). This type of variable occupies the low 16 bits (bits 0 to 15) of PMAC Y-memory, and the low 16 bits of PMAC X-memory at the same address, with the less significant bits in Y-memory. It appears to the host computer as 2 16-bit registers at consecutive even addresses, with the less significant bits at the lower address.

If there is no DPRAM, the image word will be in an otherwise unused double register in PMAC's own memory. There are several places to find unused registers. There are sixteen open registers that are automatically set to zero on power-up at PMAC addresses **$0770** to **$077F**. There are sixteen more open registers whose values are held when power is off at PMAC addresses **$07F0** to **$07FF**. Also, it is possible to use the registers of otherwise unused P and Q-variables for this purpose.

These registers should be accessed with fixed-point M-variables, not floating-point P or Q-variables! A double fixed-point register in PMAC's internal memory is defined by the D format of M-variable (e.g. **M61->D:$07F0**). This is a 48-bit register -- only the low 32 bits will be used. The low 24 bits of the I/O will be in Y-memory, and the high 8 bits of the I/O will be in the low 8 bits of X-memory.

When working with the ACC-34Dx I/O with this method of using fixed-point image variables, the only software overhead is the actual copying between image and I/O. Including program interpretation time, this amounts to about 100 microseconds per 32-bit word. Aside from this, working with the I/O through the image words is at least as fast as direct (parallel) PMAC I/O. Of course, there is a potential latency of a full PLC scan on the actual I/O which must be respected. Many systems will have a few critical I/O points that cannot tolerate this latency; these typically use PMAC's JOPTO port or ACC-14 I/O for these time-critical points, then use ACC-34Dx for I/O that do not need to be so fast.

Preventing Conflicts in Output Image Words

Care must be taken if tasks of different priority levels are trying to write to the same output image word, or if both the host computer and PMAC are trying to write to the same DPRAM output image word. If the proper techniques are not used, occasional output changes will not be executed, and because of the intermittent nature of the problem will make it very difficult to diagnose. If the application has two priority levels or two computers that write to the same ACC-34Dx output word, separate partial image words must be used, then these words combined as the output word is sent. Note that there is no conflict in having different tasks or different processors read from the same input word.

Remember that a computer cannot actually write to less than a word of memory at a time, even if it only wants to change one bit. In PMAC the word length is 24 bits; for the DPRAM, it is 16 bits. If a computer wants to change less than a full word, it must read the full word, modify the bits it wants with mask words, and then write back the full word.

There are two priority levels in PMAC that can write to these image words: the foreground level, which includes all of the motion programs and PLC 0; and the background level, which includes PLCs 1-31 and on-line commands. The problem can occur when a higher priority task interrupts a lower priority task that is in the middle of changing the image word with a read-modify-write operation. When the lower priority task resumes, it will undo the changes made by the higher priority task. Similarly, if the image word is in the DPRAM, and one side starts its read-modify-write cycle on the word but does not finish it before the other side starts its own cycle, the side that starts later can undo the changes made by the side that starts first.

Note

Two tasks at the same priority level cannot interrupt each other; one will always finish an operation before the other starts. Therefore, there is no need to worry about two motion programs writing to the same image word; or a motion program and PLC 0; because these tasks are at the same priority level. Similarly, there is no need to worry about two background PLC programs writing to the same image word, or a background PLC and on-line commands.

To prevent this possible conflict, the different priority levels or different processors must use different image words, even if they each represent only a part of the same total output word. These partial words are then combined in the act of writing to the actual output word.

The simplest way to split an image word is to use the natural X-memory vs. Y-memory split in PMAC's memory. If you are using a double word in PMAC's internal memory, you can reserve the 24 bits in Y-memory for one priority level, and the 8 bits in X-memory for the other. If you are using the DPRAM, you can reserve the 16 bits in Y-memory for one processor or priority level, and the 16 bits in X-memory for another. If you do this, no special techniques need to be used. On PMAC, simply write to the partial

words with a X or Y format M-variable; PMAC will automatically do the read-modify-write cycle without touching the other part of the word. On the host computer, access the DPRAM register with the short (16-bit) integer format, not the long.

However, if you cannot arrange your split in this fashion, you must create separate "overlapping" image words and explicitly combine them. As an example, take a system where the low 12 bits will be written to by background **PLCs** and the high 20 bits will be written to by motion programs. We create two separate image words, one for each priority level, and the actual output word:

```
M101->D:$0770    ; Image word for PLC programs (background)
M102->D:$0771    ; Image word for motion programs (foreground)
M103->TWS:6      ; ACC-34x output word; write-only
```

We also define single-bit M-variables to parts of these same internal addresses: at Y:$0770, bits 0 to 11 for the PLCs; then at **Y:$0771**, bits **12** to **23**, and **X:$0771**, bits 0 to 7 for the motion programs. At the end of a PLC scan, to create the actual output word on an ACC-34Dx from the image words, we would use the program statement:

```
M103 = (M101 & $00000FFF) | (M102 & $FFFFF000)
```

The bit-by-bit AND (**&**) operations make sure no falsely set bits in unused portions of the image words get into the output word. They are not strictly necessary if the unused bits can be guaranteed to be zero. The bit-by-bit OR (|) operation combines the word, and the assignment of the resulting value to **M103** causes it to be written to the ACC-34Dx.

If you want to be able to write to the same bit of an output image word with two different priority levels or processors, one of the tasks must do so indirectly by writing into a holding register. The other task must take this holding register and transfer the bit value into the image word. This task must decide what to do in case of any conflict (i.e. one task wants to clear the bit, and the other wants to set it).

Example

The following example should illustrate the concept of this method of working with ACC-34Dx I/O. It is a bit unrealistic, because it shows the image variables both in DPRAM and several places in internal memory. In a real application, a single location range would probably be chosen.

Set-up and Definitions:

```
; Actual ACC-34 I/O Words

M1000->TWS:1            ; First side of first ACC-34Dx board; an input here
                        ; Location is at port address 0; added 1 for read only
M1002->TWS:6            ; Second side of first ACC-34Dx board; an output here
                        ; Location is at port address 4; added 2 for write ; only
M1004->TWS:9            ; First side of second ACC-34Dx board; an input here
                        ; Location is at port address 8; added 1 for read only
M1006->TWS:14           ; Second side of second ACC-34Dx board; an output here
                        ; Location is at port address 12; added 2 for write only
; Image Words

M1001->DP:$D800         ; 32-bit fixed-point DPRAM register
M1003->D:$0770          ; 48-bit fixed-point register, set to zero on power-up
M1005->D:$07F0          ; 48-bit fixed-point register, value held thru power-down
M1007->D:$13FF          ; Register for P1023, treated as 48-bit fixed-point value

; Individual Pieces of Image Words

M100->Y:$D800,0         ; Least significant bit (bit 0) of first image word
M101->Y:$D800,1         ; Second bit (bit 1) of first image word
...
M115->Y:$D800,15        ; Bit 15 of first image word
M116->X:$D800,0         ; Bit 16 of first image word
M117->X:$D800,1
...
M131->X:$D800,15        ; Most significant bit (bit 31) of first image word
```

```
        M300->Y:$0770,0         ; Least significant bit (bit 0) of second image word
        M301->Y:$0770,1         ; Second bit (bit 1) of second image word
        ...
        M323->Y:$0770,23        ; Bit 23 of second image word
        M324->X:$0770,0         ; Bit 24 of second image word
        M325->X:$0770,1         ; Bit 25 of second image word
        ...
        M331->X:$0770,7         ; Most significant bit (bit 31) of second image word

        M500->Y:$07F0,0         ; Least significant bit (bit 0) of third image word
        ...
        M523->Y:$07F0,23        ; Bit 23 of third image word
        M524->X:$07F0,0         ; Bit 24 of third image word
        ...
        M531->X:$07F0,7         ; Most significant bit (bit 31) of third image word

        M700->Y:$13FF,0         ; Least significant bit (bit 0) of fourth image word
        ...
        M724->X:$13FF,0,8       ; Top eight bits (bits 24-31) of fourth image word

        Programs:

        ; "Reset" PLC program that only runs once on power-up or reset

        OPEN PLC 1 CLEAR

        M1003=0                 ; Clear output image word to make sure all outputs off
        M1007=0                 ; Ditto
        ...
        DISABLE PLC 1          ; To make sure this only runs once on power-up/reset
        CLOSE

        ; PLC program to copy the inputs into image words at beginning of each scan
        OPEN PLC 2 CLEAR
        M1001=M1000             ; Copy first input word into its image register
M1005=M1004^$FFFFFFFF           ; Copy second input word into its image register,
                                ; inverting
        ...
        CLOSE

        ; PLC program that works with individual bits of image words

        OPEN PLC 3 CLEAR
        IF (M100=1 AND M101=0 AND P43>50)
            M301=1
        ELSE
            M301=0
        ENDIF
        ...
        CLOSE

        ; PLC program that copies image words to outputs at end of scan

        OPEN PLC 31 CLEAR
M1002=M1003             ; Copy first output image word to ACC-34Dx
        M1004=M1005^$FFFFFFFF   ; Copy second output image word to ACC-34Dx, inverting
```

POWER SUPPLY AND OPTO-ISOLATION CONSIDERATIONS

The power for the PMAC processor side of the opto-isolation circuitry is brought in directly from J1 (JTHW). The power for the external side of the opto-isolation circuitry should be from a separate supply brought in through TB1 (5V or 12-24 volts). Note either 5V or 12-24V should be used. Do not supply power through both. E1 should be installed when +12 to 24V supply is brought in through TB1. It should be removed if +5V supply is brought in through TB1. The current requirement for on board logic circuit on the external side of the opto isolation is approximately 50 mA. However, if the power is also supplied for the external opto boards digital circuits, then up to 550 mA may be required.

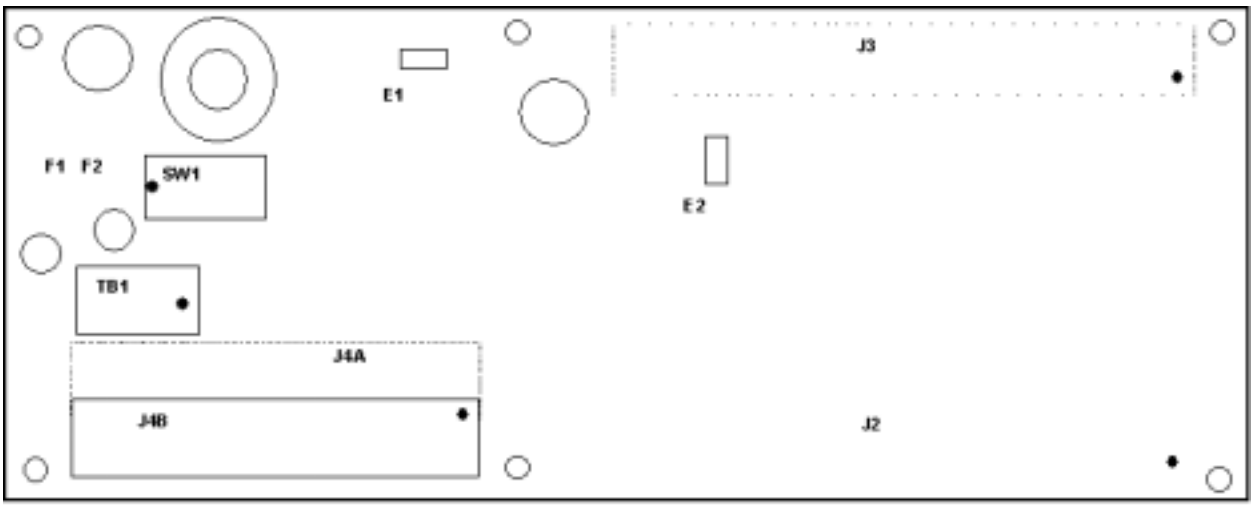
WATCHDOG TIMER (ROLE OF JUMPER E2)

Acc-34Dx has a local watchdog timer that is disabled when the jumper E2 is installed. In the factory default setup, this jumper is installed (the watchdog timer is disabled).

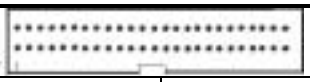
When jumper E2 is removed, the 1.5-second watchdog timer circuit is enabled on ACC-34Dx. With the watchdog circuit enabled, PMAC must read from or write to the board at least once every 1.5 seconds. If the board is not accessed within the 1.5-second period, then the watchdog circuit switches off the output circuits of the opto board(s) connected to the ACC-34Dx. A single read or write cycle will re-establish control over the outputs.

BOARD LAYOUT AND CONNECTOR PINOUTS

ACC-34D and ACC-34DD Board Layout



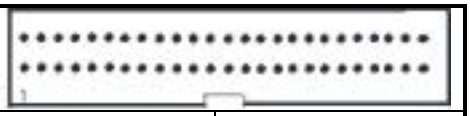
ACC-34D - J2 (50 Pin Header)



Pin #	Symbol	Function	Description	Notes
1	IN23	Input	Port A Bit 23	
2	IN24	Input	Port A Bit 24	
3	IN22	Input	Port A Bit 22	
4	IN25	Input	Port A Bit 25	
5	IN21	Input	Port A Bit 21	
6	IN26	Input	Port A Bit 26	
7	IN20	Input	Port A Bit 20	
8	IN27	Input	Port A Bit 27	
9	IN19	Input	Port A Bit 19	
10	IN28	Input	Port A Bit 28	
11	IN18	Input	Port A Bit 18	
12	IN29	Input	Port A Bit 29	
13	IN17	Input	Port A Bit 17	
14	IN30	Input	Port A Bit 30	
15	IN16	Input	Port A Bit 16	
16	IN31	Input	Port A Bit 31	
17	IN15	Input	Port A Bit 15	
18	GND	Common	Opto Common	
19	IN14	Input	Port A Bit 14	
20	GND	Common	Opto Common	
21	IN13	Input	Port A Bit 13	
22	GND	Common	Opto Common	
23	IN12	Input	Port A Bit 12	
24	GND	Common	Opto Common	
25	IN11	Input	Port A Bit 11	
26	GND	Common	Opto Common	
27	IN10	Input	Port A Bit 10	
28	GND	Common	Opto Common	
29	IN9	Input	Port A Bit 9	
30	GND	Common	Opto Common	
31	IN8	Input	Port A Bit 8	
32	GND	Common	Opto Common	
33	IN7	Input	Port A Bit 7	
34	GND	Common	Opto Common	
35	IN6	Input	Port A Bit 6	
36	GND	Common	Opto Common	
37	IN5	Input	Port A Bit 5	
38	GND	Common	Opto Common	
39	IN4	Input	Port A Bit 4	
40	GND	Common	Opto Common	
41	IN3	Input	Port A Bit 3	
42	GND	Common	Opto Common	
43	IN2	Input	Port A Bit 2	
44	GND	Common	Opto Common	
45	IN1	Input	Port A Bit 1	
46	GND	Common	Opto Common	
47	IN0	Input	Port A Bit 0	
48	GND	Common	Opto Common	
49	A +5V	Output	+5 V supply	
50	GND	Common	Opto Common	

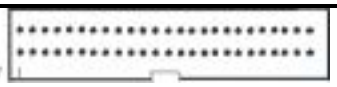
This 50-pin header provides the connection for the input lines numbered 0 to 31. In addition, this connector has a 5-volt (maximum 0.5 A) power supply outlet for external logic circuits.

ACC-34D – J3 (50 Pin Header)

Top View 

Pin #	Symbol	Function	Description	Notes
1	OUT23	Output	Port B Bit 23	
2	OUT24	Output	Port B Bit 24	
3	OUT22	Output	Port B Bit 22	
4	OUT25	Output	Port B Bit 25	
5	OUT21	Output	Port B Bit 21	
6	OUT26	Output	Port B Bit 26	
7	OUT20	Output	Port B Bit 20	
8	OUT27	Output	Port B Bit 27	
9	OUT19	Output	Port B Bit 19	
10	OUT28	Output	Port B Bit 28	
11	OUT18	Output	Port B Bit 18	
12	OUT29	Output	Port B Bit 29	
13	OUT17	Output	Port B Bit 17	
14	OUT30	Output	Port B Bit 30	
15	OUT16	Output	Port B Bit 16	
16	OUT31	Output	Port B Bit 31	
17	OUT15	Output	Port B Bit 15	
18	GND	Common	Opto Common	
19	OUT14	Output	Port B Bit 14	
20	GND	Common	Opto Common	
21	OUT13	Output	Port B Bit 13	
22	GND	Common	Opto Common	
23	OUT12	Output	Port B Bit 12	
24	GND	Common	Opto Common	
25	OUT11	Output	Port B Bit 11	
26	GND	Common	Opto Common	
27	OUT10	Output	Port B Bit 10	
28	GND	Common	Opto Common	
29	OUT9	Output	Port B Bit 9	
30	GND	Common	Opto Common	
31	OUT8	Output	Port B Bit 8	
32	GND	Common	Opto Common	
33	OUT7	Output	Port B Bit 7	
34	GND	Common	Opto Common	
35	OUT6	Output	Port B Bit 6	
36	GND	Common	Opto Common	
37	OUT5	Output	Port B Bit 5	
38	GND	Common	Opto Common	
39	OUT4	Output	Port B Bit 4	
40	GND	Common	Opto Common	
41	OUT3	Output	Port B Bit 3	
42	GND	Common	Opto Common	
43	OUT2	Output	Port B Bit 2	
44	GND	Common	Opto Common	
45	OUT1	Output	Port B Bit 1	
46	GND	Common	Opto Common	
47	OUT0	Output	Port B Bit 0	

ACC-34D – J3 (50 Pin Header) (Continued)



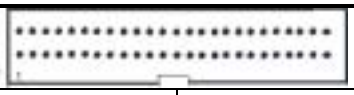
Pin #	Symbol	Function	Description	Notes
48	GND	Common	Opto Common	
49	A +5V	Output	+5 V supply	
50	GND	Common	Opto Common	

This 50-pin header provides the connection for the output lines numbered 0 to 31. In addition, this connector has a 5-volt (maximum 0.5 A) power supply outlet for external logic circuits.

ACC-34DD - J2 (50 Pin Header)

Pin #	Symbol	Function	Description	Notes
1	OUT11	Output	Port B Bit 11	
2	IN24	Input	Port A Bit 24	
3	OUT10	Output	Port B Bit 10	
4	IN25	Input	Port A Bit 25	
5	OUT09	Output	Port B Bit 9	
6	IN26	Input	Port A Bit 26	
7	OUT08	Output	Port B Bit 8	
8	IN27	Input	Port A Bit 27	
9	OUT07	Output	Port B Bit 7	
10	IN28	Input	Port A Bit 28	
11	OUT06	Output	Port B Bit 6	
12	IN29	Input	Port A Bit 29	
13	OUT05	Output	Port B Bit 5	
14	IN30	Input	Port A Bit 30	
15	OUT04	Output	Port B Bit 4	
16	IN31	Input	Port A Bit 31	
17	OUT03	Output	Port B Bit 3	
18	GND	Common	Opto Common	
19	OUT02	Output	Port B Bit 2	
20	GND	Common	Opto Common	
21	OUT01	Output	Port B Bit 1	
22	GND	Common	Opto Common	
23	OUT00	Output	Port B Bit 0	
24	GND	Common	Opto Common	
25	IN11	Input	Port A Bit 11	
26	GND	Common	Opto Common	
27	IN10	Input	Port A Bit 10	
28	GND	Common	Opto Common	
29	IN9	Input	Port A Bit 9	
30	GND	Common	Opto Common	
31	IN8	Input	Port A Bit 8	
32	GND	Common	Opto Common	
33	IN7	Input	Port A Bit 7	
34	GND	Common	Opto Common	
35	IN6	Input	Port A Bit 6	
36	GND	Common	Opto Common	
37	IN5	Input	Port A Bit 5	
38	GND	Common	Opto Common	
39	IN4	Input	Port A Bit 4	

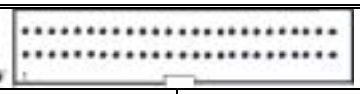
ACC-34DD - J2 (50 Pin Header) (Continued)



Pin #	Symbol	Function	Description	Notes
40	GND	Common	Opto Common	
41	IN3	Input	Port A Bit 3	
42	GND	Common	Opto Common	
43	IN2	Input	Port A Bit 2	
44	GND	Common	Opto Common	
45	IN1	Input	Port A Bit 1	
46	GND	Common	Opto Common	
47	IN0	Input	Port A Bit 0	
48	GND	Common	Opto Common	
49	A +5V	Output	+5 V supply	
50	GND	Common	Opto Common	

This 50-pin header provides the connection for the output lines numbered 12 to 31 and input lines numbered 12 to 23. In addition, this connector has a 5V (maximum 0.5A) power supply outlet for external logic circuits.

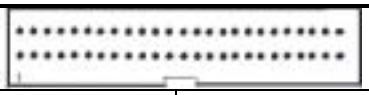
ACC-34DD – J3 (50 Pin Header)



Pin #	Symbol	Function	Description	Notes
1	OUT23	Output	Port B Bit 23	
2	OUT24	Output	Port B Bit 24	
3	OUT22	Output	Port B Bit 22	
4	OUT25	Output	Port B Bit 25	
5	OUT21	Output	Port B Bit 21	
6	OUT26	Output	Port B Bit 26	
7	OUT20	Output	Port B Bit 20	
8	OUT27	Output	Port B Bit 27	
9	OUT19	Output	Port B Bit 19	
10	OUT28	Output	Port B Bit 28	
11	OUT18	Output	Port B Bit 18	
12	OUT29	Output	Port B Bit 29	
13	OUT17	Output	Port B Bit 17	
14	OUT30	Output	Port B Bit 30	
15	OUT16	Output	Port B Bit 16	
16	OUT31	Output	Port B Bit 31	
17	OUT15	Output	Port B Bit 15	
18	GND	Common	Opto Common	
19	OUT14	Output	Port B Bit 14	
20	GND	Common	Opto Common	
21	OUT13	Output	Port B Bit 13	
22	GND	Common	Opto Common	
23	OUT12	Output	Port B Bit 12	
24	GND	Common	Opto Common	
25	IN23	Input	Port A Bit 23	
26	GND	Common	Opto Common	
27	IN22	Input	Port A Bit 22	
28	GND	Common	Opto Common	
29	IN21	Input	Port A Bit 21	
30	GND	Common	Opto Common	
31	IN20	Input	Port A Bit 20	
32	GND	Common	Opto Common	
33	IN19	Input	Port A Bit 19	

34	GND	Common	Opto Common	
35	IN18	Input	Port A Bit 18	

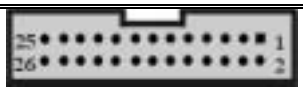
ACC-34DD – J3 (50 Pin Header) (Continued)



Pin #	Symbol	Function	Description	Notes
34	GND	Common	Opto Common	
35	IN18	Input	Port A Bit 18	35
36	GND	Common	Opto Common	
37	IN17	Input	Port A Bit 17	
38	GND	Common	Opto Common	
39	IN16	Input	Port A Bit 16	
40	GND	Common	Opto Common	
41	IN15	Input	Port A Bit 15	
42	GND	Common	Opto Common	
43	IN14	Input	Port A Bit 14	
44	GND	Common	Opto Common	
45	IN13	Input	Port A Bit 13	
46	GND	Common	Opto Common	
47	IN12	Input	Port A Bit 12	
48	GND	Common	Opto Common	
49	A +5V	Output	+5 V supply	
50	GND	Common	Opto Common	

This 50-pin header provides the connection for the output lines numbered 12 to 31 and input lines numbered 12 to 23. In addition, this connector has a 5-volt (maximum 0.5 A) power supply outlet for external logic circuits.

J4A & J4B (26-PIN Header)



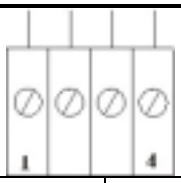
Top View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Output	Data Bit 0	
4	SEL0	Input	Address Line 0	
5	DAT1	Output	Data Bit 1	
6	SEL 1	Input	Address Line 1	
7	DAT2	Output	Data Bit 2	
8	SEL2	Input	Address Line 2	
9	DAT3	Output	Data Bit 3	
10	SEL3	Input	Address Line 3	
11	DAT4	Output	Data Bit 4	
12	SEL 4	Input	Address Line 4	
13	DAT5	Output	Data Bit 5	
14	SEL5	Input	Address Line 5	
15	DAT6	Output	Data Bit 5	
16	SEL6	Input	Address Line 6	
17	DAT7	Output	Data Bit 6	
18	SEL7	Input	Data Bit 7	
19	N.C.			
20	GND	Common	PMAC Common	
21	N.C.			
22	GND	Common	PMAC Common	
23	N.C.			
24	GND	Common		

25	+5V	Input	+5V DC Supply	
26	N.C.			

J4A (JTHW) is a 26-pin header that provides the link between PMAC's JTHW (J3) and this board. Using the supplied flat cable, PMAC's J3 should be connected to J4A. Through this connector PMAC sets the outputs and reads the inputs. In addition, the power for the processor side of the opto-isolation circuitry is provided from the PMAC board through this connector.
J4B is a 26-pin header that brings out the JTHW signals for the next accessory board on the JTHW multiplex memory map. This connector is pin-to-pin compatible with J4A

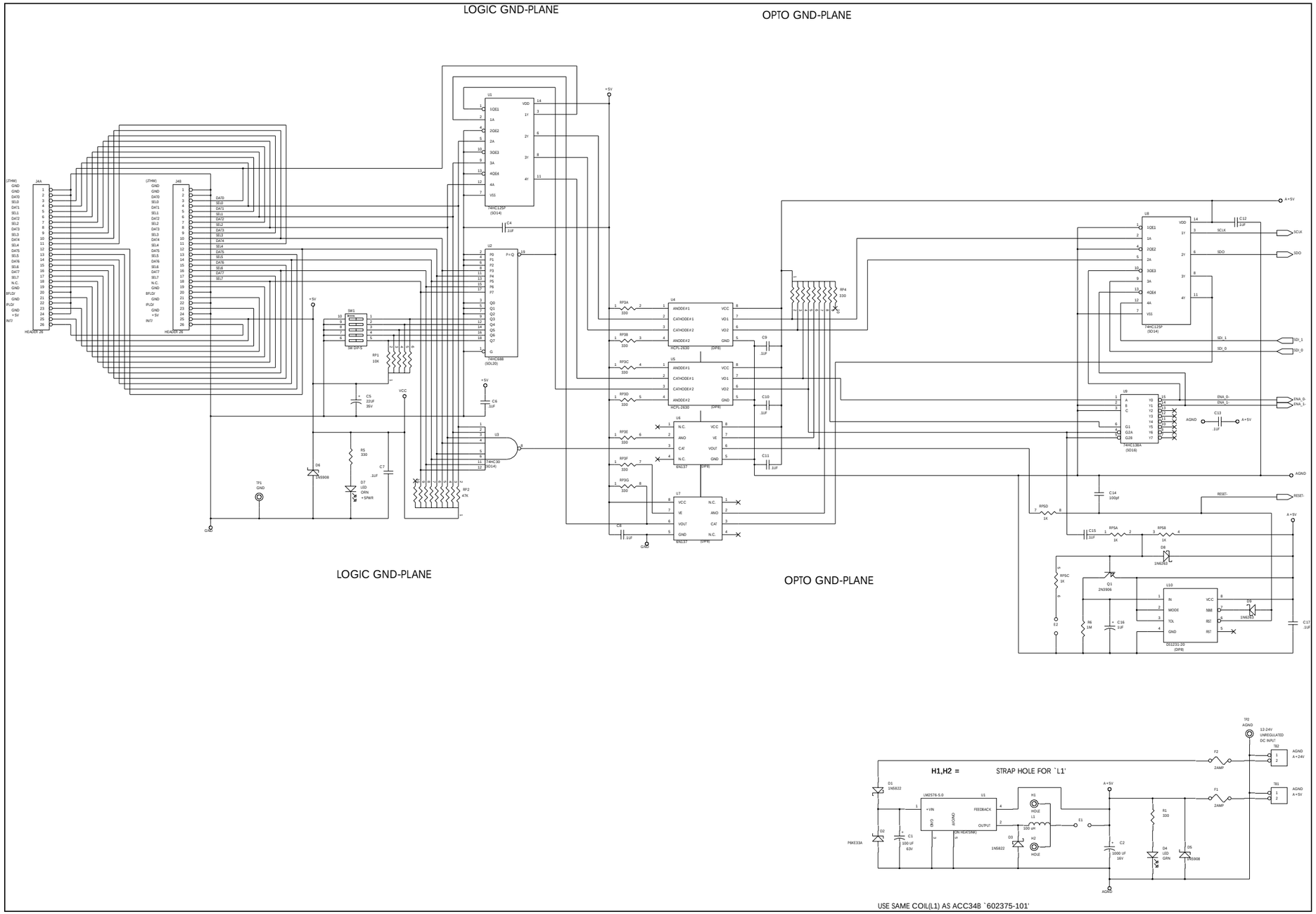
TB1 (4-pin Terminal Block)

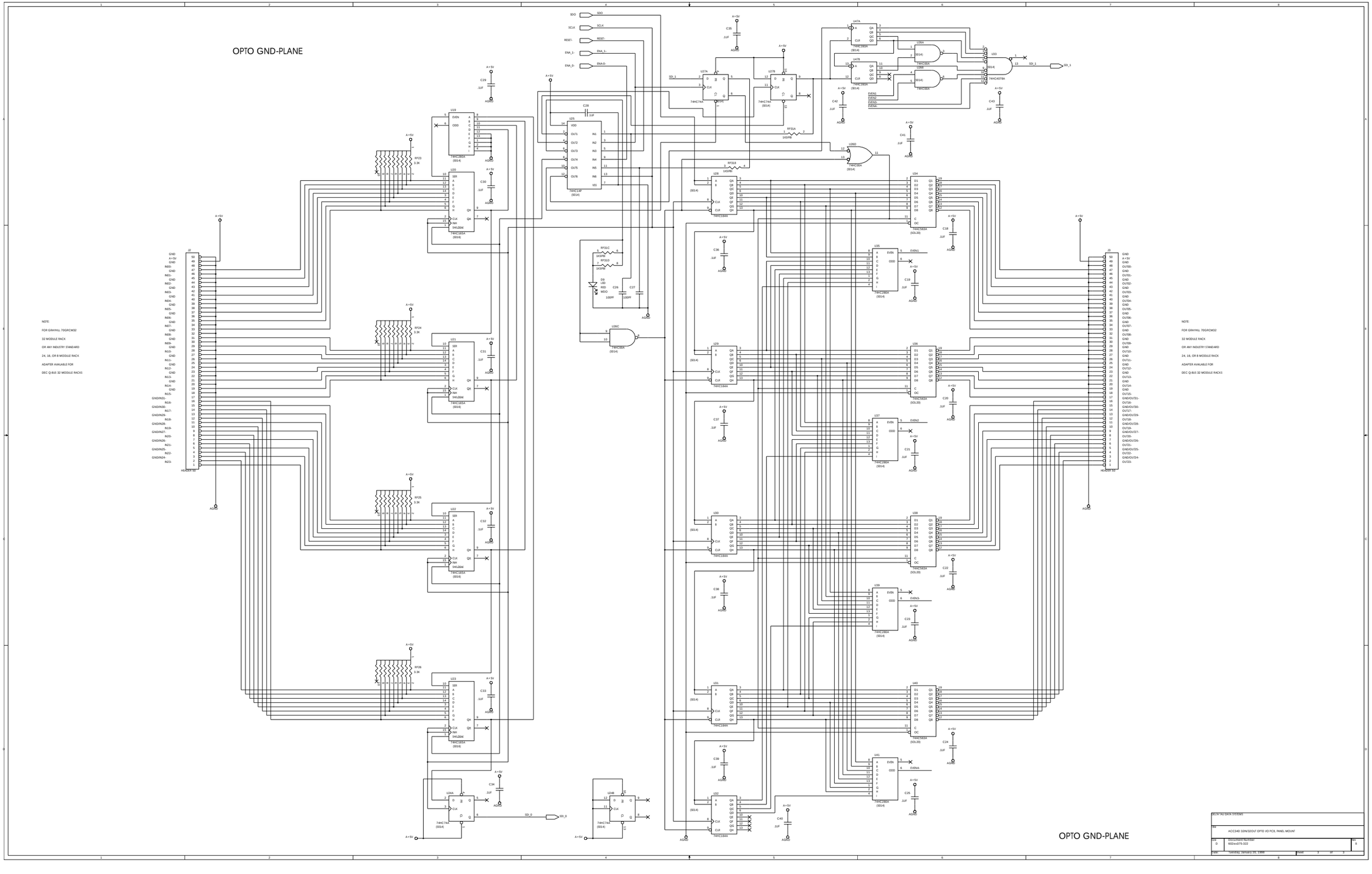


Pin #	Symbol	Function	Description	Notes
1	A+24V	Power Supply	External Supply for Optically Isolated Part of Circuitry	12V to 24 V Unregulated
2	AGND	Common	External Supply Ground	
3	AGND	Common	External Supply Ground	
4	A+5V	Power Supply	External Supply for Optically Isolated Part of Circuitry	Regulated +5 volts.

This a 4-pin terminal block through which a 5V regulated, or, a 12 to 24 volt unregulated power supply may be brought in for the optically isolated side of the circuitry on ACC-34DDX (50 mA is required). Remove jumper E1 if the power is supplied to the board via TB1-3, 4. Note that with jumper E1 installed, whenever a 12 to 24V supply is brought in from TB1-1, 2, then TB1-3, 4 can be used as a 5V power source for the logic circuits on the external opto boards (see the enclosed schematic). Do not supply power through both TB1-1, 2and TB1-3, 4.

SCHEMATICS


LOGIC GND-PLANE
OPTO GND-PLANE
LOGIC GND-PLANE
OPTO GND-PLANE
USE SAME COIL(L1) AS ACC34B `602375-101'
H1,H2 = STRAP HOLE FOR `L1'
HEADER 26
74HC125P (SO14)
74HC688 (SO20)
74HC30 (SO14)
HCPL-2630 (DIP8)
6N137 (DIP8)
74HC138A (SO16)
DS1231-20 (DIP8)
LM2576-5.0
PJKE33A
1N5822
1N6263
2N3906
SW DIP-8
TP1
TP2
12-24V UNREGULATED DC INPUT
2AMP
100 uH
1000 UF 16V
100 UF 63V
+5V
A+5V
AGND
VCC
GND
RESET-
SCLK
SDO
SDI_1
SDI_0
ENA_0-
ENA_1-


OPTO GND-PLANE
NOTE:
FOR GRAYHILL 70GRCM32
32 MODULE RACK
OR ANY INDUSTRY STANDARD
24, 16, OR 8 MODULE RACK
ADAPTER AVAILABLE FOR
DEC Q-BUS 32 MODULE RACKS
NOTE:
FOR GRAYHILL 70GRCM32
32 MODULE RACK
OR ANY INDUSTRY STANDARD
24, 16, OR 8 MODULE RACK
ADAPTER AVAILABLE FOR
DEC Q-BUS 32 MODULE RACKS
ACC34D 32IN/32OUT OPTO I/O PCB, PANEL MOUNT
Document Number
602ec/d75-322
Tuesday, January 20, 1998
OPTO GND-PLANE