QCPU-A(A Mode)

User's Manual

MITSUBISHI

Mitsubishi Programmable
Logic Controller

MELSEC-Q

Q02CPU-A
Q02HCPU-A
Q06HCPU-A

• SAFETY PRECAUTIONS •

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in the manual. Also pay careful attention to safety and handle the module properly.
These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PC system safety precautions.
These • SAFETY PRECAUTIONS • classify the safety precautions into two categories: "DANGER" and "CAUTION".

⚠ DANGER	Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.
⚠ CAUTION	Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.

Depending on circumstances, procedures indicated by ⚠CAUTION may also be linked to serious results.
In any case, it is important to follow the directions for usage.
Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[Design Precautions]

⚠ DANGER

- Install a safety circuit external to the PC that keeps the entire system safe even when there are problems with the external power supply or the PC main module. Otherwise, trouble could result from erroneous output or malfunction.
  (1) Configure the following circuits outside the PC: emergency stop circuit, protection circuit, interlocking circuit for opposite operations such as forward and reverse operations, and interlocking circuit for machine damage prevention such as upper/lower limit for positioning.
  (2) When the PC detects the following problems, it will stop calculation and turn off all output.
  The power supply module has an over current protection device and over voltage protection device.
  The PC CPUs self-diagnostic functions, such as the watchdog timer error, detect problems.
  In addition, all output will be turned on when there are problems that the PC CPU cannot detect, such as in the I/O controller. Build a failsafe circuit exterior to the PC that will make sure the equipment operates safely at such times.
  Refer to the Section 8.1 in this manual for example failsafe circuits.
  (3) Output could be left on or off when there is trouble in the output module's relay or transistor. So, build an external monitoring circuit that will monitor any single output that could cause serious trouble.
- If current over the rating or over-current due to a load short-circuit flows for a long term, it may cause smoke or fire. Prepare an external safety circuit, such as a fuse.
- Build a circuit that turns on the external power supply when the PC main module power supply is turned on. If the external power supply is turned on first, it could result in erroneous output or malfunction.

[Design Precautions]

⚠ DANGER

- When there are communication faulty with the data link, the communication faulty station will enter the following condition. Build an interlock circuit into the PC program that will make sure the system operates safely by using the communication state information.
  Not doing so could result in erroneous output or malfunction.
  (1) For the data link data, the data prior to the communication error will be held.
  (2) The MELSECNET (II, /B, /10) remote I/O station will turn all output off.
  (3) The MELSECNET/MINI-S3 remote I/O station will hold the output or turn all output off depending on the E.C. mode setting.
  Refer to manuals for corresponding data link system for how to detect the communication faulty station and the operation status when a communication error occurred.
- When configuring a system, do not leave any slots vacant on the base. Should there be any vacant slots, always use a blank cover (A1SG60) or dummy module (A1SG62).
  If the cover is not attached, the module's internal parts may be dispersed when a short-circuit test is performed or overcurrent/overvoltage is accidentally applied to the external I/O area.

⚠ CAUTION

- Do not bunch the control wires or communication cable with the main circuit or power wires, or install them close to each other.
  They should be installed 100mm (3.94 inch) or more from each other.
  Not doing so could result in noise that would cause malfunction.
- When controlling items like lamp load, heater or solenoid valve using an out put module, large current (approximately ten times greater than that present in normal circumstances) may flow when the output is turned OFF → ON. Take measures such as replacing the module with one having sufficient rated current.

[Installation Precautions]

⚠ CAUTION

- Use the PC in the environment given in the general specification section of the manual.
  Using the PC outside the range of the general specifications may result in electric shock, fire, or malfunction or may damage or degrade the product.
- Before mounting the module, securely insert the projection at the bottom of the module into the fixing hole on the base module.
  (The AnS series module must be tightened to the base module at the specified tightening torque.)
  An improperly mounted module may result in malfunction, failure, or falling.
  Excessive screw tightening may cause falling due to the breakage of the screw or module, short-circuit, or malfunction.

[Installation Precautions]

⚠ CAUTION

- Tighten the screw within the range of specified torque.
  If the screws are loose, it may result in fallout, short circuits, or malfunctions.
  Tightening the screws too far may cause damage to the screw and/or the module, resulting in fallout, short circuits, or malfunction.
- When installing extension cables, be sure that the base unit and the module connectors are installed correctly. After installation, check them for looseness. Poor connections could result in erroneous input and erroneous output.
- Correctly connect the memory card installation connector to the memory card. After installation, make sure that the connection is not loose. A poor connection could result in malfunction.
- Do not directly touch the module's conductive parts or electronic components.
  Doing so could cause malfunction or failure in the module.

[Wiring Precations]

⚠ DANGER

- Completely turn off the external power supply when installing or wiring. Not completely turning off all power supply could result in electric shock or damage to the product.
- When turning on the power or operating the module after installation or wiring work, be sure that the module's terminal covers are correctly attached. Not attaching the terminal covers could result in electric shock.

⚠ CAUTION

- Be sure to ground the FG terminals and LG terminals with a special PC ground of Type 3 or above. Not doing so could result in electric shock or malfunction.
- When wiring in the PC, check the rated voltage and terminal layout of the wiring, and make sure the wiring is done correctly. Connecting a power supply that differs from the rated voltage or wiring it incorrectly may cause fire or breakdown.
- Do not connect multiple power supply modules in parallel.
  Doing so could cause overheating, fire, or damage to the power supply module.
- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, fire, or malfunction.
  Tightening the screws too far may cause damage to the screw and/or the module, resulting in fallout, short circuits, or malfunction.
- A protective label is attached on the top of the CPU module to avoid foreign materials such as wires from entering inside during wiring process.
  Do not remove the label until the wiring is completed. Before starting the system, be sure to remove the label to ensure heat radiation.
- External connections shall be crimped or pressure welded with the specified tools, or correctly soldered.
  For information regarding the crimping and pressure welding tools, refer to the I/O module's user manual. Imperfect connections could result in short circuit, fires, or malfunction.

[Starting and Maintenance Precautions]

⚠ DANGER

- Do not touch the terminals while power is on. Doing so could cause shock or malfunction.
- Correctly connect the battery. Also, do not change, disassemble, heat, place in fire, short circuit, or solder the battery.
  Mishandling of the battery can cause overheating or cracks which could result in injury and fires.
- Make sure to switch all phases of the external power supply off before cleaning or re-tightening screws. If you do not switch off the external power supply, it will cause electric shock.
  If the screws are loose, it may result in fallout, short circuit, or malfunction. Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

⚠ CAUTION

- Carefully read manuals and confirm that it is safe enough before performing on-line operations which require to connect peripheral devices to an operating CPU module. (especially when modifying a program, performing forced output, or modifying the operation status.)
  Misoperation may damage the module or cause accidents.
- Do not disassemble or rebuild the module.
  It may cause accidents, malfunction, injury, or fire.
- When using a cellular phone, keep it 25 cm or more away from the PC.
  Otherwise, malfunction may result.
- Make sure to switch all phases of the external power supply off before mounting or removing the module. If you do not switch off the external power supply, it will cause failure or malfunction of the module.

[Disposal Precautions]

⚠ CAUTION

- Disposing of this product, treat it as industrial waste.

REVISIONS

* The manual number is given on the bottom left of the back cover.

Print Date	* Manual Number	Revision
Dec., 1999	SH (NA) 080065-A	First printing
Mar., 2000	SH (NA) 080065-B	Addition of model QA1S33B

Japanese Manual Version SH-080066-B

INTRODUCTION

Thank you for choosing a Mitsubishi MELSEC-Q Series General Purpose Programmable Controller.
Before using your new PC, please read this manual thoroughly to gain an understanding of its functions so you can use it properly.
Please forward a copy of this manual to the end user.

CONTENTS

About Manuals

The following manuals are also related to this product.
In necessary, order them by quoting the details in the tables below.

Related Manuals

Manual Name	Manual Number (Model Code)
ACPU Programming Manual (Fundamentals) Describes programming methods necessary for creating programs, device names, parameters, program types, memory area configuration, and so on. (Sold separately)	IB-66249 (13J740)
ACPU Programming Manual (Common Instructions) Describes how to use the sequence instruction, basic instructions, applied instructions and microcomputer programs. (Sold separately)	IB-66250 (13J741)
AnSHCPU/AnACPU/AnUCPU Programming Manual (Dedicated Instructions) Describes instructions that have been expanded for Q02CPU-A, Q02HCPU-A, and Q06HCPU-A. (Sold separately)	IB-66251 (13J742)
AnACPU/AnUCPU Programming Manual (AD57 Instructions) Describes dedicated instructions for A2USHCPU-S1 to control the AD57 (S1)/AD58 controller module. (Sold separately)	IB-66257 (13J743)
AnACPU/AnUCPU Programming Manual (PID Instructions) Describes dedicated instructions for A2USHCPU-S1 to perform the PID control. (Sold separately)	IB-66258 (13J744)
MELSAP-II (SFC) Programming Manual Describes the specifications, functions, instructions, and programming methods for SFC programming using MELSAP II. (Sold separately) (Sold separately)	IB-66361 (13JF40)
AnS Module type I/O User's Manual Describes the specification of the compact building block type I/O module. (Sold separately)	IB-66541 (13JE81)

Abbreviations and generic names used in this manual

In this manual, the following abbreviations and generic names are used to explain about QCPU-A unless explicitly instructed.

Abbreviation/generic name		Description
Q02CPU-A		Abbreviation for Q02CPU-A general-purpose programming logic controller
Q02HCPU-A		Abbreviation for Q02HCPU-A general-purpose programming logic controller
Q06HCPU-A		Abbreviation for Q06HCPU-A general-purpose programming logic controller
QCPU-A		Generic name for Q02CPU-A, Q02HCPU-A, and Q06HCPU-A
CC-Link		Abbreviation for Control & Communication link system
AnNCPU		Generic name for A0J2HCPU, A1SCPU, A1SCPU-S1, A1SCPUC24-R2, A1SHCPU, A1SJCPU, A1SJCPU-S3, A1SJHCPU, A1SJHCPU-S8, A1NCPU, A2CCPU, A2CCPUC24, A2CCPUC24-PRF, A2CJCPU, A2NCPU, A2NCPU-S1, A2SCPU, A2SCPU-S1, A2SHCPU, A2USHCPU-S1, and A1FXCPU
AnACPU		Generic name for A2ACPU, A2ACPU-S1, A2ACPUP21/R21, A2ACPUP21/R21-S1, A3ACPUP21/R21, A3NCPU, and A3ACPU
AnUCPU		Generic name for A2UCPU, A2UCPU-S1, A2ASCPU, A2ASCPU-S1, A2ASCPU-S30, A2USHCPU-S1, A3UCPU, and A4UCPU
QnACPU		Generic name for Q2ACPU,Q2ACPU-S1, Q2ASCPU, Q2ASCPU-S1, Q2ASHCPU, Q2ASHCPU-S1, Q3ACPU, Q4ACPU, and Q4ARCPU
ACPU		Generic name for AnNCPU, AnACPU, and AnUCPU
QCPU	A mode	Generic name for Q02CPU-A, Q02HCPU-A, and Q06HCPU-A
	Q mode	Generic name for Q02CPU, Q02HCPU, Q06HCPU, Q12HCPU, and Q25HCPU

MEMO

1. OVERVIEW

This User's Manual describes the performance, functions, and handling method of the QCPU-A general purpose PC, as well as the specifications and handling of the memory card, power supply module and the base module.

The programming modules and software packages have to be compatible with the upgraded A2UCPU, A2UCPU-S1, A3UCPU, and A4UCPU (abbreviated as AnUCPU hereafter).
When the conventional programming modules and software packages are used, the usable range varies depending on the model of the CPU (PC model name). (Refer to Section 2.2.3.)

Refer to the list of components in Section 2.3 for various modules which can be used with the QCPU-A.
Refer to Section 2.2.1 for the special function modules which have limited range of usable devices.

(1) Supplied parts

Item Name	Type name	Quantity
CPU module	Q02CPU-A	1
	Q02HCPU-A	
	Q06HCPU-A	
Battery	Q6BAT	1

1.1 Features

QCPU-A (A mode) has the following features when compared with the A2USHCPU-S1.

(1) Faster operation processing

QCPU-A offers significantly faster operation processing than that of A2USHCPU-S1.

Item	Q02CPU-A	Q02HCPU-A, Q06HCPU-A	A2USHCPU-S1
Operation processing speed ＊1	79ns	34ns	90ns

＊1: I/O processing: At refresh or LD instruction

(2) Larger program capacity

With Q06HCPU-A, the program capacity can be expanded.
Moreover, Q06HCPU-A allows the creation of sub programs.

Item	Q06HCPU-A	A2USHCPU-S1
Program capacity	30k steps (Main program) + 30k steps (Sub program)	30k step

(3) More actual I/O points

QCPU-A offers 4096 actual I/O points, 4 times that of A2USHCPU-S1.

Item	Q02CPU-A, Q02HCPU-A,Q06HCPU-A	A2USHCPU-S1
Actual I/O points	4096	1024

(4) More expansion stages

Up to 7 stages of expansion base module can be added.

(5) Faster communication speed with peripheral devices

The communication speed with peripheral devices is considerably improved than that of A2USHCPU-S1.

Item	Q02CPU-A, Q02HCPU-A, Q06HCPU-A	A2USHCPU-S1
Communication speed (kbps)	115.2＊1	9.6

＊1: Designate 9.6kbps when using GPP of SW3D5C-GPPW or earlier.

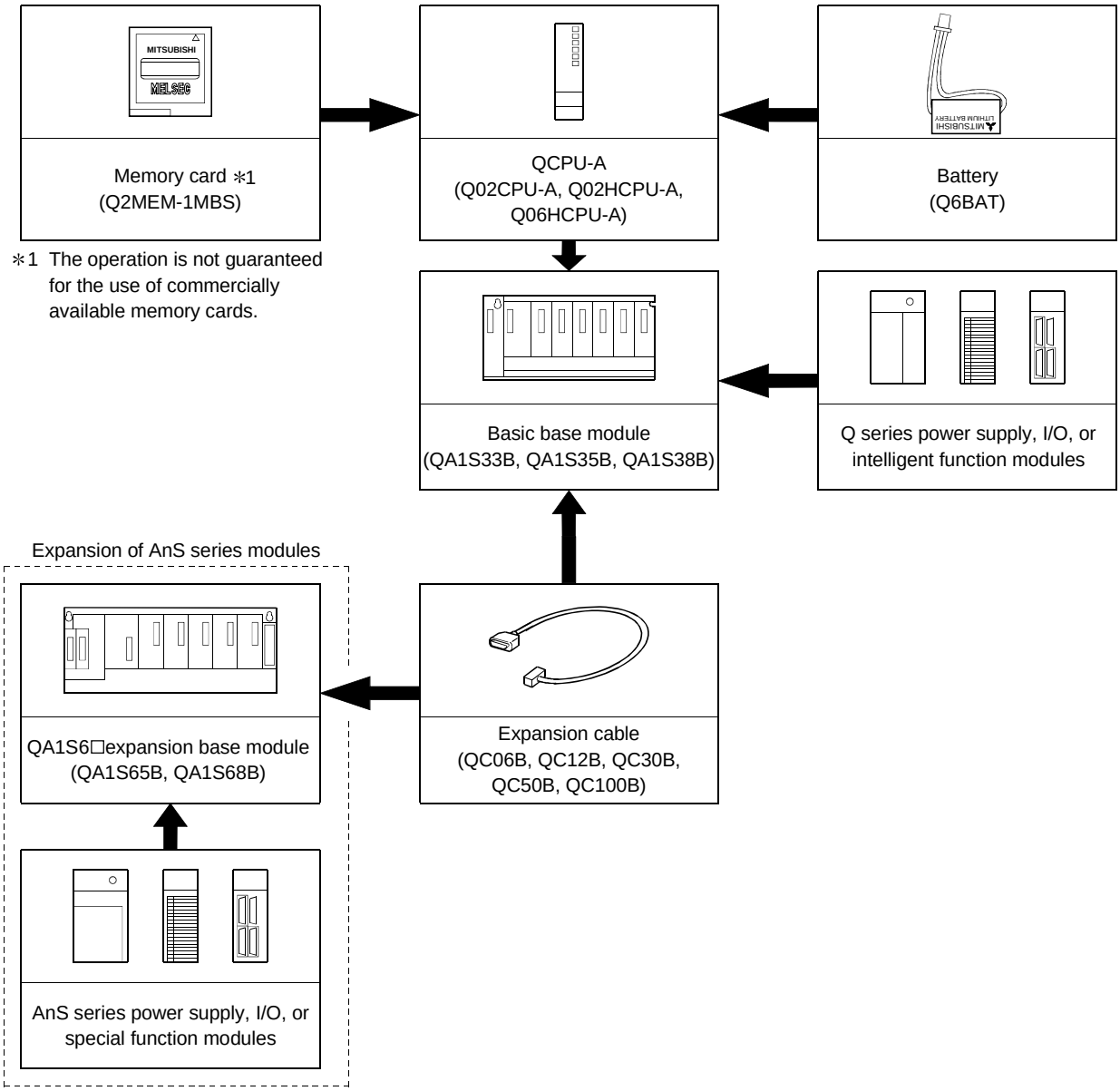
2. SYSTEM CONFIGURATION

This chapter describes the system configuration of QCPU-A, precautions for the use of the system, and system equipment.

2.1 System Configuration

This section describes the device configuration in the QCPU-A system, the configuration of peripheral devices, and the overview of the system configuration.

(1) Device configuration in the QCPU-A system



2.2 Precautions when configuring the system

The precautions when configuring the QCPU-A (A mode) system are as follows:

2.2.1 Hardware

(1) A total of 64 I/O modules or special function modules at maximum can be mounted to each of the basic base module or the expansion base module.

(2) Up to seven expansion base modules can be connected in the system. (Up to eight modules when the basic base module is included.)

(3) The total length of the expansion cable should be 13.2 m or less.

(4) The following modules have some limitations for the number of modules to be mounted.

<table>
<tr><th>Module</th><th colspan="2">No. of mountable modules</th></tr>
<tr><td>MELSECNET/10 network module
A1SJ71LP21, A1SJ71BR11</td><td>Up to 4 modules</td><td rowspan="2">UP to 4 modules in total</td></tr>
<tr><td>MELSECNET(II)/B data link module
A1SJ71AP21, A1SJ71AR21, A1SJ71AT21B</td><td>Up to 2 modules</td></tr>
<tr><td>Interruption module: A1SI61</td><td colspan="2">1 module</td></tr>
<tr><td>AnS series special function module ∗</td><td colspan="2">Up to 6 modules in total</td></tr>
</table>

∗: Applies to the following modules. Modules other than the followings do not have any limitations.
Ethernet interface module: A1SJ71E71B2-S3 (-B5-S3)
Calculating machine link module: A1SJ71UC24-R2 (-R4/-PRF)
CC-Link module (in intelligent mode): A1SJ61BT11
Interface module for data transmission: A1SJ71CMO-S3
Intelligent communication module: A1SD51S
ID interface module: A1SD21-S1
JEMANET (JPCN-1) master module: A1SJ71J92-S3 (only when GET/PUT service is used)

(5) The accessible device range will be limited when the following modules are used:

<table>
<tr><th rowspan="2">Target module</th><th colspan="2">Accessible device range in CPU</th></tr>
<tr><th>Device</th><th>Accessible range</th></tr>
<tr><td rowspan="9">MELSECNET(II) data link module:
A1SJ71AP21, A1SJ71AR21
MELSECNET/B data link module:
A1SJ71AT21B
JEMANET interface module:
A1SJ71J92-S3</td><td>Input (X), output (Y)</td><td>X/Y0~7FF</td></tr>
<tr><td>Internal relay (M)</td><td>M0~8191</td></tr>
<tr><td>Latch relay (L)</td><td>M0~8191</td></tr>
<tr><td>Link relay (B)</td><td>B0~FFF</td></tr>
<tr><td>Timer (T)</td><td>T0~2047</td></tr>
<tr><td>Counter (C)</td><td>C0~1023</td></tr>
<tr><td>Data register (D)</td><td>D0~6143</td></tr>
<tr><td>Link register (W)</td><td>W0~FFF</td></tr>
<tr><td>Annunciator (F)</td><td>F0~2047</td></tr>
</table>

(6) Among the graphic operation terminal GOT series, the GOT-A900/800 series can be used; however, bus connection is not available.

(7) It is recommended that the network and data link modules are mounted to the basic base module.
When these modules are mounted to the expansion base module, the link refresh time will become longer than the case where they are mounted to the basic base module.

2.2.2 Software package

(1) Type name setting when starting the GPP function software package

The following table shows the GPP function software package that can be used to create the QCPU-A (A mode) program, and the PC type setting at startup.
When using SW4D5C-GPPW, select the PC type from Q02(H)-A or Q06H-A according to the CPU to be used.
When using the peripheral devices and GPP function software package of SW3D5C-GPPW or earlier, specify the PC type name as "A4U". If "A4U" is not found in PC type names, specify "A3A." If both "A4U" and "A3A" are not found, specify "A3H."
Note that when "A4U" is specified, the available device range will be limited.

Peripheral device	Software package type name to start system	Type name setting for PC CPU	
		Q02(H)CPU-A	Q06HCPU-A
PC9801	SW4D5C-GPPW or later	Q02(H)-A	Q06H-A
	SW3D5□-GPPW or earlier	A4U	A4U
	SW□NX-GPPA	A4U	A4U
	SW0N-GPPA	A3A	A3A
DOS/V	SW4D5C-GPPW or later	Q02(H)-A	Q06H-A
	SW3D5□-GPPW or earlier	A4U	A4U
	SW□IVD-GPPA		
A7PHP	SW0RX-GPPA	A3A	A3A
	SW0SRX-GPPA		
	SW□SRXV-GPPA	A4U	A4U
A7HGP	SW□HX-GPPA	A4U	A4U
A6PHP	SW3GP-GPPA	A3H	A3H
	SW4GP-GPPA	A3A	A3A
	SW1GP-GPPAU	A4U	A4U
A6GPP	SW3-GPPA, SW-3GP-GPPA	A3H	A3H
	SW4GP-GPPA	A3A	A3A
	SW1GP-GPPAU	A4U	A4U
A7LMS	SW0SRX-GPPA	A3A	A3A
	SW□SRXV-GPPA	A4U	A4U
A75LMS	SW□SRXV-GPPA	A4U	A4U

POINTS

(1) Old software packages other than listed above cannot be used.

(2) To construct MELSECNET/10 network system with QCPU-A (A mode), use the AnU-compatible GPP function software package (which includes "A4U" in its PC type name).
You cannot construct a network with the GPP function software package which is not compatible with AnU (which does not include "A4U" in its PC type name).

(3) Communication with GPPW at 115.2kbps may not be available depending on the peripheral devices. In such a case, select the lower communication speed.

(4) When using Q02(H)CPU-A and conventional peripheral devices and setting the PC type as "A4U," designate the main program setting to 28k steps or less with parameters. When "Main + parameter" is written with the PC with the setting of 29k steps or more, "Cannot communicate with PC" is displayed and writing to the CPU is disabled.

(5) Sub programs cannot be used with Q02(H)CPU-A. When using conventiona peripheral devices and setting the PC type as "A4U," do not specify any sub programs. If sub programs are specified, "Cannot communicate with PC" is displayed.
With Q06HCPU, sub program 1 can be used, but sub programs 2 and 3 cannot.
When sub program 2 or 3 is specified, the same message above is displayed.

(2) Utility package

(a) None of the following utility packages for A6GPP/A6PHP can be used:

- SW□-AD57P
- SW□-UTLP-FN0
- SW□-UTLP-FN1
- SW□-UTLP-PID
- SW□-SIMA
- SW□-UTLP-FD1
- SW□-SAPA

The packages marked with * can execute the same functions using the dedicated instructions. Refer to AnACPU/AnUCPU Programming Manual (Dedicated Instruction) for details.

REMARK

The characters generators and canvas, which are necessary for AD57(S1), are created on the peripheral device using the SW□-AD57P.

POINTS

(1) Packages which access the QCPU-A by specifying a device in the utility package can specify only in the device range for A3ACPU or A3HCPU equivalent. (Refer to Section 2.2.3.)

(2) Use an AnU-compatible utility package to use the device range for the QCPU-A. (Example: SW1IVD-SAP2, etc.)

2.2.3 Precautions when using GPP function software packages and A8PU peripheral devices which are not compatible with AnU

When the QCPU-A is started up using a GPP function software package not compatible with AnU (the PC model name is "A3A" or "A3H") or from an A8PU peripheral device (including A7PU and P7PUS), the usable device range is limited as follows:

(1) Usable device range

System FD peripheral device / Item	AnACPU-compatible module		A3HCPU-compatible module	
	Modules whose PC model for system FD startup is "A3A"	A8PU	Modules whose PC model for system FD startup is "A3H"	A7PU/ A7PUS
Instruction (sequence/basic/ application/dedicated)	All instructions can be used.			
Program capacity	A maximum of 14k steps can be used for the main program.			
I/O device points (X/Y)	X/Y0 to 7FF can be used. (X/Y800 to 1FFF cannot be used.)		X/Y0 to 7FF can be used. (X/Y800 to 1FFF cannot be used.)	
M, L, S relay	M/L/S0 to 8191 can be used.		M/L/S0 to 2047 can be used. (M/L/S2048 to 8191 cannot be used.)	
Link relay (B)	B0 to BFFF can be used (B1000 to B1FFF cannot be used.)		B0 to B3FF can be used. (B400 to B1FFF cannot be used.)	
Timer (T)	T0 to T2047 can be used.		T0 to T255 can be used. (T256 to T2047 cannot be used.)	
Counter (C)	C0 to C1023 can be used.		C0 to C255 can be used. (C256 to C1023 cannot be used.)	
Data register (D)	D0 to D6143 can be used. (D6144 to D8191 cannot be used.)		D0 to D1023 can be used. (D1024 to D8191 cannot be used.)	
Link register (W)	W0 to WFFF can be used. (W1000 to W1FFF cannot be used.)		W0 to W3FF can be used. (W400 to W1FFF cannot be used.)	
Annunciator (F)	F0 to F2047 can be used.		F0 to F255 can be used. (F256 to F2047 cannot be used.)	
Index register (V, Z)	V, V_1 to V_6, Z, and Z_1 to Z_6 can be used.		V and Z can be used. (V_1 to V_6 and Z_1 to Z_6 cannot be used.)	
Expanded comment	A maximum of 3968 points		Unusable	
Latch (power failure compensation) range	The device range shown above can be latched.		The device range shown above can be latched.	
I/O assignment	Number of I/O occupied points and the module model can be registered.		Number of I/O occupied points can be registered.	

(1) The device range other than listed above is the same as that of QCPU-A.
(2) Refer to the operation manual of each peripheral device for available functions.

2.3 System Equipment

The equipment that can be used in the QCPU-A (A mode) system is as follows.
Use the power supply module, I/O module, special function module, and network module that are designed for the AnS series. You cannot use the power supply module, I/O module, special function module, and network module for the Q series, as well as the special function module and network module for the Q2AS series.
The base module and expansion cable for the AnS series and A6SIM-X64Y64 cannot be used either. For details, refer to Q Series Data Book.

Item	Type name	Description	Number of occupied points (points) [I/O allocation module type]	Current consumption (A)	
				DC5V	DC24V
CPU module	Q02CPU-A	Program capacity: 28k steps, I/O points: 4096, Processing speed for basic instruction: 79ns	—	0.60	—
	Q02HCPU-A	Program capacity: 28k steps, I/O points: 4096, Processing speed for basic instruction: 34ns	—	0.64	—
	Q06HCPU-A	Program capacity: 30k steps × 2 (Main/sub), I/O points: 4096, Processing speed for basic instruction: 34ns	—	0.64	—
Memory card	Q2MEM-1MBS	SRAM type: 1 MB	—	—	—
Basic base module	QA1S33B	AnS series module mounting base (power supply module + CPU + 3 slots for other module)	—	0.107	—
	QA1S35B	AnS series module mounting base (power supply module + CPU + 5 slots for other module)	—	0.117 (0.086) ∗	—
	QA1S38B	AnS series module mounting base (power supply module + CPU + 8 slots for other module)	—	0.118 (0.086) ∗	—
Expansion base module	QA1S65B	AnS series module mounting base (power supply module + 5 slots for other module)	—	0.117 (0.088) ∗	—
	QA1S68B	AnS series module mounting base (power supply module + 8 slots for other module)	—	0.118 (0.090) ∗	—
Expansion cable	QC06B	0.6-m expansion base cable	—	—	
	QC12B	1.2-m expansion base cable	—	—	
	QC30B	3.0-m expansion base cable	—	—	
	QC50B	5.0-m expansion base cable	—	—	
	QC100B	10.0-m expansion base cable	—	—	
Battery	Q6BAT	Battery for retaining the contents of program memory and devices in case of power failure	—	—	—
Cable	QC30R2	Communication cable for peripheral devices	—	—	—

∗: The parenthesized values are for those products not provided for CE mark.

POINTS

(1) A USB port cannot be used with QCPU-A (A mode).
(2) A RS232/422 conversion cable is required to use the conventional peripheral devices (A6GPP, A8PUJ, etc.).
Recommended cable: FA-CNV2402CBL (2m), FA-CNV2405CBL (5m)
Contact: Mitsubishi Electric Engineering Corp.

Item	Mode	Description		Number of occupied points (points) [I/O allocation module type]	Current consumption 5VDC (A)	Current consumption 24VDC (A)	Remark
Power supply module	A1S61PN	5VDC, 5A	100/200VAC input	——	——	——	Installed in the power supply slot of the basic base module and expansion base module.
	A1S62PN	5VDC, 3A/24VDC, 0.6A					
	A1S63P	5VDC, 5A	24VDC input				
Input module	A1SX10	16-point 100VAC input module		16 [16 input points]	0.05	——	
	A1SX10EU	16-point 100VAC input module		16 [16 input points]	0.05	——	
	A1SX20	16-point 200VAC input module		16 [16 input points]	0.05	——	
	A1SX20EU	16-point 200VAC input module		16 [16 input points]	0.05	——	
	A1SX30	16-point 12/24VDC, 12/24VAC input module		16 [16 input points]	0.05	——	
	A1SX40	16-point 12/24VDC input module		16 [16 input points]	0.05	——	
	A1SX40-S1	16-point 24VDC input module		16 [16 input points]	0.05	——	
	A1SX40-S2	16-point 24VDC input module		16 [16 input points]	0.05	——	
	A1SX41	32-point 12/24VDC input module		32 [32 input points]	0.08	——	
	A1SX41-S1	32-point 24VDC input module, high-speed sink type, connector included		32 [32 input points]	0.120	——	
	A1SX41-S2	32-point 24VDC input module		32 [32 input points]	0.08	——	
	A1SX42	64-point 12/24VDC input module		64 [64 input points]	0.09	——	
	A1SX42-S1	64-point 24VDC input module, high-speed sink type, connector included		64 [64 input points]	0.160	——	
	A1SX42-S2	64-point 24VDC input module		64 [64 input points]	0.09	——	
	A1SX71	32-point 5/12VDC input module		32 [32 input points]	0.075	——	
	A1SX80	16-point 12/24VDC sink/source input module		16 [16 input points]	0.05	——	
	A1SX80-S1	16-point 24VDC sink/source input module		16 [16 input points]	0.05	——	
	A1SX80-S2	16-point 24VDC sink/source input module		16 [16 input points]	0.05	——	
	A1SX81	32-point 12/24VDC sink/source input module		32 [32 input points]	0.08	——	
	A1SX81-S2	32-point 24VDC sink/source input module		32 [32 input points]	0.08	——	
	A1SX82-S1	64-point 24VDC input module, sink/source type, connector included		64 [64 input points]	0.160	——	
Output module	A1SY10	16-point relay contact output module (2A)		16 [16 output points]	0.12	0.09	
	A1SY10EU	16-point relay contact output module (2A)		16 [16 output points]	0.12	0.09	
	A1SY14EU	12-point relay contact output module (2A)		16 [16 output points]	0.12	0.10	
	A1SY18A	8-point relay contact output module (2A) for independent contacts		16 [16 output points]	0.24	0.075	
	A1SY18AEU	8-point relay contact output module (2A) for independent contacts		16 [16 output points]	0.24	0.075	
	A1SY22	16-point Triac output module (0.6A)		16 [16 output points]	0.27	(200VAC) 0.004	
	A1SY28EU	8-point Triac output module (0.6A)		16 [16 output points]	0.27	——	
	A1SY28A	8-point Triac output module (1A) All points independent		16 [16 output points]	0.11	——	
	A1SY40	16-point 12/24VDC transistor output module (0.1A) sink type		16 [16 output points]	0.27	0.016	
	A1SY41	32-point 12/24VDC transistor output module (0.1A) sink type		32 [32 output points]	0.50	0.016	
	A1SY42	64-point 12/24VDC transistor output module (0.1A) sink type		64 [64 output points]	0.93	0.016	
	A1SY50	16-point 12/24VDC transistor output module (0.5A) sink type		16 [16 output points]	0.12	0.12	
	A1SY60	16-point 24VDC transistor output module (2A) sink type		16 [16 output points]	0.12	0.015	
	A1SY60E	16-point 12DCV transistor output module (1A) source type		16 [16 output points]	0.20	0.01	

Item	Mode	Description	Number of occupied points (points) [I/O allocation module type]	Current consumption		Remark
				5VDC (A)	24VDC (A)	
Output module	A1SY68A	8-point 5/12/24/48VDC transistor output module sink/source type All points independent	16 [16 output points]	0.13	——	
	A1SY71	32-point 5/12VDC transistor output module (0.016A) sink type	32 [32 output points]	0.40	0.15	
	A1SY80	16-point 12/24VDC transistor output module (0.8A) source type	16 [16 output points]	0.12	0.04	
	A1SY81	32-point 12/24VDC transistor output module (0.1A) source type	32 [32 output points]	0.50	0.016	
	A1SY81EP	32-point 12/24VDC transistor output module (0.1/0.05A) source type	32 [32 output points]	0.50	0.016	
	A1SY82	32-point 12/24VDC output module (0.1 A), source type, connector and fuse included	64 [64 output points]	0.930	0.016	
I/O hybrid module	A1SH42	32-point 12/24VDC input module 32-point 12/24VDC transistor output module(0.1A) sink type	32 [32 output points]	0.50	0.008	
	A1SH42-S1	32-point 24VDC input/32-point 24VDC output module (0.1 A), connector and fuse included	32 [32 output points]	0.500	0.008	
	A1SX48Y18	8-point 24VDC input module 8-point relay contact output module	16 [16 output points]	0.085	0.045	
	A1SX48Y58	8-point 24VDC input module 8-point 12/24VDC transistor output module	16 [16 output points]	0.06	0.06	
Dynamic input module	A1S42X	16/32/48/64 points 12/24VDC dynamic input module	Specified number of points [Input specified number of points]	0.08	——	
Dynamic output module	A1S42Y	16/32/48/64 points 12/24VDC dynamic output module	Specified number of points [Output specified number of points]	0.10	0.008	
Blank cover	A1SG60	Dust-proof cover for unused slot	16 [Empty]	——	——	
Dummy module	A1SG62	16-point, 32-point, 48-point, or 64-point selectable module	Specified number of points [Input specified number of points]	——	——	
40-pin connector	A6CON1	Soldering type	——	——	——	
	A6CON2	Solderless type				
	A6CON3	Press-fit type				
37-pin D-sub connector	A6CON1E	Soldering type	——	——	——	
	A6CON2E	Solderless type				
	A6CON3E	Press-fit type				
Pulse catch module	A1SP60	16-point input module for short ON-time pulse input (pulse with a minimum of 0.5ms)	16 [16 output points]	0.055	——	
Analog timer module	A1ST60	8-point analog timer module whose timer setting value can be changed for different volumes (0.1 to 1.0s, 1 to 10s, 10 to 60s, 60 to 600s)	16 [16 output points]	0.055	——	
Interrupt module	A1SI61	Interrupt module for specifying the interrupt program (16-point interrupt input)	32 [32 special points]	0.057	——	
High-speed counter module	A1SD61	32-bit signed binary 50kbps, 1 channel	32 [32 special points]	0.35	——	
	A1SD62	DC input/sink output type	32 [32 special points]	0.14	——	
	A1SD62D	Differential input/sink output type (preset DC input)	32 [32 special points]	0.25	——	
	A1SD62E	DC input/source output type	32 [32 special points]	0.14	——	
A/D converter module	A1S64AD	4 to 20mA/0 to 10V 4 analog channels	32 [32 special points]	0.4	——	
	A1S68AD	Analog input: 8 channels	32 [32 special points]	0.40	——	
Temperature/ digital converter module	A1S62RD3	For Pt100 (3-wire type) connection 2 channels of temperature input	32 [32 special points]	0.54	——	
	A1S62RD4	For Pt100 (4-wire type) connection 2 channels of temperature input	32 [32 special points]	0.44	——	
	A1S68TD	Thermocouple input: 8 channels	32 [32 special points]	0.32	——	

Item	Mode	Description	Number of occupied points (points) [I/O allocation module type]	Current consumption		Remark
				5VDC (A)	24VDC (A)	
D/A converter module	A1S62DA	4 to 20mA/0 to 10V 2 analog output channels	32 [32 special points]	0.8	——	
	A1S68DAV	0 to ±10V analog output: 8 channels	32 [32 special points]	0.65	——	
	A1S68DAI	0 to ±20mA analog output: 8 channels	32 [32 special points]	0.85	——	
Analog I/O module	A1S63ADA	Analog input, 2 channels, simple loop control is allowed. Analog output, 1 channel	32 [32 special points]	0.8	——	
	A1S66ADA	Analog input: 4 channels, analog output: 2 channels	64 [64 special points]	0.16	——	
Temperature adjustment module	A1S64TCTT-S1	Thermocouple input: 4 channels	32 [32 special points]	0.42	——	
	A1S64TCTTBW-S1	Thermocouple input: 4 channels with heater disconnection detection function	32 [32 special points]	0.42	——	
	A1S64TCRT-S1	Pt100 input: 4 channels	32 [32 special points]	0.42	——	
	A1S64TCRTBW-S1	Pt100 input: 4 channels with heater disconnection detection function	32 [32 special points]	0.42	——	
	A1S62TCTT-S2	Thermocouple input: 2 channels	32 [32 special points]	0.28	——	
	A1S62TCTTBW-S2	Thermocouple input: 2 channels with heater disconnection detection function	32 [32 special points]	0.28	——	
	A1S62TCRT-S2	Pt100 input: 2 channels	32 [32 special points]	0.28	——	
	A1S62TCRTBW-S2	Pt100 input: 2 channels with heater disconnection detection function	32 [32 special points]	0.28	——	
Computer link module	A1SJ71UC24-R2	Computer link function, RS-232C, 1 channel	32 [32 special points]	0.1	——	
	A1SJ71UC24-PRF	Computer link function, printer function RS-232C, 1 channel	32 [32 special points]	0.1	——	
	A1SJ71UC24-R4	Computer link function, multidrop link function RS-422/RS-485, 1 channel	32 [32 special points]	0.1	——	
Ethernet interface module	A1SJ71E71-B2-S3	10 Base 2 (for Cheapernet)	32 [32 special points]	0.52	——	
	A1SJ71E71-B5-S3	10 Base 5 (for Ethernet)	32 [32 special points]	0.35	——	
Intelligent communication module	A1SD51S	BASIC (interpreter/compiler) RS-232C, 2 channels RS-422/485, 1 channel	32 [32 special points]	0.4	——	
Positioning module	A1SD70	Analog voltage output (0 to ±10V) for 1-axis positioning control, speed control, and speed-positioning control.	48 [First half: 16 empty points] [Second half: 32 special points]	0.3	——	
	A1SD71-S2	For positioning control, speed control, and speed-positioning control. Pulse train output, 2-axis (independent, 2-axis simultaneous, linear interpolation		0.8	——	
	A1SD71-S7	For positioning control, setting for manual pulse output speed can be changed. Pulse train output, 2-axis (independent, 2-axis simultaneous, linear interpolation)		0.8	——	
	A1SD75M1	SSC Net compatible, 1 axis	32 [32 special points]	0.70	——	
	A1SD75M2	SSC Net compatible, 2 axis				
	A1SD75M3	SSC Net compatible, 3 axis				
	A1SD75P1-S3	Pulse train output, 1 axis	32 [32 special points]	0.70	——	
	A1SD75P2-S3	Pulse train output, 2 axis				
	A1SD75P3-S3	Pulse train output, 3 axis				
	A1SD774M	4-axis motion control module	32 [32 special points]	0.90	——	
ID interface module	A1SJ71ID1-R4	One reader/writer module can be connected.	32 [32 special points]	0.25	0.1	
	A1SJ71ID2-R4	Two reader/writer modules can be connected.	32 [32 special points]	0.25	0.15	
	A1SD32D1	One reader/writer module can be connected.	32 [32 special points]	0.25	0.15	
	A1SD32D2	Two reader/writer modules can be connected.	32 [32 special points]	0.25	0.30	

Item	Mode	Description	Number of occupied points (points) [I/O allocation module type]	Current consumption		Remark
				5VDC (A)	24VDC (A)	
MELSECNET(II) data link module	A1SJ71AP21	For the master and local stations of MELSECNET(II) data link system (for the optical fiber cable)	32 [32 special points]	0.33	——	Access is allowed within the device range of the A3ACPU.
	A1SJ71AP21-S3	For the master and local stations of MELSECNET(II) data link system (for the GI-type optical fiber cable)	32 [32 special points]	0.33	——	
	A1SJ71AR21	For the master and local stations of MELSECNET(II) data link system (for the coaxial cable)	32 [32 special points]	0.8	——	
MELSECNET/B data link module	A1SJ71T21B	For the master and local stations of MELSECNET/B data link system	32 [32 special points]	0.66	——	
	A1SJ72T25B	For the remote I/O station of MELSECNET/B data link system	——	0.3	——	
Paging module	A1SD21-S1	Number of connectable transmitter: 1, Radius of transmission area: Approx. 50m	32 [32 special points]	0.14	——	
Position detection module	A1S62LS	Absolute position detection by special detector	32 [32 special points]	0.55	——	
PC simple monitoring module	A1SS91	PC simple monitoring module	16 [16 output points]	0.080	——	
Memory card interface module	A1SD59J-S2	Memory card interface module	32 [32 special points]	0.05		The current consumption data is obtained when A1SD59J-MIF is mounted.
MELSECNET/10 data link module	A1SJ71LP21	For the control, master, and normal stations of the MELSECNET/10 data link module system (For the dual loop SI-type optical fiber cable)	32 [32 special points]	0.65	——	
	A1SJ71BR11	For the control, master, and normal stations of the MELSECNET/10 data link module system (For the single bus coaxial cable)	32 [32 special points]	0.80	——	
CC-Link system master module	A1SJ61BT11	For the master and local stations of the CC-Link data link system (For the twisted pair shield cable only.)	32 [32 special points]	0.40	——	
MELSECNET/ MINI-S3 master module	A1SJ71PT32-S3	For MELSECNET/MINI-S3 master stations (max. 64 stations). Performs remote I/O and remote terminal control of a total of 512 I/O points.	I/O dedicated mode 32 [32 special points] Expanded mode 48 [48 special points]	0.35	——	
	A1SJ71T32-S3	MELSECNET/MINI-S3 master station Performs remote I/O and remote terminal control of a maximum 64 stations and a total of 512 I/O points. (For the twisted pair cable only.)	I/O dedicated mode 32 [32 special points] Expanded mode 48 [48 special points]	0.30	——	
MELSECNET-I/O LINK master module	A1SJ51T64	MELSECNET-I/O LINK master station. Controls I/O LINK remote I/O module of a maximum of 64 stations and a total of 128 I/O points.	64 [64 output points]	0.115	0.09	
Graphic operation terminal	A900GOT	A900GOT series Refer to the manual of each GOT.	——	——	——	

Item	Mode	Contents	Applicable models
Connector/terminal block converter unit	A6TBXY36	For the sink-type input module and sink-type output module. (standard type)	A1SX41(S2), A1SX42(S2), A1SY41, A1SY42, A1SH42 AX42(S1), AY42(S1/S3/S4), AH42
	A6TBXY54	For the sink-type input module and sink-type output module. (2-wire type)	
	A6TBX70	For the sink-type input module. (3-wire type)	A1SX41(S2), A1SX42(S2), A1SH42, AX42(S1), AH42
	A6TBX36-E	For the source-type input module. (standard type)	A1SX81(S2), AX82
	A6TBY36-E	For the source-type output module. (standard type)	A1SY81, AY82EP
	A6TBX54-E	For the source-type input module. (2-wire type)	A1SX81(S2), AX82
	A6TBY54-E	For the source-type output module. (2-wire type)	A1SY81, AY82EP
	A6TBX70-E	For the source-type input module. (3-wire type)	A1SX81(S2), AX82
Cable for the connector/terminal block converter unit	AC05TB	0.5m (1.64 ft.) for the source module	A6TBXY36 A6TBXY54 A6TBX70
	AC10TB	1m (3.28 ft.) for the source module	
	AC20TB	2m (6.56 ft.) for the source module	
	AC30TB	3m (9.84 ft.) for the source module	
	AC50TB	5m (16.40 ft.) for the source module	
	AC05TB-E	0.5m (1.64 ft.) for the source module	A6TBX36-E A6TBY36-E A6TBX54-E A6TBY54-E A6TBX70-E
	AC10TB-E	1m (3.28 ft.) for the source module	
	AC20TB-E	2m (6.56 ft.) for the source module	
	AC30TB-E	3m (9.84 ft.) for the source module	
	AC50TB-E	5m (16.40 ft.) for the source module	
Relay terminal unit	A6TE2-16SRN	For the sink-type output module	A1SY41, A1SY42, A1SH42, AY42, AY42-S1, AY42-S3, AY42-S4, AH42
Cable for connecting the relay terminal unit	AC06TE	0.5m (1.64 ft.) long	A6TE2-16SR(N)
	AC10TE	1m (3.28 ft.) long	
	AC30TE	3m (9.84 ft.) long	
	AC50TE	5m (16.40 ft.) long	
	AC100TE	10m (32.81 ft.) long	
Terminal block cover for the A1S I/O module and the special module	A1STEC-S	Slim-type terminal block cover for the A1S I/O module and the special module (terminal block type).	A1SX10, A1SX20, A1SX30, A1SX40(S1/S2), A1SX80(S1/S2), A1SY10, A1SY18A, A1SY22, A1SY28A, A1SY40, A1SY50, A1SY60(E), A1SY68A, A1SY80 A1SX48Y18, A1SX48Y58 A1SI61, A1S64AD, A1S62DA, A1S63ADA, A1S62RD3/4, A1SD61, A1SP60

(2) Peripheral devices

Item	Mode	Remark	
Plasma hand-held graphic programmer	A6PHP-SET	A6PHP main module • SW□GP-GPPA.....GPP function startup floppy disk for the A series. • SW□GP-GPPK.....GPP function startup floppy disk for the K series. • SW0-GPPU.....User floppy disk (2DD). • AC30R4 .....3m (9.84 ft.)-long RS-422 cable.	
Intelligent GPP	A6GPP-SET	• A6GPP main module • SW□GP-GPPA.....GPP function startup floppy disk for the A series. • SW□GP-GPPK.....GPP function startup floppy disk for the K series. • SW0-GPPU.....User floppy disk (2DD). • AC30R4 .....3m (9.84 ft.)-long RS-422 cable.	
Composite video cable	AC10MD	• Connection cable for the monitor display of the A6GPP screen. 1m (3.28 ft.)long	
RS-422 cable	AC30R4	3m (9.84 ft.) long	Connection cable for between the CPU main module and A6GPP/A6PHP
	AC300R4	30m (98.43 ft.) long	
User floppy disk	SW0-GPPU	2DD-type	Floppy disk for storing user programs (3.5-inch, pre-formatted)
Cleaning floppy disk	SW0-FDC	For A6GPP/A6PHP	Floppy disk for cleaning the floppy disk drive.
Optional keyboard for A6PHP	A6KB-SET-H	• A6KB keyboard • AC03R4H.....0.3m (0.98 ft.)-long connection cable between A6KB and A6PHP. • A6KB-C.....Key sheet for the GPP mode of A6KB.	
Optional keyboard for A6GPP	A6KB-SET	• A6KB keyboard • AC03R4L .....0.3m (0.98 ft.)-long connection cable between A6KB and A6GPP. • A6KB-C.....Key sheet for the GPP mode of A6KB.	
Printer	K6PR(S1) K6PR-K K7PR(S1) A7PR A7NPR	• For printing out program circuit diagrams and various lists.	
RS232C cable	AC30R2	Connection cable for between A6GPP/A6PHP and printer (K6PR(S1), K6PR-K, K7PR(S1), A7PR, A7NPR, and a general-purpose printer with RS-232C interface) 3m (9.84 ft.) long	
Printer paper	K6PR-Y K7PR-Y	Printer paper for K6PR(S1) and K6PR-K. 9-inch paper. 2000 sheets per unit Printer paper for A7PR and A7NPR. 11-inch paper. 2000 sheets per unit.	
Inked ribbon for K6PR (K)	K6PR-R	Replacement inked ribbon for K6PR(S1) and K6PR-K.	
Inked ribbon for A7PR	A7PR-R	Replacement inked ribbon for A7PR.	
Inked ribbon for A7NPR	A7NPR-R	Replacement inked ribbon for A7NPR.	
Programming module	A7PU	• Read/write of the program is performed by connecting to the CPU main module with a RS-422 cable (AC30R4, AC300R4). This is equipped with the MT function. (5VDC 0.4A) • A7PU comes with a connection cable for between the main module and an audio cassette recorder.	
	A7PUS	Read/write of the program is performed by connecting to the CPU main module with a RS-422 cable (AC30R4-PUS). (5VDC 0.4A)	
	A8PU A8UPU	Read/write of the program is performed by connecting to the CPU main module with a RS-422 cable (AC30R4-PUS, AC20R4-A8PU). (5VDC 0.4A)	

Item	Mode	Remark
RS-422 cable	AC30R4 AC300R4	Connection cable for between the CPU main module and A7PU. 3m/30m (9.84 ft./98.43 ft.) long
	AC30R4-PUS	Connection cable for between the CPU main module and A7PUS, A8PU, A8UPU. 3m (9.84 ft.) long
	AC20R4-A8PU	Connection cable for between the CPU main module and A8PU, A8UPU. 2m (6.56 ft.) long
Data access module	A6DU-B	• Used for monitoring the CPU devices, changing the setting values/ current values, and displaying the operation status. (5VDC 0.23A) • Connect to the CPU with an AC30R4-PUS cable.
Modem interface module	A6TEL	• An interface module which connects the PC CPU and the modem. Using a telephone line, the communication is performed between a remote peripheral device and the CPU. (5VDC 0.2A)
RS-422 cable	AC30R4 AC300R4	Connection cable for between the CPU main module and A6WU. 3m/30m (9.84 ft./98.43 ft.) long.
	AC03WU	Connection cable for between the A6PHP main module and A6WU. 0.3m (0.98 ft.) long.

2.4 System Configuration Overview

There are four system configuration types as follows:

(1) Stand-alone system ..... A system with a basic base module only, or with a basic base system and an extension base module connected with the expansion cable.

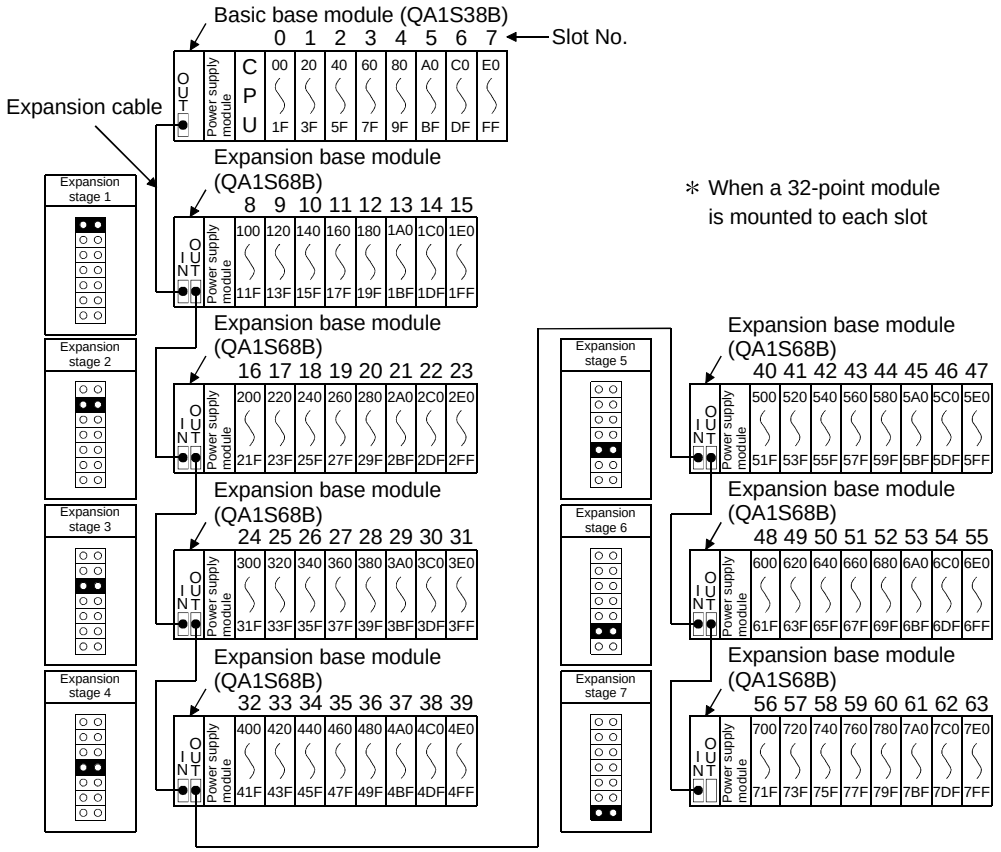
(2) Network system ..... A system for controlling multiple PCs and remote I/O modules.

(3) Computer link system ..... A system for data exchange between the QCPU-A and the computer (personal computer, etc.) by using an A1SJ71UC24 computer link module.

(4) Composite system ..... A system which has a combination of a network system and a computer link system.

The details of the system configuration, number of I/O points, I/O number assignment, etc., of a stand-alone system are listed on the following page.

2.4.1 QCPU-A (A mode) system

System configuration	
Max. number of expansion stages	Expansion stage 7
Max. number of I/O modules to be mounted	64 modules
Max. I/O points	4096
Type name of basic base module	QA1S33B, QA1S35B, QA1S38B
Type name of expansion base module	QA1S65B, QA1S68B
Type name of expansion cable	QC06B, QC12B, QC30B, QC50B, QC100B
Caution	(1) Up to seven expansion base modules can be added. (2) Limit the total length of the expansion cable to 13.2m or less. (3) When using the expansion cable, do not bind it with or place it close to the main circuit (high-voltage, large-current) lines. (4) Assign the expansion stages in ascending order. Do not assign two or more modules to one stage. (5) Connect the expansion cable from OUT of the expansion cable connector of the base module to IN of the connector of the next expansion base module.

3. GENERAL SPECIFICATION

The general specification common to various modules is shown.

Table 3.1 General specification

<table>
<tr><th>Item</th><th colspan="5">Specification</th></tr>
<tr><td>Operation ambient temperature</td><td colspan="5">0 to 55°C</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">-20 to 75°C</td></tr>
<tr><td>Operation ambient humidity</td><td colspan="5">10 to 90%RH, no condensation</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90%RH, no condensation</td></tr>
<tr><td rowspan="8">Vibration durability</td><td rowspan="8">Conforms to the JIS B 3501 and IEC 61131-2</td><td colspan="4">When there is intermittent vibration</td></tr>
<tr><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep count</td></tr>
<tr><td>10 to 57Hz</td><td>——</td><td>0.075mm (0.003 in.)</td><td rowspan="5">10 times each in X, Y, and Z directions (80 minutes)</td></tr>
<tr><td>57 to 150Hz</td><td>9.8m/s^2 {1G}</td><td>——</td></tr>
<tr><td colspan="3">When there is continuous vibration</td></tr>
<tr><td>Frequency</td><td>Acceleration</td><td>Amplitude</td></tr>
<tr><td>10 to 57Hz</td><td>——</td><td>0.035mm (0.001 in.)</td></tr>
<tr><td>57 to 150Hz</td><td>4.9m/s^2 {0.5G}</td><td>——</td></tr>
<tr><td>Shock durability</td><td colspan="5">Conforms to the JIS B 3501 and IEC 61131-2 (147 m/s^2 {15G}), 3 times each in 3 directions)</td></tr>
<tr><td>Operation ambiance</td><td colspan="5">No corrosive gas</td></tr>
<tr><td>Operation height</td><td colspan="5">2000m (6562 ft.) or less</td></tr>
<tr><td>Installation area</td><td colspan="5">On the control panel</td></tr>
<tr><td>Over-voltage category ＊1</td><td colspan="5">II or less</td></tr>
<tr><td>Pollution level ＊2</td><td colspan="5">2 or less</td></tr>
</table>

＊1: Indicates the location the device is connected, from the public cable network to the device structure wiring area.
Category II applies to the devices to which the power is supplied from a fixed equipment.
Surge withstand voltage for devices with up to 300V of rated voltage is 2500V.

＊2: This is an index which indicates the degree of conductive object generation in the environment where the device is used. Pollution level 2 is when only non-conductive pollution occurs. A temporary conductivity caused by condensation must be expected occasionally.

＊3: Do not use or store the PC in the environment where the pressure is higher than the atmospheric pressure at sea level. Otherwise, malfunction may result. To use the PC in high-pressure environment, contact your nearest Mitsubishi representative.

MEMO

4. CPU MODULE

4.1 Performance Specification

The performance specifications of QCPU-A are shown below:

Item		Q02CPU-A	Q02HCPU-A	Q06HCPU-A	Remark
Control method		Repeated operation of stored program			
I/O control method		Refresh method (Partial refresh is available with a program.)			
Program language		Dedicated language for sequence control (Ladder, list, SFC)			
Processing speed (LD instruction)		79 (ns/step)	34 (ns/step)		
Number of instructions (type)	Sequence instructions	25			
	Basic and application instructions	233			
	Dedicated instructions	213			
Memory capacity		144k bytes of program memory + 144k bytes of standard ROM			
Program capacity (steps)	Main program	28k steps max.		30k steps max.	Set by parameters
	Sub program	None		30k steps max.	
I/O device points [X/Y] (points)		8192 (X/Y 0 to 1FFF) (Total points available on programs including remote I/O)			Note that the available device range may be limited depending on the programming software to be used.
I/O points [X/Y] (points)		4096 (Points can be controlled on basic and expansion base modules)			
Device points	Internal relay [M] (points)	7144 (M0 to M999, M2048 to M8191)			
	Latch relay [L] (points)	1048 (L1000 to L2047)			Total of 8192 are shared by M, L, and S.
	Step relay [S] (points)	0 (None for the initial state)			
	Link relay [B] (points)	8192 (B0 to B1FFF)			
	Timer [T] (points)	2048 (Default: 256 points) • 100ms timer (T0 to T199).....Setting time: 0.1 to 3276.7s • 10ms timer (T200 to T255).....Setting time: 0.01 to 327.67s • 100ms retentive timer (None for initial state).....Setting time: 0.1 to 3276.7s • Expansion timer (T256 to T2047).....Count value is set by word device (D, W, and R). • 1ms timer (None for initial state) .....Setting time: 0.001 to 32.767s (The latter half of the retentive timer can be used by ZHTIME instruction.)			
	Counter [C] (points)	1024 (Default: 256 points) • Normal counter (C0 to C255).....Setting range: 1 to 32767 counts • Interrupt counter (None for initial state).....C224 to C255 are possible depending on setting. • Expansion counter (C256 to C1023).....Count value is set by word device (D, W, and R).			
	Data register [D] (points)	8192 (D0 to D8191)			
	Link register [W] (points)	8192 (W0 to W1FFF)			
	Annunciator [F] (points)	2048 (F0 to F2047)			
	File register [R] (points)	8192 (R0 to R8191)			
	Accumulator [A] (points)	2 (A0, A1)			
	Index register [V, Z] (points)	14 (V, V_1 to V_6, Z, Z_1 to Z_6)			
	Pointer [P] (points)	256 (P0 to P255)			
	Interrupt pointer [I] (points)	32 (I0 to I31)			
	Special relay [M] (points)	256 (M9000 to M9255)			
	Special register [D] (points)	256 (D9000 to D9255)			

(Performance specifications--continued)

Item	Q02CPU-A	Q02HCPU-A	Q06HCPU-A	Remark
Comment (point)	4032 max. (Can be set in units of 64 points)			
Expansion comment (point)	3968 max. (Can be set in units of 64 points)			
Output mode selection from STOP to RUN	Selectable from re-outputting operation status before STOP (default) or starting output after operation			Set by parameters
Self-diagnostic function	Monitoring congestion of operations (watchdog timer: 200ms fixed), Detection of abnormality in memory, CPU, I/O, or battery			
Operation mode at error	Selectable from stop or continue			Set by parameters
Latch (power failure compensation) range	L1000 to L2047 (default) (Latch range can be set for L, B, T, C, D, and W.)			
Remote RUN/PAUSE contact	One point set for each of RUN/PAUSE contact from X0 to X1FFF			
Print title registration	Available (128 characters)			
Keyword registration	Available			
I/O assignment	Registration of occupied I/O points and module type name			
Step operation	Execute/stop of sequence program operations			
Constant scan (ms)	10 to 190 (Can be set in units of 10ms)			Set at special register D9020
Clock function	Year, month, day, hour, minute, second, day of week (leap year automatic detection) Accuracy – 3.18 to + 5.25s (TYP. + 2.12s)/d at 0 °C – 3.93 to + 5.25s (TYP. + 1.90s)/d at 25 °C – 14.69 to + 3.53s (TYP. – 3.67s)/d at 55 °C			
Internal current consumption at 5VDC (A)	0.60	0.64	0.64	
Weight (kg)	0.20	0.20	0.20	
Dimensions (mm)	98 (H) × 27.4 (W) × 89.3 (D)			

4.1.1 Overview of operation processing

An overview of processing subsequent to starting power supply for QCPU-A to execution of the sequence program is explained.
QCPU-A's processing may be categorized roughly into the following four kinds:

(1) Initial processing

This is a preprocess to execute sequence operations, and is performed only once upon power-on or reset.

(a) Resets the I/O module and initialize it.

(b) Initializes the range of data memory for which latch is not set up (sets the bit device to OFF and the word device to 0).

(c) Allocates I/O address of the I/O module automatically based on the I/O module number or the position of installation on the extension base module.

(d) Executes the check items for power-on and reset among the PC CPU's self-diagnosis items (Refer to 4.1.4).

(e) For the control station of the MELSECNET/10 or the master station of MELSECNET (II)/B, sets the network/link parameter information to the network/data-link module, and commences the network communication/data link.

(2) Refresh processing of I/O module

Executes the refresh processing of I/O module. (Refer to the ACPU Programming Manual (Fundamentals).)

(3) Operation processing of a sequence program

Executes a sequence program from step 0 to the END instruction written in the PC CPU.

(4) END processing

This is a post-process to finish one cycle of operation processing of the sequence program and to return the execution of the sequence program to the step 0.

(a) Performs self-diagnosis checks, such as fuse blown, I/O module verification, and low battery. (Refer to Section 4.1.4.)

(b) Updates the current value of the timer, sets the contact ON/OFF, updates the current value of the counter and sets the contact to ON. (Refer to the ACPU Programming Manual (Fundamentals).)

(c) Performs data exchange between PC CPU and computer link module when there is a data read or write request from a computer link module. (A1SJ71UC24-R2, AJ71C24(S3), AD51(S3), etc.)

(d) Performs the refresh processing when there is a refresh request from the network module or link module.

(e) When the trace point setting of sampling trace is by each scan (after the execution of END instruction), stores the condition of the device for which it is setup into the sampling trace area.

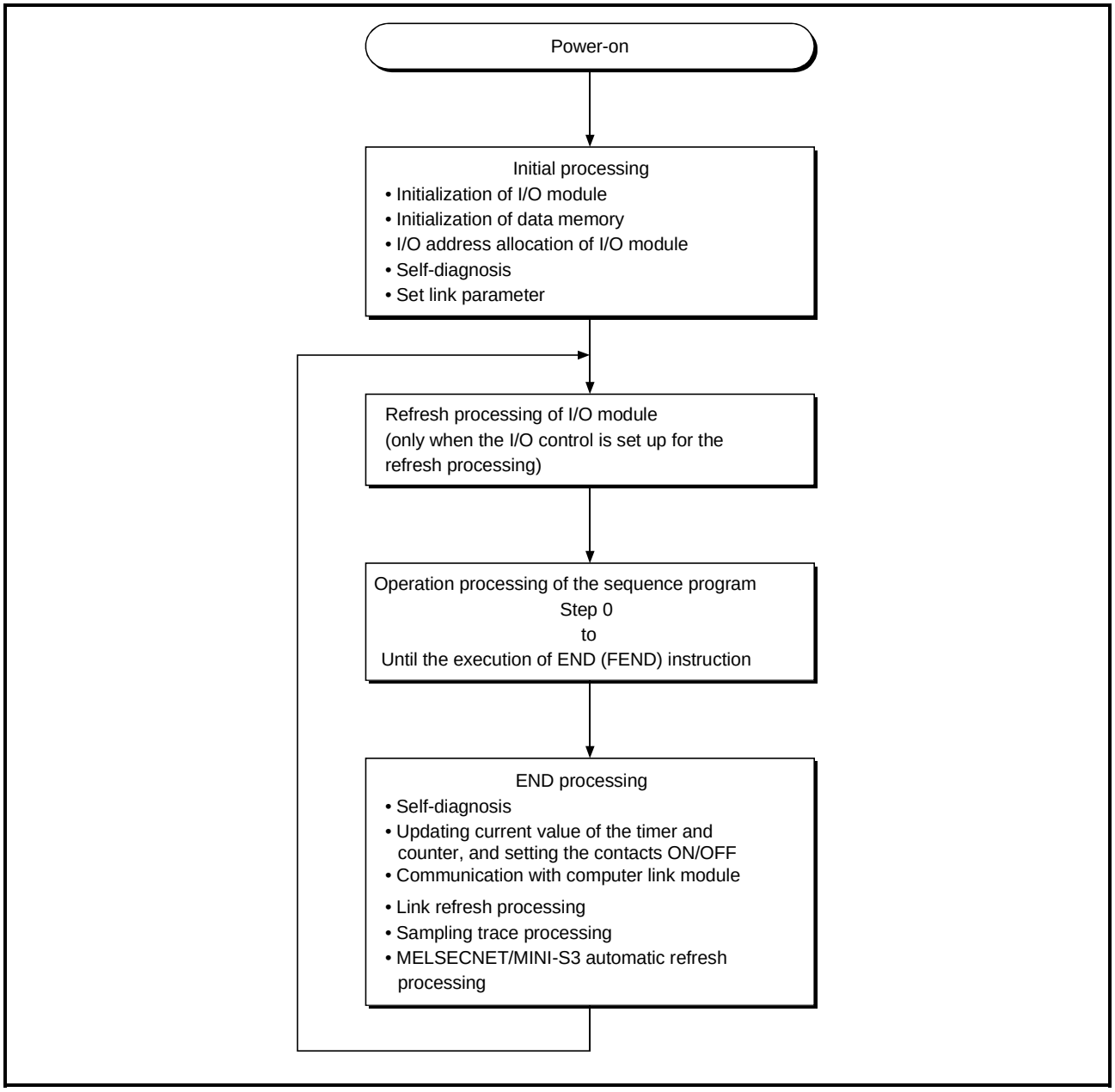


Figure 4.1 QCPU-A operation processing

4.1.2 Operation processing of RUN, STOP, PAUSE, and STEP RUN

The PC CPU has four kinds of operation states: RUN state, STOP state, PAUSE state, and step operation (STEP RUN) state.
Operation processing of PC CPU in each operation state is explained.

(1) RUN state operation processing

(a) The repetition of sequence program operation in the order from step 0 → END (FEND) instruction → step 0 is called the RUN state.

(b) When entering the RUN state, the output state escaped by STOP is output depending on the output mode setting of parameter upon STOP → RUN.

(c) Processing time from switching from STOP to RUN until the startup of sequence program is usually one to three seconds, yet it may vary depending on the system configuration.

(2) STOP state operation processing

(a) The termination of operation of the sequence program by the use of RUN/STOP switch or the remote STOP is called the STOP state. (Refer to Section 4.3.)

(b) When entering the STOP state, it escapes the output state and sets all output points to OFF. Data memories except for output (Y) are retained.

(3) PAUSE state operation processing

(a) The termination of operation of sequence program while retaining output and data memories is called the PAUSE state. (Refer to Section 4.3.)

(4) Step operation (STEP RUN) operation processing

(a) Step operation is an operation mode wherein operation processing of a sequence program can be paused/resumed by each instruction from peripheral device(s). (Refer to Section 4.3.)

(b) Since an operation processing is paused while retaining the output and data memories, condition of the execution can be confirmed.

(5) Operation processing of PC CPU when RUN/STOP switch is operated

PC CPU operation processing / RUN/STOP key switch operation	Operation processing of the sequence program	External output	Data memories (Y, M, L, S, T, C, D)	Remark
RUN → STOP	Executes up to the END instruction, then stops.	OS escapes the output state, and sets all the output points to OFF.	Maintains the condition immediately prior to entering the STOP state.	
STOP → RUN	Starts.	Determined by the output mode of the parameter upon STOP → RUN.	Starts operations from the condition immediately prior to entering the STOP state.	

POINTS

Whether in the RUN, STOP or PAUSE state, PC CPU is performing the following:

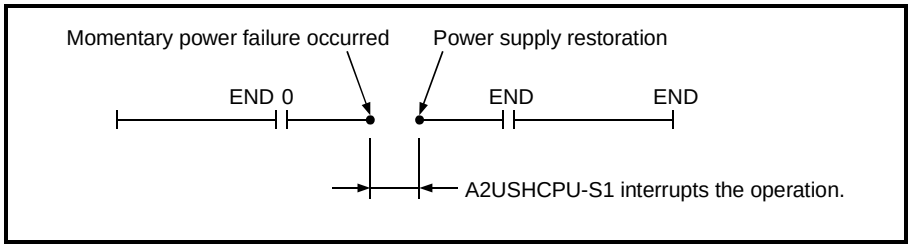
- Refresh processing of I/O module
- Data communication with computer link module
- Link refresh processing.

Thus, even in the STOP or PAUSE state, monitoring or testing I/O with peripheral devices, reading or writing from a computer link module, and communication with other stations by MELSECNET are possible.

4.1.3 Operation processing upon momentary power failure

The PC CPU detects a momentary power failure when input power voltage supplied to the power supply module becomes lower than the specified range.
When the PC CPU detects a momentary power failure, following operation processing is performed.

(1) When a momentary power failure shorter than allowable period of momentary power failure occurred:
   (a) When a momentary power failure occurred, operation processing is interrupted while the output state is retained.
   (b) When the momentary power failure is reset, operation processing will be continued.
   (c) When a momentary power failure occurred and the operation was interrupted, measurement of the watchdog timer (WDT) continues. For instance, when the scan time is 190ms and a momentary power failure of 15ms occurs, it causes the watchdog timer error (200ms).



Operation processing upon momentary power failure

(2) When a momentary power failure longer than the allowable period of momentary power failure occurred:
   The PC CPU performs the initial start. The operation processing is the same as power-on or reset operation with the reset switch.

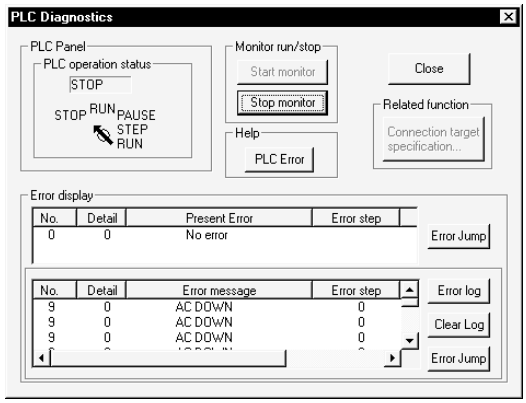
4.1.4 Self-diagnosis

Self-diagnosis is a function with which A2USHCPU-S1 diagnoses itself for the presence of any abnormalities.

(1) Upon turning on the power supply to PC or when an abnormality occurred while the PC is running, the QCPU-A's self-diagnosis processing prevents malfunctions of the PC and performs preventive maintenance by detecting the abnormality, displaying an error display, halting the operation of QCPU-A, and so on.

(2) QCPU-A stores the error occurred last to a special register D9008 as an error code, and stores further detailed error code to a special register D9091.

(3) Even with the power-off, the latest error information and 15 errors in the past are stored by battery back-up. With the AnUCPU-supporting system FD, contents of up to 16 errors can be confirmed from the peripheral devices. Display example with SWcIVD-GPPA is shown below:



(4) When the self-diagnosis detects an error, the module will be in one of the two modes below:
- Mode wherein operation of the PC is stopped
- Mode wherein operation of the PC continues

In addition, there are errors with which the operation can be selected to stop or to continue by the parameter setting.

(a) When a stop-operation mode error is detected by the self-diagnosis, the operation is stopped at the time of detection of the error, and sets the all outputs(Y) to OFF.

(b) When a continue-operation mode error is detected, the only part of the program with the error is not executed while the all other part is executed. Also, in case of I/O module verification error, the operation is continued using the I/O address prior to the error.

When an error is detected, error generation and error contents are stored in the special relay (M) and special register (D), so that in case of the continue-operation mode, the program can use the information to prevent any malfunctions of the PC or devices.

Error descriptions detected by the self-diagnosis are shown in the next page.

REMARK

1 As to the LED display message, the order of priority of the LED display can be changed if CPU is in the operation mode. (An error code is stored in the special register).
2 When the special relay M9084 is ON, checking on blown fuse, I/O verification and the battery are not performed (an error code is not stored in the special register).
3 The "Error display of peripheral device" in the table of self-diagnostic functions are messages displayed by the PC diagnosis of peripheral devices.

Self-diagnostic functions

Diagnosis item		Diagnosis timing	CPU status	Status of "RUN" LED	Error display of peripheral devices	Error code (D9008)
Memory error	Instruction code check	Upon execution of each instruction	Stop	Flickering	INSTRCT. CODE ERR.	10
	Parameter setting check	• Upon power-on and reset • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			PARAMETER ERROR	11
	No END instruction	• When M9056 or M9057 is ON • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			MISSING END INS.	12
	Unable to execute instruction	• CJ SCJ JMP CALL(P) FOR to NEXT CHG Upon execution of each instruction • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			CAN'T EXECUTE (P)	13
	Format (CHK instruction) check	Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			CHK FORMAT ERR.	14
	Unable to execute instruction	• When interruption occurred • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			CAN'T EXECUTE (I)	15
CPU error	RAM check	• Upon power-on and reset • When M9084 is ON during STOP	Stop	Flickering	RAM ERROR	20
	Operation circuit check	• Upon power-on and reset			OPE. CIRCUIT ERR.	21
	Watchdog error supervision	• Upon execution of END instruction			WDT ERROR	22
	END instruction not executed	• Upon execution of END instruction			END NOT EXECUTE	24
	Main CPU check	Always			MAIN CPU DOWN	26
I/O error	I/O module verification ＊1 (Default: stop)	Upon execution of END instruction (However, not checked when M9084 or M9094 is ON.)	Stop / Operate	Flickering / ON	UNIT VERIFY ERR.	31
	Fuse blown ＊1 (Default: operate)	Upon execution of END instruction (However, not checked when M9084 or M9094 is ON.)			FUSE BREAK OFF.	32
Special function module error	Control bus check	Upon execution of FROM, TO instruction	Stop	Flickering	CONTROL-BUS ERR.	40
	Special function module error	Upon execution of FROM, TO instruction			SP. UNIT DOWN	41
	Link module error	• Upon power-on and reset • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			LINK UNIT ERROR	42
	I/O interrupt error	When interruption occur			I/O INT. ERROR	43
	Special function module allocation error	• Upon power-on and reset • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)			SP. UNIT LAY. ERR.	44
	Special function module error ＊1 (Default: stop)	Upon execution of FROM, TO instructions	Stop	Flickering	SP. UNIT ERROR	46
	Link parameter error	• Upon power-on and reset • Upon switching from (STOP, PAUSE) to (RUN, STEP-RUN)	Stop / Operate	Flickering / ON	LINK PARA. ERROR	47
Battery	Low battery	Always (However, not checked when M9084 is ON.)	Operate	Flickering	BATTERY ERROR	70
Operation check error ＊1 (Default: operate)		Upon execution of each instruction	Stop / Operate	Flickering / ON	OPERATION ERROR ＊2 [<CHK> ERROR □□□]	50

＊1: Can be changed by the parameter settings of a peripheral device.
＊2: Displayed as a three-digit trouble code only for errors with the "CHK" instruction.

4.1.5 Device list

Usage range of QCPU-A devices is shown below.

Device list

Device		Range of usage (points) QCPU-A	Description of device
X	Input	X, Y 0 to FFF (4096 points)	Used to supply PC commands and data from peripheral devices such as push buttons, select switches, limit switches and digital switches.
Y	Output		Used to output control results of a program to external devices such as solenoids, magnetic switches, signal lights and digital display device.
X	Input	X, Y 0 to 1FFF (8192 points)	• Possible to use in a program after the I/O points usage range per each QCPU-A (described above) to a maximum of 8192 points (external output is not allowed). • Objective is to allocate for automatic I/O refresh of MELSECNET/MINI or for remote I/O of MELSECNET/10.
Y	Output		
M	Special relay	M9000 to 9255 (256 points)	An auxiliary relay used inside a PC set in advance for a specialized use.
	Internal relay	M/L/S 0 to 8191 (8192 points) 8192 points as a total of M, L, S	An auxiliary relay inside a PC which cannot output directly to external devices.
L	Latch relay		An auxiliary relay inside a PC which cannot output directly to external devices. Has the power failure compensation function.
S	Step relay		Used in the same manner as the internal relay (M). Used as a relays to indicate the stage number of process stepping program, etc.
B	Link relay	B0 to B1FFF (8192 points)	An internal relay for data link and cannot output to external devices. The range not setup by link parameters can be used as the internal relay.
F	Annunciator	F0 to F2047 (2048 points)	For fault detection. A fault detection program is created in advance, and if it becomes ON during RUN, the number is stored in a special register D.
T	100ms timer	T0 to T2047 (2048 points) (Register for storing setting value(s) is required for T256 and later.)	Up-timing-timer. There are four kinds: 100ms timer, 10ms timer, 100ms retentive timer and 1ms timer. • 1ms timer: ZHTIME instruction enables 1ms timer using the latter half of the retentive timer.
	10ms timer		
	100ms retentive timer		
	1ms timer		
C	Counter	C0 to C1023 (1024 points) (Interrupt counter C224 to C255 fixed. Register for storing setting value(s) is required for C256 and later.)	There are two kinds: up-timing counter used in PC programs and interrupt counter which counts number of interrupts.
	Interrupt counter		
D	Data register	D0 to D8191 (8192 points)	Memory used to store data inside PC.
	Special register	D9000 to D9255 (256 points)	Data memory set up in advance for a specialized use.
W	Link register	W0 to W1FFF (8192 points)	Register for data link. The range not set by link parameters can be used as a substitute for a data register.
R	File register	R0 to R8191 (8192 points)	For expanding the data register. User memory area is used for this.
A	Accumulator	A0, A1 (2 points)	Data register used to store a operation result of basic and application instructions.
Z V	Index register	V, V_1 to V_6, Z, Z_1 to Z_6 (14 points)	Used for qualification of devices (X, Y, M, L, B, F, T, C, D, W, R, K, H, P)
N	Nesting	N0 to N7 (8 levels)	Indicates nesting structure of master control.
P	Pointer	P0 to P255 (256 points)	Indicates destination of branch instructions (CJ, SCJ, CALL, JMP).
I	Interrupt pointer	I0 to I31 (32 points)	When an interruption factor is generated, it indicates the destination of the interrupt program corresponding to the interruption factor.
K	Decimal constant	K-32768 to 32767 (16-bit instruction) K-2147483648 to 2147483647 (32-bit instruction)	Used to set timer/counter, pointer number, interrupt pointer number, bit device digits, and values for basic and application instructions.
H	Hexadecimal constant	H0 to FFFF (16-bit instruction) H0 to FFFFFFFF (32-bit instruction)	Used to set values for basic and application instructions.

4.2 Parameter Setting Ranges

A list of parameter setting ranges is provided below. User memory allocation contents, I/O device allocation method and automatic refresh procedure for MELSECNET/MINI-S3 are also explained.

4.2.1 List of parameter setting range

Parameters are used for allocating the user memory area inside the memory cassette, setting various functions and device ranges.
A parameter is usually stored in the first 3k bytes of the user memory area.
Among the parameters, the network parameter for MELSECNET/10 is allocated and stored after the main sequence program area. (Refer to Section 4.2.2 for details).
As shown in the list below, a default value is given to each parameter.
Even though a default value can be used, parameter value can be changed to a value suitable for a particular application within a setting range by a peripheral device.

Item \ Setting		Default value	Setting range	
			Q02CPU-A, Q02HCPU-A	Q06HCPU-A
Main sequence program capacity		6k steps	1 to 28k steps (1k steps = in 2k-byte units)	1 to 30k steps (1k steps = in 2k-byte units)
Contents of sub sequence program		——	——	1 to 30k steps (1k steps units)
File register		——	0 to 8k points (1k points = in 2k-byte units)	
Expansion file register		——	1 block = 16k bytes (Block setting for from No.1 to No.8, from No.10 to the end of unused area in the memory) [Automatically setup in the unused area in the memory based on the file register setting.]	
Comment capacity		——	0 to 4032 points (64 point unit = in 1k byte units) [When comment capacity is set up, 1k byte is added to the memory area.]	
Expansion comment capacity		——	0 to 3968 points (64 point unit = in 1k byte units)	
Status latch		——	No parameter setting (Performed by setting up expansion file registers to store device and result in each of status latch and sampling trace modes. Refer to ACPU Programming Manual (Fundamentals).)	
Sampling trace		——		
Latch range setting (power failure compensation)	Link relay (B)	• Latch: L1000 to L2047 only. • None for others.	B0 to B1FFF (unit: 1 point)	
	Timer (T)		T0 to T255 (unit: 1 point) T256 to T2047 (unit: 1 point)	
	Counter (C)		C0 to C255 (unit: 1 point) C256 to C1023 (unit: 1 point)	
	Data register (D)		D0 to D8191 (unit: 1 point)	
	Link register (W)		W0 to W1FFF (unit: 1 point)	
Link range setting for MELSECNET/10	Number of link stations	——	Optical link: maximum 64 stations Coaxial link: maximum 32 stations	
	I/O (X/Y)		X/Y0 to X/Y1FFF (unit: 16 points)	
	Link relay (B)		B0 to B1FFF (unit:16 points)	
	Link register (W)		W0 to W1FFF (unit: 1 point)	
Settings for internal relay (M) latch relay (L) step relay (S)		M0 to M999 M2048 to M8191 L1000 to L2047 None for S	M/L/S 0 to 8191 (where M, L, S are continuous numbers)	
Timer settings	T0 to T255	T0 to T199 (100ms) T200 to T255 (10ms)	• 256 points by 100ms, 10ms, and retentive timers (in 8 point units) • Timers are continuously numbered.	
	T256 to T2047	——	• 1792 points by 100ms, 10ms, and retentive timers (in 16 point units) • Timers are continuously numbered. • Devices set: D, R, W (Setting required if 257 points or more.)	
Counter setting	Interrupt counter setting	——	•· Sets whether to use interrupt counter (C224 to C225) or not.	
	Points used	256 points (C0 to C255)	• 0 to 1024 points (in 16 point units) • Devices set: D, R, W (Setting required if 257 points or more.)	

Item \ Setting		Default value	Setting range
			A2USHCPU-S1
I/O number allocation		——	• 0 to 64 points (in 16 point units) .....Input module/output module/special function module/empty slot • Module model name registration is possible.
Remote RUN/PAUSE contact setting		——	• X0 to X1FFF • RUN/PAUSE..... 1 point (Setting of PAUSE contact only is not allowed.)
Operation modes when error occurred	Fuse blown	Continue	Stop/Continue
	I/O verification error	Stop	
	Operation error	Continue	
	Special function module check error	Stop	
	END batch processing	No	Yes/No
STOP → RUN display mode		Re-output operation status prior to the stop	Output before STOP/after operation
Print title registration		——	• 128 characters
Keyword registration		——	• Up to 6 characters in hexadecimal (0 to 9, A to F)
Link range settings for MELSECNET II	Number of link stations	——	• 0 to 64 station(s)
	I/O (X/Y)		X/Y0 to 3FF (in 16 point units)
	Link relay (B)		• B0 to BFFF (in 16 point units)
	Link register (W)		• W0 to WFFF (in 1 point units)
Link range settings for MELSECNET/MINI, MELSECNET/MINI-S3		——	Number of supported modules : 0 to 8
			Head I/O number 0 to FE0 (in 10^H units)
			Model name registration : MINI, MINI-S3
			Transmission/reception data : X, M, L, B, T, C, D, W, R, none (16 point units for bit devices)
			Number of retries : 0 to 32 times
			FROM/TO response setting : Link priority; CPU priority
			Data clear setting at faulty station : Retain/ Clear
			Faulty station detection : M, L, B, T, C, D, W, R, none (16 point units for bit devices)
			Error number : T, C, D, W, R
			Number of total remote stations : 0 to 64 station(s)
			Sending state setting during communication error : Test message, OFF data, retain (sending data)

4.2.2 Memory capacity setting (for main program, file register, comment, etc.)

QCPU-A has 144k bytes of user memory (RAM) as a standard. Parameters, T/C set value main program, MELSECNET/10 network parameters, expansion comment, file register, and comment data are stored in the user memory.

(1) Calculation of memory capacity

Determine the data types to be stored and the memory capacity with parameters before using the user memory.
Calculate the memory capacity according to Table 4.1.

Table 4.1 Parameter setting and memory capacity

<With Q02CPU-A/Q02HCPU-A>

Item		Setting unit	Calculation of memory capacity (bytes)	Max. available memory capacity (bytes)			Change into ROM	Remark
Parameter		—	3k	3k		Total: 144k	Available	
Main program	T/C set value	—	1k	1k				
	Sequence program	1k step	Number of steps × 2	56k	Total: 60k			
	Microcomputer program	1k byte	Preset number of bytes	54k				Dedicated to SFC
MELSECNET/10 parameter ✻		—	See note 1.	16k				
Expansion comment		1k byte	Preset number of bytes (1k byte = 64 points)	63k			Not available	✻1
Expansion file register (built-in)		8k points	Number of file register points × 2	128k				
File register		1k point	Number of file register points × 2	16k				
Comment		1k byte	Preset number of bytes (1k byte = 64 points)	64k				✻1
Expansion file register (memory card)		8k points	Number of file register points × 2	302k				

<With Q06HCPU-A>

Item		Setting unit	Calculation of memory capacity (bytes)	Max. available memory capacity (bytes)			Change into ROM	Remark
Parameter		—	3k	3k		Total: 144k	Available	
Main program	T/C set value	—	1k	1k				
	Sequence program	1k step	Number of steps × 2	60k	Total: 60k			
	Microcomputer program	1k byte	Preset number of bytes	58k				Dedicated to SFC
MELSECNET/10 parameter ✻		—	See note 1.	16k				
Sub program	T/C set value	1k byte	1k	1k				
	Sequence program	1k step	Number of steps × 2	58k				
	Microcomputer program	—	5k	5k				
Expansion comment		1k byte	Preset number of bytes (1k byte = 64 points)	63k			Not available	✻1
Expansion file register (built-in)		8k points	Number of file register points × 2	128k				
File register		1k point	Number of file register points × 2	16k				
Comment		1k byte	Preset number of bytes (1k byte = 64 points)	64k				✻1
Expansion file register (memory card)		8k points	Number of file register points × 2	302k				

✻1: When the capacity of comment or expansion comment is specified, the system occupies 1k byte for each.

* The capacity for network parameters of MELSECNET/10 changes depending on the contents set. The area for the network parameters shall be secured in 2k byte units based on the total of capacity for each setting. The memory capacity of each network parameter is as follows:

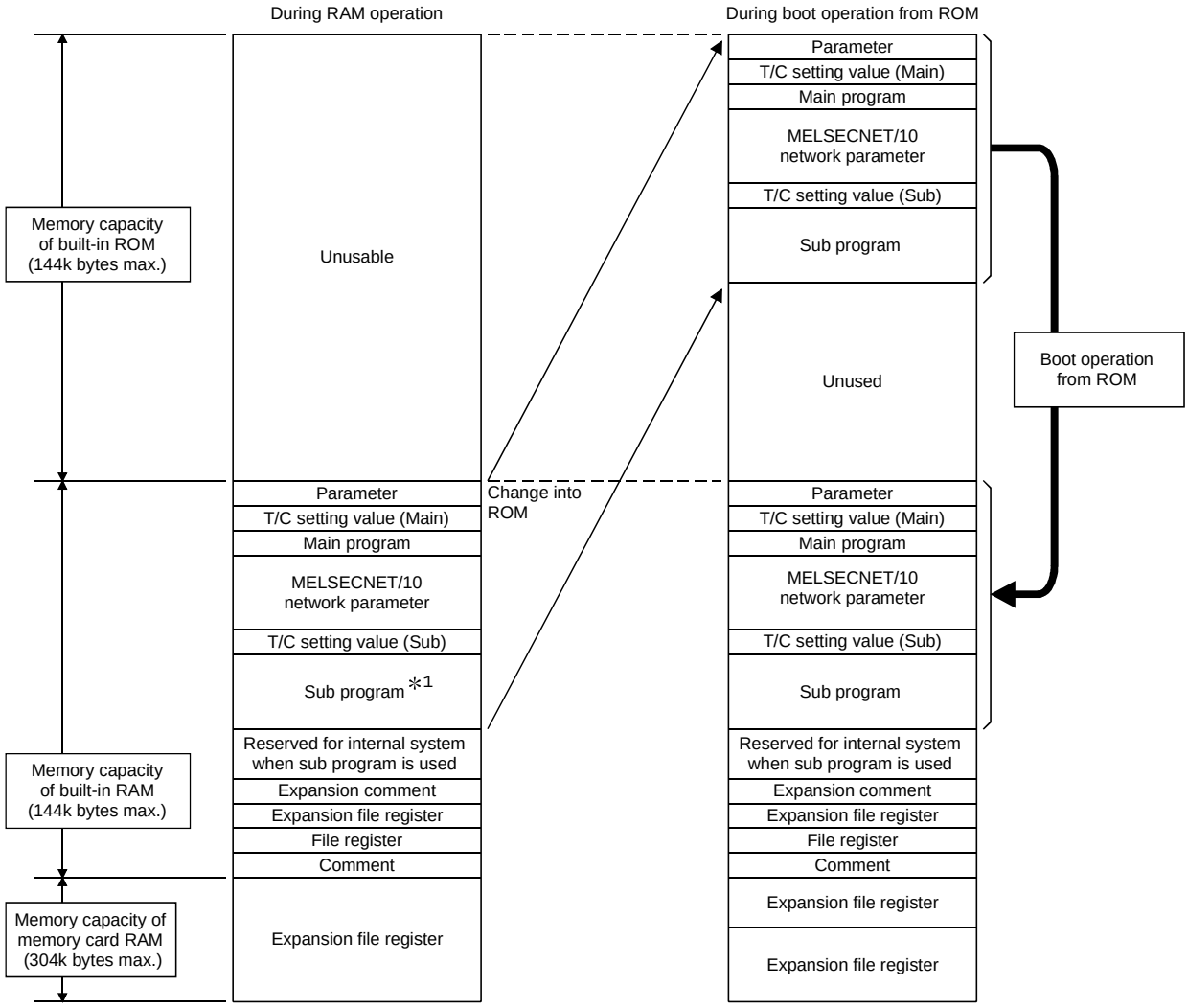
Item	Memory capacity (bytes)
Internal data	30
Routing parameter	390
Transfer parameter between data links	246
Common parameter	2164/module *1
Refresh parameter	92/module
Station specific parameter	1490/module

*1 It is 2722 bytes in case of a remote master station.

The network parameter capacity for MELSECNET/10 is determined from the total of the memory capacities calculated from above.

Total of the capacity	Capacity for network parameter setting
30 to 2048 bytes	2k bytes
2049 to 4096 bytes	4k bytes
4097 to 6144 bytes	6k bytes
6145 to 8192 bytes	8k bytes
8193 to 10240 bytes	10k bytes
10241 to 12288 bytes	12k bytes
12289 to 14336 bytes	14k bytes
14337 to 16384 bytes	16k bytes

(2) Order of user memory storage



*1 Sub programs can be used only with Q06HCPU-A.

POINT

Note that the sequence program can use only up to 22k steps when the maximum 16k bytes are used for the MELSECNET/10 network parameters.
The memory area for the sequence program for QCPU-A is the same as that for MELSECNET/10. Therefore, the remainder of subtracting the memory area used by MELSECNET/10 network parameters from the maximum 30k steps can be used for the memory area for the sequence program.

4.2.3 Setting ranges of timer and counter

(1) Timer setting range

(a) Default values of the timer setting ranges are as follows:

Timer points : 256 points
100ms timer : T0 to T199
10ms timer : T200 to T255
Retentive timer : none

(b) When timer-use points are set to 257 or more, the default values will be as follows:

100ms timer : T0 to T199
10ms timer : T200 to T255
100ms timer : T256 to T2047

(c) The timer type can be arbitrarily set in continuous numbers, with T0 to T255 in 8 point units, and T256 to T2047 in 16 point units.
By setting the timer points actually to be used, the timer processing time subsequent to the END instruction can be shortened.

(d) Timer setting values are as follows:

T0 to T255 : constant or word device (D)
T256 to T2047 : word device (D, W, R)
(Allocate a storage device for the set value by setting parameters.)

(e) Refer to section 4.4.2 for the usage of 1ms timer.

(2) Counter setting range

(a) Default values of counter setting ranges are as follows:

Counter points : 256 points
Normal counter : C0 to C255
Interrupt counter : none

(b) When the counter-use points are set to 256 points or more, the default values will become as follows:

Normal counter : C0 to C255
Normal counter : C256 to C1024

(c) A counter which can be setup as an interrupt counter must only be in the range C244 to C255, and any counters outside the range cannot be set up. Set up is made with parameters in C224 to C255 in one point unit for the interrupt counter. Any counter in the range C224 to C255 which is not set up as an interrupt counter can be used as a normal counter.

The interrupt counters in C224 to C255 are allocated to the interrupt pointers I0 toI31 as shown below, and count the occurrences of interrupts in I0 to I31.

Interrupt pointer	Interrupt counter	Interrupt pointer	Interrupt counter	Interrupt pointer	Interrupt counter	Interrupt pointer	Interrupt counter
I0	C224	I8	C232	I16	C240	I24	C248
I1	C225	I9	C233	I17	C241	I25	C249
I2	C226	I10	C234	I18	C242	I26	C250
I3	C227	I11	C235	I19	C243	I27	C251
I4	C228	I12	C236	I20	C244	I28	C252
I5	C229	I13	C237	I21	C245	I29	C253
I6	C230	I14	C238	I22	C246	I30	C254
I7	C231	I15	C239	I23	C247	I31	C255

(d) Counter-use points can be set arbitrarily in 16 point units using continuous numbers. By setting the counter which points to the number actually used, the counter processing time subsequent to the END instruction can be shortened.

(e) The counter set values are as follows:
C0 to C255 : constant or word device (D)
C256 to C1023 : word device (D, W, R)
(Allocate a storage device for the set value by setting parameters.)

POINT

When timer-use points are set to 257 points or more or counter-use points are set to 256 points or more, the set value storage devices (D, W, R), specified at the time of timer/counter use point setup, are automatically set in continuous numbers.
<Example>
When timer-use points are set to 512 points and set value storage device is set to D1000, D equivalent to 256 points (D1000 to D1255) in T256 to T511 become the devices, with continuous numbers, for the set values

4.2.4 I/O devices

QCPU-A has 8192 I/O device points (X/Y0 to 1FFF) each for input (X) and output (Y). There are actual I/O devices and remote I/O devices in this I/O range.

(1) Actual I/O device

This is the device range where an I/O module or special function module can be installed to the basic base module/extension base module and controlled.
QCPU-A: 4096 points (X/Y0 to FFF)

(2) Remote I/O device

The remote I/O devices, following the actual I/O devices, can be used for the following objectives:

(a) Allocate to a remote I/O station in the MELSECNET(II) data link system.

(b) Allocate to a remote I/O station in the MELSECNET/10 network system.

(c) Allocate to the reception data storage device or transmission data storage device in the MELSECNET/MINI-S3's automatic refresh setting.

(d) Use as the substitute to an internal relay.

4.2.5 I/O allocation of special function modules

By registering the model name of the following special function modules upon the I/O allocation from a peripheral device, dedicated commands for special function modules can be used.

Model name of special function module	Model name of the module to be set
A1SJ71UC24-R2	A1SJ71C24
A1SJ71UC24-R4	
A1SJ71UC24-PRF	
A1SJ71PT32-S3	A1SPT32S3

4.2.6 MELSECNET/MINI (S3) automatic refresh

By setting link information, I/O storage device, etc. of MELSECNET/MINI (S3) to parameters, the module automatically communicates with the buffer memory area for the batch refresh send/received data of A1SJ71PT32-S3/AJ71PT32-S3 master module (abbreviated as the master module hereafter).

Sequence programs can be created using the I/O devices as they are allocated to send/received by the automatic refresh setting. (The FROM/TO instructions are not required.)

POINTS

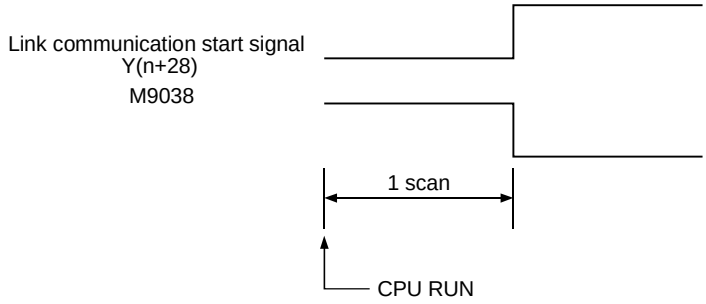
(1) Since up to 8 master modules can be set for automatic refresh by the parameter, automatic refresh is possible for up to 8 modules. If 9 or more modules are desired, use the FROM/TO instruction in the sequence program from the 9th module.

(2) Since automatic refresh is not possible with send/received data for separate refresh I/O module and for remote terminal modules No.1 to No.14, use the FROM/TO instruction for them. However, the remote terminal modules shown below are subject of automatic refresh in a limited area:
- AJ35PTF-R2 RS-232C interface module
- AJ35PT-OPB-M1-S3 mount-type tool box
- AJ35PT-OPB-P1-S3 portable type tool box

(3) For the master modules set up for automatic refresh, CPU automatically turns ON the link communication start signal Y(n+18) or Y(n+28), so it is not necessary to turn it on from the sequence program.

(4) Automatic refresh of I/O data is performed by batch after the CPU executes the END instruction. (Automatic refresh processing is performed when the CPU is in the RUN/PAUSE/STEP RUN state).

(5) The master module may perform the processing while link communication start signal Y(n+28) is OFF depending on the remote terminal module connected. For instance, if the AJ35PTF-R2 RS-232C interface module is used without protocol, it is necessary to write parameters to the parameter area (buffer memory address 860 to 929) while the link communication start signal is OFF. The link communication start signal becomes ON after CPU enters the RUN state and one scan is performed, so write the parameters during the first 1 scan.

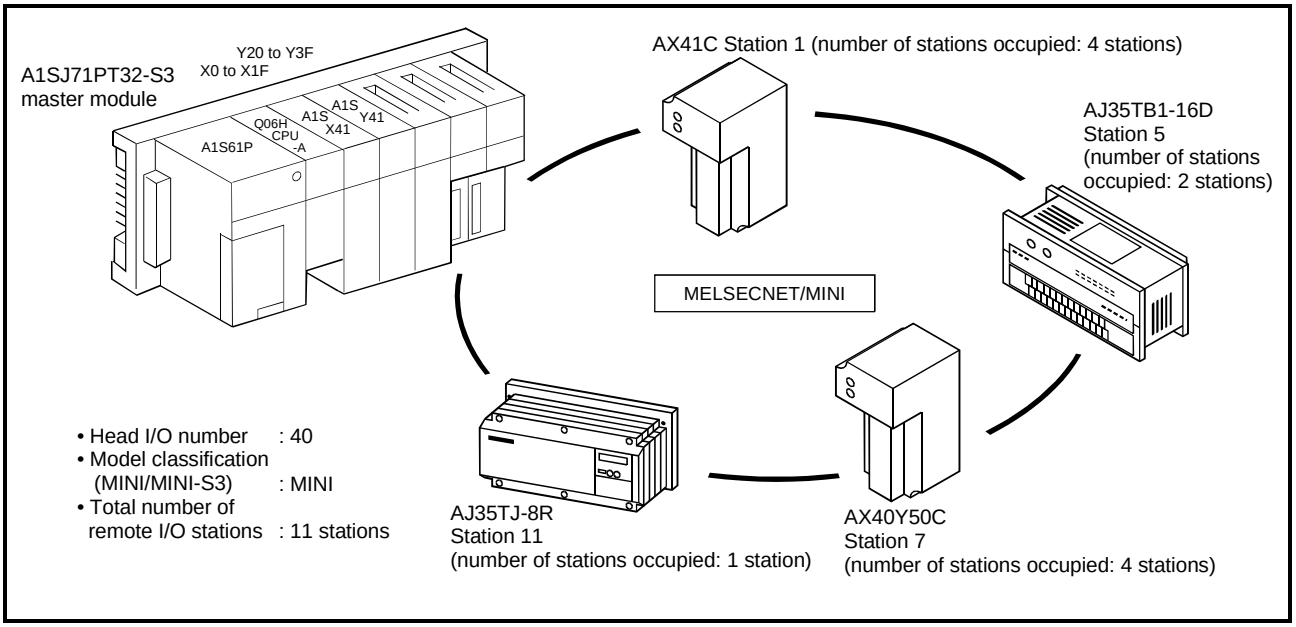


(1) Parameter setting items, setting ranges and contents of automatic refresh, as well as the buffer memory address of the master module which is used for exchanging data with QCPU-A are shown below.
Set the parameters for the number of A1SJ71PT32-S3/AJ71PT32-S3 master modules used.

I/O signal from the master module	Buffer memory address of the master module	Item	Setting range	Description
——	——	Number of master modules	1 to 8 module (s)	• Sets the total number of master modules to be used.
——	——	Head I/O No.	I/O points of CPU	• Sets the head I/O number where the master module is installed.
——	——	Model classification of MINI/MINI-S3	• MINI or MINI-S3	• MINI ..... In I/O mode (occupies 32 points) • MINI-S3 ..... In expansion mode (occupies 48 points)
——	0	Total number of remote I/O stations	0 to 64 station (s)	• Set only when MINI is set. • In MINI-S3, the number of master module's initial ROMs becomes valid, so the setting is not necessary .(When it is set, the setting is ignored).
——	110 to 141	Received data storage device	• X • M, L, B, T, C, D, W, R, none (Bit device: multiples of 16)	• Sets the devices to store received/send data for batch refresh. • Specify the head number of a device. • Occupies as the automatic refresh area from the head of the device for the number of stations (8 points/station × 64 station = 512 points: bit device) ＊2 • Use of X/Y remote I/O range is recommended for devices.
——	10 to 41	Send data storage device	• Y • M, L, B, T, C, D, W, R, none (Bit device: multiples of 16)	
——	1	Number of retries	0 to 32 times	• Sets the number of retries upon a communication error. • Error is not output if communication is restored within the number of retries set.
＊1 Y(n + 1A)	——	FROM/TO response specification	Link priority, CPU priority (Priority selection of access to the master module buffer memory)	(1) Link priority..... Link access by MINI-S3 has the priority. During the link access, FROM/TO is caused to wait. • Possible to read out the received data refreshed at the same timing. • Maximum (0.3ms + 0.2ms × number of separate refresh stations) of FROM/TO instruction wait time may be generated. (2) CPU priority..... Access by FROM/TO instruction of CPU has the priority. Even during the link access, it interrupts and accesses. • Depending on the timing, received data in the midst of I/O refresh may be read. • No wait time for FROM/TO instruction.
＊1 Y(n + 1B)	——	Data clear specification for communication faulty station	Retain, clear (received data)	• Retain ..... Retains the received data for batch and separate refresh. • Clear ..... Sets all points to OFF
——	100 to 103 195	Error station detection	M, L, B, T, C, D, W, R, none (Bit device: multiples of 16)	• Sets the head device to store the faulty station detection data. • MINI ..... occupies 4 words; MINI-S3: occupies 5 words.
——	107 196 to 209	Error No.	T, C, D, W, R	• Sets the head device to store the error code on the occurrence of an error. • MINI ..... occupies 1 word; MINI-S3 ..... occupies (1 + number of remote terminal modules) words
——	4	Line error check setting (Line error)	• Test message sending • OFF data sending • Transmit data immediately before line error	• Sets data sending method for verification of error location on the occurrence of a line error.

＊1 "n" is determined by the installation location of the master module.
＊2 When the total number of remote I/O station is odd, add 1 to the station number to obtain storage devices occupied.

(2) Setting of send/received data storage device is explained using the system example shown below.
<Example> When device X/Y400 and later are used as remote I/O stations:



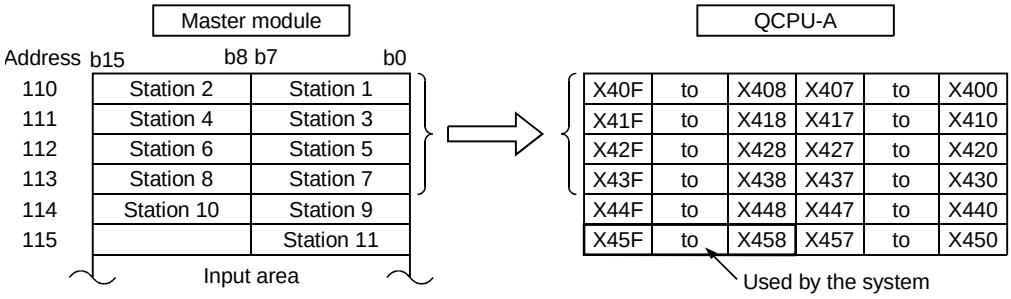
Sample parameter setting of the GPP function software package for the above system configuration is shown below:

Number of modules [1] (0-8)

I/O No.	0040
Model	MINI
Number of stations	11
Received	X0400
Send	Y0400
Retries	5
Response	CPU
Data clear	Clear
Detection	
Error number	
Error	Retain

The storage devices for send/received data for the present system example are as follows:

(a) Storage device for received data



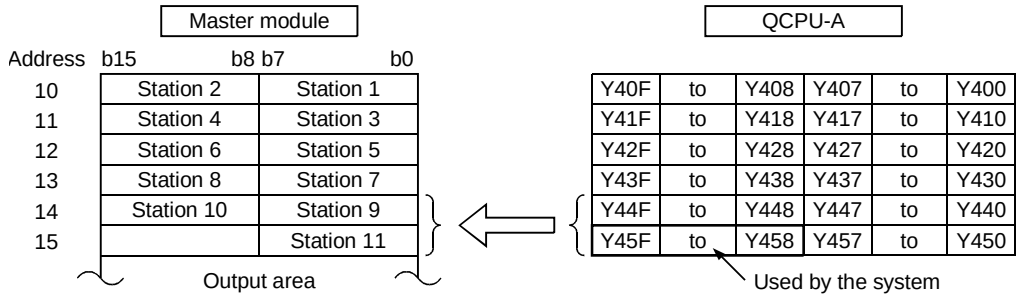
① Set the device number (X400) for b0 of the station 1 as a received data storage device.

② The received data storage device occupies from X400 to X45F.
For the present system example, the total number of stations is odd, so it is occupied for one extra station.

③ The device numbers of input modules connected are as follows:
Stations 1 to 4 AX41C → X400 to X41F
Stations 5 to 6 AJ35TB-16D → X420 to X42F
Stations 7 to 8 AX40Y50C → X430 to X43F

With respect to X440 to X45F, they are simultaneously refreshed, and set to OFF at any time.
Do not use X440 to X45F in the sequence program.

(b) Send data storage device



① Set the device number (Y400) for b0 of the station 1 as a send data storage device.

② The send data storage device occupies from Y400 to Y45F.
For the present system example, the total number of the stations is odd, so it occupies for one extra station.

③ The device numbers of output modules connected are as follows:
Stations 9 to 10 AX40Y50C → Y400 to Y44F
Station 11 AJ35TJ-8R → Y450 to Y457

With respect to Y400 to Y43F and Y458 to Y44F, they are simultaneously refreshed, but are not output.

POINTS

(1) Set the send and received data storage devices so that device numbers do not overlap.
When the received data storage device is set to B0 in the system configuration example, it occupies B0 to B5F as the device range.
Set the send data storage device to B60 or later. When the send data storage device is set to B60, the device range will be B60 to BBF.

(2) If a bit device is specified as the send/received data storage device, the device number set must be a multiple of 16.
<Example> X0, X10.....X100,.....
M0, M16,.....M256,.....
B0, B10,.....B100,.....

(3) Device range used is (8 points) × (Number of stations).
When the number of stations is an odd number, extra 8 points are necessary.

4.3 Function List

Various functions of QCPU-A are explained below.

Function (application)	Description	Outline of setting and operation
Constant scan (Program execution at constant intervals Simplified positioning)	• Makes the processing time for a single scan in the sequence program constant. • Set the processing time within the range of 10ms to 190ms in 10ms units.	• Write to the special register D9020 by the sequence program
Latch (power failure compensation) (Continuous control by data retention on power failure)	• On power supply failure of 20ms or longer/CPU reset/power supply off, data contents of the devices for which latches have been set up in advance are retained. • Latch-enabled devices: L, B, T, C, D, W • Latched data are stored in the CPU and backed up by the batteries of the memory cassette.	• Latch device and latch range are specified by setting of peripheral device parameters.
Automatic refresh of MELSECNET/MINI-S3 (Simplification of sequence program)	• Performs I/O automatic refresh communication with send/received data area for the batch refresh of AJ71PT32-S3/A1SJ71PT32-S3 up to a maximum of 8 modules. • Automatic refresh is executed in a batch after END processing. • The FROM/TO instruction for I/O in the sequence program becomes unnecessary. Programming is possible with I/O devices which are allocated directly.	• Performed by setting the automatic refresh parameter of a peripheral device. (Refer to Section 4.2.6.)
Remote RUN/STOP (When performing RUN/STOP control from outside the PC)	• When PC CPU is in RUN (the key switch is set to RUN), performs the PC's STOP/RUN from outside the PC (external input, peripheral devices, computer) with a remote control.	• When performed with the external input (X), parameter is set with a peripheral device. • When performed by a peripheral device, perform in the PC test mode. • When performed via a computer link module, perform using dedicated commands.
PAUSE (• When stopping operation of CPU while retaining the output (Y) • When performing RUN/PAUSE control from outside the PC)	• Stops the operation processing of PC CPU while retaining the ON/OFF of all the outputs (Y). (When the operation is stopped by STOP, all the outputs (Y) are set to OFF.) • When PC CPU is in RUN (the key switch is set to RUN), performs the PC's PAUSE/RUN from outside the PC (external input, peripheral devices) with a remote control.	• Performed by a peripheral device in the PC test mode. • When performed with the external input (X), perform parameter setting with a peripheral device, set the special relay M9040 to ON with the sequence program, then perform.
Status latch (Carries out operation check and failure factor check on each device when debugging or a failure condition is met.)	• With respect to devices to which status latches are set up, when status latch conditions are met, data contents of the devices are stored in the extension file register for status latch area in the memory cassette. (Stored data are cleared by the latch clear operation). • The criteria for satisfied condition can be selected from when the SLT instruction is executed by the sequence program or when the device value matches the set condition.	• Using a peripheral device, set the device to which the status latch is performed and the extension file register where the data will be stored. • Using a peripheral device, monitor the status latch data.
Sampling trace (Performs chronological checking on the behavior status of devices set up when debugging or an abnormal behavior is detected.)	• With respect to a device to which the sampling trace is set up, the operating condition of the device is sampled for the number of times specified per scan or per period, and the results are stored in the expansion file register for sampling trace (the data stored are cleared by the latch clear operation). • Sampling trace is performed by the STRA instruction in the sequence program.	• Using a peripheral device, set up the device to perform sampling trace, trace point, and the expansion file register where number of times and the data will be stored. • Using a peripheral device, monitor the result of sampling trace.

Function (application)	Description	Outline of setting and operation
Step operation (Checks conditions of program execution and behavior during debugging, etc.)	• Executes operations of the sequence program with one of the conditions (1) to (5) given below, then stops. (1) Executes by each instruction. (2) Executes by each circuit block. (3) Executes by the step intervals and the number of loops. (4) Executes by the number of loops and break point. (5) Executes when the device values concur.	• Chooses a stepping operation condition for the peripheral device and executes.
Clock ＊1 (Program control by clock data/external display of clock data	• Executes operation of the clock built into the CPU module. • Clock data: year, month, day , hour, minute, second, day of the week • When the clock data read request (M9028) is ON, the clock data are read out and stored in D9025 to D9028 by the clock element after the END processing of the sequence operation. • The clock element is backed up by the battery of the memory cassette.	• Sets data for D9025 to D9028 by a peripheral device, turns M9025 ON, then write to the clock element. • Writes to the clock element by the sequence program. (Dedicated instructions can be used.)
Priority order of LED display (Changing priority order of display/canceling display	• Changes the display order of or cancels the ERROR LED displays other than the error display by an operation stop and the default display items on the LED display device.	• Writes data as to whether change order/cancel display to D9038 or D9039 by the sequence program.
Self-diagnostic function (Detection of abnormal CPU behavior Preventive maintenance	• When an error that matches one of the self-diagnosis items is generated at the CPU power on or during RUN, it prevents malfunctions by stopping the CPU operation and displaying the error. • Stores the error code corresponding to the self-diagnosis item.	• There is a self-diagnosis item with which an operation can be continued or stopped by the setting of peripheral device parameters. • Reads out error code with a peripheral device and performs troubleshooting. (Refer to Section 4.1.4.)
Boot operation from standard ROM (Retains program at power OFF.)	• Boot operation is possible by booting parameters and sequence programs from the standard ROM to the standard RAM at startup.	• Sets DIP switch 3 to ON and turn ON or reset the module. (BOOT LED turns ON.) (Refer to section 4.3.3.)
1ms timer (Setting of 1ms timer)	• In addition to the conventional high-speed timer (10ms) and low-speed timer (100ms), a 1ms timer can be used.	• Adds "ZHTIME", a 1ms timer setting instruction, in a program. (Refer to section 4.3.3.)
Sequence accumulation time processing (Avoids influence of processing FROM/TO instruction on special function modules.	• When the faster scan time affects the processing of FROM/TO instruction or the scan time for special function modules, a special relay and special register are used to avoid such problems.	• Uses M9077 and D9077 as interlock to execute FROM/TO instruction in the unit of several ms. (Refer to section 4.3.3.)

＊1 Regarding the treatment of the year 2000

The year 2000 is a leap year, and the next day of the 28th of February is February 29th.

With A2USHCPU-S1, the clock element built in the CPU module automatically corrects the date, so resetting the date to the clock element by the user is not necessary.

If the clock data is read out from PC CPU and used for sequence control, the year data is the last two digits of the year. Thus, depending on the use of the data, correction of the year data by the sequence program will become necessary.

Year 1999 → "99"

Year 2000 → "00"

If a decision is made on the last two digits of year data solely by a magnitude comparison command alone, the years 2000 and after will be judged to be older than the year 1999.

4.4 Functions added to QCPU-A

This section describes the new functions added to QCPU-A (A mode) which are not available with A2USHCPU-S1.

4.4.1 Boot operation from standard ROM

Boot operation is enabled by booting parameters and sequence programs from the standard ROM to the standard RAM at startup.
The boot operation from the standard ROM allows the retention of sequence programs without using batteries even when the power is OFF.
The procedure of the boot operation from the standard ROM is described below:

(1) Operation methods

There are two methods to operate QCUP-A: The RAM operation uses the standard RAM. The boot operation uses the standard ROM and boots parameters and sequence programs from the standard ROM to the standard RAM at startup.
QCPU-A allows you to check the current operation method by the settings of DIP switch 3 and M9073. The following table shows the setting combination.

Status of M9073 / Status of DIP switch 3	OFF	ON
OFF	RAM operation D9076: 0 M9076: OFF	RAM operation D9076: 0 M9076: OFF
ON	RAM operation D9076: 1 M9076: OFF	Boot operation from standard ROM D9076: 2 M9076: ON (Writing available with standard ROM)

(a) Procedure to boot program (at startup only)
Boot a program from the standard ROM to the standard RAM.
① Set DIP switch 3 to ON.

② Turn ON or reset the module. (BOOT LED turns ON.)

(b) Procedure to write to standard ROM
Write a program from standard RAM to standard ROM.
① Set DIP switch 3 to ON and turn M9073 ON. → "2" is stored in D9076 and "1" is stored in M9076.

② Start writing to the standard ROM. (M9074 is turned ON.)

③ When writing to the standard ROM is successfully completed, M9075 turns ON and D9075 stores the result of writing to the standard ROM operation. (M9074 is turned ON.)

④ To repeat writing, turn M9074 OFF once and turn it ON again.
(When M9074 is turned OFF, M9075 is turned OFF.)

(c) Detailed contents of D9075

The following table shows the detailed contents of special register D9075.

Value in D9075	Description
00_H	Successful completion
$F1_H$	RAM operation (Set DIP switch 3 to ON.)
$F2_H$	M9073 is OFF. (Turn M9073 ON.)
$F3_H$	Failed erasing the standard ROM
$F4_H$	Failed writing to the standard ROM
FE_H	Checking erasing the standard ROM
FF_H	Writing to the standard ROM

(d) Details of special relays during boot operation

The following table shows the details of special relays during boot operation

Special relay	Name	Description	Details
M9073	Setting of writing to standard ROM	OFF: Disables writing to ROM ON : Enables writing to ROM	To enable writing to the standard ROM, turn this relay ON. (DIP switch 3 should be set to ON.)
M9074	Request for writing to standard ROM	OFF → ON: Starts writing to ROM	When this relay is turned from OFF to ON, writing to the standard ROM is started.
M9075	Successful completion of writing to standard ROM	OFF: Failed writing to ROM ON : Successfully completed to writing to ROM	Turns ON when writing to the standard ROM is successfully completed. (The writing status is stored in D9075.)
M9076	Status of writing to standard ROM	OFF: Writing to ROM disabled ON : Writing to ROM enabled	Turns ON when writing to standard ROM is enabled. (Turns ON when DIP switch 3 and M9075 are ON.)

POINTS

(1) Like the conventional A2USHCPU-S1, the available capacity of the standard memory (file register, comment, etc.) does not increase even if the ROM operation is selected.

(2) During the ROM operation, the program stored in the standard RAM is overwritten with the program stored in the ROM.
Before starting the boot operation, be sure to back up the program with peripheral devices.

(3) The capacity of the standard ROM is 144k bytes, the same as that of the standard RAM. Writing is disabled when the total capacity of parameters and programs exceeds 144k bytes. (Comments and file registers cannot be written to the standard ROM.)

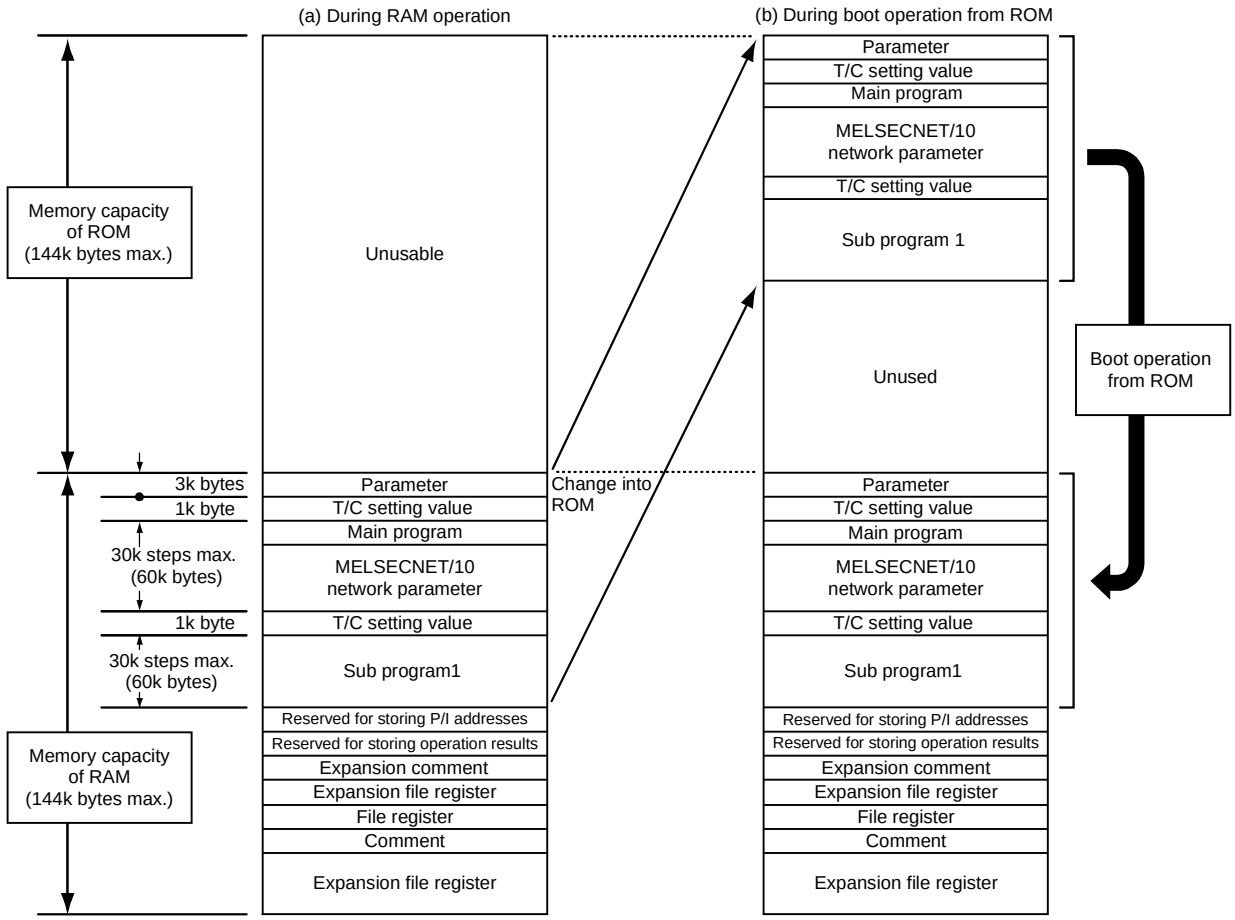
(4) When the attempt is made to boot parameters and programs from the standard ROM to the standard RAM but the standard ROM does not contain proper programs, a parameter error occurs. (Detailed error code: 114)

(5) Writing during RUN is performed to the standard RAM. When the boot operation is used, be sure to write the program which is written to the standard RAM during RUN also to the standard ROM.

(2) Configuration of user memory area

The following figure shows the configuration of the user memory area during the RAM operation and during the boot operation from the standard ROM.

Configuration example of user memory area (in case of Q06HCPU)



4.4.2 Usage of 1ms timer

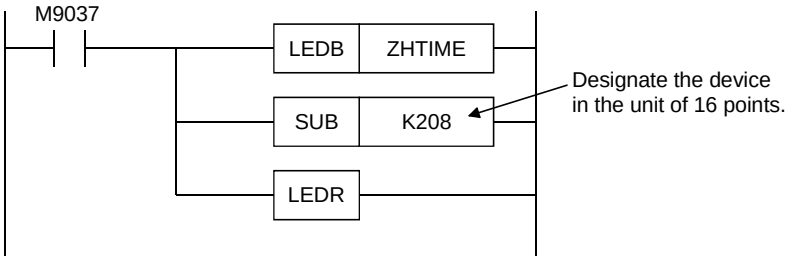
With QCPU-A, a 1ms timer can be used in addition to the conventional high-speed timer (10ms) and low-speed timer (100ms).

(1) Usage

Adding "ZHTIME", a 1ms timer setting instruction, in a program enables the use of a 1ms timer. (The ZHTIME instruction must be written in the main program.)
The ZHTIME instruction is checked at startup and at switching from STOP to RUN. When this instruction exists in the main program, the 1ms timer can be used.
If the ZHTIME instruction does not exist in the main program, only the 100ms/10ms timer can be used, and the 1ms timer is disabled.
The number of occupied points is set as the total points of the 100ms timer, 10ms timer, retentive timer, and 1ms timer.
The area for the 1ms timer is reserved following that of the retentive timer. Consequently, the constant specified with the ZHTIME instruction is designated as the device number following that of the retentive timer specified by parameters in the unit of 16 points.

(2) Use example of the ZHTIME instruction

The use example of the ZHTIME instruction is shown below.
Example) When the timer in 1ms is set at T208 and later:



(3) Accuracy of 1ms timer

The following table shows the accuracy of 1ms timer.

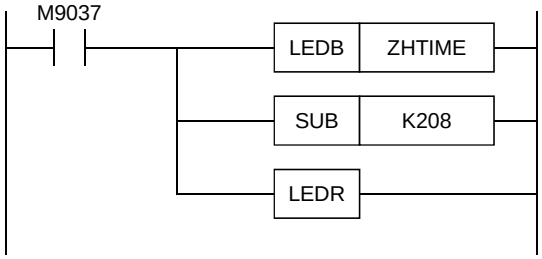
Timer type	Scan time	Accuracy
1ms	T < 1ms	+ 2 scan time to - 1 ms
	T ≧ 1ms	+ 2 scan time to - 1 scan time

(4) Setting example

The followings are the setting examples with and without the expansion timer:

(a) Setting example when the expansion timer is not used

Number of occupied points: 256 (100ms timer: 120 points, 10ms timer: 40 points, retentive timer: 48 points, 1ms timer: 48 points)



A parameter

Memory capacity | PLC RAS | PLC system | I/O assignment | Device

Device setup

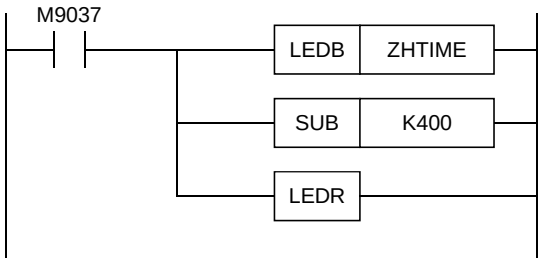
	Sym.	Digit.	Points	Start	End	Latch Start	End	Setting value stored	End
Inside relay(1st half)	M	10	1000	0	999				
Latch relay	L	10	1048	1000	2047	1000	2047		
Step relay	S	10							
Inside relay(2nd half)	M	10	6144	2048	8191				
Link relay	B	16	8192	0	1FFF				
Link register	W	16	8192	0	1FFF				
Data register	D	10	8192	0	8191				
Counter all points	C	10	256						
Counter	C	10	256	0	255				
Extension counter	C	10							
Timer all points	T	10	256						
Low speed timer	T	10	120	0	119				
high speed timer	T	10	40	120	159				
Retentive timer	T	10	96	160	255				
Extension low speed timer	T	10							
Extension high speed timer	T	10							
Extension retentive timer	T	10							

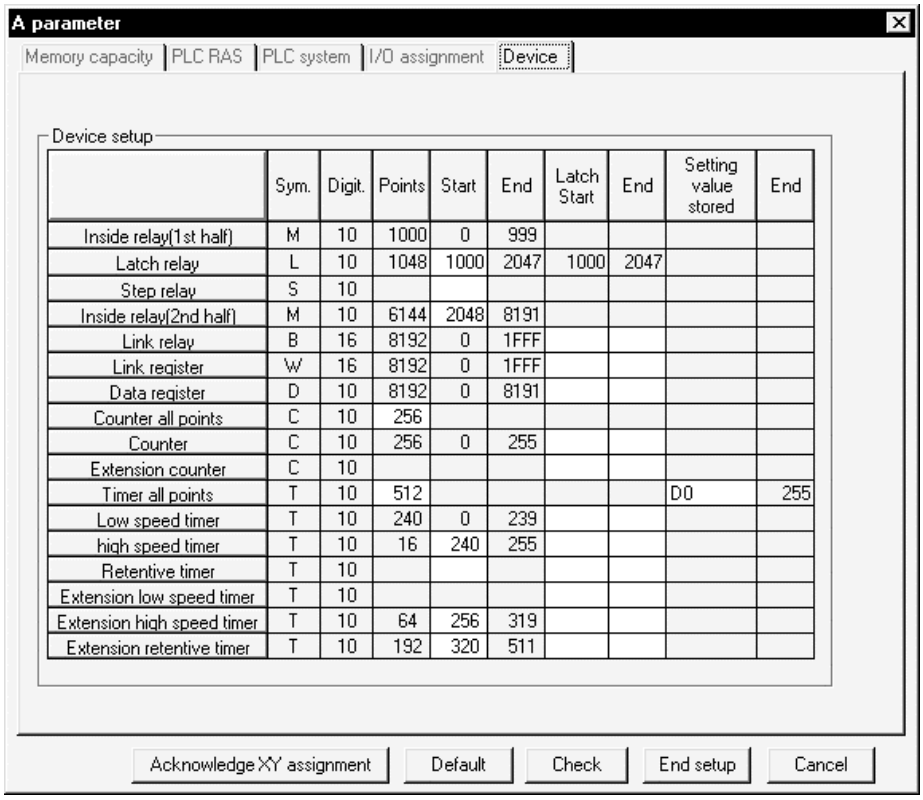
Acknowledge XY assignment | Default | Check | End setup | Cancel

According to the setting above, the devices designated for the 100ms timer are T0 to T119, for the 10ms timer are T120 to T159, for the retentive timer are T160 to T207, and for the 1ms timer are T208 to T255.

(b) Setting example when the expansion timer is used

Number of occupied points: 512 (100ms timer: 240 points, 10ms timer: 80 points, retentive timer: 80 points, 1ms timer: 112 points)





	Sym.	Digit.	Points	Start	End	Latch Start	End	Setting value stored	End
Inside relay(1st half)	M	10	1000	0	999				
Latch relay	L	10	1048	1000	2047	1000	2047		
Step relay	S	10							
Inside relay(2nd half)	M	10	6144	2048	8191				
Link relay	B	16	8192	0	1FFF				
Link register	W	16	8192	0	1FFF				
Data register	D	10	8192	0	8191				
Counter all points	C	10	256						
Counter	C	10	256	0	255				
Extension counter	C	10							
Timer all points	T	10	512					D0	255
Low speed timer	T	10	240	0	239				
high speed timer	T	10	16	240	255				
Retentive timer	T	10							
Extension low speed timer	T	10							
Extension high speed timer	T	10	64	256	319				
Extension retentive timer	T	10	192	320	511				

According to the setting above, the devices designated for the 100ms timer are T0 to T239, for the 10ms timer are T240 to T319, for the retentive timer are T320 to T399, and for the 1ms timer are T400 to T511.

POINTS

Note the following points to use the ZHTIME instruction.

(1) The ZHTIME instruction must be written in the main program.

(2) The ZHTIME instruction must be designated in the unit of 16 points.

(3) The number of occupied points designated in the timer setting by parameters should include those for the 1ms timer.

(4) When the range for the timer setting by parameters is between T256 and 2047, the initial device number to be used should be set at the item of the retentive timer between T256 and 2047.
The 100ms timer should be used as the retentive timer.

4.4.3 Sequence accumulation time processing

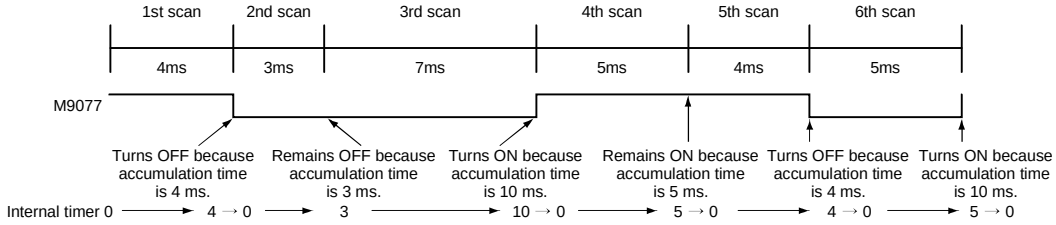
With QCPU-A, as the scan time becomes faster, it may affect the processing of FROM/TO instruction or the scan time for special function modules.
Such problems can be avoided by using the following special relay and special register as interlock and executing FROM/TO instruction in the unit of several ms.

(1) Procedure

Number	Name	Description	Details	Set by (Set at)
M9077	Sequence accumulation time measurement	ON : Time elapsed OFF: Time not elapsed	• Compares the setting value at D9077 with the time elapsed from the start of measurement (accumulation time) at every scan. Then, performs the following operations: Setting value ≤ Accumulation time : Turns M9077 ON and clears the accumulation time. Setting value > Accumulation time : Turns M9077 from ON to OFF and clears the accumulation time. When M9077 is already OFF, clears the accumulation time. ✻ When 1 to 255 is designated at D9077, M9077 is turned ON at the first scan. ✻ When a value other than 1 to 255 is designated at D9077, the value in D9077 is reset to 0 and M9077 is always turned OFF.	System
D9077	Sequence accumulation time measurement	Accumulation time setting	• Stores the accumulation time used by M9077. Setting range: 1 to 255ms (Default: 5ms) ✻ When a value other than 1 to 255 ms is designated, the value in D9077 is reset to 0.	User

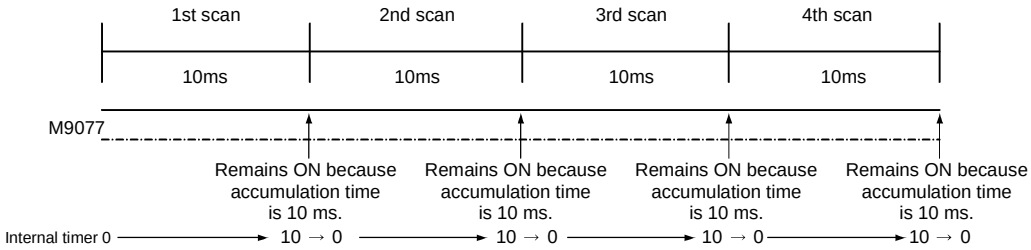
The operation of M9077 above is shown below:

(a) When 5ms is set at D9077 (The scan time is shorter than the setting value.)



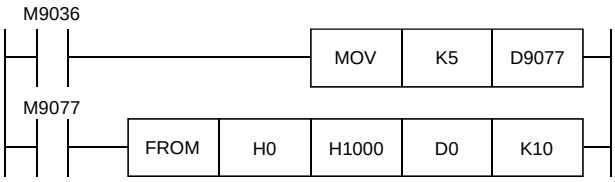
In the diagram above, M9077 is ON at the first scan so that the instruction is executed. At the beginning of the second scan, the accumulation time does not reach 5 ms. As a result, M9077 turns OFF, the accumulation time is cleared, and the instruction is not executed. At the end of the second scan, the accumulation time does not reach 5 ms, so that M9077 remains OFF and the instruction is not executed. At the end of the third scan, the accumulation time exceeds 5 ms. As a result, M9077 turns ON, the accumulation time is cleared, and the instruction is executed at the forth scan. At the end of the forth scan, the accumulation time exceeds 5 ms, so that M9077 remains ON and the instruction is executed at the fifth scan. At the end of the fifth scan, the accumulation time does not reach 5 ms so that M9077 turns OFF. The accumulation time is cleared and the instruction is not executed at the sixth scan.

(b) When 5ms is set at D9077 (The scan time is longer than the setting value.)



In the diagram above, M9077 is always ON when the scan time is always longer than the setting value (D9077).

The following program example executes the FROM/TO instruction in the unit of several seconds using M9077 and D9077 above.



Sets the accumulation time as 5ms.

Executes the FROM instruction only when the interval between sequence scans becomes 5ms or more. (Executes it at first scan.)

∗1: The setting range for the sequence accumulation time is 1 to 255ms (default: 5ms).
The value in D9077 should be in the range between 1 and 255. Otherwise, the value in D9077 is reset to 0 and M9077 is always OFF.

∗2: If the instruction signal for the FROM/TO instruction is a pulse signal, the interlock with M9077 may mask the FROM/TO instruction, disabling execution. In such a case, keep the instruction signal once in the other device.

∗3: If execution order is set to the FROM/TO instruction, adding M9077 may change the execution order. In such a case, do not use M9077, and make the execution interval of the FROM/TO instruction longer with a user program.

4.5 Precautions When Handling the Module

Precautions when handling the CPU module, from unpacking to installation, are described below.

⚠CAUTION

- Use the PC in the environment given in the general specifications of this manual. Using the PC outside the range of the general specifications may result in electric shock, fire or malfunctioning, or may damage or degrade the module.
- Insert the tabs at the bottom of the module into the mounting holes in the base module before installing the module, and tighten the module fixed screws with the specified torque. Improper installation may result in malfunctioning, breakdowns or cause the module to fall out.
- Tighten the screws with the specified torque. If the screws are loose, it may result in short circuits, malfunctioning or cause the module to fall out.
  If the screws are tightened too much, it may damage the screws and the module may result in short circuits, malfunctioning or cause the module to fall out.
- Make sure the memory card is installed securely in its installation connector. After installation, confirm that it is securely tightened. Defective contact may cause malfunctioning.
- Do not touch the conducted part of the module or electric parts. This may cause malfunctioning or breakdowns.

(1) Module case, memory card, terminal block connector and pin connector are made of resin. Do not fall them or apply a strong shock to them.

(2) Do not remove the printed board of each module from its case. Doing so may cause breakdown.

(3) While wiring, be careful not to let foreign matter such as wire chips get inside the module. If it does get in, remove it immediately.

(4) When using the expansion base module (QA1S6□B), be sure to install the power supply module. Although the module may work without the power supply module under light load, stable operation is not guaranteed.

(5) Perform tightening of module installation screws and terminal screws on the CPU module, power supply module, I/O module and special function module with the following torque:

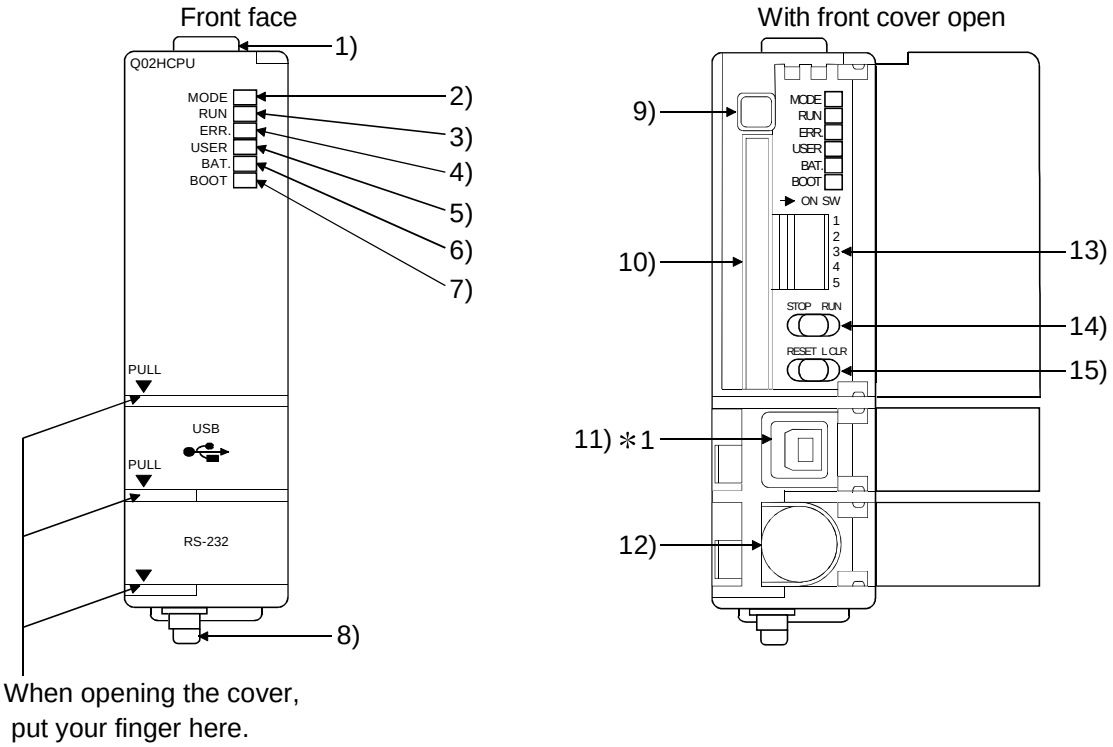
Screw location	Tightening torque range
QCPU-A module fastening screw (M3 × 12)	36 to 48N • cm
AnS series, Module installation screws (M4 screw)	78 to 118N • cm
Terminal screws for power supply module and I/O module (M3.5 screw)	59 to 88N • cm

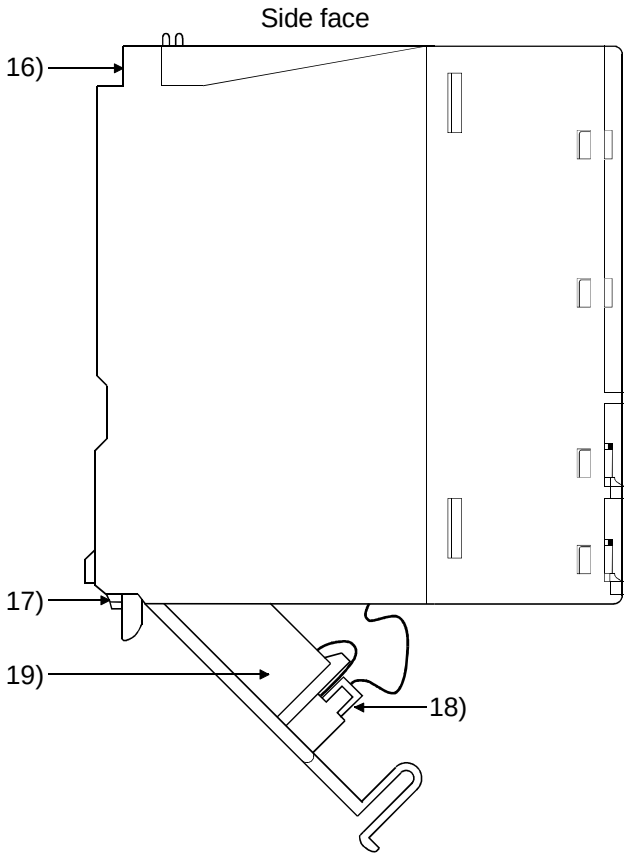
(6) When using the expansion cable, do not bind it with or place it close to the main circuit (high-voltage, large-current) lines.

4.6 Part Names and Settings of the CPU Module

4.6.1 Part names and settings

This section explains the names and settings of the CPU module.

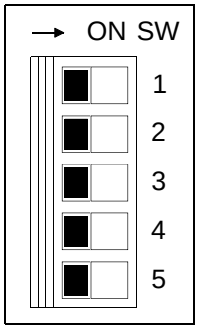




∗1: Not provided for Q02CPU-A.

No.	Name	Applications
1)	Module fixing hook	Hook used to fix the module to the base unit. (Single-motion installation)
2)	Mode judging LED	Indicates the mode of the CPU. Lit (orange) : A mode Lit (green) : Q mode
3)	RUN LED	Indicates the operating status of the CPU. ON : During operation in "RUN" or "STEP RUN" mode. OFF : During a stop in "STOP", "PAUSE" or "STEP RUN" mode or detection of error whose occurrence stops operation.
4)	ERROR LED	ON : Detection of self-diagnostic error which will not stop operation, except battery error. (When operation continued at error detection is set in the parameter) OFF : Normal Flicker : Detection of error whose occurrence stops operation.
5)	USER LED	ON : Annunciator ON OFF : Normal Flicker : Execution of latch clear
6)	BAT. ALARM LED	ON : Occurrence of battery error due to reduction in battery voltages of CPU and memory card. OFF : Normal
7)	BOOT LED	ON : Execution of boot operation OFF : Non-execution of boot operation
8)	Module loading lever	Used to load the module to the base unit.
9)	Memory card EJECT button	Used to eject the memory card from the CPU.
10)	Memory card loading connector	Connector used to load the memory card to the CPU.
11)	USB connector ＊2	Unusable (Usable for Q mode only)
12)	RS-232 connector ＊2	Connector for connection with a peripheral device. Can be connected by RS-232C connection cable (QC30R2).

＊2: When normally connecting a cable to the USB connector or RS-232 connector, clamp the cable to prevent it from coming off due to the dangling, moving or carelessly pulling of the cable.

No.	Name	Applications
13)	DIP switches 	Used to set the items for operation of the CPU. For OS boot designation and RAM/ROM operation, refer to the QCPU-A (A mode) additional manual.
		SW1: Must not be used. Normally OFF. (Shipped in OFF position)
		SW2: Must not be used. Normally OFF. (Shipped in OFF position)
		SW3: RAM/boot operation designation. (Shipped in OFF position) ON : Boot operation OFF : RAM operation
		SW4: Must not be used. Normally OFF. (Shipped in OFF position)
		SW5: Must not be used. Normally OFF. (Shipped in OFF position)
14)	RUN/STOP switch	RUN : Executes sequence program operation. STOP : Stops sequence program operation.
15)	RESET/L.CLR switch	RESET : Used to perform hardware reset, operation fault rest, operation initialization, etc. If this switch is left in the RESET position, the whole system will be reset and the system will not operate properly. After performing reset, always return this switch to the neutral position. L.CLR : Used to turn "OFF" or "zero" all data in the parameter-set latch area. Used to clear the sampling trace and status latch registration.
16)	Module fixing screw hole	Hole for the screw used to fix to the base unit. (M3 × 12 screw)
17)	Module fixing hook	Hook used to fix to the base unit.
18)	Battery connector pin	For connection of battery lead wires. (When shipped from the factory, the lead wires are disconnected from the connector to prevent the battery from consuming.)
19)	Battery	Backup battery for use of standard RAM and power failure compensation function.

4.6.2 Switch operation after program write

(1) When writing a program during STOP of CPU

Write a program during STOP of the CPU in the following procedure.

1) RUN/STOP switch: STOP
   RUN LED: OFF..... CPU STOP status → Program write
2) RUN/STOP switch: RUN
   RUN LED: Flicker ..... CPU STOP status
3) RUN/STOP switch: STOP → RUN
   RUN LED: ON ..... CPU RUN status

(2) When you wrote a program during RUN

When you wrote a program during RUN of the CPU, do not operate the switch.

POINT
The CPU will not go into the RUN status if you move the key switch to RUN immediately after writing a program in the STOP status of the CPU. After writing a program, perform rest with the RESET/L.CLR switch, then move the RUN/STOP switch to RUN to set the CPU to the RUN status.

4.6.3 Latch clear operation

To perform latch clear, operate the RESET/L.CLR switch in the following procedure.

1) RESET/L.CLR switch: Move the switch to L.CLR several times until the USER LED flickers.
   (Do not move it to RESET.)
   USER LED: Flicker..... Ready for latch clear.
2) RESET/L.CLR switch: Move the switch to L.CLR once more.
   USER LED: OFF ..... Latch clear complete.

POINT
Latch clear can be set to be valid or invalid device-by-device by making device setting in the parameter mode.

4.6.4 Installation and removal of memory card during power-on

Do not install or remove the memory card while power is on.

POINT
If you installed or removed the memory card while power was on, the data within the memory card may be corrupted.

MEMO

5. POWER SUPPLY MODULE

5.1 Specifications

The specification of the power supply module are shown below.

Table 5.1 Power supply module specifications

Item		Performance specifications		
		A1S61PN	A1S62PN	A1S63P
Base installation location		Power supply module installation slot		
Input power supply		100 to 240VAC $^{+10\%}_{-15\%}$ (85 to 264VAC)		24VDC $^{+30\%}_{-35\%}$ (15.6 to 31.2VDC)
Input frequency		50/60Hz±5%		——
Maximum input apparent power		105VA		41W
Inrush current		20A 8ms or less		81A 1ms or less
Output current rating	5VDC	5A	3A	5A
	24VDC	——	0.6A	——
Overcurrent ＊1 protection	5VDC	5.5A or above	3.3A or above	5.5A or above
	24VDC	——	0.66A or above	——
Overvoltage ＊2 protection	5VDC	5.5 to 6.5V		
	24VDC	——		
Efficiency		65% or above		
Allowable period of momentary power failure ＊3		20ms or less		1ms or less
Dielectric withstand voltage	Primary-5VDC	Between input: batch LG and output: batch FG, 2830VAC rms/3 cycle (altitude 2,000m (6562 ft)		500VAC
	Primary-24VDC			——
Insulation resistance		Between input: batch LG and output: batch FG, 500VAC (5MΩ or above by insulation resistance tester)		5MΩ or above by insulation resistance tester
Noise durability		By noise simulator with noise voltage of 1,500Vp-p, noise width of 1μs, and noise frequency of 25 to 60Hz. Noise voltage IEC801-4, 2kV		By noise simulator with noise voltage of 500Vp-p, noise width of 1μs, and noise frequency of 25 to 60Hz.
Operation display		LED display (ON for 5VDC output)		
Terminal screw size		M3.5 × 7		
Applicable wire size		0.75 to 2mm^2		
Applicable crimp-style terminal		RAV1.25-3.5, RAV2-3.5		
Applicable tightening torque		59 to 88N•cm		
External dimensions (mm (inch))		130 (5.12) × 55 (2.17) × 93.6 (3.69)		
Weight (kg)		0.60	0.60	0.50

POINTS

∗1: Overcurrent protection

If the current above the spec value flows in the 5VDC or 24VDC circuit, overcurrent protection device interrupts the circuit and stops the system operation. LED display of the power supply module is either OFF or ON dimly, due to the voltage drop.

When this device is once activated, remove factors of insufficient current capacity and short-circuit before starting up the system. When the current restores to the normal value, the system performs the initial start.

∗2: Overvoltage protection

When 5.5V to 6.5V of overvoltage is applied to the 5VDC circuit, overvoltage protection device interrupts the circuit and stops the system operation.

LED display of the power supply module turns OFF. To restart the system, turn OFF the input power supply, then back to ON. The system performs the initial start.

If the system does not start and LED display remains OFF, the power supply module needs to be replaced

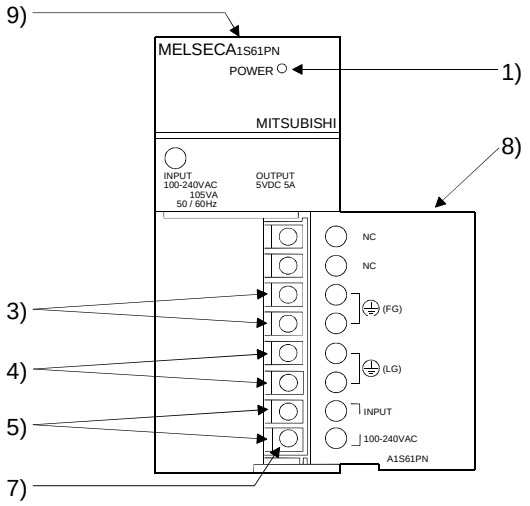
∗3: Allowable period of momentary power failure

This indicates allowable period of momentary power failure of PC CPU, and is determined by the power supply module used. Allowable period of momentary power failure for a system using A1S63P is the period it takes until the 24VDC falls below the specified voltage (15.6VDC) after cutting off the primary power supply of the stabilized power supply, which supplies the 24VDC power to A1S63P.

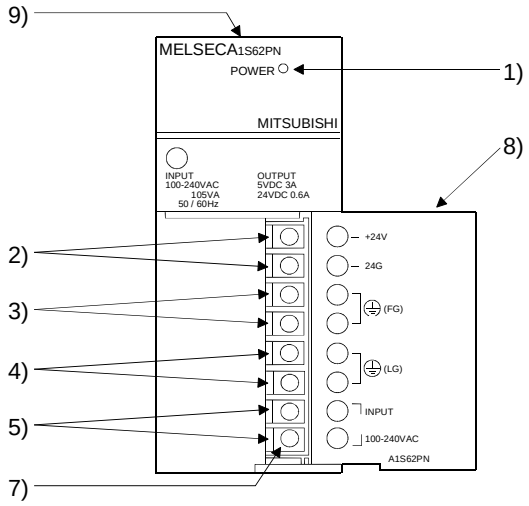
5.2 Name and Setting of Each Part

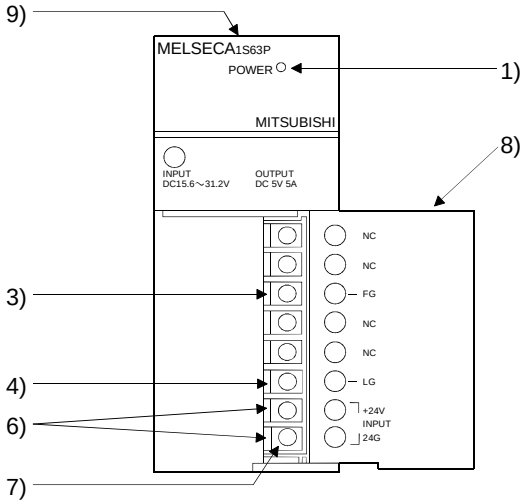
5.2.1 Name of each part of different power supply modules is provided below.

(1) A1S61PN



(2) A1S62PN





(3) A1S63P

No.	Name	Usage
1)	"POWER" LED	An LED which turns ON when 5VDC power is supplied
2)	24VDC/24GDC terminals	Supplies power to the output module that requires 24VDC power supply (through external wiring).
3)	FG terminals	A ground terminal connected to the shielded pattern on the PC board
4)	LG terminals	A ground for power supply filter. With A1S61PN or A1S62PN, the potential is half the input voltage.
5)	Power supply input terminals	A power supply input terminal used to be connected with AC power supply between 100VAC and 200VAC
6)	Power supply input terminals	A power supply input terminal used to be connected with 24VDC power supply
7)	Terminal screw	M3.5 × 7
8)	Terminal cover	A protective cover for the terminal block
9)	Module fastening screw	A screw that fastens the module to the base module (M4 screw, tightening torque: 59 to 88 N•cm)

POINTS

(1) Do not use the terminal marked NC in the terminal block.
(2) Be sure to ground LG and FG terminals with Type D (Type 3) or higher grounding.

MEMO

6. BASE MODULE AND EXPANSION CABLE

This chapter describes the specifications of the base module (basic base module and expansion base module) and expansion cable used in the system, as well as the use standard of the expansion base module.

6.1 Specifications of Base Modules

(1) Specifications of basic base module

Item \ Type name	QA1S33B	QA1S35B	QA1S38B
Allowable number of I/O module to be mounted	3	5	8
Expansion	Available		
Applicable module	QCPU-A/AnS series module		
Current consumption (A)	0.107	0.117 (0.086) ∗	0.118 (0.086) ∗
Mounting hole size	M5 screw hole or Ø5.5 hole (for M5 screw)		
Dimensions	255 (W) × 130 (H) × 51.2 (D)	325 (W) × 130 (H) × 51.2 (D)	430 (W) × 130 (H) × 51.2 (D)
Weight (kg)	0.75		1.00
Accessory	Installation screw: M5 × 25 (4), DIN rail mounting adapter		

∗: The parenthesized values are for those products not provided for CE mark.

(2) Specifications of expansion base module

Item \ Type name	QA1S65B	QA1S68B
Allowable number of I/O module to be mounted	5	8
Expansion	Available	
Applicable module	AnS series module	
Current consumption (A)	0.117 (0.088) ∗	0.118 (0.090) ∗
Mounting hole size	M5 screw hole or Ø5.5 hole (for M5 screw)	
Dimensions	315 (W) × 130 (H) × 51.2 (D)	420 (W) × 130 (H) × 51.2 (D)
Weight (kg)	0.75	1.00
Accessory	Installation screw: M5 × 25 (4), DIN rail mounting adapter	

∗: The parenthesized values are for those products not provided for CE mark.

6.2 Specifications of Expansion Cable

The specifications of the expansion cable used for the QCPU system are shown below:

Item \ Type name	QC06B	QC12B	QC30B	QC50B	QC100B
Cable length (m)	0.6	1.2	3.0	5.0	10.0
Usage	Connection between the basic base module and the expansion base module, or between the expansion base modules				
Weight (kg)	0.16	0.22	0.40	0.60	1.11

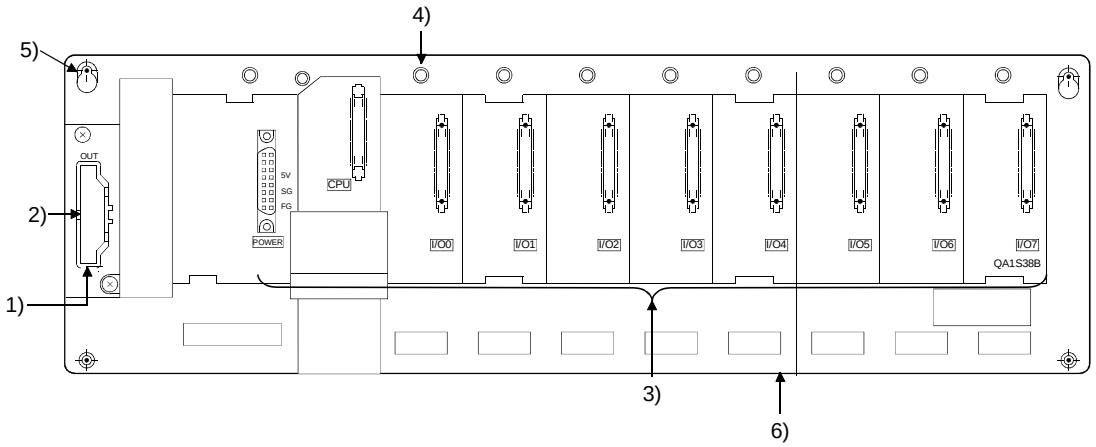
POINT

When using two or more expansion cables, limit the total length of the cable to 13.2m or less.

6.3 Part Names of Base Module

This section describes the part names of the base module.

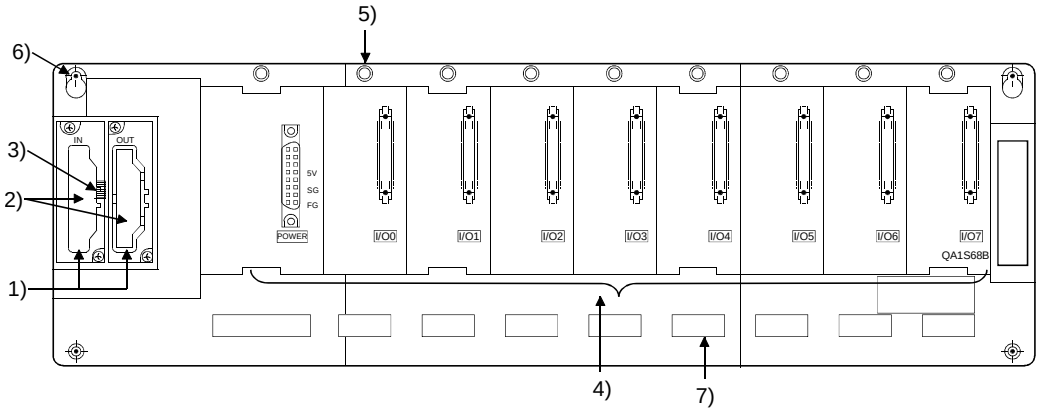
(1) Basic base module (QA1S33B, QA1S35B, QA1S38B)



No.	Name	Usage
1)	Expansion cable connector	A connector for signal transmission with the expansion base module. Connects the expansion cable.
2)	Base cover	A protective cover of expansion cable connector. Before connecting a cable, it is necessary to remove the section enclosed with a groove below OUT of the base cover with nippers or other tools.
3)	Module connector	A connector connects the power supply module, CPU module, I/O module, or special function module. Attach the supplied connector cover to the reserved connectors with no module to prevent the ingress of dust.
4)	Screw hole for fastening modules	A screw hole used for fastening a module to the base. Screw size for CPU module : M3 × 12 Screw size for modules other than CPU module : M4 × 12
5)	Base module installation hole	A hole used for installing the base module to a panel such as a control panel. (M5 screw)
6)	DIN rail hook	A hook used for DIN rail mounting.

(2) Expansion base module (QA1S65B, QA1S68B)

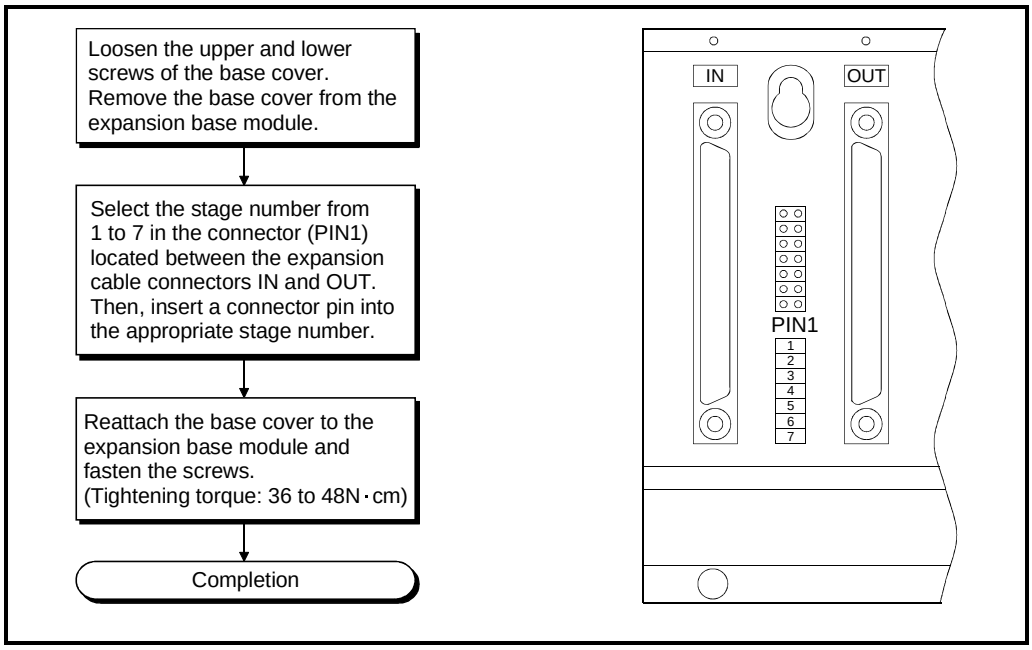
QA1S65B,QA1S68B



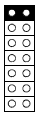
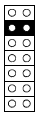
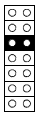
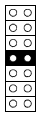
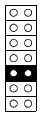
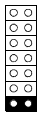
No.	Name	Usage
1)	Expansion cable connector	A connector for signal transmission with the basic base module or the other expansion base module. Connects the expansion cable. Do not remove the supplied connector cover.
2)	Base cover	A protective cover of expansion cable connector.
3)	Stage number setting switch	A switch used to set the stage numbers of the expansion base modules. Refer to section 6.4 for the setting procedure.
4)	Module connector	A connector connects the power supply module, I/O module, or special function module. Attach the supplied connector cover (or a blank cover module for QA1S6□B base module) on the reserved connectors with no module to prevent the ingress of dust. Blank cover unit for QA1S65B/QA1S68B: A1SG60
5)	Screw hole for fastening modules	A screw hole used for fastening a module to the base. Screw size: M4 × 12
6)	Base module installation hole	A hole used for mounting the base module to a panel such as a control panel. (M5 screw)
7)	DIN rail hook	A hook used for DIN rail mounting.

6.4 Setting the Expansion Stage Numbers

This section describes how to set the expansion stage number to use the expansion base module.



Stage number setting for expansion base modules

	Stage number setting						
	1th stage	2th stage	3th stage	4th stage	5th stage	6th stage	7th stage
Position of connector pin in stage number setting connector							

POINTS

(1) To set the stage number setting connector, select the appropriate number from 1 through 7 in ascending order according to the number of expansion modules.

(2) Do not assign the same stage number to several modules or skip any stage numbers. Otherwise, improper I/O operation results.

MEMO

7. MEMORY CARD AND BATTERY

This chapter explains the specifications and handling of the memory card and the battery that can be used with QCPU-A.

7.1 Specifications of Memory Card

The memory card that can be used with QCPU-A conforms to the specifications of JEIDA/PCMCIA small PC card.
QCPU-A can contain only one memory card.

(1) SRAM card

Item \ Type name	Q2MEM-1MBS
Memory capacity after format	1011.5kbyte
Number of storable files	256
Number of insertions	5000 times max.
Dimensions	42.8 (W) × 45 (H) × 3.3 (D)
Weight (kg)	15

7.2 Specifications of Battery (for CPU module and memory card)

(1) Battery for CPU module

Item \ Type name	Q6BAT
Type	Manganese dioxide lithium primary battery
Initial voltage (V)	3.0
Nominal current (mA/h)	1800
Expected life (Storage life)	10 years (at ordinary temperature)
Total length of power failure	Refer to section 7.7.1.
Usage	Retains the contents of program memory and standard RAM during power failure.

(2) Battery for memory card

Item \ Type name	Q2MEM-BAT
Type	Graphite fluoride lithium primary battery
Initial voltage (V)	3.0
Nominal current (mA/h)	48
Expected life (Storage life)	4 years (at ordinary temperature)
Total length of power failure	Refer to section 7.7.1.
Usage	Retains the contents of SRAM card during power failure.

7.3 Handling the memory card

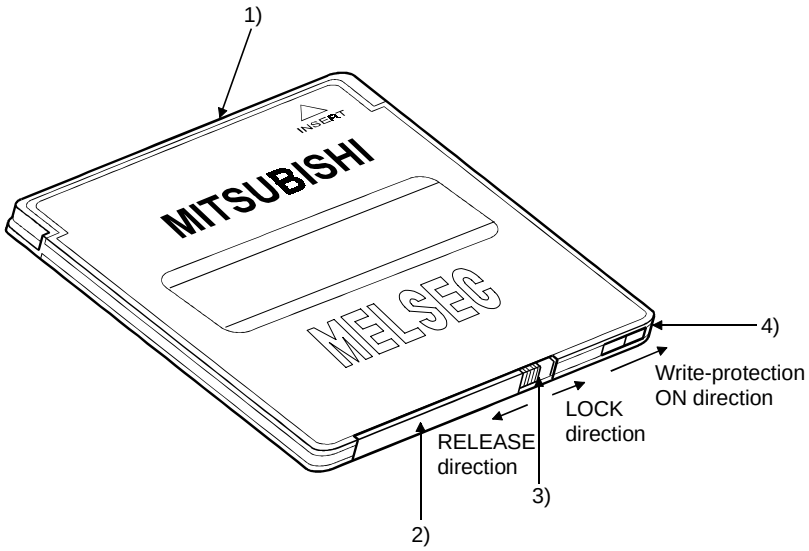
(1) Inserting a battery into the SRAM card

A battery is packaged with your SRAM card in order to retain memory during power failure. Be sure to insert the battery into the SRAM card before using the card.

POINT
Although a battery is inserted into the CPU module, the memory of the SRAM card will not be backed up until a battery is inserted into the card. Also, if a battery is inserted into the SRAM card but not into the CPU module, the memory of the standard RAM of the CPU module will not be backed up.

7.4 Part names of memory card

This section describes the part names of the memory card.



No.	Name	Usage
1)	Connector section	A connector section connected to the CPU module.
2)	Battery holder	Holds the lithium battery for data backup of the SRAM memory.
3)	Battery holder lock switch＊	A switch to fasten the battery holder to the memory card. It is fastened at LOCK position (write-protect switch side). LOCK: The holder is fastened. RELEASE: The holder is released.
4)	Write-protect switch	Sets the write protection of the memory. The factory setting is OFF. ON : Disables writing data. OFF : Enables writing data.

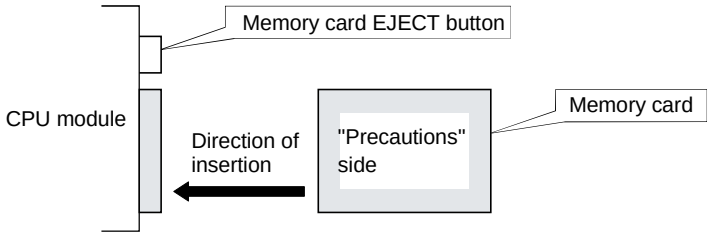
＊: The battery holder lock switch automatically returns from the RELEASE to LOCK position when the battery holder is removed.

7.5 Insertion/removal of the memory card

Be sure to turn OFF the CPU module before inserting/removing the memory card into/from the CPU module.

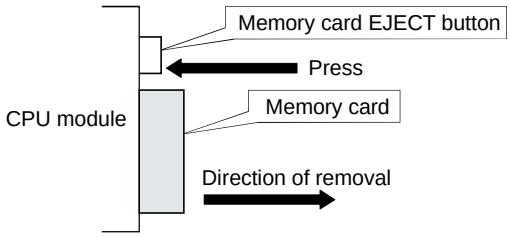
(1) Inserting the memory card

To insert the memory card into the CPU module, check the right orientation and fully insert the memory card into the connector so that the remaining section of the memory card is as high as the memory card EJECT button.



(2) Removing the memory card

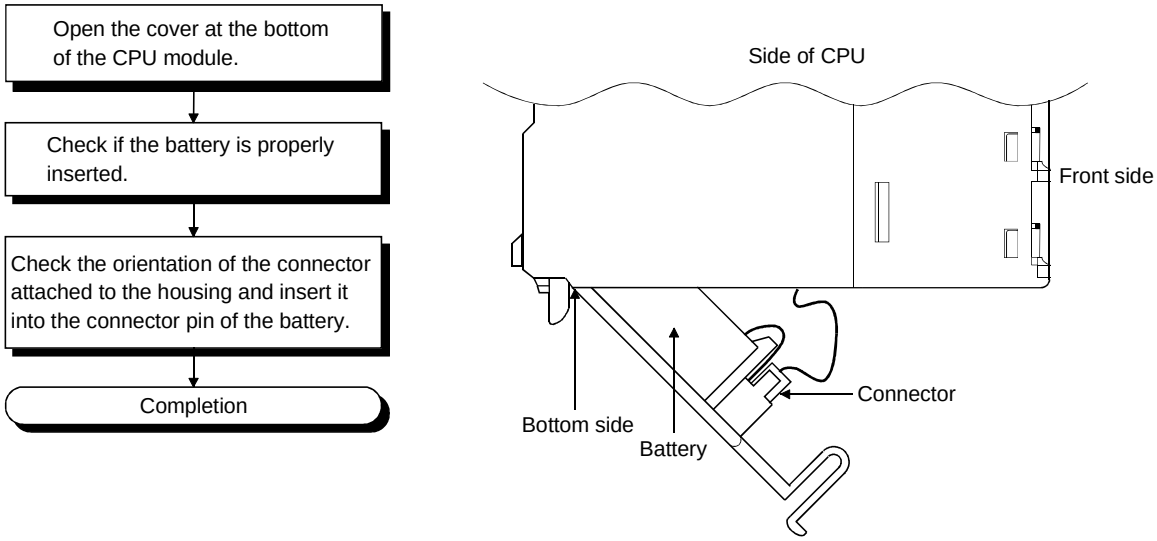
To remove the memory card from the CPU module, press the memory card EJECT button to push out the memory card.



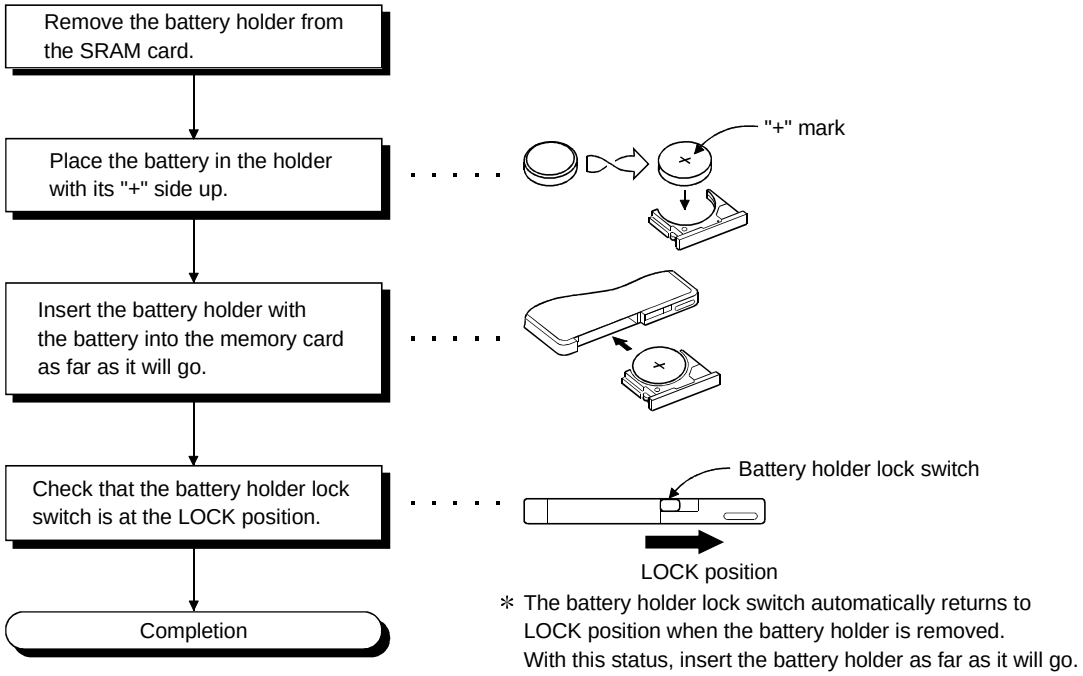
POINT
Note that the data in the memory card may be corrupted if the proper procedure above is not followed.

7.6 Inserting batteries (for CPU module and memory card)

(1) The battery for the CPU module is shipped with its connector removed. Connect the connector according to the procedure below:



(2) The battery for the SRAM card is shipped separately from the battery holder. To use the SRAM memory, set the battery holder according to the procedure below:



* The battery holder lock switch automatically returns to LOCK position when the battery holder is removed. With this status, insert the battery holder as far as it will go.

7.7 Battery replacement

Special relay M9006 or M9007 turns ON at the voltage drop of the backup battery for program and memory retention during power failure. The contents of the program and memory are not cleared immediately after these special relays turns ON, but they may be lost if you overlook these relays being turned ON.
Be sure to replace the battery before the total of power failure time after M9006 or M9007 turns ON reaches the specified retention time.

POINT

M9006 gives an alarm about low voltage of the battery. Data is retained within the specified time after M9006 turns ON; however, the battery should be replaced as soon as possible.

M9048 turns ON at the voltage drop of the battery for the standard RAM or SRAM card.

POINTS

The following table shows the relationship between the batteries in the CPU module and SRAM card and the memory backup.
The following two are the key factors:

① The battery in the CPU module does not back up the memory of the SRAM card.

② The battery in the SRAM card does not back up the memory of the CPU module.

AC power supply to CPU module	Battery in CPU module	Battery in SRAM card	Memory of CPU module	Memory of SRAM card
ON	ON	ON	○	○
		OFF	○	○
	OFF	ON	○	○
		OFF	○	○
OFF	ON	ON	○	○
		OFF	○	×
	OFF	ON	×	○
		OFF	×	×

○: Backup available ×: Backup not available

The reference battery service life and replacement procedures are described on the subsequent pages.

7.7.1 Battery service life

(1) Service life of the battery for the CPU module

The service life of the battery for the CPU module varies depending on the type of the CPU.

The battery service life for each CPU is shown below:

Battery service life / CPU type name	Battery service life (Total power failure time) [Hrs.]		
	Guaranteed value (minimum)	Actual value (typical)	After M9006 turns ON
Q02CPU-A	50625	79024	120
Q02HCPU-A, Q06HCPU-A	2140	16200	120

∗ The actual value indicates the average service life; the guaranteed value indicates the shortest service life.

(2) Service life of the battery for the SRAM card

The battery service life for the SRAM card is shown below:

Battery service life / Battery type name		Battery service life (Total power failure time) [Hrs.]		
		Guaranteed value (minimum)	Actual value (typical)	After M9006 turns ON
Q02MEM-BAT	At storage	690	6336	8
	During operation	11784	13872	8

∗ The actual value indicates the average service life; the guaranteed value indicates the shortest service life.

The life at storage indicates the time while the SRAM card is inserted into the PC CPU and the CPU is turned OFF, or while the SRAM card is removed from the CPU.

The life during operation is the time while the SRAM card is inserted into the PC CPU and the CPU is turned ON.

POINT

Note that the SRAM card in the CPU consumes the battery voltage even when the CPU is turned ON.

For guidance, the service life of the battery for the SRAM card is guaranteed as approximately 1.1 years on the condition that it is inserted into the CPU and the CPU is turned on one hour a day.

The service life of Q6BAT is approximately 10 years when it is not connected with the CPU module, or when it is connected with the CPU and is always live. Q6BAT should be immediately replaced when the total of power failure time exceeds the guaranteed life in the table above and M9006 turns ON.

Even when the total of power failure time is less than the guaranteed life in the table above, it is recommended to replace the battery within the following years in terms of preventive maintenance.

① Ten years for Q02CPU-A

② Four to five years for Q02HCPU-A or Q06HCPU-A

The battery for the SRAM card should be replaced immediately after M9048 turns ON.

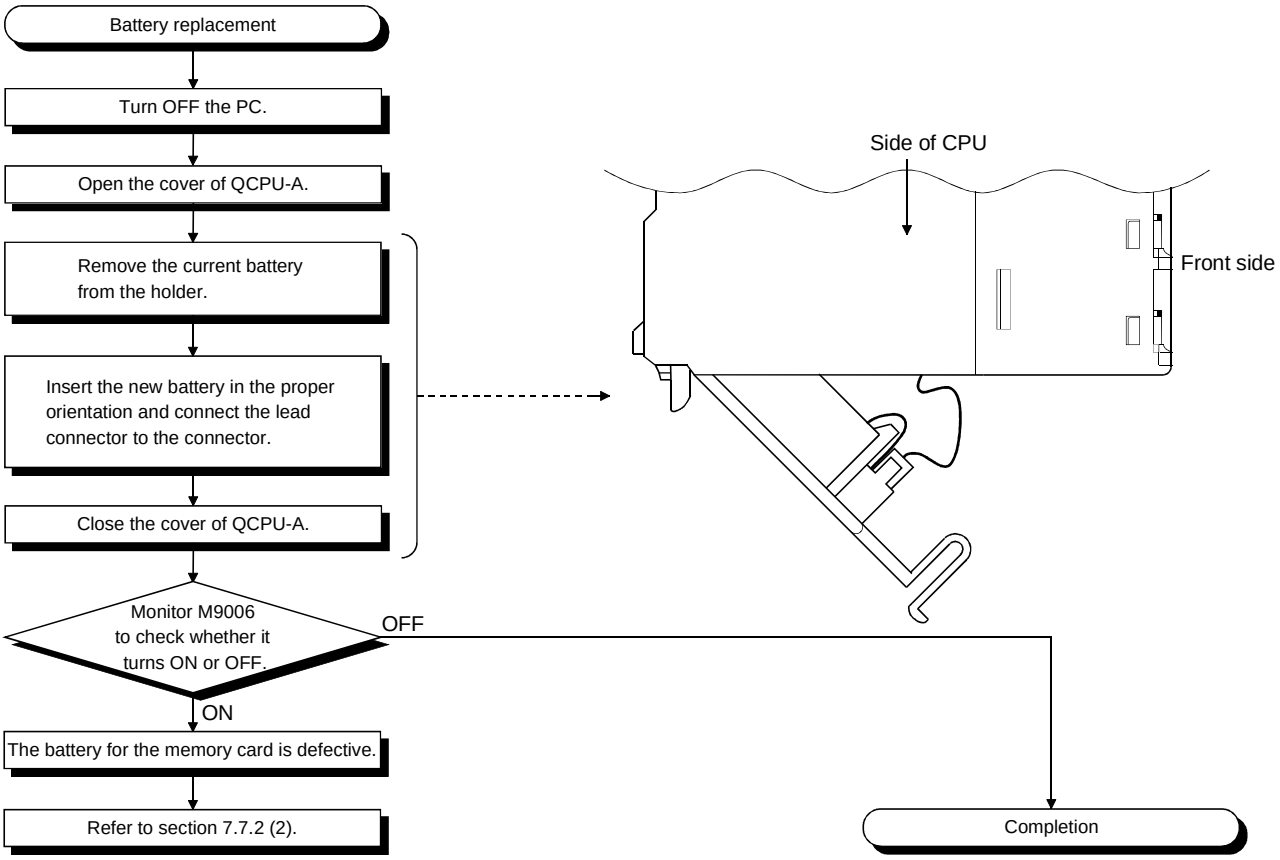
7.7.2 Battery replacement procedure

(1) Replacing the battery for the CPU module

When the service life of the battery for the CPU module expires, replace the battery in the following procedure:
Turn ON the CPU module 10 minutes or more before removing the battery.
The capacitor backs up the memory for several minutes even when the battery is removed. When the battery is removed for the following guaranteed time, the contents of the memory may be lost. Replace the battery as quickly as possible.
You can also replace the battery while the CPU is turned ON. In such a case, the contents of the memory are retained with the power supply voltage from the power supply module.

Backup time by capacitor

Backup time by capacitor [min.]
3



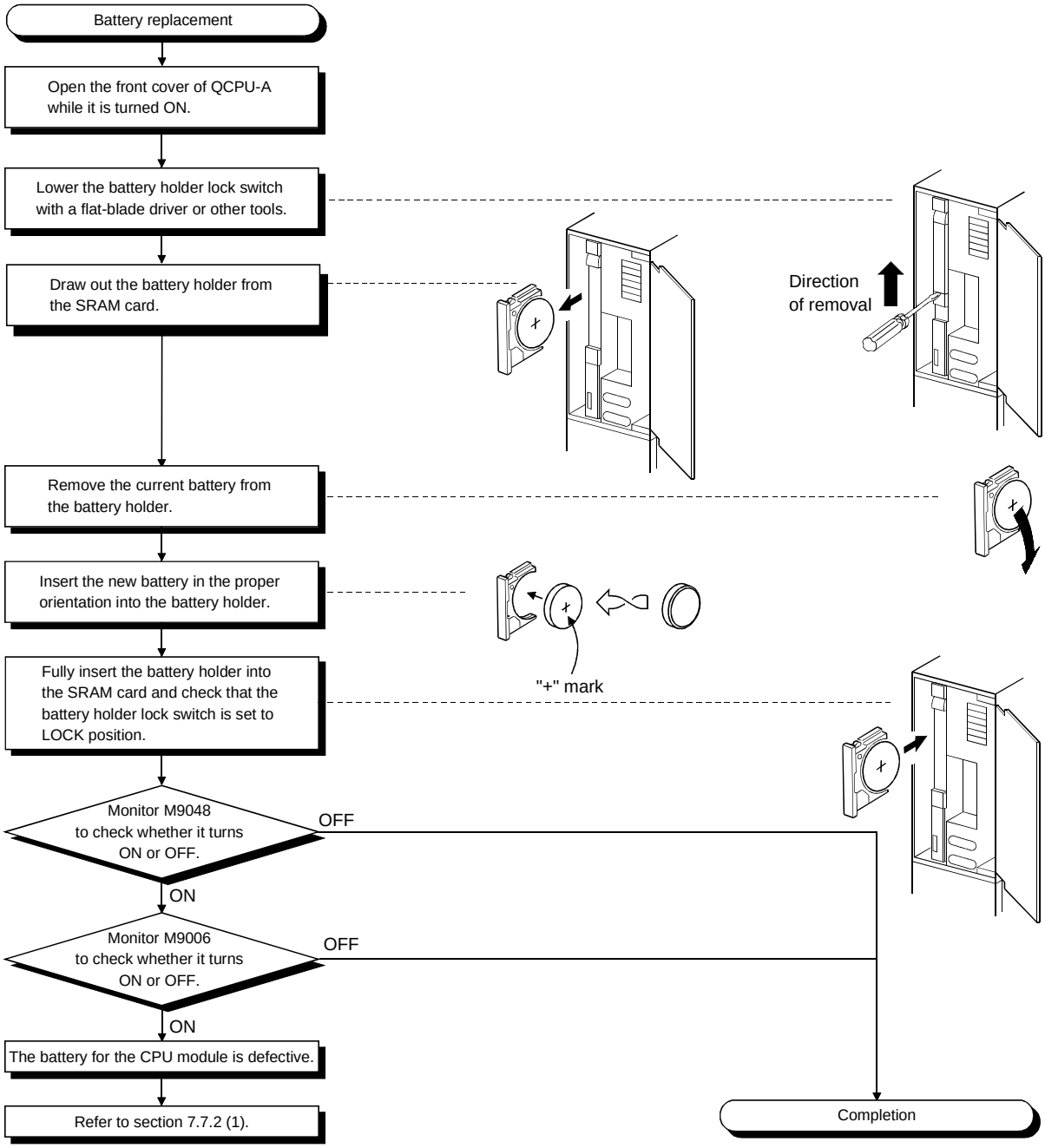
(2) Replacing the battery for SRAM card

When the service life of the battery for the SRAM card expires, replace the battery in the following procedure. The memory card does not have the secondary battery to back up the memory. Therefore, to retain data, the battery should be replaced while the SRAM card is inserted into the CPU module that is turned ON.

POINTS

Note the following precautions before replacing the battery.

① Back up the data with GPPW before replacing the battery.
② The battery is replaced while the CPU module is turned ON. Be extremely careful with surroundings to avoid an electric shock.
③ When removing/inserting the battery holder from/into the SRAM card, be careful not to drop the battery from the battery holder.



8. EMC DIRECTIVE AND LOW-VOLTAGE INSTRUCTION

For the products sold in the European countries, the conformance to the EMC Directive, which is one of the European Directives, has been legally obliged to be certified since 1996. Also, the conformance to the Low Voltage Directive, which is one of the European Directives, has been legally obliged to be certified since 1997.
The manufacturers who recognize their products to conform to the EMC Directive and Low Voltage Directive require to declare that their products conform to these Directives and put "CE mark" on their products.

8.1 Requirements for conformance to EMC Directive

The EMC Directive specifies both "emission (electromagnetic interference) which means that an intense electromagnetic wave is not emitted to the outside" and "immunity (electromagnetic sensitivity) which means that products are not affected by the electromagnetic wave from the outside". The applicable products are requested to meet these requirements. The sections 8.1.1 through 8.1.6 summarize the precautions on conformance to the EMC Directive of the machinery constructed using the MELSEC-Q series sequencers.
The detail of these precautions has been prepared based on the requirements for the control and the applicable standards owned by us and with our best efforts. However, we will not assure that the overall machinery manufactured according to that detail conform to the above-mentioned directives. The method of conformance to the EMC directive and the judgment on whether or not the machinery conforms to the EMC Directive must be determined finally by the manufacturer of the machinery.

8.1.1 Standards on EMC Directive

The standards on the EMC Directive are listed below.

Specification	Test item	Test detail	Standard value
EN50081-2 : 1995	EN55011 Radiation noise ∗2	Radio waves emitted from the product are measured.	30 M-230 M Hz QP : 30 dBμ V/m (30 m in measurement range) ∗1 230 M-1000 M Hz QP : 37 dBμ V/m (30 m in measurement range)
	EN55011 Conductive noise	Noise emitted from the product to the power line is measured.	150 k-500 k Hz QP : 79 dB, Mean : 66 dB ∗1 500 k-30 M Hz QP : 73 dB, Mean : 60 dB
EN61131-2 : 1996	EN61000-4-2 Electrostatic immunity ∗2	Immunity test in which static electricity is applied to the cabinet of the equipment.	15 k V Aerial discharge
	EN61000-4-4 First transient burst noise ∗2	Immunity test in which burst noise is applied to the power line and signal lines.	Power line : 2 k V Digital I/O (24 V or higher) : 1 k V (Digital I/O (24 V or less)) > 250 V (Analog I/O, signal lines) > 250 V
	EN61000-4-3 Radiation field AM modulation ∗2	Immunity test in which field is irradiated to the product.	10 V/m, 26-1000 M Hz, 80%AM modulation@1 k Hz
	EN61000-4-12 Damped oscillation wave immunity	Immunity test in which damped oscillatory wave is superimposed on the power line.	Power line : 1 k V Digital I/O (24 V or higher) : 1 k V

(∗1) QP : Quasi-peak value, Mean : Average value
(∗2) The PC is an open type device (device installed to another device) and must be installed in a conductive control box.
The tests for the corresponding items were performed while the PC was installed to inside the control box.

8.1.2 Installation instructions for EMC

(1) Control cabinet

When constructing a control cabinet where the PC system will be installed, the following instructions must be followed.

(a) Use a conductive control cabinet.

(b) When attaching the control cabinet's top plate or base plate, mask painting and weld so that good surface contact can be made between the cabinet and plate.

(c) To ensure good electrical contact with the control cabinet, mask the paint on the installation bolts of the inner plate in the control cabinet so that contact between surfaces can be ensured over the widest possible area.

(d) Earth the control cabinet with a thick wire so that a low impedance connection to ground can be ensured even at high frequencies. (22 mm^2 wire or thicker is recommended.)

(e) Holes made in the control cabinet must be 10 cm (3.94 in.) diameter or less. If the holes are 10 cm (3.94 in.) or larger, radio frequency noise may be emitted.
In addition, because radio waves leak through a clearance between the control panel door and the main unit, reduce the clearance as much as practicable.
The leakage of radio waves can be suppressed by the direct application of the EMI gasket listed below on the paint surface.
Our tests have been carried out on the panel having the damping characteristics of 37 db max. and 30 db mean (measured by 3 m method with 30 to 300 M Hz).

(2) Connection of power and earth wires

Earthing and power supply wires for the PC system must be connected as described below.

(a) Provide an earthing point near the power supply module. Earth the power supply's LG and FG terminals (LG : Line Ground, FG : Frame Ground) with the thickest and shortest wire possible. (The wire length must be 30 cm (11.18 in.) or shorter.) The LG and FG terminals function is to pass the noise generated in the PC system to the ground, so an impedance that is as low as possible must be ensured. As the wires are used to relieve the noise, the wire itself carries a large noise content and thus short wiring means that the wire is prevented from acting as an antenna.

(b) The earth wire led from the earthing point must be twisted with the power supply wires. By twisting with the earthing wire, noise flowing from the power supply wires can be relieved to the earthing. However, if a filter is installed on the power supply wires, the wires and the earthing wire may not need to be twisted.

8.1.3 Cables

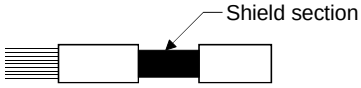
The cables extracted from the control panel contain a high frequency noise component. On the outside of the control panel, therefore, they serve as antennas to emit noise. To prevent the noise emission, ensure to use a shielded cable for the cables which are connected to the I/O unit and intelligent function unit and may be extracted to the outside of the control panel.
The use of a shielded cable is also increases noise resistance. The signal lines connected to the sequencer I/O unit and intelligent function unit use shielded type cables to assure a noise resistance under the conditions where the shield is earthed. If a shielded cable is not used or not earthed correctly, the noise resistance cannot meet the specified requirements.

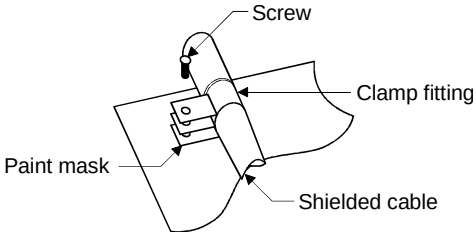
When a shield of the shielded cable is earthed to the cabinet body, please ensure that the shield contact with the body is over a large surface area. If the cabinet body is painted it will be necessary to remove paint from the contact area. All fastenings must be metallic and the shield and earthing contact must be made over the largest available surface area. If the contact surfaces are too uneven for optimal contact to be made either use washers to correct for surface inconsistencies or use an abrasive to level the surfaces. The following diagrams show examples of how to provide good surface contact of shield earthing by use of a cable clamp.

(1) Earthing of shielded of shield cable

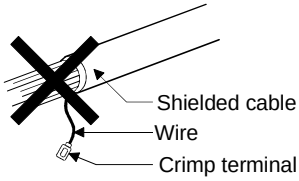
(a) Earth the shield of the shielded cable as near the unit as possible taking care so that the earthed cables are not induced electromagnetically by the cable to be earthed.

(b) Take an appropriate measure so that the shield section of the shielded cable from which the outer cover was partly removed for exposure is earthed to the control panel on an increased contact surface. A clamp may also be used as shown in the figure below. In this case, however, apply a cover to the painted inner wall surface of the control panel which comes in contact with the clamp.



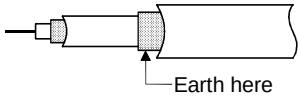


Note) The method of earthing by soldering a wire onto the shield section of the shielded cable as shown below is not recommended. The high frequency impedance will increase and the shield will be ineffective.



(2) MELSECNET (II) and MELSECNET/10 units

(a) Ensure to use a double-shielded coaxial cable for the MELSECNET unit which uses coaxial cables such as A1SJ71AF21 and A1SJ71BR11. Noise in the range of 30 MHz or higher in radiation noise can be suppressed by the use of double-shielded coaxial cables (Mitsubishi Cable: 5C-2V-CCY). Earth the outer shield to the ground. The precautions on shielding to be followed are the same as those stated in item (1) above.

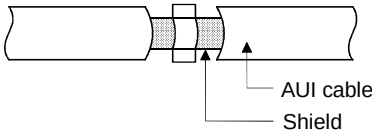


(b) Ensure to attach a ferrite core to the double-shielded coaxial cable connected to the MELSECNET unit. In addition, position the ferrite core on each cable near the outlet of the control panel. The ferrite core of the TDK-make ZCAT3035 is recommended.

(3) Ethernet module

Precautions to be followed when AUI cables and coaxial cables are used are described below.

(a) Ensure to earth also the AUI cables connected to the 10BASE5 connectors of the A1SJ71E71-B5. Because the AUI cable is of the shielded type, as shown in the figure below, partly remove the outer cover of it, and earth the exposed shield section to the ground on the widest contact surface.



(b) Ensure to use a double-shielded cable for the coaxial cables connected to the 10BASE2 connectors of the A1SJ71E71-B2. The precautions on earthing are the same as those for the MELSECNET unit.

(c) For the A1SJ71E71-B2/B5, ensure to attach a ferrite core after completing items (a) and (b) above. The ferrite core of the TDK-make ZCAT3035 is recommended.

Ethernet is the registered trademark of XEROX, US.

(4) Positioning Modules

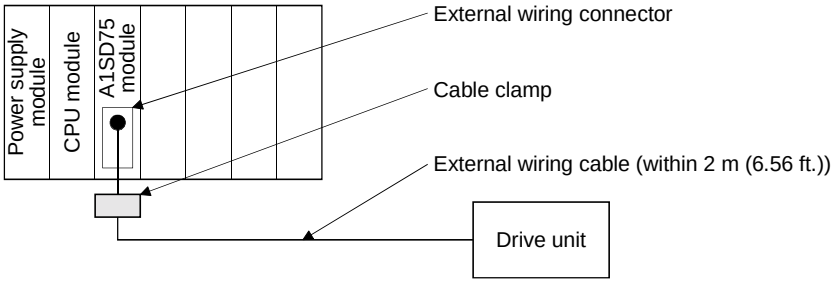
Precautions to be followed when the machinery to conform to the EMC Directive are configured using the A1SD75P□ -S3 are described below.

(a) When wiring with a 2 m (6.6 ft.) or less cable

Ground the shield section of the external wiring cable with the cable clamp. (Ground the shield at the closest location to the A1SD75 external wiring connector.)

Wire the external wiring cable to the drive unit and external device with the shortest distance.

Install the drive unit in the same panel.

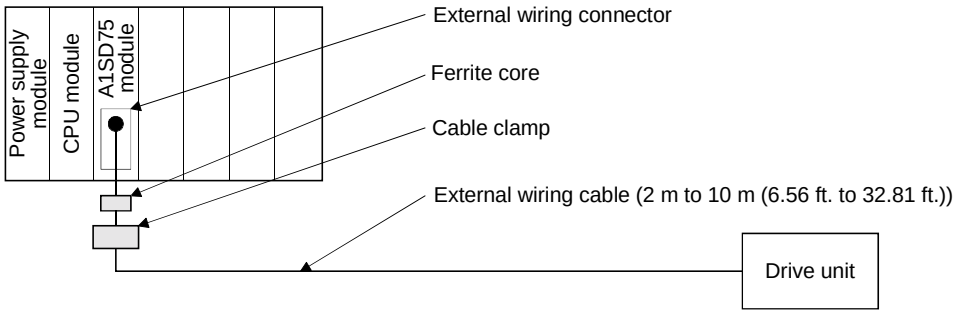


(b) When wiring with cable that exceeds 2 m (6.6 ft.), but is 10 m (32.8 ft.) or less

Ground the shield section of the external wiring cable with the cable clamp. (Ground the shield at the closest location to the AISD75 external wiring connector.)

Install a ferrite core.

Wire the external wiring cable to the drive unit and external device with the shortest distance.



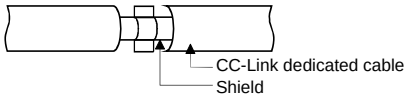
(c) Ferrite core and cable clamp types and required quantities

- Cable clamp
  Type : AD75CK (Mitsubishi Electric)
- Ferrite core
  Type : ZCAT3035-1330 (TDK ferrite core)
- Required quantity

Cable length	Prepared part	Required Qty		
		1 axis	2 axes	3 axes
Within 2 m (6.6 ft.)	AD75CK	1	1	1
2 m (6.6 ft.) to 10m (32.8 ft.)	AD75CK	1	1	1
	ZCAT3035-1330	1	2	3

(5) CC-Link Module

(a) Be sure to ground the cable shield that is connected to the CC-Link module close to the exit of control panel or to any of the CC-Link stations within 30 cm (11.8 in.) from the module or stations.
The CC-Link dedicated cable is a shielded cable. As shown in the illustration below, remove a portion of the outer covering and ground as large a surface area of the exposed shield part as possible.

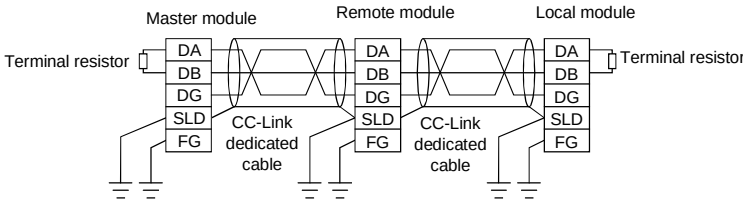


(b) Always use the specified CC-Link dedicated cable.

(c) Do not use a ferrite core for the CC-Link module or CC-Link stations.

(d) The CC-Link module, the CC-Link stations and the FG line inside the control panel should be connected at both the FG terminal and the SLD terminal as shown in the diagram below.

[Simplified diagram]



(6) I/O and other communication cables

For the I/O signal lines and other communication cables (RS232C, RS422), if extracted to the outside of the control panel, also ensure to earth the shield section of these lines and cables in the same manner as in item (1) above.

8.1.4 Power supply module

The precautions required for each power supply module are described below. Always observe the items noted as precautions.

Model	Precautions
A1S61P A1S62P	Unused
A1S63P (∗1)	Use the 24 V DC panel power equipment conforming to the CE standard.
A1S61PEU A1S62PEU A1S61PN A1S62PN	Always ground the LG and FG terminals after short-circuiting them.

(∗1) If a sufficient filter circuitry is built into a 24 V DC external power supply module, the noise generated by A1S63P will be absorbed by that filter circuit, so a line filter may not be required.
Filtering circuitry of version F or later of A1S63P is improved so that a external line filter is not required.

8.1.5 Ferrite core

A ferrite core has the effect of reducing radiation noise in the 30 M Hz to 100 M Hz band. With the exception of some models, it is not required to fit ferrite cores to cables, but it is recommended to fit ferrite cores if shield cables pulled out of the enclosure do not provide sufficient shielding effects. The ferrite cores used in our tests are TDK's ZCAT3035.
It should be noted that the ferrite cores should be fitted to the cables in the position immediately before they are pulled out of the enclosure. If the fitting position is improper, the ferrite will not produce any effect.

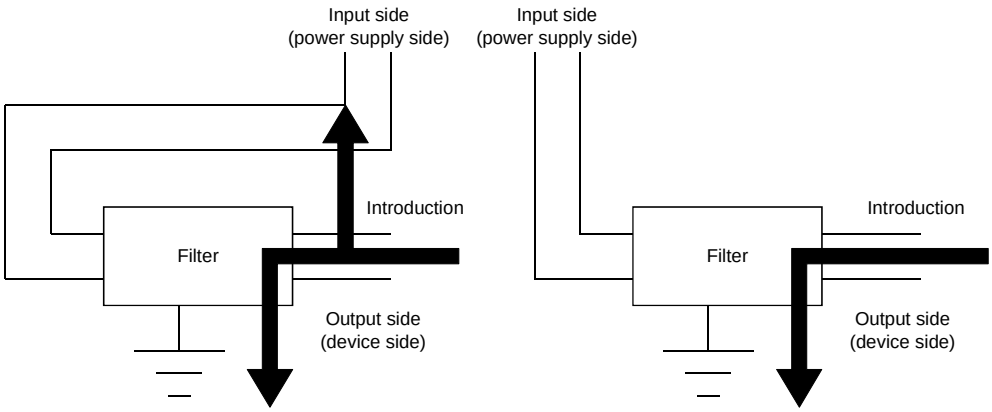
8.1.6 Noise filter (power supply line filter)

A noise filter is a component which has an effect on conductive noise. With the exception of some models, it is not required to fit the noise filter to the power supply line, but fitting it can further suppress noise. (The noise filter has the effect of reducing conductive noise in the 10 M Hz or less band.) Use any of the following noise filters (double π type filters) or equivalent.

Model name	FN343-3/01	FN660-6/06	ZHC2203-11
Manufacturer	SCHAFFNER	SCHAFFNER	TDK
Rated current	3 A	6 A	3 A
Rated voltage	250 V		

The precautions required when installing a noise filter are described below.

(1) Do not bundle the wires on the input side and output side of the noise filter. When bundled, the output side noise will be induced into the input side wires from which the noise was filtered.



(a) The noise will be included when the input and output wires are bundled.

(b) Separate and lay the input and output wires.

(2) Earth the noise filter earthing terminal to the control cabinet with the shortest wire possible (approx. 10 cm (3.94 in.)).

8.2 Requirement to Conform to the Low-Voltage Instruction

The low-voltage instruction, one of the European Instructions, is now regulated.
The low-voltage instruction require each device which operates with power supply ranging from 50 V AC to 1000 V and 75 V DC to 1500 V to satisfy necessary safety items.
In the Sections from 8.2.1 to 8.2.7, cautions on installation and wiring of the MELSEC-AnS series PC to conform to the low-voltage instruction regulation are described.
We have put the maximum effort to develop this material based on the requirements and standards of the regulation that we have collected. However, compatibility of the devices which are fabricated according to the contents of this manual to the above regulation is not guaranteed. Each manufacturer who fabricates such device should make the final judgement about the application method of the low-voltage instruction and the product compatibility.

8.2.1 Standard applied for MELSEC-AnS

The standard applied for MELSEC-AnS is EN61010-1 safety of devices used in measurement rooms, control rooms, or laboratories.

For the modules which operate with the rated voltage of 50 V AC/75 V DC or above, we have developed new models that conform to the above standard.

For the modules which operate with the rated voltage under 50 V AC/75 V DC, the conventional models can be used, because they are out of the low-voltage instruction application range.

8.2.2 Precautions when using the MELSEC-AnS series PC

Module selection

(1) Power module

For a power module with rated input voltage of 100/200 V AC, select a model in which the internal part between the first order and second order is intensively insulated, because it generates hazardous voltage (voltage of 42.4 V or more at the peak) area.
For a power module with 24 V DC rated input, a conventional model can be used.

(2) I/O module

For I/O module with rated input voltage of 100/200 V AC, select a model in which the internal area between the first order and second order is intensively insulated, because it has hazardous voltage area.
For I/O module with 24 V DC rated input, a conventional model can be used.

(3) CPU module, memory cassette, base unit

Conventional models can be used for these modules, because they only have a 5 V DC circuit inside.

(4) Special module

Conventional models can be used for the special modules including analog module, network module, and positioning module, because the rated voltage is 24 V DC or smaller.

(5) Display device

Use the display conforming to the CE standard.

8.2.3 Power supply

The insulation specification of the power module was designed assuming installation category II. Be sure to use the installation category II power supply to the PC.
The installation category indicates the durability level against surge voltage generated by a thunderbolt. Category I has the lowest durability; category IV has the highest durability.

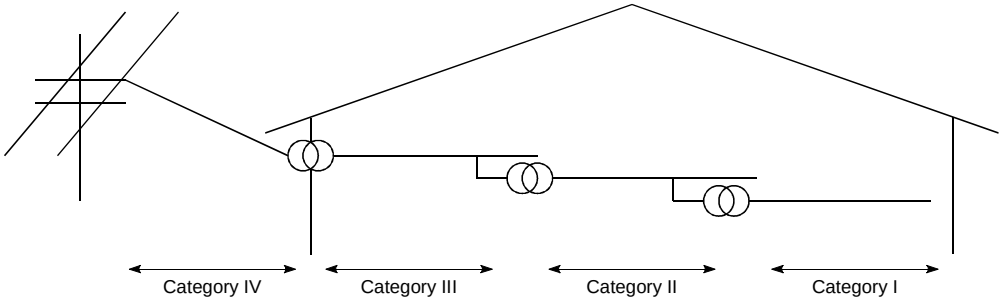


Figure 1. : Installation Category

Category II indicates a power supply whose voltage has been reduced by two or more levels of isolating transformers from the public power distribution.

8.2.4 Control box

Because the PC is an open device (a device designed to be stored within another module), be sure to use it after storing in the control box.

(1) Electrical shock prevention

In order to prevent persons who are not familiar with the electric facility such as the operators from electric shocks, the control box must have the following functions :

(a) The control box must be equipped with a lock so that only the personnel who has studied about the electric facility and have enough knowledge can open it.

(b) The control box must have a structure which automatically stops the power supply when the box is opened.

(2) Dustproof and waterproof features

The control box also has the dustproof and waterproof functions. Insufficient dustproof and waterproof features lower the insulation withstand voltage, resulting in insulation destruction. The insulation in our PC is designed to cope with the pollution level 2, so use in an environment with pollustion level 2 or below.

Pollution level 1 :	An environment where the air is dry and conductive dust does not exist.
Pollution level 2 :	An environment where conductive dust does not usually exist, but occasional temporary conductivity occurs due to the accumulated dust. Generally, this is the level for inside the control box equivalent to IP54 in a control room or on the floor of a typical factory.
Pollution level 3 :	An environment where conductive dust exits and conductivity may be generated due to the accumulated dust. An environment for a typical factory floor.
Pollution level 4 :	Continuous conductivity may occur due to rain, snow, etc. An outdoor environment.

As shown above, the PC can realize the pollution level 2 when stored in a control box equivalent to IP54.

8.2.5 Module installation

(1) Installing modules contiguously

In AnS series PCs, the left side of each I/O module is left open. When installing an I/O module to the base, do not make any open slots between any two modules. If there is an open slot on the left side of a module with 100/200 V AC rating, the printed board which contains the hazardous voltage circuit becomes bare. When it is unavoidable to make an open slot, be sure to install the blank module (A1SG60).

8.2.6 Grounding

There are two kinds of grounding terminals as shown below. Either grounding terminal must be used grounded.
Be sure to ground the protective grounding for the safety reasons.

Protective grounding : Maintains the safety of the PC and improves the noise resistance.

Functional grounding : Improves the noise resistance.

8.2.7 External wiring

(1) 24 V DC external power supply

For special modules that require a 24 V DC I/O module or external power supply, use a model whose 24 V DC circuit is intensively insulated from the hazardous voltage circuit.

(2) External devices

When a device with a hazardous voltage circuit is externally connected to the PC, use a model whose circuit section of the interface to the PC is intensively insulated from the hazardous voltage circuit.

(3) Intensive insulation

Intensive insulation refers to the insulation with the dielectric withstand voltage shown in Table 2.

Table 2 : Intensive Insulation Withstand Voltage
(Installation Category II, source : IEC664)

Rated voltage of hazardous voltage area	Surge withstand voltage (1.2/50 μs)
150 V AC or below	2500 V
300 V AC or below	4000 V

MEMO

9. LOADING AND INSTALLATION

9.1 Module Installation

9.1.1 Precautions on handling modules

This section describes the precautions to handle the CPU, I/O, special function, power supply, and base modules.

(1) Do not drop or apply a strong impact to the module housing, memory card, terminal block connectors, and pin connectors.

(2) Do not remove the PC board of the modules from housing. Otherwise, malfunctions may result.

(3) When using the expansion base module QA1S6□B, be sure to install the power supply module.
Although the module may work without the power supply module under light load, stable operation is not guaranteed.

(4) Limit the tightening torque for the module installation screws and terminal block screws within the following range:

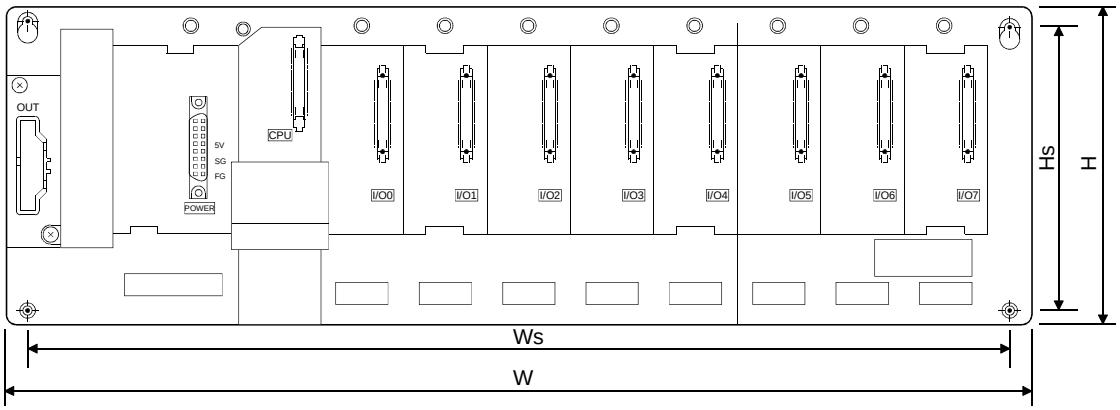
Location of screw	Tightening torque range
QCPU-A module fastening screw (M3 × 12)	36 to 48N • cm
AnS series module installation screw (M4)	78 to 118N • cm
I/O module terminal block installation screw (M3.5)	59 to 88N • cm
Power supply module terminal screw (M3.5)	

(5) When using the expansion cable, do not bind it with or place it close to the main circuit (high-voltage, large-current) lines.

9.1.2 Precautions on the base module installation

(1) Installing dimensions

The base modules are installed in the following dimensions:

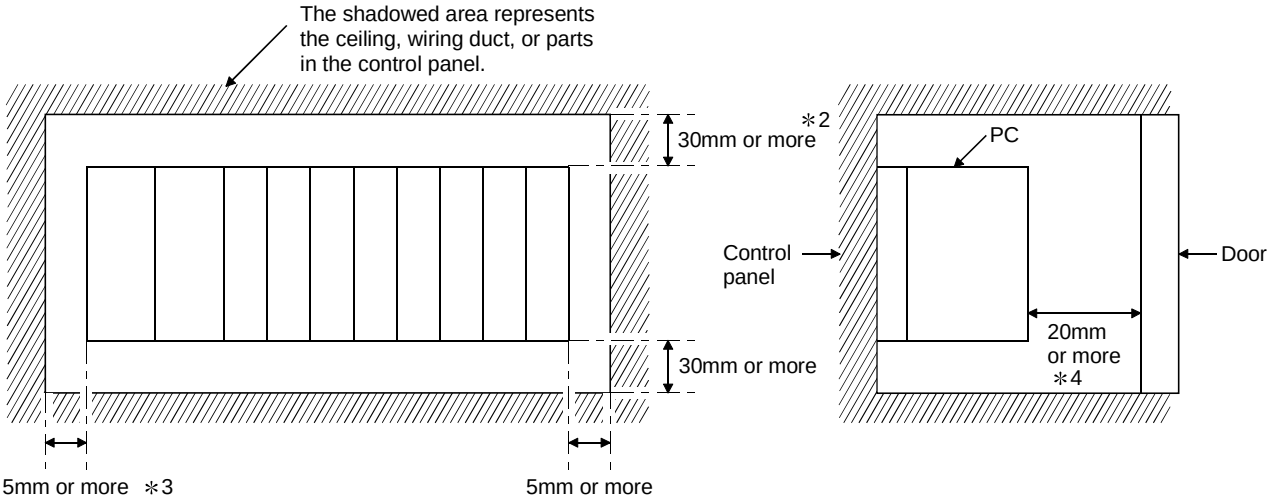


	QA1S33B	QA1S35B	QA1S38B	QA1S65B	QA1S68B
W	255	325	430	315	420
Ws ＊1	235	305	410	295	400
H	130				
Hs ＊1	110				

Unit: mm

＊1: The tolerances of Ws and Hs are ±0.3 mm, respectively.

(2) Position of module installation



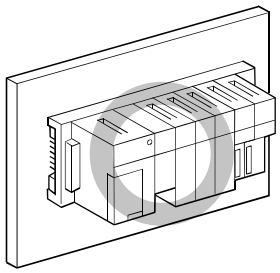
＊2: In the case where the wiring duct has the height of 50mm or less. In other cases, the figure should be 40mm or more.

＊3: The figure should be 20mm or more if an expansion cable is connected without removing the next module.

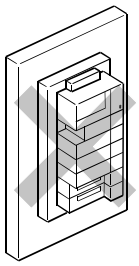
＊4: The figure should be 80mm or more for the connector type module.

(3) Module installing position

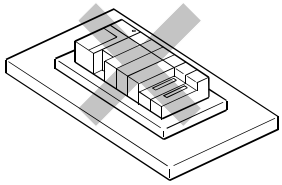
(a) Install the PC in the following position to ensure ventilation for heat radiation.



(b) Do not install the PC in the following positions.



Vertical position

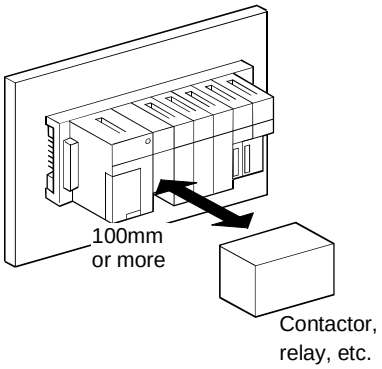


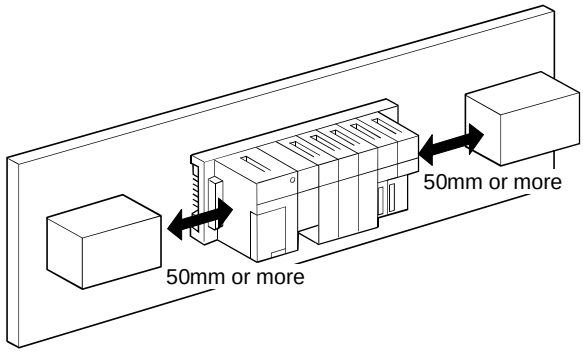
Horizontal position

(4) Install the base module on a flat surface.
When the base module is installed on an uneven surface, the PC board may be strained, resulting in malfunction.

(5) Do not install the PC close to a vibration source such as a large electromagnetic contactor or no-fuse breaker. Install the PC to the separate panel or isolate it as far as possible.

(6) Provide the following distances between the PC and devices (contactor or relay) to avoid the influence of radiation noise or heat.
- Devices installed in front of the PC: 100mm or more
- Devices installed on either side of the PC: 50mm ore more

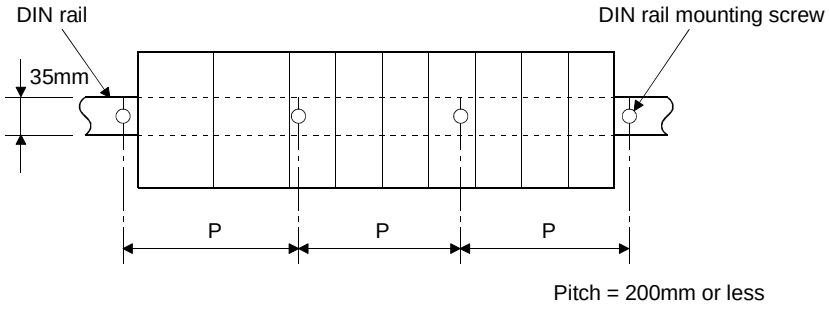




(7) Note the followings to mount the PC to the DIN rail.

(a) Applicable type name of the DIN rail (JIS-C2B12)
TH35-7.5Fe
TH35-7.5A1
TH35-15Fe

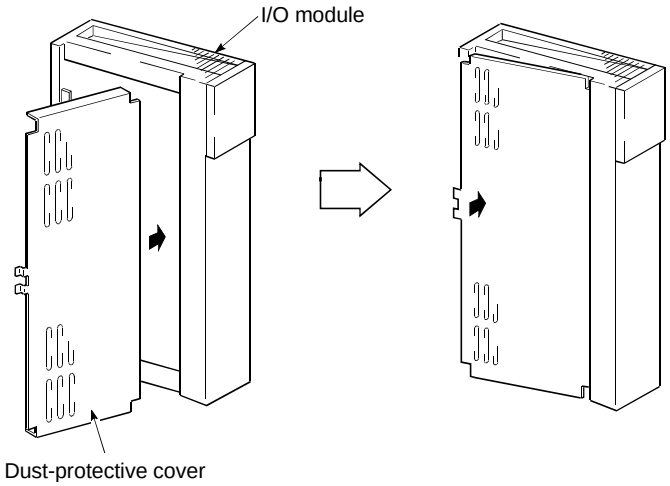
(b) Interval between DIN rail mounting screws
To use DIN rail TH35-7.5Fe or TH35-7.5A1, secure the rail with the DIN rail mounting screws with the pitch of 200mm or less to ensure strength.



9.1.3 Installing/removing the dust-protective cover

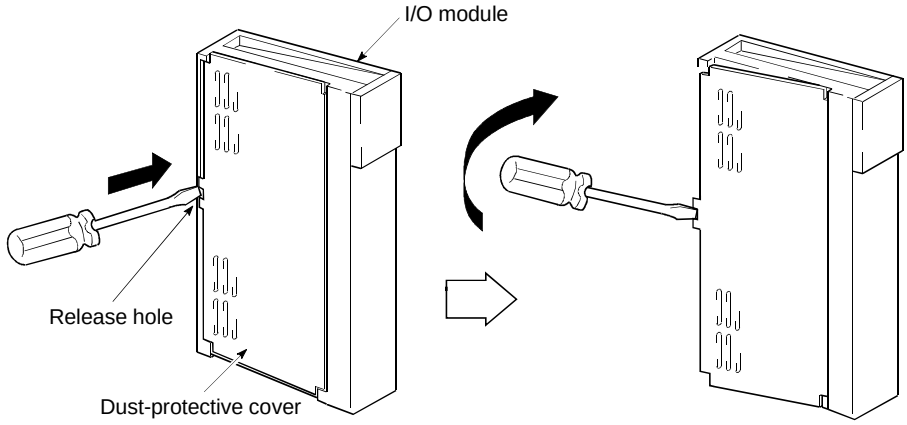
To use QCPU-A, it is necessary to install the dust-protective cover supplied with the basic base module to the I/O module on the right of the QCPU-A to prevent foreign objects from entering the I/O module.
Be sure to install the dust-protective cover. Otherwise, foreign objects may enter the I/O module, causing breakdown.
The installing/removing procedure of the dust-protective cover is described below:

(1) Installing the dust-protective cover



As illustrated above, insert the connector/terminal side of the dust-protective cover into the I/O module first, then press the cover against the I/O module. This completes the installation.

(2) Removing the dust-protective cover



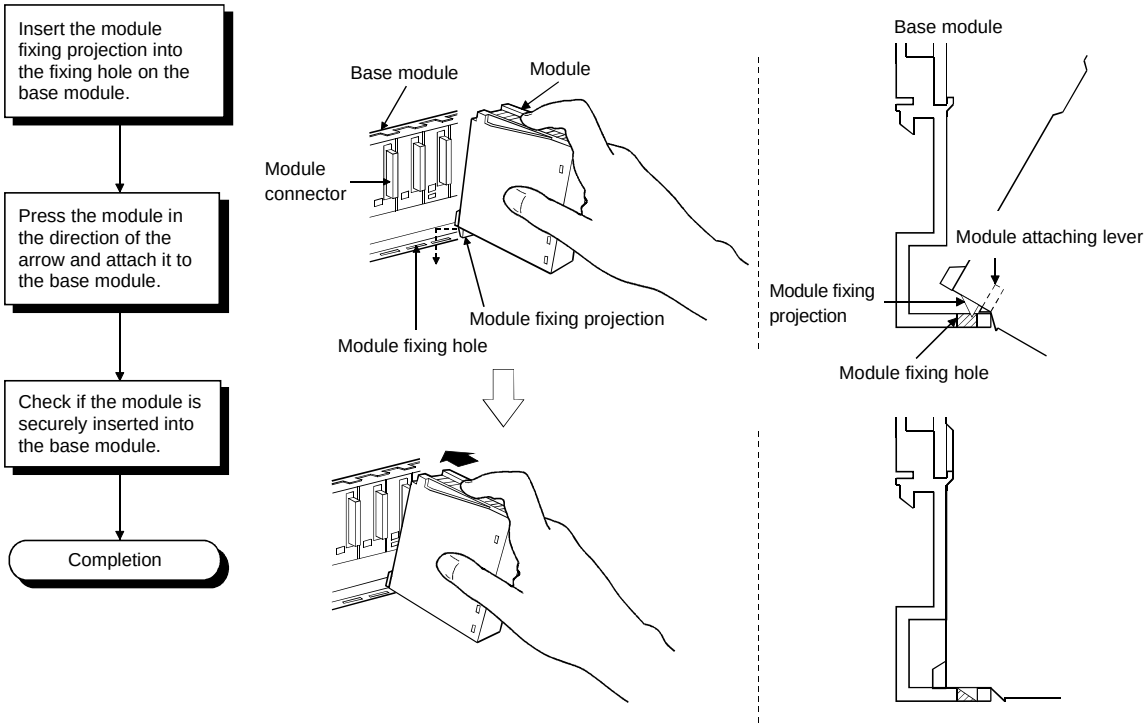
To remove the dust-protective cover from the I/O module, inset the tip of the flat-blade driver into the release hole as illustrated above, move the driver to the rear of the module, and release the claw of the cover from the release hole.

9.1.4 Installing/removing modules

This section describes how to install/remove the power supply, CPU, I/O, and special function modules to/from the base module.

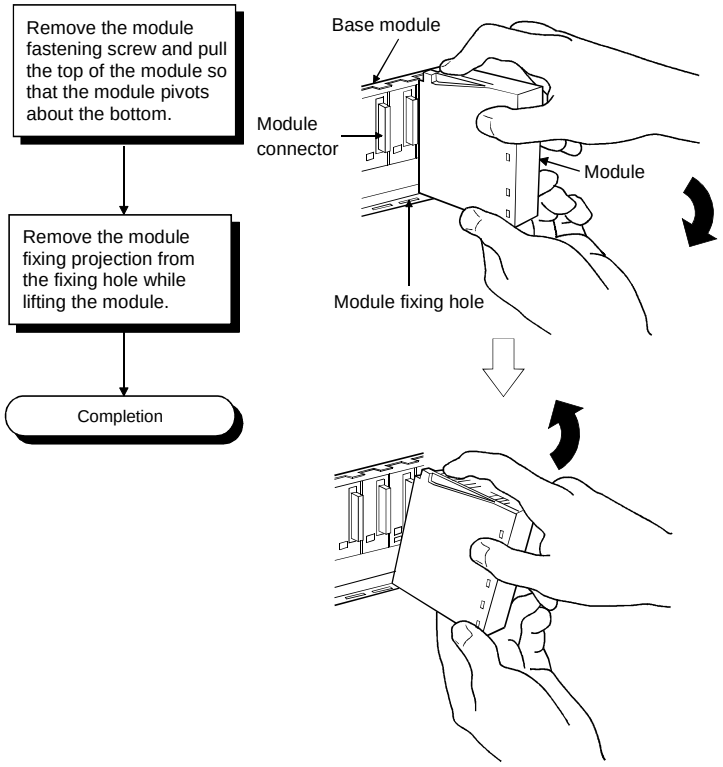
(1) Installing/removing QCPU-A

(a) Installing QCPU-A



POINTS
(1) Be sure to insert the module fixing projection into the fixing hole first. Forcefully mounting the module without inserting the projection into the hole may damage the module connector or the module itself.
(2) When using the modules in a place subjected to especially large vibration or impacts, secure the CPU module to the base module with a screw. QCPU-A module fastening screw: M3 × 12 (prepared by user)

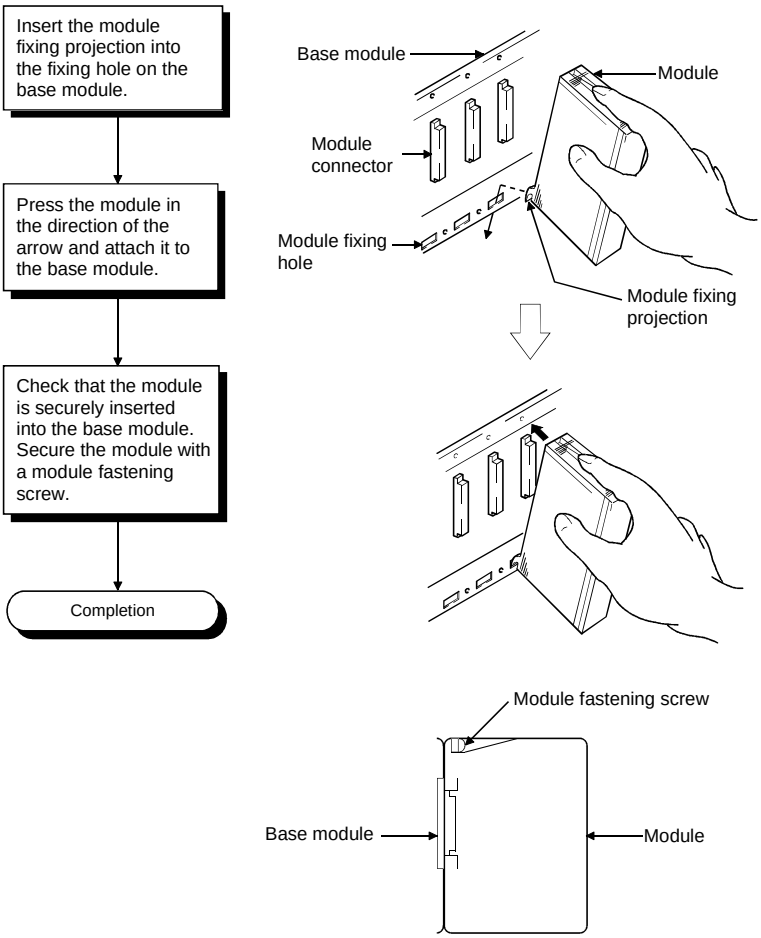
(b) Removing QCPU-A



POINT
When the CPU module is secured to the base module with a module fastening screw, be sure to remove the screw first, then remove the module fixing projection from the hole. Forcefully removing the module from the base module may damage the module.

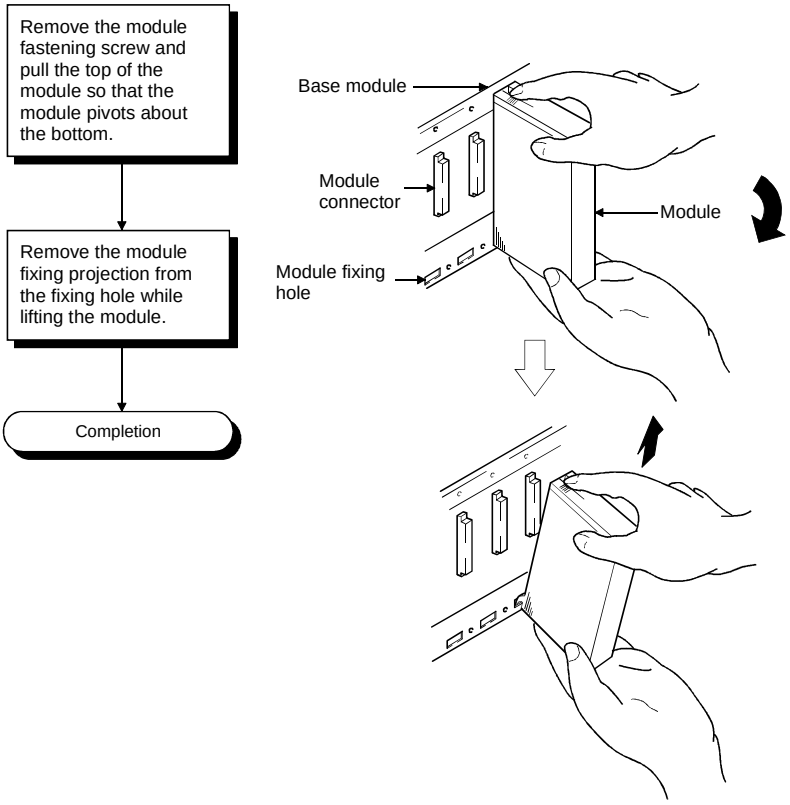
(2) Installing/removing modules other than QCPU-A

(a) Installing the module other than QCPU-A



POINT
Be sure to insert the module fixing projection into the fixing hole first. Forcefully mounting the module without inserting the projection into the hole may damage the module connector or the module itself.

(b) Removing the module other than QCPU-A

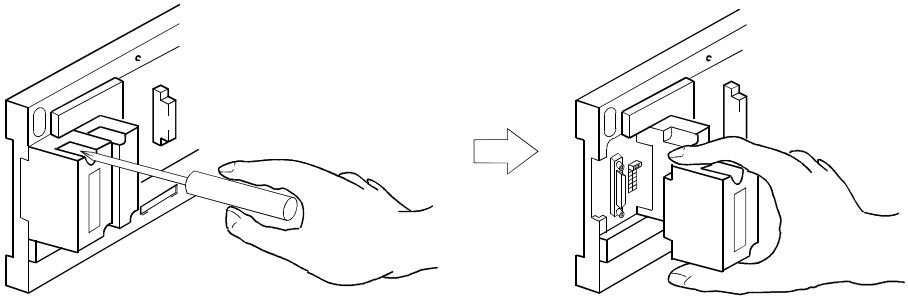


POINT
When the module is secured to the base module with a module fastening screw, be sure to remove the screw first, then remove the module fixing projection from the hole. Forcefully removing the module from the base module may damage the module.

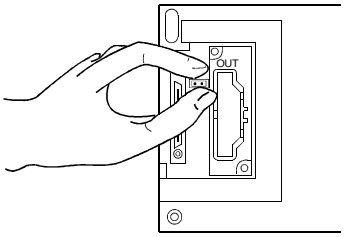
9.1.5 Setting expansion stages for the expansion base module

When two or more expansion base modules are used, the expansion stage number should be set with the stage number setting connector of the expansion base module. The expansion stage number is factory-set to "1," so that the first expansion base module requires no setting.
Set the expansion stage number in the following procedure.

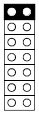
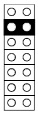
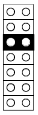
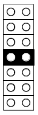
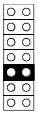
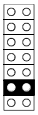
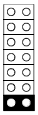
(1) The stage number setting connector is located inside the base cover of the IN connector of the expansion base module.
First, loosen the upper and lower screws on the base cover of the IN connector, and remove the base cover from the expansion base module.



(2) Insert a connector pin into the position of the desired stage number in the connector (PIN1) located between the IN and OUT expansion cable connectors.



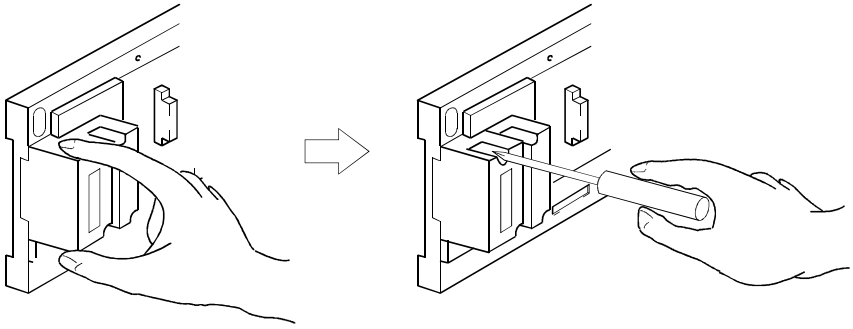
Stage number setting for expansion base modules

	Stage number setting						
	1st stage	2nd stage	3rd stage	4th stage	5th stage	6th stage	7th stage
Position of connector pin in stage number setting connector							

POINT

To set the stage number setting connector, select the appropriate number from 1 through 7 in ascending order according to the number of expansion modules.
Do not assign the same stage number to several modules or skip any stage numbers. Otherwise, improper I/O operation results.

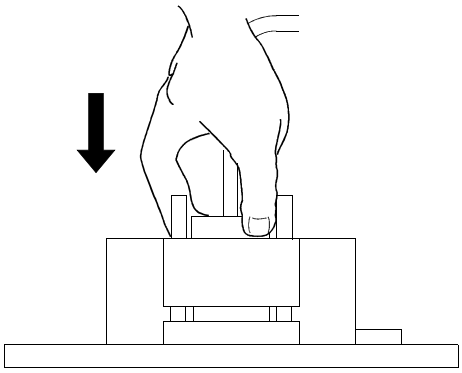
(3) Reattach the base cover to the expansion base module and fasten the screws.



9.1.6 Connecting/disconnecting the expansion cable

(1) Precautions on handling the expansion cable

- Do not step on the expansion cable.
- Be sure to attach the base cover to the base module before connecting the expansion cable to the base module.
  (After setting the stage number of the expansion base module, reattach the base cover and fasten it with screws.)
- When routing the expansion cable, provide 55mm or more minimum bend radius for the cable.
  If the bend radius is less than 55mm, malfunctions may occur due to the cable deterioration or breakage.
- Do not hold the ferrite cores at both ends of the cable when connecting/disconnecting the expansion cable.
  Instead, hold the connectors of the expansion cable to connect/disconnect it.
  Holding the ferrite cores may cause cable breakage inside the connector.
  Moreover, the change in the positions of the ferrite cores may change the cable characteristics.
  Be careful not to change the positions of the ferrite cores when handling the cable.

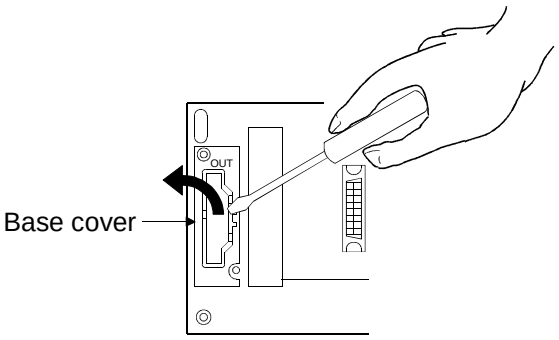


(2) Connecting the expansion cable

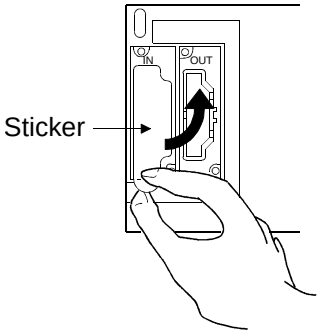
POINT

To connect the expansion cable to the basic base module and expansion base module, be sure to connect it from the OUT connector of the basic base module to the IN connector of the expansion base module. The system does not properly operate when the cable is connected from IN to IN, from OUT to OUT, or from OUT to IN connectors.
To connect two or more expansion base module, be sure to connect the cable from the OUT connector of the first expansion base module to the IN connector of the second expansion base module.

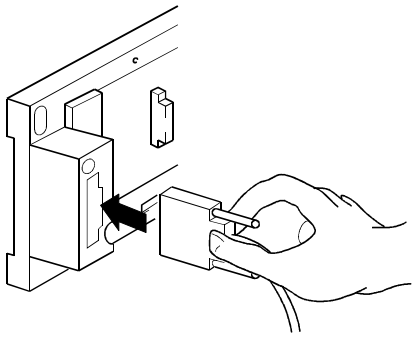
(a) To connect the expansion cable to the basic base module, remove the section below OUT of the base cover with a flat-blade driver (5.5 × 75.6 × 100) or other tools. Perform the same procedure also to connecting the expansion cable to the OUT connector of the expansion base module.



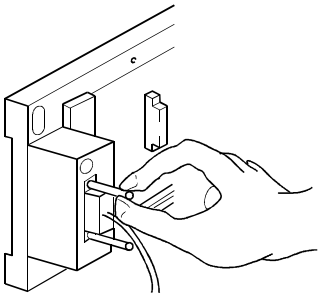
(b) To connect the expansion cable to the next expansion base module, remove the sticker attached on the section below IN of the base cover.



(c) Hold the connector of the expansion cable to connect the expansion cable to each base module.



(d) After connecting the expansion cable, be sure to tighten the fastening screws of the expansion cable connector.
(Tightening torque: 20N • cm)



(3) Disconnecting the expansion cable

To disconnect the expansion cable, confirm that the fastening screws are completely removed. Then, hold the connector of the expansion cable and disconnect it.

9.2 Concept of fail-safe circuit

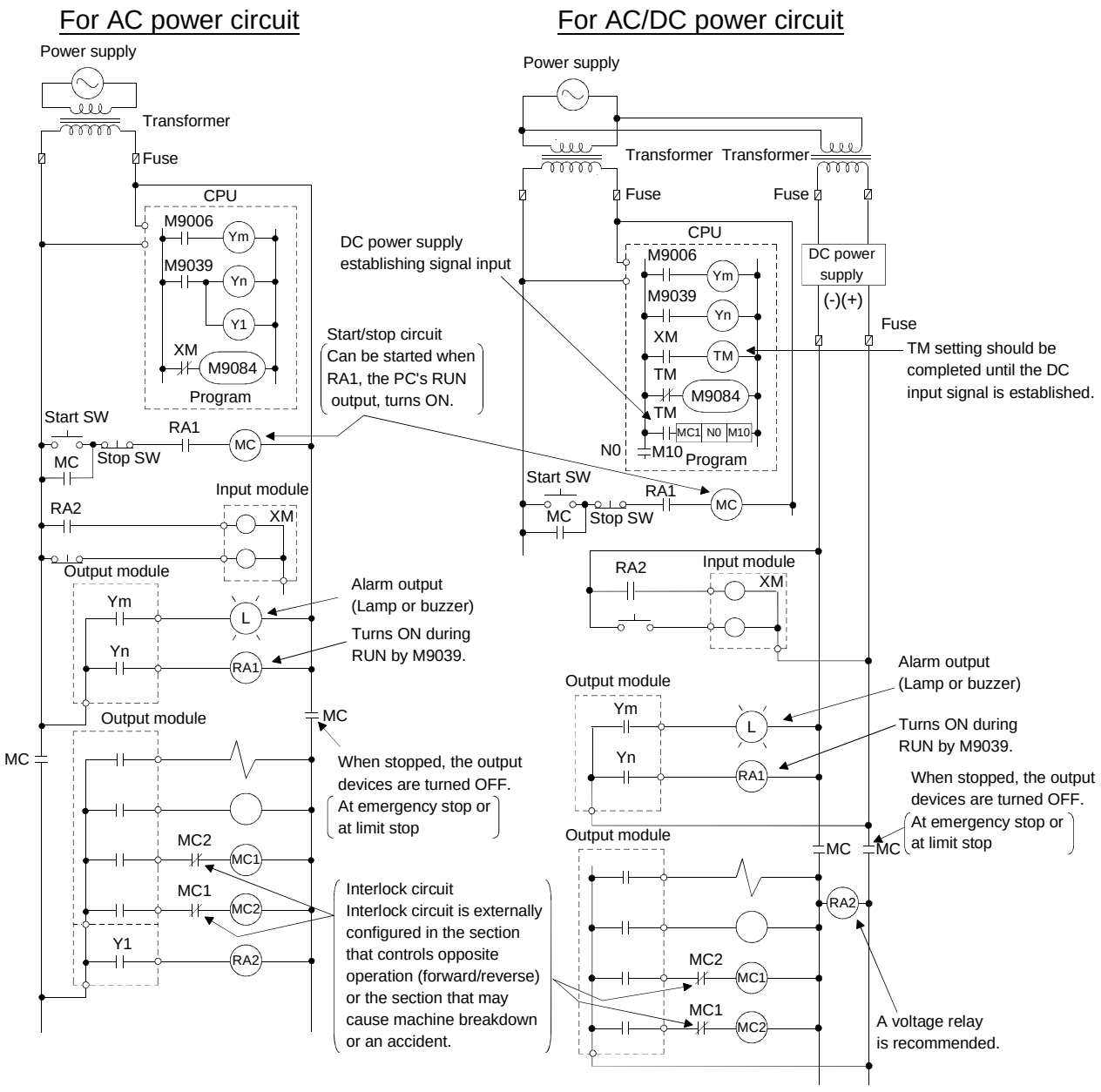
To prevent improper I/O operation of the PC, design the circuit configuration and program so that the PC system is started up only in the following procedures.

① Turn ON the power supply to the PC.
② Turn ON the external power supply for processing.
③ Turn ON the start SW.
④ The program turns ON the power supply to the output devices.
⑤ After the program confirms that all external power supplies are turned ON, the program for I/O control is executed.

If the startup procedure is changed so that, for example, the PC is turned ON after the external power supply for processing the DC output module is turned ON, the DC output module may produce improper output momentarily.
We have fully inspected the quality of the PC; however, some factor may cause breakdown or abnormal operation. In preparation for such problems, it is recommended to configure the circuit externally to the PC for the sections that may lead to the abnormal operation of whole system, the machine breakdown or an accident (such as an emergency stop, protection circuit, or interlock circuit).

The subsequent pages describe the examples of system circuit design and fail-safe provisions against PC breakdown from the standpoints above.

(1) Example of system circuit design



The startup procedure is as follows.

For AC power circuit

[1] Set the CPU to "RUN."
[2] Turn the power supply "ON."
[3] Set the start SW to "ON."
[4] When the electromagnetic contactor (MC) turns "ON," the program starts up the output devices.

For AC/DC power circuit

[1] Set the CPU to "RUN."
[2] Turn the power supply "ON."
[3] Set the start SW to "ON."
[4] When the DC power supply is established, turn RA2 "ON."
[5] When the DC power supply is established 100%, set the timer (TM) to "ON."
(The TM setting value is the time between the instant when RA2 is turned ON and the instant when the DC voltage is established 100%. Designate 0.5 seconds as the setting value.)
[6] When the electromagnetic contactor (MC) turns "ON," the program starts up the output devices.
(If a voltage relay is used as RA2, the timer (TM) in the program is unnecessary.)

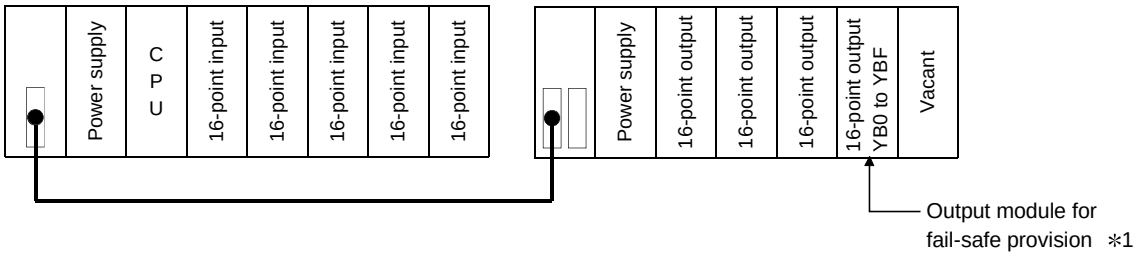
(2) Fail-safe provisions against PC breakdown

The self-diagnostic function can detect the breakdown of the CPU or memory of the PC. However, when the I/O control becomes abnormal, the CPU cannot detect it. In such a case, all points may turn ON/OFF depending on the breakdown level, so that the normal operation and safety of the controlled objects may not be ensured.

As a manufacturer, we have fully inspected the product quality. However, it is recommended to configure the fail-safe circuit externally to the PC to prevent machine breakdown or an accident in case of the PC breakdown due to some factors.

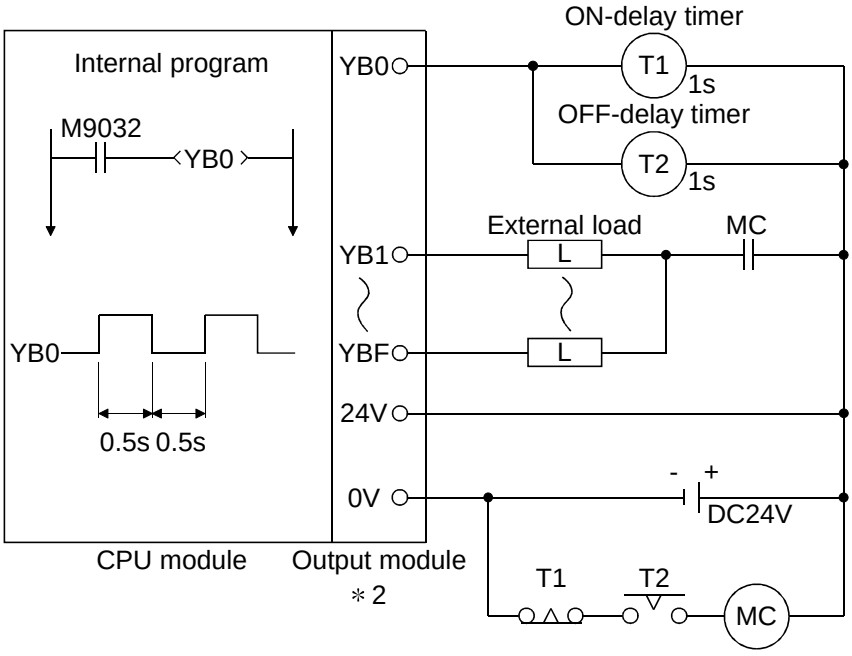
The examples of system configuration and fail-safe circuit are shown below:

<Example of system configuration>



∗1: The output module for the fail-safe provision should be installed to the last slot of the system (In the system example above, YB0 to YBF).

<Example of fail-safe circuit>



∗2: YB0 repeats ON and OFF at 0.5-second interval. Use the non-contact output module for YB0 (A transistor is used in the example above.).

9.3 Installation Environment

Avoid the following conditions for the installation location of QCPU-A system:

(1) Location where the ambient temperature exceeds the range of 0 to 55°C.

(2) Location where the ambient humidity exceeds the range of 10 to 90%RH.

(3) Location where condensation occurs due to a sudden temperature change.

(4) Location where corrosive gas or flammable gas exists.

(5) Location where a lot of conductive powdery substance such as dust and iron filing, oil mist, salt, or organic solvent exists.

(6) Location exposed to direct sunlight.

(7) Location where strong electric fields or magnetic fields form.

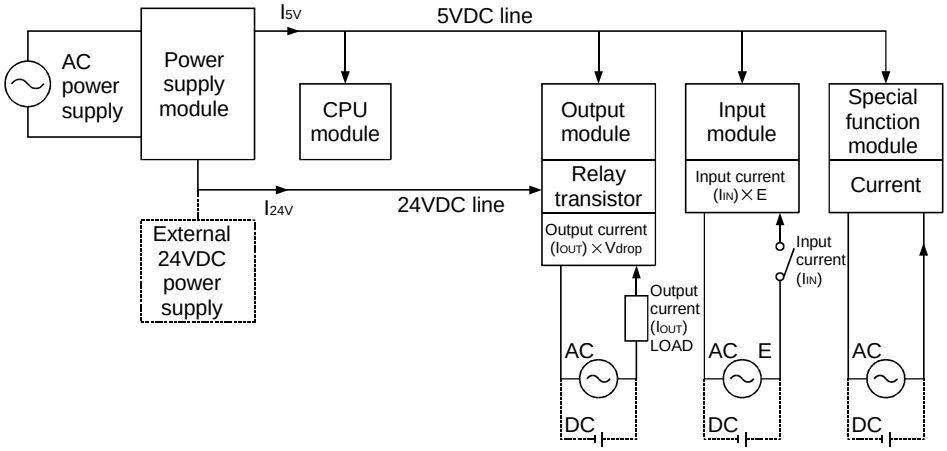
(8) Location where vibration or impact is directly applied to the main module.

9.4 Calculation Method of Heat Amount Generated by the PC

It is necessary to keep the temperature of the panel which stores the PC to the operating ambient temperature of the PC, which is 55°C, or below.
For radiation design of the panel, it is necessary to know the average power consumption (heat generation) of the devices and machinery stored inside. In this section, a method to obtain the average power consumption of the QCPU-A system is explained. Calculate the temperature increase in the panel from the power consumption.

Calculation method of average power consumption

The power consuming parts of the PC may be roughly classified into the blocks as shown below:



(1) Power consumption by power supply module
The power conversion efficiency of the power supply module is about 70%, and 30% is consumed as heat generated, thus, 3/7 of the output power is the power consumption. Therefore, the calculation formula is:

$$Wpw = \frac{3}{7}\{(I_{5V} \times 5) + (I_{24V} \times 24)\}\ (W)$$

I_{5V} : Current consumption of 5VDC logic circuit of each module
I_{24V} : Average current consumption of 24VDC power supply for internal consumption of the output module
(Current consumption equivalent to the points simultaneously ON)
……. Not applicable to a system where 24VDC is supplied externally and a power module which does not have a 24VDC output is used.

(2) Total power consumption of each module at 5VDC logic part
Power of the 5VDC output circuit of the power supply module is the power consumption of each module.

$W_{5V}=I_{5V} \times 5$ (W)

(3) Total 24VDC average power consumption of the output module (power consumption equivalent to the points simultaneously ON)
Average power of the 24VDC output circuit of the power supply module is the total power consumption of each module.

$W_{24V}=I_{24V} \times 24$ (W)

(4) Average power consumption of the output modules due to voltage drops at the output part (power consumption equivalent to the points simultaneously ON)

$W_{OUT}= I_{OUT} \times Vdrop \times$ Output points $\times$ Simultaneous ON ratio (W)

I_{OUT} : Output current (current actually used) (A)
Vdrop : Voltage drop of each output module (V)

(5) Average power consumption of the input modules at the input part (power consumption equivalent to the points simultaneously ON)

$W_{IN}= I_{IN} \times E \times$ Input points $\times$ Simultaneous ON ratio (W)

I_{IN} : Input current (actual value in case of AC) (A)
E : Input voltage (voltage for actual usage) (V)

(6) Power consumption of the power supply part of the special function module is:

$W_S= I_{5V} \times 5 \times I_{24V} \times 24 + I_{100V} \times 100$ (W)

The total of the power consumption calculated for each block as above is the power consumption of the PC system as a whole.

$W= W_{PW} + W_{5V} + W_{24V} + W_{OUT} + W_{IN} + W_S$ (W)

Calculate the amount of heat generation and temperature increase inside the panel from the total power consumption (W).
Simplified calculation formula to obtain temperature increase inside panel is shown next:

$$T= \frac{W}{UA} \ [°C]$$

W : Power consumption of the PC system as a whole (the value obtained above)
A : Inside surface area of the panel [m^2]
U : When inside temperature of the panel is kept constant by a fan, etc.....6
When the air inside the panel is not circulated.....4

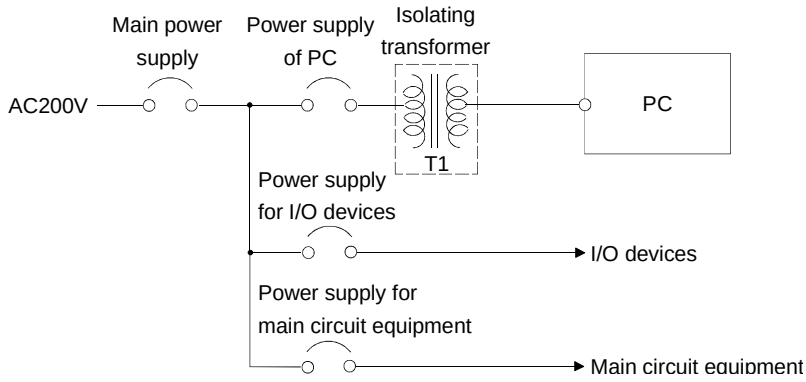
POINT

When the temperature increase inside the panel exceeds the specified range, it is recommended to lower the temperature inside the panel by installing a heat exchanger to the panel.
If a conventional ventilation fan is used, it sucks dust along with the outside air, which may affect the PC, so care must be taken.

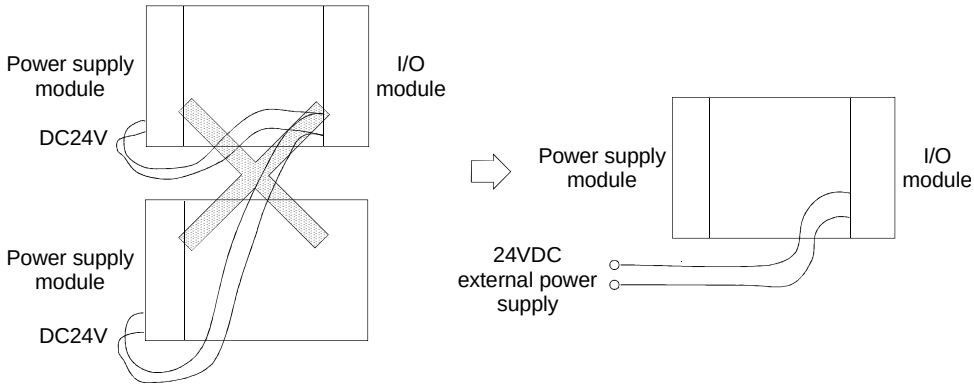
9.5 Wiring the power supply

This section describes the precautions on wiring the power supply.

(1) Separate the wiring systems for the power supply of the PC, the I/O devices, and the power equipment as shown below.
In a high-noise environment, connect an isolating transformer.



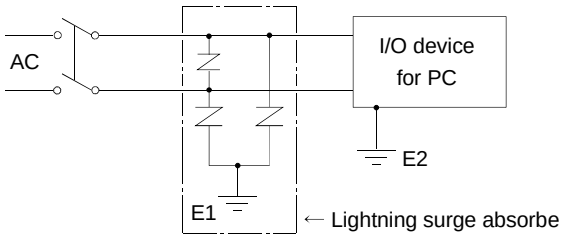
(2) Do not connect the 24VDC outputs of several power supply modules in parallel to supply power to a single I/O module. The parallel connection may damage the power supply module.



(3) Twist the 100VAC, 200VAC, and 24VDC cables as tight as possible and connect them between modules in the shortest distance.
To minimize the voltage drop, use the cable as thick as possible (2 mm^2 max.).

(4) Do not bind the 100VAC and 24VDC cables with or place them close to the main circuit (high-voltage, large-current) lines or I/O signal lines. Isolate them 100mm or more if possible.

(5) To avoid lightning surges, connect the lightning surge absorber as shown below:

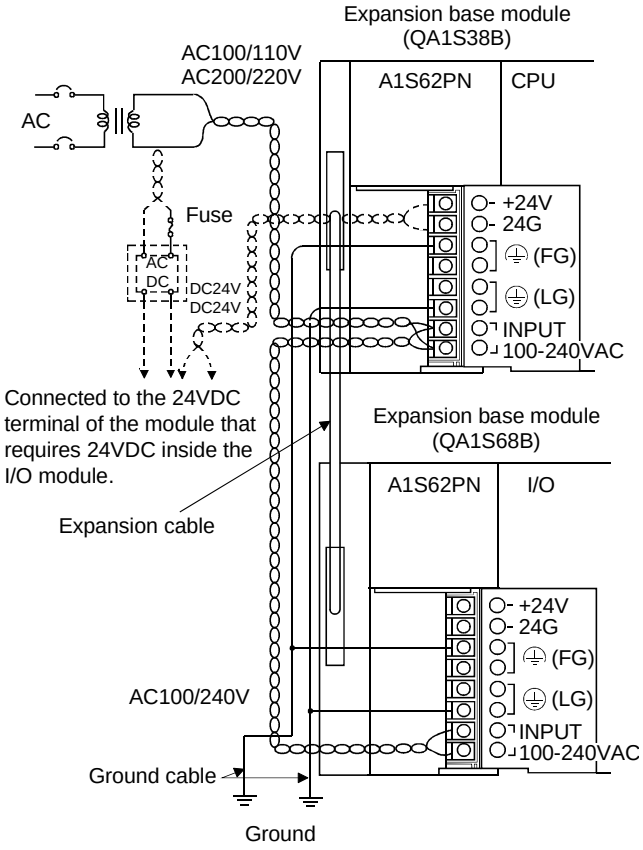


POINTS

(1) Isolate the ground for the lightning surge absorber (E1) and the ground for the PC (E2).

(2) Select the lightning surge absorber so that even the maximum power supply voltage does not exceed the allowable circuit voltage of the surge absorber.

(6) The following is the wiring example of the power supply and grounding cables for the connection of the basic and expansion base modules.



POINTS
(1) Use the cable as thick as possible (2mm^2 max.) for the 100/200VAC and 24VDC cables. Be sure to twist the cable from the connected terminal. Use the crimp terminal with an insulating sleeve to prevent short-circuit when a screw is loosened.
(2) When connecting the LG and FG terminals, be sure to connect them to the ground. Otherwise, they may easily be affected by noise. Touching the LG terminal may cause an electric shock because it has the potential of half the input voltage.
(3) A1S61PN and A1S62PN feature the wide range of 100 to 240VAC. They do not require switching.

9.6 Precautions on the connection with an uninterruptible power supply (UPS)

Note the following precautions when connecting the QCPU-A system with the uninterruptible power supply (hereafter abbreviated as UPS).

Use the UPS of constant inverter feeding system with the voltage distortion factor of 5% or less.
Do not use the UPS of constant commercial feeding system.

10. MAINTENANCE AND INSPECTION

DANGER	• Do not touch the terminals while the power is on. Doing so may cause electric shock or malfunctioning. • Be sure to connect the battery correctly. Do not charge, disassemble, heat, throw into fire, short, or solder batteries. Improper handling of batteries may cause injury to the operator or fire due to heat generation, explosion, or ignition. • Before cleaning the module or retightening the screws, make sure all phases of the power supply have been obstructed from the outside. Failure to completely shut off the power-supply phases may cause electric shock. If the screws are loose, it may result in short circuits, fire or malfunctioning. If the screws are tightened too much, it may damage the screws and the module may result in short circuits, malfunctioning or cause the module to fall out.

CAUTION	• Never disassemble or modify the module. This may cause breakdowns, malfunctioning, injury and fire. • Before attaching or detaching the module, make sure all phases of the power supply have been obstructed from the outside. Failure to completely shut off the power-supply phases may cause module breakdowns and malfunctioning. • When using a cellular phone, keep it 25 cm or more away from the PC. Otherwise, malfunction may result.

In order to use the PC always in good condition, conducting daily and periodical maintenance/inspection on the following items are strongly recommended.

10.1 Routine Inspection

Routine inspection items recommended are shown in Table 10.1.

Table 10.1 Routine Inspection

Item	Inspection Item		Content of Inspection	Decision Criteria	Action
1	Installation condition of the base unit		Confirm if installation screws are not loose or cover is not detached.	It is installed securely.	Retighten the screw.
2	Installation condition of the I/O modules		Confirm if the module installation screw is firmly tightened.	The installation screws are firmly tightened.	Tighten the module installation screw firmly.
3	Connection conditions		Loosening of terminal screw	No loosening.	Retighten the terminal screw.
			Closeness of crimp-style terminals	There is an appropriate distance.	Correct the distance.
			Connectors of extension cable	No loosening at connectors.	Retighten the connector fixed screw.
4	LEDs on the main module	"POWER" LED	Confirm it is lit.	The LED is ON. (Faulty if it is OFF.)	Per Section 11.2.2.
		"MODE" LED	Confirm it is lit.	The LED is ON. (Faulty if it is OFF.)	Per section 11.2.3.
		"RUN" LED	Confirm it is lit in the "RUN" state.	The LED is ON. (Faulty if it is OFF or flashing.)	Per Sections 11.2.4 and 11.2.5.
		"ERROR" LED	Confirm it is lit at error occurrence.	The LED is OFF. (ON when error has occurred.)	Per Sections 11.2.6 and 11.2.7.
		Input LED	Confirm if it correctly turns on and off.	The LED is ON when input is ON, and OFF when input is OFF. (Faulty other than the above.)	Per Section 11.4.1.
		Output LED	Confirm if it correctly turns on and off.	The LED is ON when output is ON, and OFF when output is OFF. (Faulty other than the above.)	Per Section 11.4.2.

10.2 Periodic Inspection

Inspection on items shown below should be conducted once or twice every six months to a year. Conduct the inspection when the equipment is moved or modified, or wiring is changed.

Table 10.2 Periodic Inspection

Item	Inspection Item		Content of Inspection	Decision Criteria	Action
1	Ambient environment	Ambient temperature	Measure with temperature and humidity gauge. Measure presence of corrosive gasses.	0 to 55°C	When used in a panel, temperature inside the panel is the ambient temperature.
		Ambient humidity		10 to 90%RH	
		Atmosphere		There is no corrosive gas present.	
2	Power supply voltage check		Measure voltage between 100/200VAC.	85 to 132VAC	Change the power supply source.
				170 to 264VAC	
3	Installation condition	Loosening, play	Test by moving the module.	Must be attached solidly.	Retighten the screw.
		Adhesion of dirt or foreign substance	Visual inspection	No adhesion.	Remove and clean.
4	Connection conditions	Loosening of terminal screw	Retighten with a screwdriver.	No loosening.	Retighten.
		Closeness of crimp-style terminals	Visual inspection	There is an appropriate distance.	Correct the distance.
		Loosening of connector	Visual inspection	No loosening.	Retighten the connector fixed screw.
5	Battery		Confirm M9006 or M9007 is OFF with a peripheral device in the monitor mode.	(Preventive maintenance)	Even when there is no low-battery display, replace if specified battery life is over. ∗1

∗1: Refer to section 7.7 to the battery replacement procedure.

MEMO

11. TROUBLESHOOTING

The description, cause determination, and corrective actions of each error which may occur during system usage are described.

11.1 Fundamentals of Troubleshooting

Besides using obviously highly-reliable devices to increase system reliability, it is an important point to quickly startup the system again when an error occurs.
In order to quickly startup the system, find the cause of the problem and resolve it.
There are the following three basic points to be aware of when performing troubleshooting.

(1) Visual confirmation

Confirm the following points:

(a) Machine operation (stop status and operation status)
(b) Power supply ON/OFF
(c) I/O equipment status
(d) Wiring status (I/O line and cable)
(e) Display status of each display module (POWER LED, RUN LED, ERROR LED, I/O LED, etc.)
(f) Status of each setting switch (extension base, power failure protection, etc.)

After confirming (a) to (f), connect a peripheral device and observe the operation status of the PC and program contents.

(2) Error confirmation

Observe how the error changes by performing the following operations:

(a) Set the RUN/STOP switch to "STOP."
(b) Reset using the RUN/STOP switch.
(c) Turn ON/OFF the power.

(3) Narrow down the range

By performing the (1) and (2) above, assume the faulty area in the following:

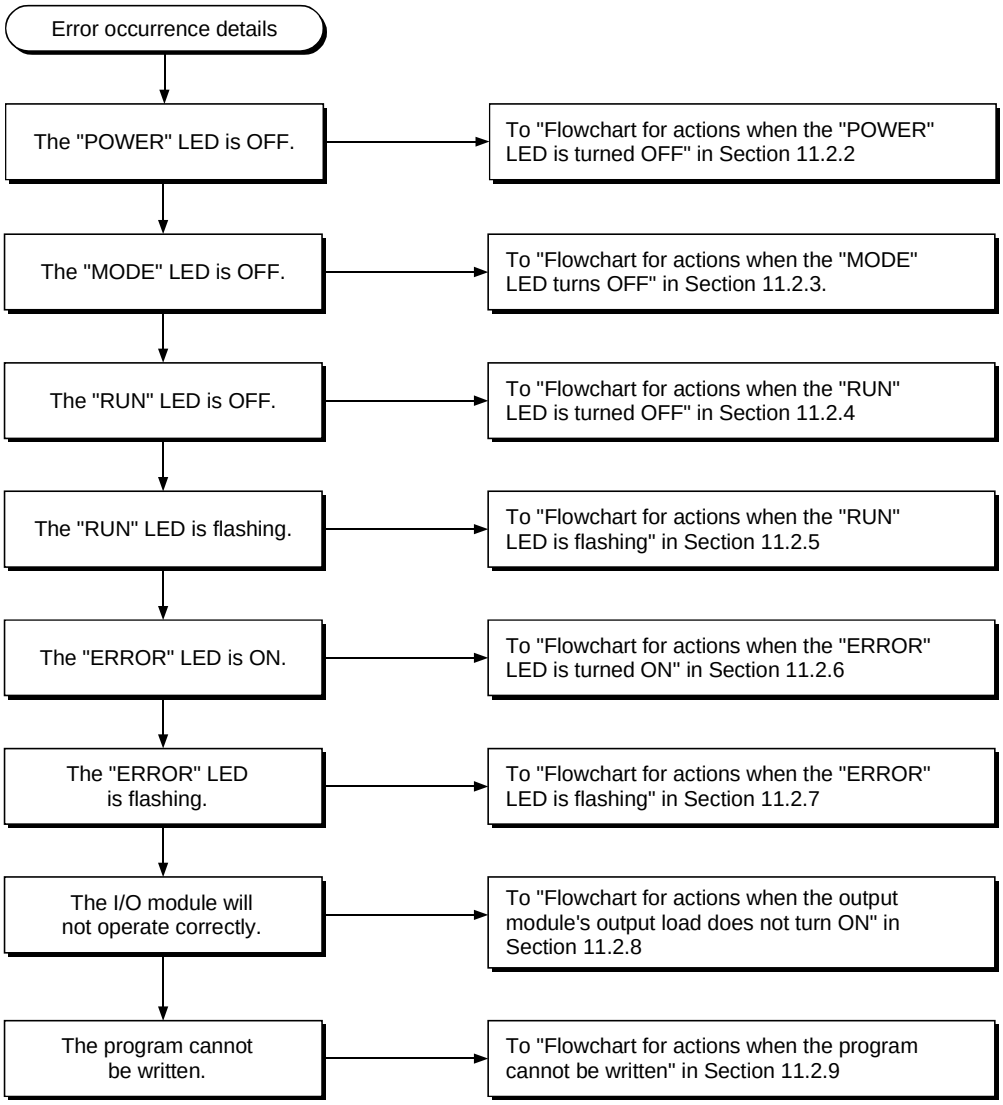
(a) PC or external?
(b) I/O module or others?
(c) Sequence program?

11.2 Troubleshooting

The error detail determination method, error details corresponding to the error code, and corrective actions are described.

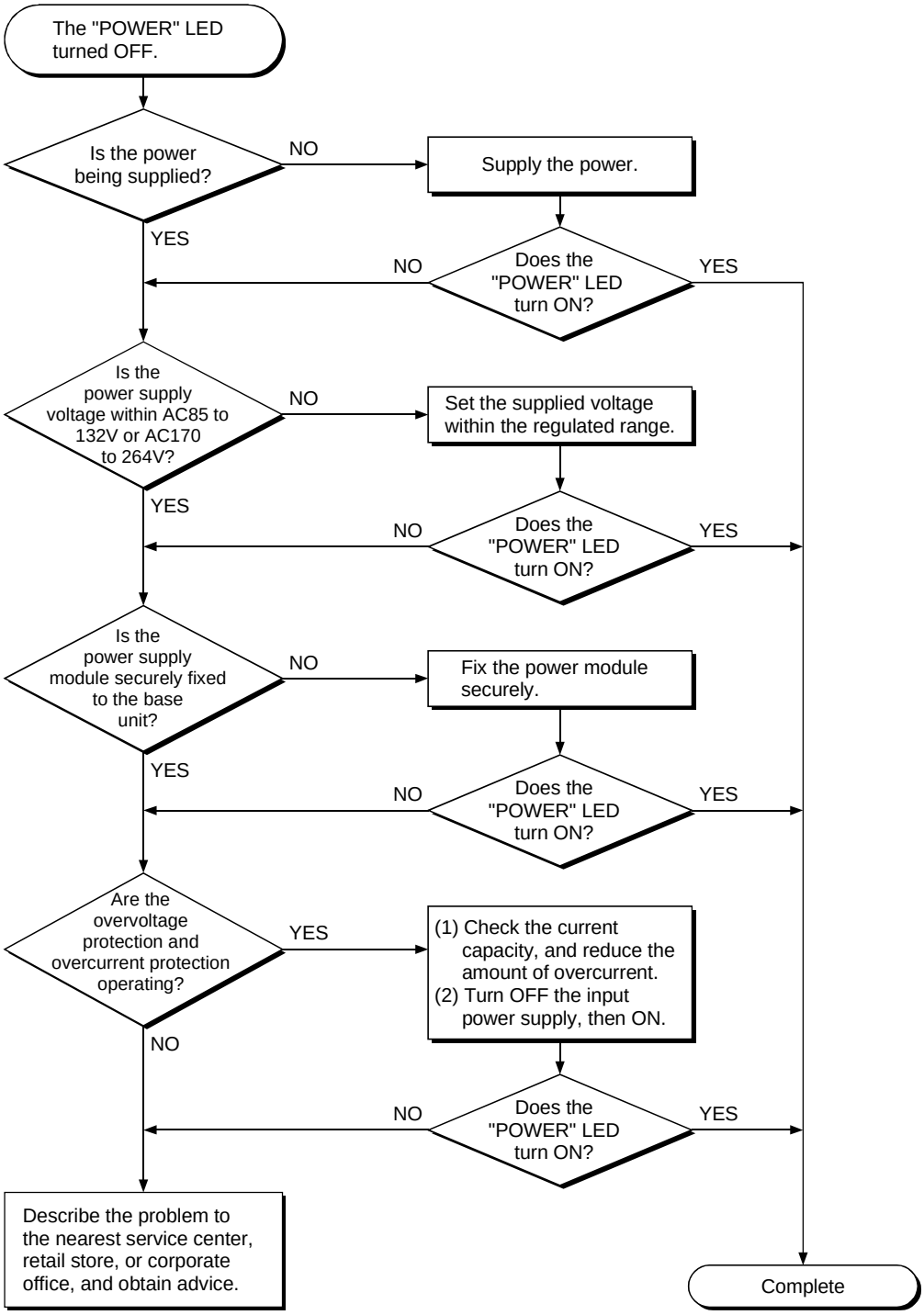
11.2.1 Troubleshooting flowchart

The error details are described by events.



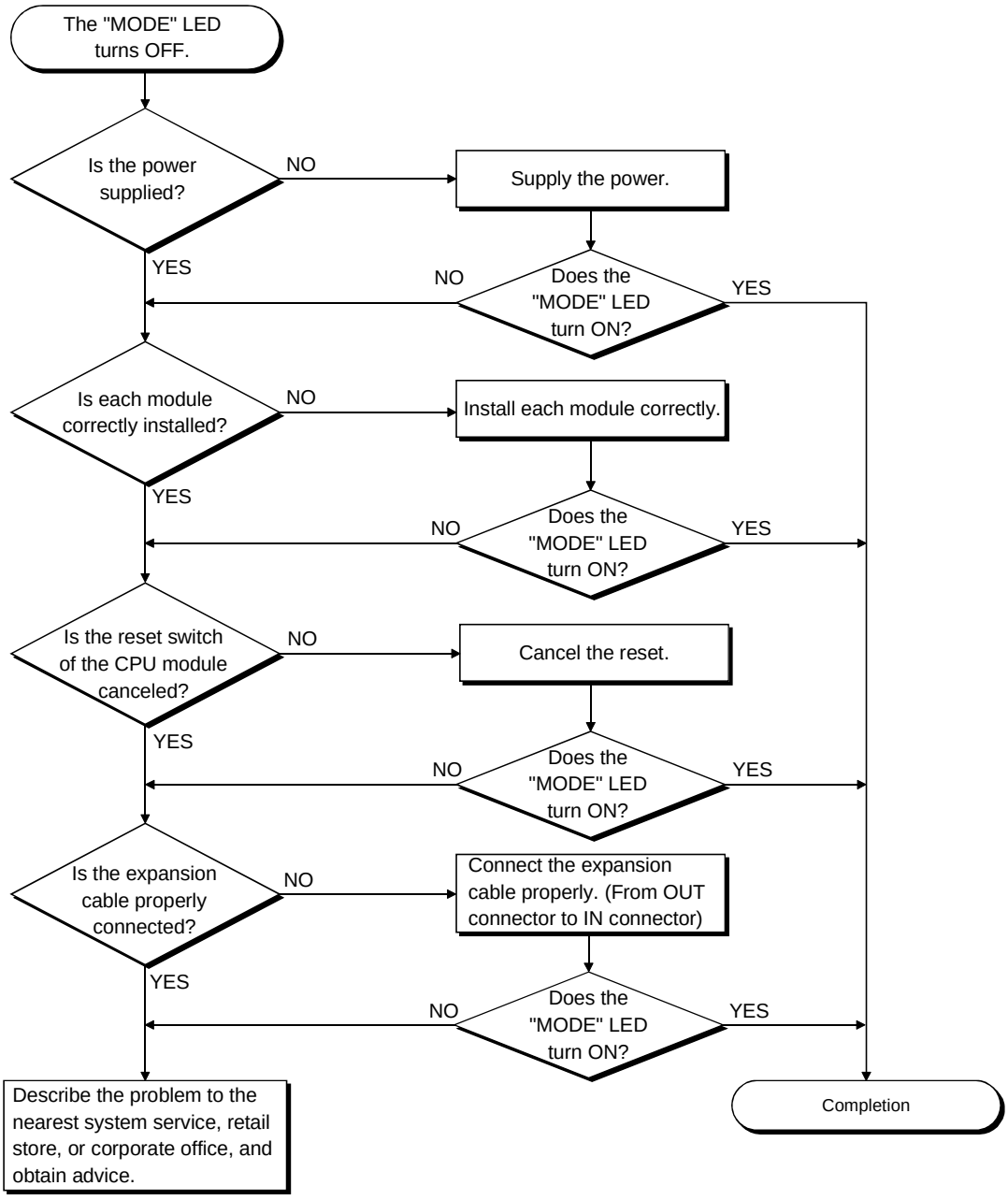
11.2.2 Flowchart for actions when the "POWER" LED is turned OFF

The corrective action when the "POWER" LED turns OFF when the power is turned ON or during operation is described.



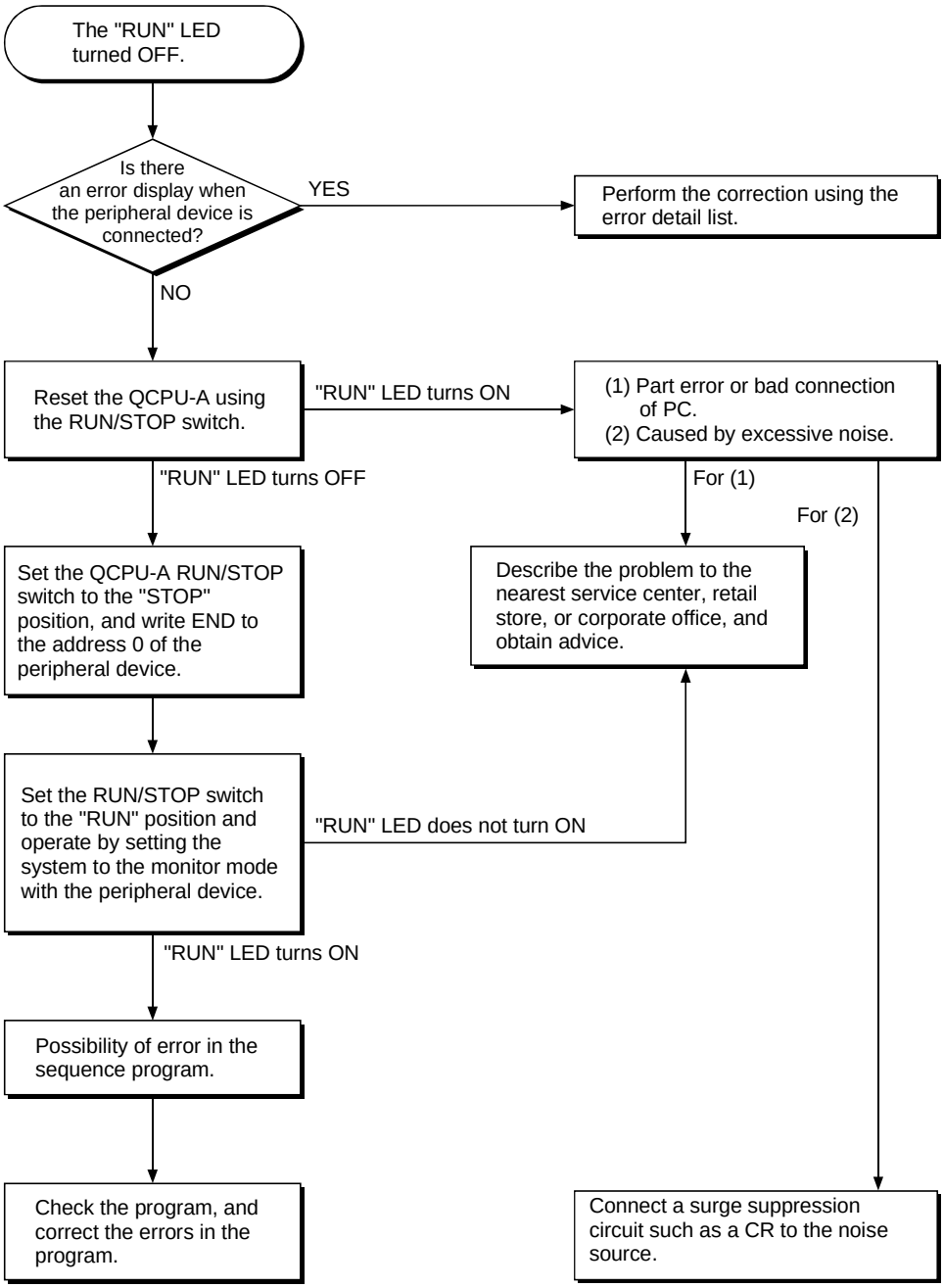
11.2.3 Flowchart for actions when the "MODE" LED turns OFF

The flowchart when the "MODE" LED turns OFF at power on is described.



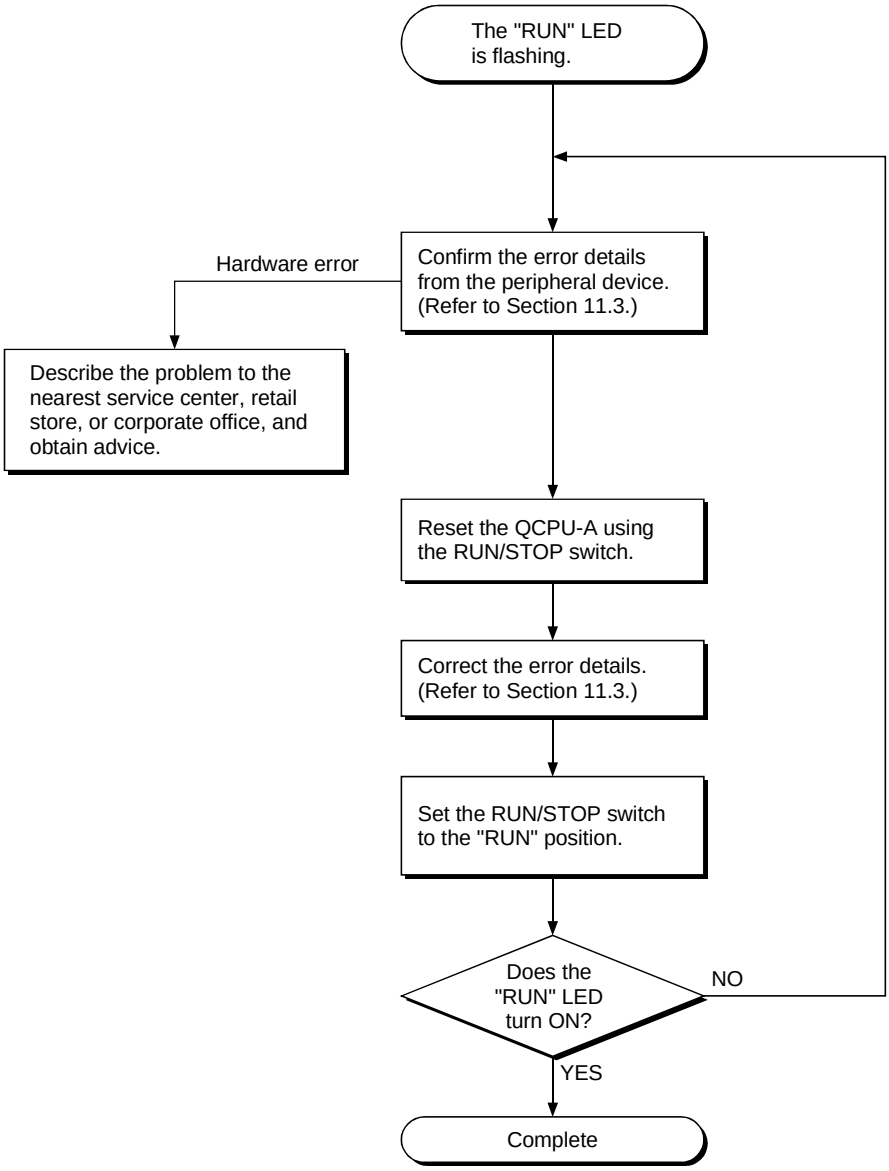
11.2.4 Flowchart for actions when the "RUN" LED is turned OFF

The corrective action when the "RUN" LED turns OFF during operation is described.



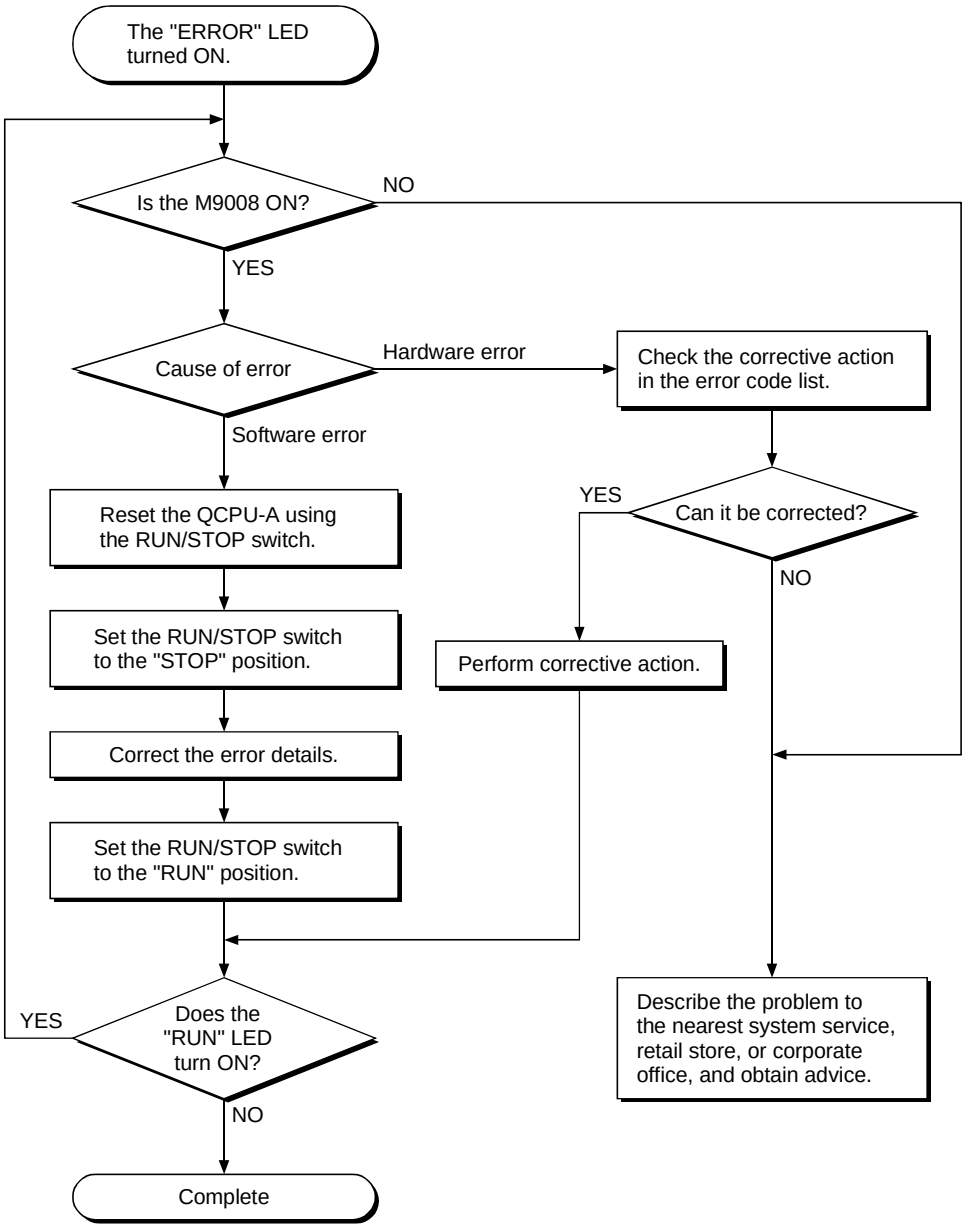
11.2.5 Flowchart for actions when the "RUN" LED is flashing

The corrective action when the "RUN" LED is flashing when turning on the power, starting operation, or during operation is described.



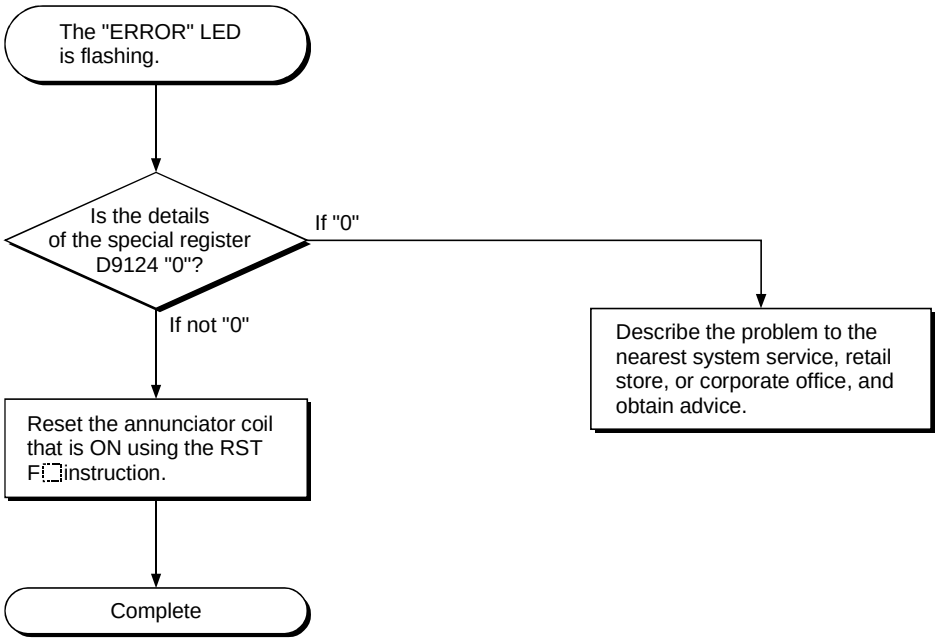
11.2.6 Flowchart for actions when the "ERROR" LED is turned ON

The flowchart when the "ERROR" LED turns ON during operation is described.



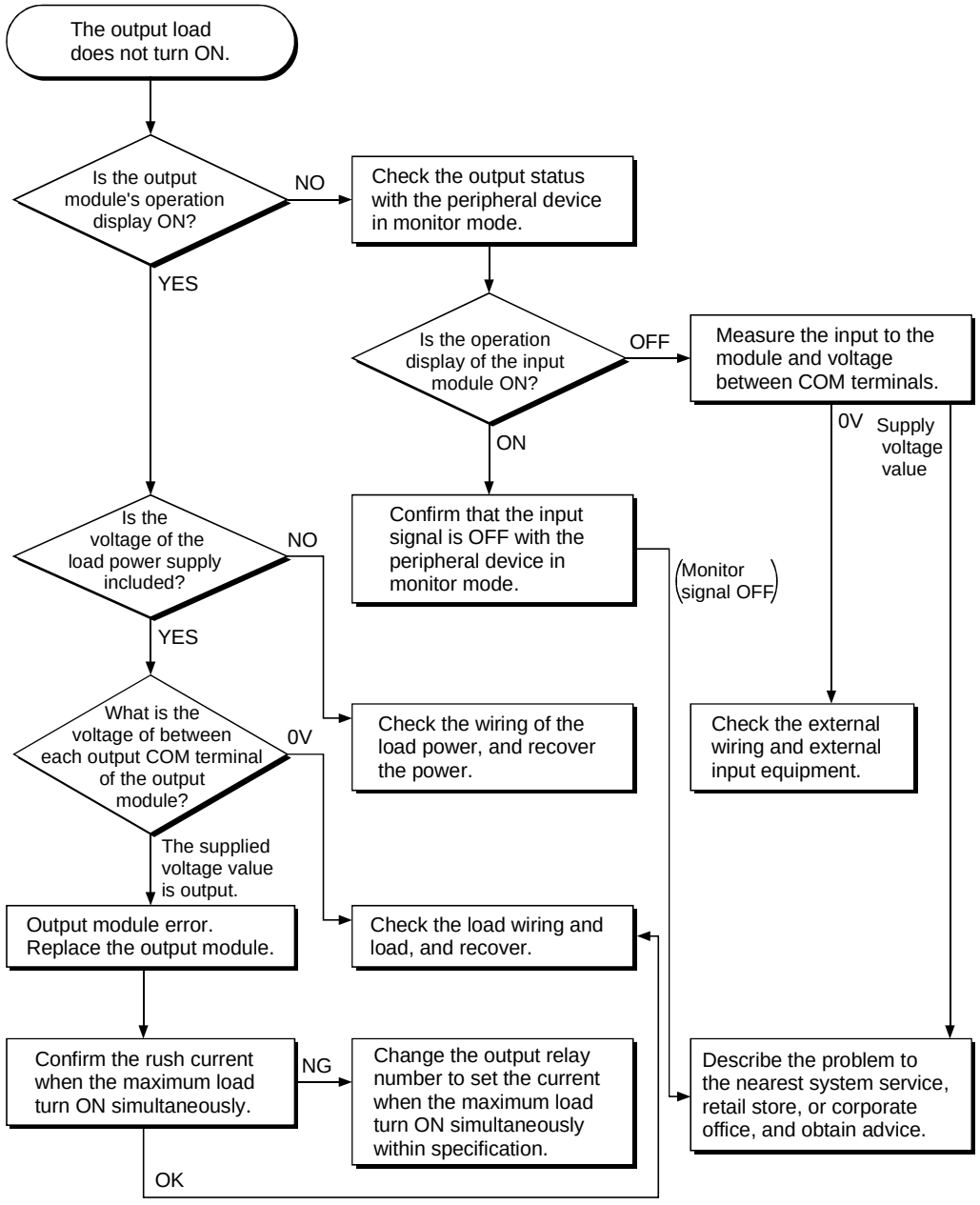
11.2.7 Flowchart for actions when the "ERROR" LED is flashing

The flowchart when the "ERROR" LED is flashing during operation is described.



11.2.8 Flowchart for actions when the output module's output load does not turn ON

The corrective action when the output load of the output module does not turn ON during operation is described.

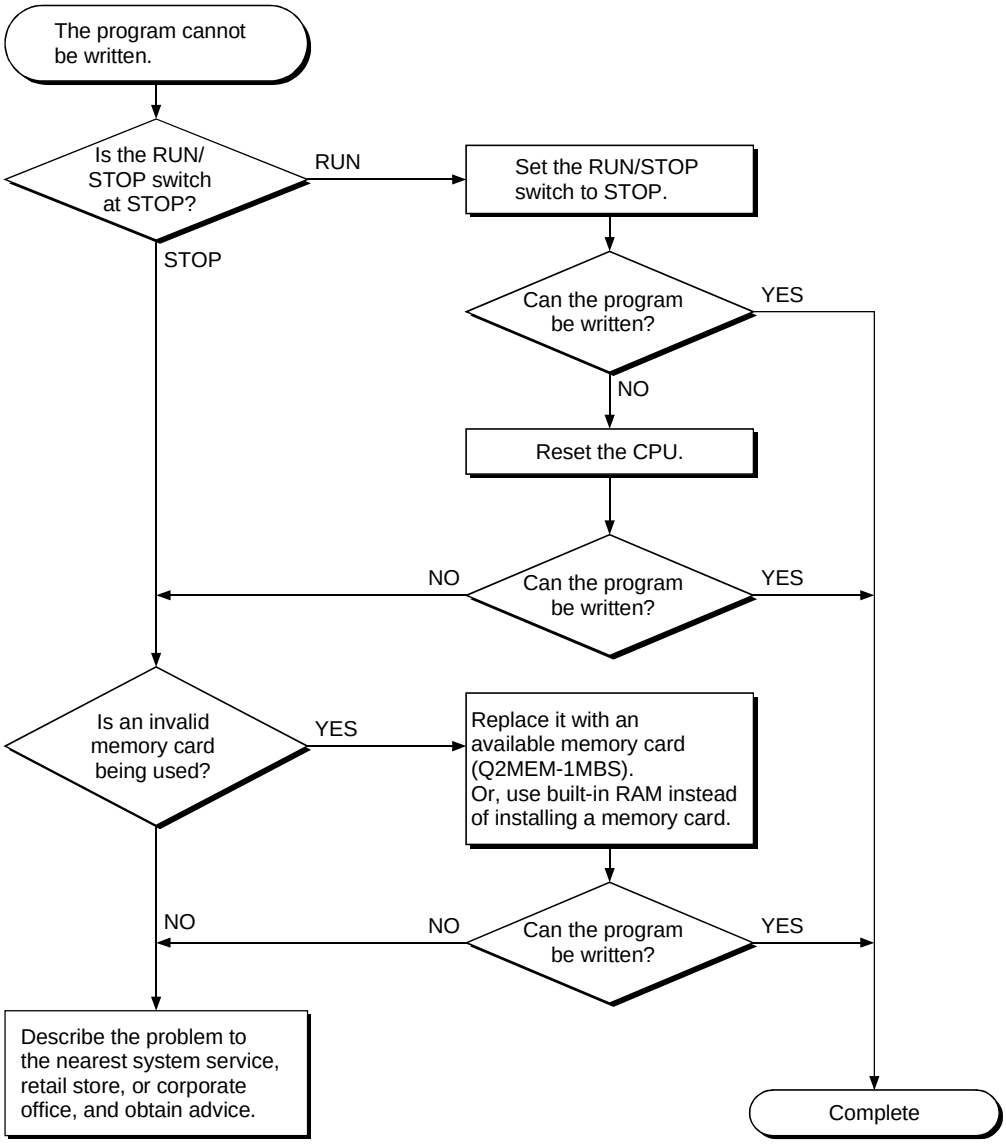


POINT

For problems when the input signal does not turn off and load does not turn off, perform troubleshooting by referring to the problem examples for the I/O module in section 11.4.

11.2.9 Flowchart for actions when the program cannot be written

The flowchart when the program and other data cannot be written to the CPU is described.



11.3 Error Code List

When an error occurs while the PC is running or during RUN, error is displayed, or error code, detailed error code and error step are stored to special registers, D9008, D9091 and D9010, respectively, by the self-diagnosis function.
Details of errors and corrective actions are shown below.

11.3.1 Procedure to read an error code

When an error occurs, the error code can be read with a peripheral device. Refer to the operating manuals of the peripheral device for operating procedures.

11.3.2 Error code list

Meanings and causes of error message, error codes, detailed error codes and corrective actions are described.

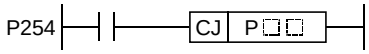
Error Code List

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"INSTRCT CODE ERR" (Checked when STOP → RUN or at execution of instruction.)	10	101	Instruction codes which the CPU cannot decode are included in the program.	(1) Read the error step using a peripheral device and correct the program of the step. (2) Check the ROM if it contains instruction codes which cannot be decoded. If it does, replace it with a correct ROM.
		102	Index qualification is specified for a 32-bit constant.	Read the error step using a peripheral device and correct the program of the step.
		103	Device specified by an dedicated instruction is not correct.	
		104	An dedicated instruction has incorrect program structure.	
		105	An dedicated instruction has incorrect command name.	
		106	Index qualification using Z or V is included in the program between LEDA/B IX and LEDA/B IXEND.	
		107	(1) Index qualification is specified for the device numbers and set values in the OUT instruction of timers and counters. (2) Index qualification is specified at the label number of the pointer (P) provided to the head of destination of the CJ, SCJ, CALL, CALLP, JMP, LEDA/B FCALL and LEDA/B BREAK instructions or at the label number of the interrupt pointer (I) provided to the head of an interrupt program.	
		108	Errors other than 101 to 107 mentioned above.	

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"PARAMETER ERROR" (Checked at power on and at STOP/PAUSE ⟶ RUN.)	11	111	Capacity settings of the main and sub programs, microcomputer program, file register comments, status latch, sampling trace and extension file registers are not within the usable range of the CPU.	Read parameters in the CPU memory, check the contents, make necessary corrections and write them again to the memory.
		112	Total of the set capacity of the main and sub programs, file register comments, status latch, sampling trace and extension file registers exceeds capacity of the memory cassette.	
		113	Latch range set by parameters or setting of M, L or S is incorrect.	Read parameters in the CPU memory, check the contents, make necessary corrections and write them again to the memory
		114	Sum check error	
		115	Either of settings of the remote RUN/PAUSE contact point by parameters, operation mode at occurrence of error, annunciator indication mode, or STOP ⟶ RUN indication mode is incorrect.	
		116	The MNET-MINI automatic refresh setting by parameters is incorrect.	
		117	Timer setting by parameters is incorrect.	
		118	Counter setting by parameters is incorrect.	
"MISSING END INS" (Checked at STOP ⟶ RUN.)	12	121	The END (FEND) instruction is not given in the main program.	Write the END instruction at the end of the main program.
		122	The END (FEND) instruction is not given in the sub program if the sub program is set by parameters.	Write the END instruction at the end of the sub program.
"CAN'T EXECUTE (P)" (Checked at execution of instruction.)	13	131	The same device number is used at two or more steps for the pointers (P) and interrupt pointers (I) used as labels to be specified at the head of jump destination.	Eliminate the same pointer numbers provided at the head of jump destination.
		132	Label of the pointer (P) specified in the CJ, SCJ, CALL, CALLP, JMP, LEDA/B FCALL or LEDA/B BREAK instruction is not provided before the END instruction.	Read the error step using a peripheral device, check contents and insert a jump destination pointer (P).
		133	(1) The RET instruction was included in the program and executed though the CALL instruction was not given. (2) The NEXT and LEDA/B BREAK instructions were included in the program and executed though the FOR instruction was not given. (3) Nesting level of the CALL, CALLP and FOR instructions is 6 levels or deeper, and the 6th level was executed. (4) There is no RET or NEXT instruction at execution of the CALL or FOR instruction.	(1) Read the error step using a peripheral device, check contents and correct program of the step. (2) Reduce the number of nesting levels of the CALL, CALLP and FOR instructions to 5 or less.

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CAN'T EXECUTE (P)" (Checked at execution of instruction.)	13	134	The CHG instruction was included in the program and executed though no sub program was provided.	Read the error step using a peripheral device and delete the CHG instruction circuit block.
		135	(1) LEDA/B IX and LEDA IXEND instructions are not paired. (2) There are 33 or more sets of LEDA/B IX and LEDA IXEND instructions.	(1) Read the error step using a peripheral device, check contents and correct program of the step. (2) Reduce the number of sets of LEDA/B IX and LEDA IXEND instructions to 32 or less.
"CHK FORMAT ERR" (Checked at STOP/PAUSE → RUN.)	14	141	Instructions (including NOP) other than LDX, LDIX, ANDX and ANIX are included in the CHK instruction circuit block.	Check the program of the CHK instruction and correct it referring to contents of detailed error codes.
		142	Multiple CHK instructions are given.	
		143	The number of contact points in the CHK instruction circuit block exceeds 150.	
		144	The LEDA CHK instructions are not paired with the LEDA CHKEND instructions, or 2 or more pairs of them are given.	
		145	Format of the block shown below, which is provided before the CHK instruction circuit block, is not as specified. 	
		146	Device number of D1 in the CHK D1 D2 instruction is different from that of the contact point before the CJ P□ instruction.	
		147	Index qualification is used in the check pattern circuit.	
		148	(1) Multiple check pattern circuits of the LEDA CHK - LEDA CHKEND instructions are given. (2) There are 7 or more check condition circuits in the LEDA CHK - LEDA CHKEND instructions. (3) The check condition circuits in the LEDA CHK - LEDA CHKEND instructions are written without using X and Y contact instructions or compare instructions. (4) The check pattern circuits of the LEDA CHK - LEDA CHKEND instructions are written with 257 or more steps.	
"CAN'T EXECUTE (I)" (Checked at occurrence of interrupt.)	15	151	The IRET instruction was given outside of the interrupt program and was executed.	Read the error step using a peripheral device and delete the IRET instruction.
		152	There is no IRET instruction in the interrupt program.	Check the interrupt program if the IRET instruction is given in it. Write the IRET instruction if it is not given.
		153	Though an interrupt module is used, no interrupt pointer (I) which corresponds to the module is given in the program. Upon occurrence of error, the problem pointer (I) number is stored at D9011.	Monitor special register D9011 using a peripheral device, and check if the interrupt program that corresponds to the stored data is provided or if two or more interrupt pointers (I) of the same number are given. Make necessary corrections.

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CASSETTE ERROR"	16	—	(1) A memory card is inserted or removed while the CPU module is ON. (2) An invalid memory card is inserted.	(1) Do not insert or remove a memory card while the CPU module is ON. (2) Insert an available memory card.
"RAM ERROR" (Checked at power on.)	20	201	The sequence program storage RAM in the CPU module caused an error.	Since this is CPU hardware error, consult Mitsubishi representative.
		202	The work area RAM in the CPU module caused an error.	
		203	The device memory in the CPU module caused an error.	
		204	The address RAM in the CPU module caused an error.	
"OPE CIRCUIT ERROR" (Checked at power on.)	21	211	The operation circuit for index qualification in the CPU does not work correctly.	Since this is CPU hardware error, consult Mitsubishi representative.
		212	Hardware (logic) in the CPU does not operate correctly.	
		213	The operation circuit for sequential processing in the CPU does not operate correctly.	
"OPE. CIRCUIT ERR." (Checked at execution of the END instruction)		214	In the END processing check, the operation circuit for index qualification in the CPU does not work correctly.	
		215	In the END processing check, the hardware in the CPU does not operate correctly.	
"WDT ERROR" (Checked at execution of END processing.)	22	—	Scan time is longer than the WDT time. (1) Scan time of the user's program has been extended due to certain conditions. (2) Scan time has been extended due to momentary power failure occurred during scanning.	(1) Check the scan time of the user's program and shorten it using the CJ instructions. (2) Monitor contents of special register D9005 using a peripheral device. If the contents are other than 0, power supply voltage may not be stable. Check power supply and reduce variation in voltage.
"END NOT EXECUTE" (Checked at execution of the END instruction.)	24	241	Whole program of specified program capacity was executed without executing the END instructions. (1) When the END instruction was to be executed, the instruction was read as other instruction code due to noise. (2) The END instruction changed to other instruction code due to unknown cause.	(1) Reset and run the CPU again. If the same error recurs, Since this is CPU hardware error, consult Mitsubishi representative.
"MAIN CPU DOWN"	26	—	The main CPU is malfunctioning or faulty.	Since this is CPU hardware error, consult Mitsubishi representative
"UNIT VERIFY ERR" (Checked continuously.)	31	—	Current I/O module information is different from that recognized when the power was turned on. (1) The I/O module (including special function modules) connection became loose or the module was disconnected during operation, or wrong module was connected.	Read detailed error code using a peripheral device and check or replace the module which corresponds to the data (I/O head number). Or, monitor special registers D9116 to D9123 using a peripheral device and check or replace the modules if corresponding data bit is "1".

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"FUSE BREAK OFF" (Checked continuously.)	32	—	(1) There is an output module of which fuse is blown. (2) The external power supply for output load is turned OFF or is not connected.	(1) Check the FUSE BLOWN indicator LED on the output module and replace the fuse. (2) Read detailed error code using a peripheral device and replace the fuse of the output module which corresponds to the data (I/O head number). Or, monitor special registers D9100 to D9107 using a peripheral device and replace the fuse of the output module of which corresponding data bit is "1". (3) Check the ON/OFF status of the external power supply for output load.
"CONTROL-BUS ERR"	40	401	Due to the error of the control bus which connects to special function modules, the FROM/TO instruction cannot be executed.	Since it is a hardware error of special function module, CPU module or base module, replace and check defective module(s). Consult Mitsubishi representative for defective modules.
		402	If parameter I/O assignment is being executed, special function modules are not accessible at initial communication. At error occurrence, the head I/O number (upper 2 digits of 3 digits) of the special function module that caused error is stored at D9010.	
		403	Hardware failure. The factor is stored in D9184.	
		405	(1) The expansion cable is not properly connected. (2) QA1S base failure. The base information is different from that obtained at power on. The failed base is stored in D9068 as a bit pattern. The failed base is stored in D9010 from the upper stage.	(1) Connect the expansion cable properly. (2) The hardware failure occurs in the special function, CPU, or base module. Replace the module and find the faulty one. Describe the problem to the nearest system service, retail store, or corporate office, and obtain advice.
"SP.UNIT DOWN"	41	411	Though an access was made to a special function module at execution of the FROM/TO instruction, no response is received.	Since it is hardware error of the special function module to which an access was made, consult Mitsubishi representative.
		412	If parameter I/O assignment is being executed, no response is received from a special function module at initial communication. At error occurrence, the head I/O number (upper 2 digits of 3 digits) of the special function module that caused error is stored at D9011.	
"LINK UNIT ERROR"	42	—	Two of A1SJ71AP21/R21 and A1SJ71AT21B are specified as master stations.	Specify one of A1SJ71AP21/R21 and A1SJ71AT21B as a master station and another as a local station.
"I/O INT. ERROR"	43	—	Though the interrupt module is not loaded, an interrupt occurred.	Since it is hardware error of a module, replace and check a defective module. For defective modules, consult Mitsubishi representative.

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"SP.UNIT LAY.ERR."	44	441	A special function module is assigned as an I/O module, or vice versa, in the I/O assignment using parameters from the peripheral device.	Execute I/O assignment again using parameters from the peripheral device according to the loading status of special function modules.
		442	There are 9 or more special function modules (except A1SI61) which can execute interruption to the CPU module loaded.	Reduce the special function modules (except A1SI61) which can execute interrupt start to 8 or less.
		443	Three or more A1SJ71AP21/R21 and A1SJ71AT21B are installed.	Reduce the number of A1SJ71AP21/R21 and A1SJ71AT21B to two or less.
		444	There are 7 or more modules such as a computer link module loaded to one CPU module.	Reduce the computer link modules to 6 or less.
		445	There are 2 or more A1SI61 modules loaded.	Reduce the A1SI61 module to 1.
		446	Modules assigned by parameters for MNT/MINI automatic refresh from the peripheral device do not conform with the types of station modules actually linked.	Perform again module assignment for MNT/MINI automatic refresh with parameters according to actually linked station modules.
		447	The number of modules of I/O assignment registration (number of loaded modules) per one CPU module for the special function modules which can use dedicated instructions is larger than the specified limit. (Total of the number of computers shown below is larger than 1344.) Number of A1SJ71C24-R2 (PRF/R4) being installed × 10 Number of A1SJ71UC24 being installed × 10 Number of A1SJ71PT32-S3 being installed × 125 Number of A1SJ71PT32 (S3)* being installed × 125	Reduce the number of loaded special function modules.
		448	(1) Five or more A1SJ71LP21 and A1SJ71BR11 are installed. (2) Five or more A1SJ71AP21/R21, A1SJ71AT21B, A1SJ71LP21, and A1SJ71BR11 are installed in total.	(1) Reduce the number to four or less. (2) Reduce the total number to four or less.
		449	An invalid base module is used. Failure of base module hardware	Use an available base module. Replace the failed base module.
"SP.UNIT ERROR" (Checked at execution of the FROM/TO instruction or the dedicated instructions for special function modules.)	46	461	Module specified by the FROM/TO instruction is not a special function module.	Read the error step using a peripheral device and check and correct contents of the FROM/TO instruction of the step.
		462	Module specified by the dedicated instruction for special function module is not a special function module or not a corresponding special function module.	Read the error step using a peripheral device and check and correct contents of the dedicated instruction for special function modules of the step.

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"LINK PARA. ERROR"	47	0	[When using MELSECNET/(II)] (1) When the link range at a data link CPU which is also a master station (station number = 00) is set by parameter setting at a peripheral device, for some reason the data written to the link parameter area differs from the link parameter data read by the CPU. Alternatively, no link parameters have been written. (2) The total number of slave stations is set at 0.	(1) Write the parameters again and check. (2) Check the station number settings. (3) Persistent error occurrence may indicate a hardware fault. Consult your nearest Mitsubishi representative, explaining the nature of the problem.
		470	[When using MELSECNET/10] (1) The contents of the network refresh parameters written from a peripheral device differ from the actual system at the base unit. (2) The network refresh parameters have not been written	Write the network refresh parameters again and check.
		471	[When using MELSECNET/10] (1) The transfer source device range and transfer destination device range specified for the inter-network transfer parameters are in the same network. (2) The specified range of transfer source devices or transfer destination devices for the inter-network transfer parameters spans two or more networks. (3) The specified range of transfer source devices or transfer destination devices for the inter-network transfer parameters is not used by the network.	Write the network parameters again and check.
		472	[When using MELSECNET/10] The contents of the routing parameters written from a peripheral device differ from the actual network system.	Write the routing parameters again and check.
		473	[When using MELSECNET/10] (1) The contents of the network parameters for the first link unit, written from a peripheral device, differ from the actual network system. (2) The link parameters for the first link unit have not been written. (3) The setting for the total number of stations is 0.	(1) Write the parameters again and check. (2) Check the station number settings. (3) Persistent error occurrence may indicate a hardware fault. Consult your nearest Mitsubishi representative, explaining the nature of the problem.
		474	[When using MELSECNET/10] (1) The contents of the network parameters for the second link unit, written from a peripheral device, differ from the actual network system. (2) The link parameters for the second link unit have not been written. (3) The setting for the total number of stations is 0.	
		475	[When using MELSECNET/10] (1) The contents of the network parameters for the third link unit, written from a peripheral device, differ from the actual network system. (2) The link parameters for the third link unit have not been written. (3) The setting for the total number of stations is 0.	

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"LINK PARA. ERROR"	47	476	[When using MELSECNET/10] (1) The contents of the network parameters for the fourth link unit, written from a peripheral device, differ from the actual network system. (2) The link parameters for the fourth link unit have not been written. (3) The setting for the total number of stations is 0.	(1) Write the parameters again and check. (2) Check the station number settings. (3) Persistent error occurrence may indicate a hardware fault. Consult your nearest Mitsubishi representative, explaining the nature of the problem.
"OPERATION ERROR" (Checked at execution of instruction.)	50	501	(1) When file registers (R) are used, operation is executed outside of specified ranges of device numbers and block numbers of file registers (R). (2) File registers are used in the program without setting capacity of file registers.	Read the error step using a peripheral device and check and correct program of the step.
		502	Combination of the devices specified by instruction is incorrect.	
		503	Stored data or constant of specified device is not in the usable range.	
		504	Set number of data to be handled is out of the usable range.	
		505	(1) Station number specified by the LEDA/B|LRDP, LEDA/B|LWTP, LRDP, LWTP instructions is not a local station. (2) Head I/O number specified by the LEDA/B|RFRP, LEDA/B|RTOP, RFRP, RTOP instructions is not of a remote station.	
		506	Head I/O number specified by the LEDA/B|RFRP, LEDA/B|RTOP, RFRP, RTOP instructions is not of a special function module.	
		507	(1) When the AD57(S1) or AD58 was executing instructions in divided processing mode, other instructions were executed to either of them. (2) When an AD57(S1) or AD58 was executing instructions in divided processing mode, other instructions were executed in divided mode to another AD57(S1) or AD58.	AD57 (S1) and AD58 cannot be used with QCPU-A. Review the program.
		509	(1) An instruction which cannot be executed by remote terminal modules connected to the MNET/MINI-S3 was executed to the modules. (2) When the PRC instruction was executed to a remote terminal, the communication request registration areas overflowed. (3) The PIDCONT instruction was executed without executing the PIDINIT instruction. The PID57 instruction was executed without executing the PIDINIT or PIDCONT instruction. The program presently executed was specified by the ZCHG instruction.	(1) Read the error step using a peripheral device and correct the program, meeting loaded conditions of remote terminal modules. (2) Provide interlock using M9081 (communication request registration areas BUSY signal) or D9081 (number of vacant areas in the communication request registration areas) when the PRC instruction is executed to a remote terminal. (3) Correct the program specified by the ZCHG instruction to other.

Error Code List (Continue)

Error Massage	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"MAIN CPU DOWN"	60	—	(1) The CPU malfunctioned due to noise. (2) Hardware failure.	(1) Take proper countermeasures for noise. (2) Since it is hardware error, consult Mitsubishi representative.
	61			
"BATTERY ERROR" (Checked at power on.)	70	—	(1) The battery voltage for the CPU module has dropped below the specified value. (2) The lead connector of the CPU module battery is disconnected. (M9006 is ON.) (3) The battery voltage for the memory card has dropped below the specified value. (M9048 is ON.)	(1) Replace the battery of the CPU module. (2) Connect the lead connector when using the standard RAM or the memory retention function during power failure. (3) Replace the battery of the memory card.

11.4 Possible Troubles with I/O Modules

Examples of troubles concerning I/O circuits and the countermeasures are explained.

11.4.1 Troubles with the input circuit and the countermeasures

Examples of troubles concerning input circuits and the countermeasures are explained.

Table 11.2 Troubles with the input circuit and the countermeasures

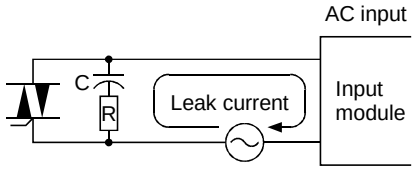
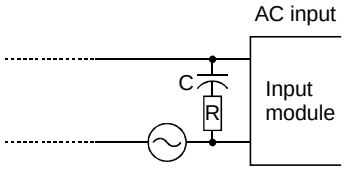
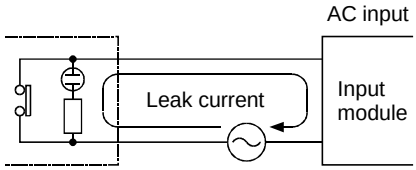
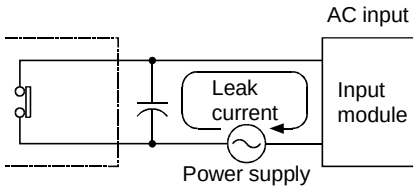
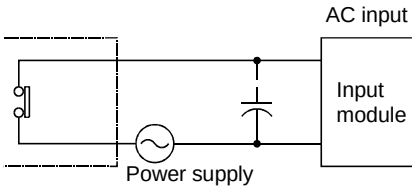
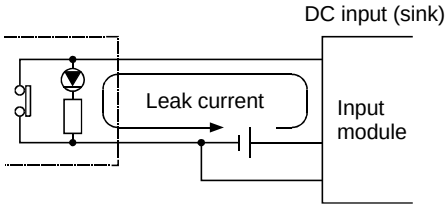
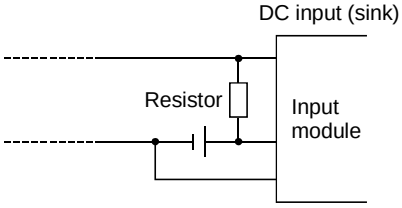
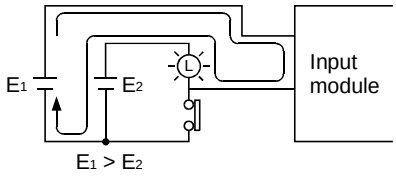
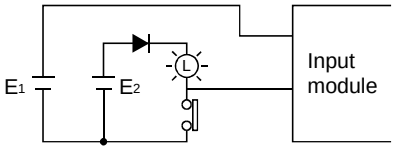
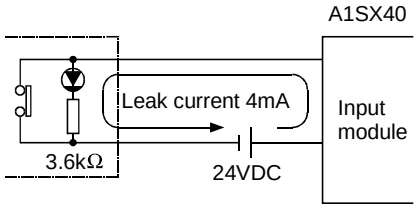
	Situation	Cause	Countermeasure
Example 1	Input signal does not turn OFF.	• Leak current from input switch (driven by a contactless switch, etc.) 	• Connect an appropriate resistance so that voltage between the terminals of the input module is lower than the OFF voltage.  For OR constant, 0.1 to 0.47μF+47 to 120Ω (1/2W) is recommended.
Example 2	Input signal does not turn OFF.	• Driven by a limit switch with a neon lamp 	• Same as the example 1. • Or, provide a totally independent display circuit separately.
Example 3	Input signal does not turn OFF.	• Line capacity C of the leak current twisted pair cable due to line capacity of the wiring cable is about 100PF/m. 	• Same as the example 1. • However, it does not occur when power supply is on the side of input device as shown below. 
Example 4	Input signal does not turn OFF.	• Driven by a switch with LED display 	• Connect an appropriate resistance so that voltage between the terminal of the input module and the common is lower than the OFF voltage as shown below.  * An example of calculation of resistance to be connected is provided on the following page.

Table 11.2 Troubles with the input circuit and the countermeasures

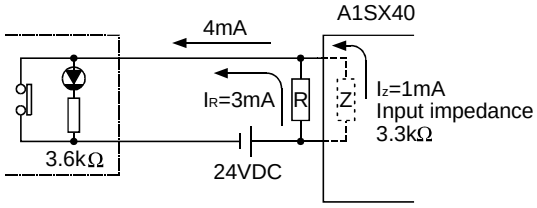
	Situation	Cause	Countermeasure
Example 5	Input signal does not turn OFF.	• Revolving path due to the use of two power supplies. 	• Use only one power supply. • Connect a diode to prevent the revolving path (figure below). 

<Calculation example for example 4>

When a switch with a LED display is connected to A1SX40 and there is a leak current at 4mA:



(1) Since OFF current of A1SX40 does not satisfy the 1mA, it does not turn OFF. Thus, a resistance is connected as shown below.



(2) Calculation of resistance R connected will be as follows:
To satisfy the OFF current of 1mA for A1SX40, a resistance R with which 3mA flows to the connected resistance is required.
$I_R : I_Z = Z$ (Input impedance) : R

$$R \leq \frac{I_Z}{I_R} \times \text{(Input impedance)} = \frac{1}{3} \times 3.3 = 1.1\ [k\Omega]$$

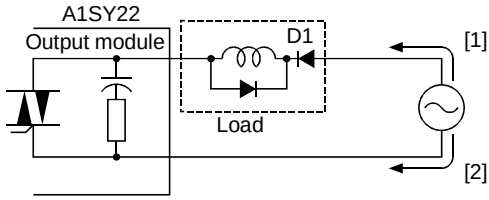
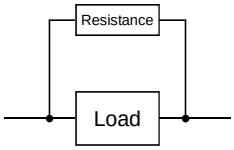
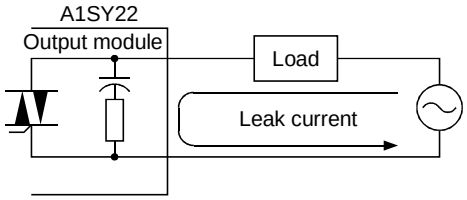
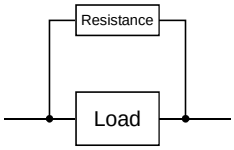
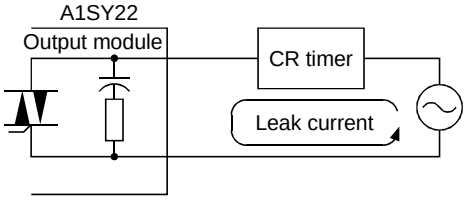
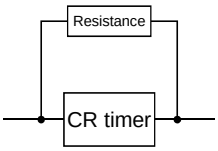
$R < 1.1k\Omega$
If resistance R is 1kΩ, power capacity W of the resistance R is:
$W = (\text{Input voltage})^2 \div R = 26.4^2 \div 1000 = 0.7\ (W)$

(3) Since the power capacity of a resistance is selected at 3 to 5 times the actual power consumption, a resistance at 1[kΩ], 2 to 3[W] needs to be connected to the terminal causing the problem.

11.4.2 Possible troubles in the output circuit

Examples of troubles concerning output circuits and the countermeasures are explained.

Table 11.3 Troubles with the output circuit and the countermeasures

	Situation	Cause	Countermeasure
Example 1	An excessive voltage is impressed to the load when output is off.	• When the load is subjected to half wave rectification inside. (Solenoids have these types).  • When the polarity of the power supply is [1], C is charged, and when the polarity is [2], the voltage charged in C + voltage of the power supply are impressed to the both ends of D1. The maximum value of the voltage is about 2.2E.	• Connect a resistance at several tens to several hundred of k to the both ends of the load. (With this kind of usage, there is no problem with the output element, but the diode built-in to the load may deteriorate and burn-out.) 
Example 2	Load does not OFF (Triac output)	• Leak current caused by built-in surge killer 	• Connect a resistance to the both ends of the load. (When the wiring distance from the output card to the load is long, be aware of the risk of a leak current due to line capacity.) 
Example 3	When load is CR type timer, the time limit fluctuates. (Triac output)		• Start the relay first, then start the CR-type timer at the contact. (In some timers, internal circuit may be half wave rectification type, so the caution as to the example 1 is necessary here.)  Calculate the constant of the resistance based on the load.

APPENDICES

Appendix 1 Instruction List

The list of instructions that can be used with the QCPU-A is shown.
Refer to the following programming manuals for the details of the instructions.

• ACPU Programming Manual (Basics)	IB-66249
• ACPU Programming Manual (Common Instructions)	IB-66250
• AnACPU/AnUCPU Programming Manual (Dedicated Instructions)	IB-66251
• AnACPU/AnUCPU Programming Manual (AD57 Instructions)	IB-66257
• AnACPU/AnUCPU Programming Manual (PID Control Instructions)	IB-66258

(1) Sequence instructions

(a) Contact instruction

Contact	LD, LDI, AND, ANI, OR, ORI

(b) Connection instruction

Contact	ANB, ORB, MPS, MRD, MPP

(c) Output instruction

Output	OUT, SET, RST, PLS, PLF

(d) Shift instruction

Shift	SFT, SFTP

(e) Master control instruction

Master control	MC, MCR

(f) End instruction

Program end	FEND, END

(g) Other instructions

Stop	STOP
No operation	NOP
Page break (Page break operation for printer output)	NOPLF

(2) Basic instructions

(a) Comparison instruction

=	16-bit	LD=, AND=, OR=
	32-bit	LDD=, ANDD=, ORD=
< >	16-bit	LD< >, AND< >, OR< >
	32-bit	LDD< >, ANDD< >, ORD< >
>	16-bit	LD>, AND>, OR>
	32-bit	LDD>, ANDD>, ORD>
≤	16-bit	LD<=, AND<=, OR<=
	32-bit	LDD<=, ANDD<=, ORD<=
<	16-bit	LD<, AND<, OR<
	32-bit	LDD<, ANDD<, ORD<
≥	16-bit	LD>=, AND>=, OR>=
	32-bit	LDD>=, ANDD>=, ORD>=

(b) BIN arithmetic operation instructions

+ Addition	16-bit	Two types each for +, +P
	32-bit	Two types each for D+, D+P
– Subtraction	16-bit	Two types each for –, – P
	32-bit	Two types each for D –, D – P
✻ Multiplication	16-bit	✻, ✻ P
	32-bit	D ✻, D ✻P
/ Division	16-bit	/, /P
	32-bit	D/, D/P
+1 Addition	16-bit	INC, INCP
	32-bit	DINC, DINCP
-1 Subtraction	16-bit	DEC, DECP
	32-bit	DDEC, DDECP

(c) BCD arithmetic operation instructions

+ Addition	BCD 4-digit	Two types each for B+, B+P
	BCD 8-digit	Two types each for DB+, DB+P
– Subtraction	BCD 4-digit	Two types each for B–, B–P
	BCD 8-digit	Two types each for DB, DB–P
✻ Multiplication	BCD 4-digit	B ✻, B ✻ P
	BCD 8-digit	DB ✻, DB ✻P
/ Division	BCD 4-digit	B/, B/P
	BCD 8-digit	DB/, DB/P

(d) BCD-BIN conversion instructions

BIN → BCD	16-bit	BCD, BCDP
	32-bit	DBCD, DBCDP
BCD → BIN	16-bit	BIN, BINP
	32-bit	DBIN, DBINP

(e) Data transfer instructions

Transfer	16-bit	MOV, MOVP
	32-bit	DMOV, DMOVP
Exchange	16-bit	XCH, XCHP
	32-bit	DXCH, DXCHP
Negation transfer	16-bit	CML, CMLP
	32-bit	DCML, DCMLP
Batch transfer	16-bit	BMOV, BMOVP
Batch transfer same data	16-bit	FMOV, FMOVP

(f) Program branch instructions

Jump	CJ, SCJ, JMP
Call subroutine	CALL, CALLP, RET
Enable/disable an interrupt program	EI, DI, IRET

(g) Refresh instructions

Link refresh	COM
Partial refresh	SEG

(3) Application instructions

(a) Logical operation instructions

Logical product	16-bit	Two types each for WAND, WANDP
	32-bit	DAND, DANDP
Logical sum	16-bit	Two types each for WOR, WORP
	32-bit	DOR, DORP
Exclusive logical sum	16-bit	Two types each for WXOR, WXORP
	32-bit	DXOR, DXORP
Not exclusive logical sum	16-bit	Two types each for WXNR, WXNRP
	32-bit	DXNR, DXNRP
Complements of 2 (sign invert)	16-bit	NEG, NEGP

(b) Rotation instructions

Right rotation	16-bit	ROR, RORP, RCR, RCRP
	32-bit	DROR, DRORP, DRCR, DRCRP
Left rotation	16-bit	ROL, ROLP, RCL, RCLP
	32-bit	DROL, DROLP, DRCL, DRCLP

(c) Shift instructions

Right shift	16-bit	SFR, SFRP, BSFR, BSFRP
	Device	DSFR, DSFRP
Left shift	16-bit	SFL, SFLP, BSFL, BSFLP
	Device	DSFL, DSFLP

(d) Data processing instruction

Search data	16-bit	SER, SERP
Check bit	16-bit	SUM, SUMP
	32-bit	DSUM, DSUMP
Decode	2^n-bit	DECO, DECOP
	16-bit	SEG
Encode	2^n-bit	ENCO, ENCOP
Set bit	16-bit	BSET, BSETP
Reset bit	16-bit	BRST, BRSTP
Separate	16-bit	DIS, DISP
Connection	16-bit	UNI, UNIP

(e) FIFO instructions

Write	16-bit	FIFW, FIFWP
Read	16-bit	FIFR, FIFRP

(f) ASCII instructions

ASCII conversion	ASC
Print ASCII	PR (two types), PRC

(g) Buffer memory access instructions

Read data	1 word	FROM, FROMP
	2 word	DFRO, DFROP
Write data	1 word	TO, TOP
	2 word	DTO, DTOP

(h) FOR to NEXT instructions

Repeat	FOR, NEXT

(i) Display instructions

Display	LED, LEDC
Reset display	LEDR

(j) Data link module instructions

Read data	1 word	LRDP, RFRP
Write data	1 word	LWTP, RTOP

(k) Other instructions

Reset WDT		WDT, WDTP
Failure check		CHK
Status latch		SLT, SLTR
Sampling trace		STRA, STRAR
Set/reset carry flag	1-bit	STC, CLC
Timing clock	1-bit	DUTY

(4) Dedicated instructions

(a) Direct processing instructions

Direct output	DOUT
Direct set	DSET
Direct reset	DRST

(b) Structured program instructions

Add circuit index	IX, IXEND
Repeat forced end	BREAK
Call subroutine	FCALL
Change failure check circuit pattern	CHK, CHKEND

(c) Data operation instructions

Search 32-bit data	DSER
Swap 16-bit upper/lower byte	SWAP
Separate data	DIS
Connection data	UNI
Test bit	TEST, DTEST

(d) I/O operation instructions

Flip-flop control	FF
Numeric key input from keyboard	KEY

(e) Real value processing instructions (BCD format processing)

BCD 4-digit square root	BSQR
BCD 8-digit square root	BDSQR
SIN (sine) operation	BSIN
COS (cosine) operation	BCOS
TAN (tangent) operation	BTAN
SIN^{-1} (arcsine) operation	BASIN
COS^{-1} (arccosine) operation	BACOS
TAN^{-1} (arctangent) operation	BATAN

(f) Real value processing instructions (Floating point format real value processing)

Real value → 16/32-bit BIN conversion	INT, DINT
16/32-bit BIN → real value conversion	FLOAT, DFLOAT
Addition	ADD
Subtraction	SUB
Multiplication	MUL
Division	DIV
Angle → radian conversion	RAD
Radian → angle conversion	DEG
SIN (sine) operation	BSIN
COS (cosine) operation	BCOS
TAN (tangent) operation	BTAN
SIN^{-1} (arcsine) operation	BASIN
COS^{-1} (arccosine) operation	BACOS
TAN^{-1} (arctangent) operation	BATAN
Square root	SQR
Exponential	EXP
Logarithm	LOG

(g) Text string processing instructions

16/32-bit BIN → decimal ASCII conversion	BINDA, DBINDA
16/32-bit BIN → hexadecimal ASCII conversion	BINHA, DBINHA
16/32-bit BCD → decimal ASCII conversion	BCDDA, DBCDDA
Decimal ASCII → 16/32-bit BIN conversion	DABIN, DDABIN
Hexadecimal ASCII → 16/32-bit BIN conversion	HABIN, DHABIN
Decimal ASCII → 16/32-bit BCD conversion	DABCD, DDABCD
Read device comment data	COMRD
Detect text string length	LEN
16/32-bit BIN → decimal text string conversion	STR, DSTR
Decimal text string → 16/32-bit BIN conversion	VAL, DVAL
Hexadecimal data → ASCII conversion	ASC
ASCII → hexadecimal data conversion	HEX
Transfer text string	SMOV
Concatenate text string	SADD
Compare text string	SCMP
Separate in byte units	WTOB
Concatenate byte-unit data	BTOW

(h) Data control instructions

Control upper/lower limit	LIMIT, DLIMIT
Control dead band	BAND, DBAND
Control zone	ZONE, DZONE

(i) Clock instructions

Read clock data	DATERD
Write clock data	DATEWR

(j) Extension file register instructions

Expansion file register block number conversion	RSET
Block transfer between expansion file registers	BMOVR
Block exchange between expansion file register	BXCHR
Direct read of expansion file register in 1 word units	ZRRD
Direct read of expansion file register in 1 byte units	ZRRDB
Direct write of expansion file register in 1 word units	ZRWR
Direct write of expansion file register in 1 byte units	ZRWRB

(k) 1ms timer instruction

Set 1ms timer	ZHTIME

(l) Data link instructions

*1: New instructions set for exclusive use with AnUCPU

	Read local station word device	LRDP
	Write local station word device	LWTP
	Read data from the remote I/O station special function module	RFRP
	Write data from the remote I/O station special function module	RTOP
*1	Read word device from connected station	ZNRD
*1	Write word device to connected station	ZNWR
*1	Network refresh instruction	ZCOM

(m) AD61(S1) high-speed counter module control instructions

(The AD61 dedicated instructions cannot be executed with A1SD61.)

Set preset value	PVWR1, PVWR2
Write setting data for large/small/match determination	SVWR1, SVWR2
Read current value from CH1/CH2	PVRD1, PVRD2

(n) AJ71C24(S8) computer link module control instructions

Data send	Character up to 00H code	PR
	Intended number of characters	PRN
Data received		INPUT
Read communication status		SPBUSY
Communication processing forced interrupt		SPCLR

(o) AJ71C21(S1) terminal interface module control instructions

Output data to RS-232C (data up to 00H code)	PR2
Output data to RS-422 (data up to 00H code)	PR4
Output data to RS-232C (for number of intended points)	PRN2
Output data to RS-422 (for number of intended points)	PRN4
Read input data from RS-232C	INPUT2
Input data from RS-422	INPUT4
Read data from RAM	GET
Write data to RAM	PUT
Read communication status	SPBUSY
Communication processing forced interrupt	SPCLR

(p) MELSECNET/MINI-S3 master module control instructions

Key input from operation box	INPUT
Data send/received for specified number of bytes to/from AJ35PTF-R2	PR, PRN, INPUT
Read/write data for MINI standard protocol module	MINI
Reset error for remote terminal module	MINIERR
Read communication status	SPBUSY
Communication status forced interrupt	SPCLR

(q) PID operation instructions

Set control data	PIDINIT
PID operation	PIDCONT
Monitor PID operation result for AD57(S1)	PID57

(r) AD59(S1) memory card/centronix interface module control instructions

Output to printer	Characters up to 00H code	PR
	Intended number of characters	PRN
Read data to memory card		GET
Write data to memory card		PUT

(s) AD57(S1) control instructions

Display mode setting instructions		CMODE
Screen display control instructions	Display canvas screen	CPS1
	Change VRAM display address	CPS2
	Transfer canvas	CMOV
	Clear screen	CLS
	Clear VRAM	CLV
	Scroll up/down	CSCRU, CSCRD
Cursor control instructions	Display cursor	CON1, CON2
	Erase cursor	COFF
	Set cursor position	LOCATE
Display condition setting instructions	Normal/inverted display of characters to be displaye	CNOR, CREV
	Normal/inverted display of characters	CRDSP, CRDSPV
	Specify color of characters	COLOR
	Change color characters	CCDSP, CCDSPV
Specified character display instructions	Display ASCII character	PR, PRN
	Write ASCII character	PRV, PRNV
	Display character	EPR, EPRN
	Write character	EPRV, EPRNV
	Continuous display same character	CR1, CR2, CC1, CC2
Fixed character display instructions	Display – (minus)	CINMP
	Display - (hyphen)	CINHP
	Display . (period, decimal point)	CINPT
	Display numeric characters	CIN0 to CIN9
	Display alphanumeric characters	CINA to CINZ
	Display space	CINSP
Specified column clear instruction		CINCLR
Conversion instructions for displayed text string into ASCII code		INPUT
VRAM data control instructions	Read data	GET
	Write data	PUT
Display status read instruction		STAT

(t) CC-Link dedicated instructions

Link parameter setting	PLPA
Refresh parameter setting	RRPA
Read master station buffer memory	RIFR
Write to master station buffer memory	RITO
Read buffer memory of intelligent remote station	RIRD
Write to buffer memory of intelligent remote station	RIWT
Write to buffer memory of intelligent remote station (with handshaking)	RISEND
Read buffer memory of intelligent remote station (with handshaking)	RIRCV

Appendix 2 Lists of Special Relays and Special Registers

The list of the special relays and special registers that can be used by the QCPU-A is shown below:

Appendix 2.1 List of special relays

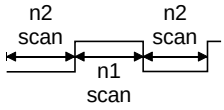
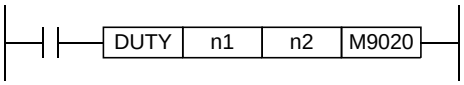
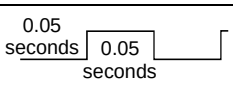
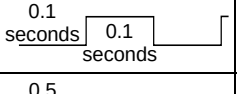
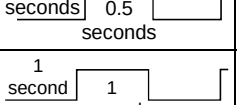
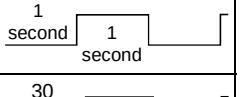
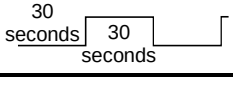
The special relays are the internal relays that have specific applications in the sequencer. Therefore, the coil cannot be turned ON/OFF on the program. (Except for the ones marked by ∗1 or ∗2 in the table.)

Refer to the Network System Reference Manual for the special relays after M9200.

Special Relay List

Number	Name	Description	Details	Applicable CPU	
∗1 M9000	Fuse blown	OFF: Normal ON: Fuse blown unit	• Turned on when there is one or more output units of which fuse has been blown. Remains on if normal status is restored. Output modules of remote I/O stations are also checked fore fuse condition.	○	Usable with all types of CPUs (Only remote I/O station information is valid for A2C.)
∗1 M9002	I/O unit verify error	OFF: Normal ON: Error	• Turned on if the status of I/O module is different from entered status when power is turned on. Remains on if normal status is restored. I/O module verification is done also to remote I/O station modules. (Reset is enabled only when special registers D9116 to D9123 are reset.)	○	Usable with all types of CPUs (Only remote I/O station information is valid for A2C.)
M9004	MINI link master module error	OFF: Normal ON: Error	• Turned on when the MINI (S3) link error is detected on even one of the AJ71PT32(S3) modules being loaded. Remains on if normal status is restored.	—	Dedicated to AnA, A2AS, AnU and QCPU-A (A Mode).
∗1 M9005	AC DOWN detection	OFF: AC power good ON: AC power DOWN	• Turned on when an momentary power failure of 20 msec or less occurred. Reset when POWER switch is moved from OFF to ON position.	○	Usable with all types of CPUs.
M9006	Battery low	OFF: Normal ON: Battery low	• Turned on when battery voltage reduces to less than specified. Turned off when battery voltage becomes normal.	○	Usable with all types of CPUs.
∗1 M9007	Battery low latch	OFF: Normal ON: Battery low	• Turned on when battery voltage reduces to less than specified. Remains on if battery voltage becomes normal	○	Usable with all types of CPUs.
∗1 M9008	Self-diagnostic error	OFF: No error ON: Error	• Turned on when error is found as a result of self-diagnosis.	○	Usable with all types of CPUs.
M9009	Annunciator detection	OFF: No detection ON: Detected	• Turned on when OUT F of SET F instruction is executed. Switched off when D9124 data is zeroed.	○	Usable with all types of CPUs.
M9010	Operation error flag	OFF: No error ON: Error	• Turned on when operation error occurs during execution of application instruction. Turned off when error is eliminated.	△	Unusable with A3H, A3M, AnA, A2AS, AnU and QCPU-A (A Mode).
∗1 M9011	Operation error flag	OFF: No error ON: Error	• Turned on when operation error occurs during execution of application instruction. Remains on if normal status is restored.	○	Usable with all types of CPUs.
M9012	Carry flag	OFF: Carry off ON: Carry on	• Carry flag used in application instruction.	○	Usable with all types of CPUs.

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
M9016	Data memory clear flag	OFF: No processing ON: Output clear	• Clears the data memory including the latch range (other than special relays and special registers) in remote run mode from computer, etc. when M9016 is on.	○	Usable with all types of CPUs.
M9017	Data memory clear flag	OFF: No processing ON: Output clear	• Clears the unlatched data memory (other than special relays and special registers) in remote run mode from computer, etc. when M9017 is on.	○	Usable with all types of CPUs.
＊2 M9018	Data link monitor switching	OFF: F link ON: R link	• Specifies the lines to be monitored for link monitoring.	—	Dedicated to A3V.
M9020	User timing clock No. 0		• Relay which repeats on/off at intervals of predetermined scan. • When power is turned on or reset is per-formed, the clock starts with off. • Set the intervals of on/off by DUTY instruction. 	○	Usable with all types of CPUs.
M9021	User timing clock No. 1				
M9022	User timing clock No. 2				
M9023	User timing clock No. 3				
M9024	User timing clock No. 4				
＊2 M9025	Clock data set request	OFF: No processing ON: Set requested	• Writes clock data from D9025-D9028 to the clock element after the END instruction is executed during the scan in which M9025 has changed from off to on.	△	Unusable with An, A3H, A3M, A3V, A2C, A52G, and A0J2H.
M9026	Clock data error	OFF: No error ON: Error	• Switched on by clock data (D9025 to D9028) error.	△	Unusable with An, A3H, A3M, A3V, A2C, A52G and A0J2H.
M9027	Clock data display	OFF: No processing ON: Display	• Clock data is read from D9025-D9028 and month, day, hour, minute and minute are indicated on the CPU front LED display.	△	Usable with A3N, A3A, A3U, A4U, A73 and A3N board.
＊2 M9028	Clock data read request	OFF: No processing ON: Read request	• Reads clock data to D9025-D9028 in BCD when M9028 is on.	△	Unusable with An, A3H, A3M, A3V, A2C and A0J2H.
M9030	0.1 second clock		• 0.1 second, 0.2 second, 1 second, 2 second, and 1 minute clocks are generated. • Not turned on and off per scan but turned on and off even during scan if corresponding time has elapsed. • Starts with off when power is turned on or reset is performed.	△	Unusable with A3V.
M9031	0.2 second clock				
M9032	1 second clock				
M9033	2 second clock				
M9034	1 minute clock				

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
M9036	Normally ON	ON OFF	• Used as dummy contacts of initialization and application instruction in sequence program. • M9036 and M9037 are turned on and off without regard to position of key switch on CPU front. M9038 and M9039 are under the same condition as RUN status except when the key switch is at STOP position, and turned off and on. Switched off if the key switch is in STOP position. M9038 is on for one scan only and M9039 is off for one scan only if the key switch is not in STOP position.	○	Usable with all types of CPU
M9037	Normally OFF	ON OFF			
M9038	On only for 1 scan after run	ON OFF 1 scan			
M9039	RUN flag (off only for 1 scan after run)	ON 1 scan OFF			
M9040	PAUSE enable coil	OFF: PAUSE disabled ON: PAUSE enabled	• When RUN key switch is at PAUSE position or remote pause contact has turned on and if M9040 is on, PAUSE mode is set and M9041 is turned on.	○	Usable with all types of CPU
M9041	PAUSE status contact	OFF: Not during pause ON: During pause			
M9042	Stop status contact	OFF: During stop ON: Not during stop	• Switched on when the RUN key switch is in STOP position.	○	Usable with all types of CPU
M9043	Sampling trace completion	OFF: During sampling trace ON: Sampling trace completion	• Turned on upon completion of sampling trace performed the number of times preset by parameter after [STRA] instruction is executed. Reset when [STRAR] instruction is executed.	△	Unusable with A1 and A1N.
M9044	Sampling trace	OFF ↔ ON: [STRA] Same as execution ON ↔ OFF: [STRAR] Same as execution	• Turning on/off M9044 can execute [STRA] / [STRAR] instruction. (M9044 is forcibly turned on/off by a peripheral device.) When switched from OFF to ON: [STRA] instruction When switched from ON to OFF: [STRAR] instruction The value stored in D9044 is used as the condition for the sampling trace. At scanning, at time → Time (10 msec unit)	△	Unusable with A1 and A1N.
M9046	Sampling trace	OFF: Except during trace ON: During trace	• Switched on during sampling trace.	△	Unusable with A1 and A1N.
M9047	Sampling trace preparation	OFF: Sampling trace stop ON: Sampling trace start	• Switched on to start sampling trace. • Switched off to stop sampling trace.	△	Unusable with A1 and A1N.
＊2 M9048	RUN LED flicker flag	ON: Flickers at annunciator on. OFF: No flicker at annunciator on.	• Sets whether the RUN LED flickers or not when the annunciator relay F□ is turned on when the A0J2H is used.	—	Usable with A0J2H.
M9048	Memory card battery voltage detection	OFF: Low voltage is not detected. ON: Low voltage is detected.	• Turned ON when the drop in the battery voltage for the memory card is detected. (Automatically turned OFF when the voltage recovers to normal.)	—	Dedicated to QCPU-A (A Mode)
M9049	Switching the number of output characters	OFF: Up to NUL code are output. ON: 16 characters are output.	• When M9049 is off, up to NUL (00H) code are output. • When M9049 is on, ASCII codes of 16 characters are output.	△	Unusable with An, A3V, A2C and A52G

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
＊2 M9050	Operation result storage memory change contact (for CHG instruction)	OFF: Not changed ON: Changed	• Switched on to exchange the operation result storage memory data and the save area data.	—	Dedicated to A3
M9051	CHG instruction execution disable	OFF: Disable ON: Enable	• Switched on to disable the CHG instruction. • Switched on when program transfer is requested and automatically switched off when transfer is complete.	—	Usable with A3, A3N, A3H, A3M, A3V, A3A, A3U, A4U, A73 and A3N board
＊2 M9052	SEG instruction switching	OFF: 7SEG display ON: I/O partial refresh	• Switched on to execute the SEG instruction as an I/O partial refresh instruction. Switched off to execute the SEG instruction as a 7SEG display instruction.	△	Unusable with An, A3V and A3N board
＊2 M9053	EI / DI instruction switching	OFF: Sequence interrupt control ON: Link interrupt control	• Switched on to execute the link refresh enable, disable (EI, DI) instructions.	△	Unusable with An, A3V and A3N board
M9054	STEP RUN flag	OFF: Other than step run ON: During step run	• Switched on when the RUN key switch is in STEP RUN position.	△	Unusable with An, AnS, AnSH, A1FX, A2C, A0J2H, and A52G
M9055	Status latch complete flag	OFF: Not complete ON: Complete	• Turned on when status latch is completed. Turned off by reset instruction.	△	Unusable with A1 and A1N.
M9056	Main program P, I set request	OFF: Other than P, I set request ON: P, I set request	• Provides P, I set request after transfer of the other program (for example subprogram when main program is being run) is complete during run. Automatically switched off when P, I setting is complete.	—	Usable with A3, A3N, A3H, A3M, A3V, A3A, A73, A3U, A4U and A3N board
M9057	Subprogram 1 P, I set request	OFF: Except during P, I set request ON: During P, I set request			
M9060	Subprogram 2 P, I set request			—	Dedicated to A4U
M9061	Subprogram 3 P, I set request				
M9060	Remote terminal error	OFF: Normal ON: Error	• Turned on when one of remote terminal modules has become a faulty station. • Communication error is detected when normal communication is not restored after the number of retries set at D9174. • Turned off when communication with all re-mote terminal modules is restored to normal with automatic online return enabled. • Remains on when automatic online return is disabled. • Not turned on or off when communication is suspended at error detection.	—	Usable with A2C and A52G
M9061	Communication error	OFF: Normal ON: Error	• Turned on when communication with a remote terminal module or an I/O module is faulty. • Communication error occurs due to the following reasons. • Initial data error • Cable breakage • Power off for remote terminal modules or I/O modules • Turned off when communication is restored to normal with automatic online return enabled. • Remains on when communication is suspended at error detection with automatic online return disabled.	—	Usable with A2C and A52G

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
M9065	Divided transfer status	OFF: Other than divided processing ON: Divided processing	• Turned on when canvas screen transfer to AD57(S1)/AD58 is done by divided processing, and turned off at completion of divided processing.	—	Usable with AnA and AnU.
＊2 M9066	Transfer processing switching	OFF: Batch transfer ON: Divided transfer	• Turned on when canvas screen transfer to AD57(S1)/AD58 is done by divided processing.	—	Usable with AnA and AnU.
M9067	I/O module error detection	OFF: Normal ON: Error	• Turned on when one of I/O modules has become a faulty station. • Communication error is detected when normal communication is not restored after the number of retries set at D9174. • Turned off when communication with all I/O modules is restored to normal with automatic online return enabled. • Remains on when automatic online return is disabled. • Not turned on or off when communication is suspended at error detection.	—	Usable with A2C and A52G.
M9068	Test mode	OFF: Automatic online return enabled Automatic online return disabled Communication suspended at online error ON: Line check	• Turned on when line check with I/O modules and remote terminal modules is performed. • Turned off when communication with I/O modules and remote terminal modules is per-formed.	—	Usable with A2C and A52G.
M9069	Output at line error	OFF: All outputs are turned off. ON: Outputs are retained.	• Sets whether all outputs are turned off or retained at communication error. OFF: ..... All outputs are turned off at communication error. ON: ..... Outputs before communication error are retained.	—	Usable with A2C and A52G.
＊1 M9073	WDT error flag	OFF: No WDT error ON:WDT error	• Set when WDT error is detected by the self-check of the PCPU.	—	Dedicated to A73.
M9073	Setting of writing to flash ROM	OFF: Disables writing to ROM ON: Enables writing to ROM	• Turned ON to enable writing to the flash ROM. (DIP switch 3 should be set to ON.)	—	Dedicated to QCPU-A (A Mode)
M9074	PCPU ready complete flag	OFF: PCPU ready incomplete ON: PCPU ready complete	• Set if the motor is not running when it is checked at PC ready (M2000) on. Reset when M2000 is turned off.	—	Dedicated to A73.
M9074	Request for writing to flash ROM	OFF → ON: Starts writing to ROM	• When turned from OFF to ON, writing to the standard ROM is started.	—	Dedicated to QCPU-A (A Mode)
M9075	Test mode flag	OFF: Other than test mode ON: Test mode	• Set when a test mode request is made from a peripheral device. Reset when test mode is finished.	—	Dedicated to A73.

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
M9075	Successful completion of writing to standard ROM	OFF: Failed writing to ROM ON: Successfully completed writing to ROM	• Turns ON when writing to the standard ROM is successfully completed. (This status is stored in D9075.)	—	Dedicated to QCPU-A (A Mode)
M9076	External emergency stop input flag	OFF: External emergency stop input is on. ON: External emergency stop input is off.	• Reset when the external emergency stop input connected to the EMG terminal of A70SF is turned on. Set when the external emergency stop input is turned off.	—	Dedicated to A73.
M9076	Status of writing to standard ROM	OFF: Writing to ROM disabled ON: Writing to ROM enabled	• Turns ON when writing to standard ROM is enabled. (Turns ON when DIP switch and M9073 are ON.)	—	Dedicated to QCPU-A (A Mode)
M9077	Manual pulse generator axis setting error flag	OFF: All axes normal ON: Error axis detected	• Set when there is an error in the contents of manual pulse generator axis setting. Reset if all axes are normal when the manual pulse generator enable flag is set.	—	Dedicated to A73.
M9077	Sequence accumulation time measurement	OFF: Time not elapsed ON: Time elapsed	• Compares the setting value at D9077 with the time elapsed from the start of measurement (accumulation time) at every scan. Then, performs the following operations: Setting value > Accumulation time: Turns M9077 ON and clears the accumulation time. Setting value < Accumulation time: Turns M9077 from ON to OFF and clears the accumulation time. When M9077 is already OFF, clears the accumulation time. * When 1 to 255 is designated at D9077, M9077 is turned ON at the first scan. * When the value other than 1 to 255 is designated at D9077, the value in D9077 is reset to 0 and M9077 is always turned OFF.	—	Dedicated to QCPU-A (A Mode)
M9078	Test mode request error flag	OFF: No error ON: Error	• Set when test mode is not available though a test mode request was made from a peripheral device. Reset if test mode becomes available by making another test mode request.	—	Dedicated to A73.
M9079	Servo program setting error flag	OFF: No data error ON: Data error	• Turned on when the positioning data of the servo program designated by the DSFRP instruction has an error. Turned off when the data has no error after the DSFRP instruction is executed again.	—	Dedicated to A73.

Special Relay List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>M9080</td><td>BUSY flag for execution of CC-Link dedicated instruction</td><td>OFF: Number of remaining instructions executable simultaneously: 1 to 10
ON: Number of remaining instructions executable simultaneously: 0</td><td>Turned ON/OFF according to the number of remaining instructions (RIRD/RIWT/RISEND/RIRCV) being executable simultaneously at one scan.
OFF: Number of remaining instructions executable simultaneously: 1 to 10
ON: Number of remaining instructions executable simultaneously: 0
By assigning M9080 as execution condition, the number of instructions above executed simultaneously at one scan can be limited to 10 or less.
*4: This function is available with the CPU of the following S/W versions or later.
<table>
<tr><th>CPU Type Name</th><th>Software Version</th></tr>
<tr><td>Q02CPU-A, Q02HCPU-A, Q06HCPU-A</td><td rowspan="2">Available with all versions</td></tr>
<tr><td>A1SJHCPU, A1SHCPU, A2SHCPU</td></tr>
<tr><td>A2UCPU(S1), A3UCPU, A4UCPU</td><td>S/W version Q (Manufactured in July, 1999)</td></tr>
<tr><td>A2USCPU(S1)</td><td>S/W version E (Manufactured in July, 1999)</td></tr>
<tr><td>A2USHCPU-S1</td><td>S/W version L (Manufactured in July, 1999)</td></tr>
</table></td><td>△</td><td>Can be used only with AnU, A2US, AnSH or QCPU-A (A Mode) *4</td></tr>
<tr><td>M9081</td><td>Communication request to remote terminal modules</td><td>OFF: Communication request to remote terminal modules enabled
ON: Communication request to remote terminal modules disabled</td><td>• Indication of communication enable/disable to remote terminal modules connected to the AJ71PT32-S3, A2C or A52G.</td><td>—</td><td>Usable with AnA, AnA, AnU, A2AS, QCPU-A (A Mode) A2C and A52G.</td></tr>
<tr><td>M9082</td><td>Final station number disagreement</td><td>OFF: Final station number agreement
ON: Final station number disagreement</td><td>• Turned on when the final station number of the remote terminal modules and remote I/O modules connected to the A2C or A52G disagrees with the total number of stations set in the initial setting.
• Turned off when the final station number agrees with the total number of stations at STOP→RUN.</td><td>—</td><td>Dedicated to A2C and A52G.</td></tr>
<tr><td>*2
M9084</td><td>Error check</td><td>OFF: Checks enabled
ON: Checks disabled</td><td>• Specify whether the following errors are to be checked or not after the END instruction is executed (to reduce END processing time):
• Fuse blown
• I/O unit verify error
• Battery error</td><td>△</td><td>Unusable with An, A2C and A3V.</td></tr>
<tr><td>M9086</td><td>BASIC program RUN flag</td><td>OFF: A3M-BASIC stop
ON: A3M-BASIC run</td><td>• Set when the A3M-BASIC is in RUN state, and reset when it is in STOP state.</td><td>—</td><td>Dedicated to A3M</td></tr>
<tr><td>M9087</td><td>BASIC program PAUSE flag</td><td>OFF: A3M-BASIC RUN enable
ON: A3M-BASIC disable</td><td>• Specifies enable/disable of A3M-BASIC execution when the A3MCPU is in PAUSE state.
OFF: A3M-BASIC is executed.
ON: A3M-BASIC is not executed.</td><td>—</td><td>Dedicated to A3M.</td></tr>
</table>

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
＊1 M9091	Operation error detail flag	OFF: No error ON: Error	• Set when an operation error detail factor is stored at D9091, and remains set after normal state is restored.	—	Usable with AnA, A2AS, AnU and QCPU-A (A Mode).
＊ M9091	Microcomputer subroutine call error flag	OFF: No error ON: Error	• Set when an error occurred at execution of the microcomputer program package, and remains set after normal state is restored.	△	Unusable with AnA, A2AS, AnU and QCPU-A (A Mode).
M9092	Duplex power supply overheat error	OFF: Normal ON: Overheat	• Turned on when overheat of a duplex power supply module is detected.	—	Dedicated to A3V.
M9093	Duplex power supply error	OFF: Normal ON: Failure or AC power supply down	• Turned on when a duplex power supply module caused failure or the AC power supply is cut down.	—	Unusable with A3V.
＊2 ＊3 M9094	I/O change flag	OFF: Changed ON: Not changed	• After the head address of the required I/O module is set to D9094, switching M9094 on allows the I/O module to be changed in online mode. (One module is only allowed to be changed by one setting.) • To be switched on in the program or peripheral device test mode to change the module during CPU RUN. To be switched on in peripheral device test mode to change the module during CPU STOP. • RUN/STOP mode must not be changed until I/O module change is complete.	△	Usable with AnN, AnA and AnU.
M9095	Duplex operation verify error	OFF: Normal ON: Duplex operation verify error	• During duplex operation of the operating CPU with a stand-by CPU, verification is performed by the both to each other. Turned on when a verify error occurred.	—	Dedicated to A3V.
M9096	A3VCPU A self-check error	OFF: No error ON: Error	• Turn on when a self-check error occurred on the A3VCPU A mounted next to the A3VTU.	—	Dedicated to A3V.
M9097	A3VCPU B self-check error	OFF: No error ON: Error	• Turn on when a self-check error occurred on the A3VCPU B mounted next to the A3VCPU A.	—	Dedicated to A3V.
M9098	A3VCPU C self-check error	OFF: No error ON: Error	• Turn on when a self-check error occurred on the A3VCPU C mounted next to the A3VCPU B.	—	Dedicated to A3V.
M9099	A3VTU self-check error	OFF: No error ON: Error	• Turned on when a self-check error occurred on the A3VTU.	—	Dedicated to A3V.
M9100	SFC program registration	OFF: No SFC program ON: SFC program registered	• Turned on if the SFC program is registered, and turned off if it is not.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
＊2 M9101	SFC program start/stop	OFF: SFC program stop ON: SFC program start	• Should be turned on by the program if the SFC program is to be started. If turned off, operation output of the execution step is turned off and the SFC program is stopped.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.

＊: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-II Programming Manual.

Special Relay List (Continue)

Number	Name	Description	Details	Applicable CPU	
＊2 M9102	SFC program starting status	OFF: Initial start ON: Continuous start	• Selects the starting step when the SFC program is restarted using M9101. ON: All execution conditions when the SFC program stopped are cleared, and the program is started with the initial step of block 0. OFF: Started with the step of the block being executed when the program stopped. • Once turned on, the program is latched in the system and remains on even if the power is turned off. Should be turned off by the sequence program when turning on the power, or when starting with the initial step of block 0.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
＊2 M9103	Consecutive step transfer enable/disable	OFF: Consecutive step transfer disable ON: Consecutive step transfer enable	• Selects consecutive or step-by-step transfer of steps of which transfer conditions are established when all of the transfer conditions of consecutive steps are established. ON: Consecutive transfer is executed. OFF: One step per one scan is transferred.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
M9104	Consecutive transfer prevention flag	OFF: Transfer complete ON: Transfer incomplete	• Set when consecutive transfer is not executed with consecutive transfer enabled. Reset when transfer of one step is completed. Consecutive transfer of a step can be prevented by writing an AND condition to corresponding M9104.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
＊2 M9108	Step transfer monitoring timer start (corresponds to D9108)	OFF: Monitoring timer eset ON: Monitoring timer eset start	• Turned on when the step transfer monitoring timer is started. Turned off when the monitoring timer is reset.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
＊2 M9109	Step transfer monitoring timer start (corresponds to D9109)				
＊2 M9110	Step transfer monitoring timer start (corresponds to D9110)				
＊2 M9111	Step transfer monitoring timer start (corresponds to D9111)				
＊2 M9112	Step transfer monitoring timer start (corresponds to D9112)				

＊: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-II Programming Manual.

Special Relay List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th colspan="4">Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>＊2
M9113</td><td>Step transfer monitoring timer start (corresponds to D9113)</td><td colspan="4" rowspan="2">OFF: Monitoring timer reset
ON: Monitoring timer reset start</td><td rowspan="2">• Turned on when the step transfer monitoring timer is started. Turned off when the monitoring timer is reset.</td><td rowspan="2">—</td><td rowspan="2">Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>＊2
M9114</td><td>Step transfer monitoring timer start (corresponds to D9114)</td></tr>
<tr><td>M9180</td><td>Active step sampling trace complete flag</td><td colspan="4">OFF: Trace start
ON: Trace complete</td><td>• Set when sampling trace of all specified blocks is completed. Reset when sampling trace is started.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>M9181</td><td>Active step sampling trace execution flag</td><td colspan="4">OFF: Trace not executed.
ON: Trace being executed.</td><td>• Set when sampling trace is being executed. Reset when sampling trace is completed or suspended.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>＊2
M9182</td><td>Active step sampling trace enable</td><td colspan="4">OFF: Trace disable/suspend
ON: Trace enable</td><td>• Selects sampling trace execution enable/disable.
ON: Sampling trace execution is enabled.
OFF: Sampling trace execution is disabled. If turned off during sampling trace execution, trace is suspended.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>＊2
M9196</td><td>Operation output at block stop</td><td colspan="4">OFF: Coil output off
ON: Coil output on</td><td>• Selects the operation output when block stop is executed.
ON: Retains the ON/OFF status of the coil being used by using operation output of the step being executed at block stop.
OFF: All coil outputs are turned off. (Operation output by the SET instruction is retained regardless of the ON/OFF status of M9196.)</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td rowspan="2">M9197

M9198</td><td rowspan="5">Fuse blow, I/O verify error display switching</td><td>M9197</td><td>M9198</td><td>I/O numbers to be displayed</td><td rowspan="5">• Switches I/O numbers in the fuse blow module storage registers (D9100 to D9107) and I/O module verify error storage registers (D9116 to D9123) according to the combination of ON/OFF of the M9197 and M9198.</td><td rowspan="5">—</td><td rowspan="5">Usable with AnU, A2AS and QCPU-A (A Mode).</td></tr>
<tr><td>OFF</td><td>OFF</td><td>X/Y0 to 7F0</td></tr>
<tr><td>ON</td><td>OFF</td><td>X/Y800 to FF0</td></tr>
<tr><td>OFF</td><td>ON</td><td>X/Y1000 to 17F0</td></tr>
<tr><td>ON</td><td>ON</td><td>X/Y1800 to 1FF0</td></tr>
</table>

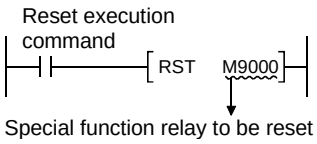
＊: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-II Programming Manual.

POINTS

(1) Contents of the M special relays are all cleared by power off, latch clear or reset with the reset key switch. When the RUN key switch is set in the STOP position, the contents are retained.

(2) The above the relays with numbers marked ＊1 remain "on" if normal status is restored. Therefore, to turn them "off", use the following method:

(a) Method by use program
Insert the circuit shown at right into the program and turn on the reset execution command contact to clear the special relay M.



(b) Perform forced reset by use of the test function of peripheral devices.
For the operation procedure, refer to the manuals for peripheral devices.

(c) By moving the RESET key switch on the CPU front to the RESET position, the special relays are turned off.

(3) Special relays marked ＊2 above are switched on/off in the sequence program.

(4) Special relays marked ＊3 above are switched on/off in test mode of the peripheral equipment.

Appendix 2.2 Special relays for link

The link special relays are internal relays which are switched on/off by various factors occurring during data link operation.
Their ON/OFF status will change if an error occurs during normal operation.

(1) Link special relays only valid when the host is the master station

Link Special Relay List

Number	Name	Description	Details
M9200	LRDP instruction received	OFF: Unreceived ON: Received	• Depends on whether or not the LRDP (word device read) instruction has been received. • Used in the program as an interlock for the LRDP instruction. • Use the RST instruction to reset.
M9201	LRDP instruction complete	OFF: Incomplete ON: Complete	• Depends on whether or not the LRDP (word device read) instruction execution is complete. • Used as a condition contact for resetting M9200 and M9201 after the LRDP instruction is complete. • Use the RST instruction to reset.
M9202	LWTP instruction received	OFF: Unreceived ON: Received	• Depends on whether or not the LWTP (word device write) instruction has been received. • Used in the program as an interlock for the LWTP instruction. • Use the RST instruction to reset.
M9203	LWTP instruction complete	OFF: Incomplete ON: Complete	• Depends on whether or not the LWTP (word device write) instruction execution is complete. • Used as a condition contact to reset M9202 and M9203 after the LWTP instruction is complete. • Use the RST instruction to reset.
M9206	Link parameter error in the host	OFF: Normal ON: Error	Depends on whether or not the link parameter setting of the host is valid.
M9207	Link parameter unmatched between master station	OFF: Normal ON: Unmatched	Depends on whether or not the link parameter setting of the master station in tier two matches that of the master station in tier three in a three-tier system. (Valid only for the master stations in a three-tier system.)
M9210	Link card error (master station)	OFF: Normal ON: Error	Depends on presence or absence of the link card hardware error. Judged by the CPU.
M9224	Link status	OFF: Online ON: Offline, station-to-station test, or self-loopback test	Depends on whether the master station is online or offline or is in station-to-station test or self-loopback test mode.
M9225	Forward loop error	OFF: Normal ON: Error	Depends on the error condition of the forward loop line.
M9226	Reverse loop error	OFF: Normal ON: Error	Depends on the error condition of the reverse loop line.
M9227	Loop test status	OFF: Unexecuted ON: Forward or reverse loop test being executed	Depends on whether or not the master station is executing a forward or a reverse loop test.

Link Special Relay List (Continue)

Number	Name	Description	Details
M9232	Local station operating status	OFF: RUN or STEP RUN mode ON: STOP or PAUSE mode	Depends on whether or not a local station is in STOP or PAUSE mode.
M9233	Local station error detect	OFF: No error ON: Error detected	Depends on whether or not a local station has detected an error in another station.
M9235	Local or remote I/O station parameter error detect	OFF: No error ON: Error detected	Depends on whether or not a local or a remote I/O station has detected any link parameter error in the master station
M9236	Local or remote I/O station initial communicating status	OFF: Noncommunicating ON: Communicating	Depends on whether or not a local or a remote I/O station is communicating initial data (such as parameters) with the master station.
M9237	Local or remote I/O station error	OFF: Normal ON: Error	Depends on the error condition of a local or remote I/O station.
M9238	Local or remote I/O station forward/ reverse loop error	OFF: Normal ON: Error	Depends on the error condition of the forward and reverse loop lines of a local or a remote I/O station.

(2) Link special relays only valid when the host is a local station

Link Special Relay List

Number	Name	Description	Details
M9204	LRDP instruction complete	OFF: Incomplete ON: Complete	On indicates that the LRDP instruction is complete at the local station.
M9205	LWTP instruction complete	OFF: Incomplete ON: Complete	On indicates that the LWTP instruction is complete at the local station.
M9211	Link card error (local station)	OFF: Normal ON: Error	Depends on presence or absence of the link card error. Judged by the CPU.
M9240	Link status	OFF: Online ON: Offline, station-to-station test, or self-loopback test	Depends on whether the local station is online or offline, or is in station-to-station test or self-loopback test mode.
M9241	Forward loop error	OFF: Normal ON: Error	Depends on the error condition of the forward loop line.
M9242	Reverse loop error	OFF: Normal ON: Error	Depends on the error condition of the reverse loop line.
M9243	Loopback execution	OFF: Non-executed ON: Executed	Depends on whether or not loopback is occurring at the local station.
M9246	Data unreceived	OFF: Received ON: Unreceived	Depends on whether or not data has been received from the master station.
M9247	Data unreceived	OFF: Received ON: Unreceived	Depends on whether or not a tier three station has received data from its master station in a three-tier system.
M9250	Parameter unreceived	OFF: Received ON: Unreceived	Depends on whether or not link parameters have been received from the master station.
M9251	Link break	OFF: Normal ON: Break	Depands on the data link condition at the local station.
M9252	Loop test status	OFF: Unexecuted ON: Forward or reverse loop test is being executed	Depends on whether or not the local station is executing a forward or a reverse loop test.
M9253	Master station operating status	OFF: RUN or STEP RUN mode ON: STOP or PAUSE mode	Depends on whether or not the master station is in STOP or PAUSE mode.
M9254	Operating status of other local stations	OFF: RUN or STEP RUN mode ON: STOP or PAUSE mode	Depends on whether or not a local station other than the host is in STOP or PAUSE mode.
M9255	Error status of other local stations	OFF: Normal ON: Error	Depends on whether or not a local station other than the host is in error.

Appendix 2.3 Special registers

Special registers are data registers of which applications have been determined inside the PC. Therefore, do not write data to the special registers in the program (except the ones with numbers marked ∗2 in the table).

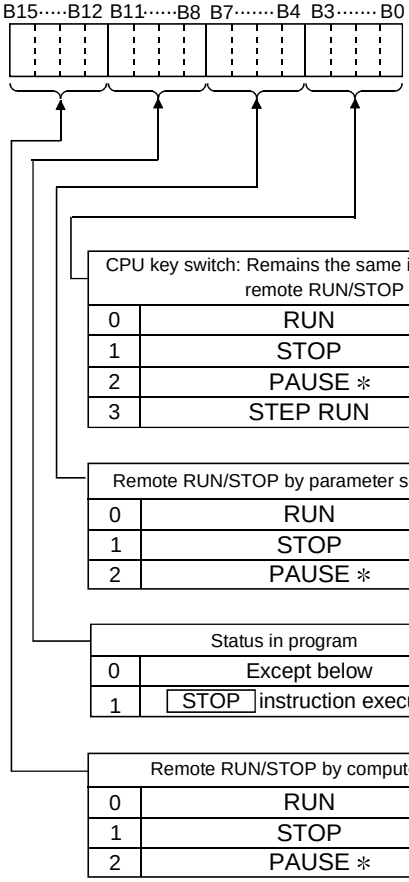
Special Register List

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9000</td><td>Fuse blow</td><td>Fuse blow module number</td><td>• When fuse blown modules are detected, the lowest number of detected units is stored in hexadecimal. (Example: When fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) To monitor the number by peripheral devices, perform monitor operation given in hexadecimal. (Cleared when all contents of D9100 to D9107 are reset to 0.)
• Fuse blow check is executed also to the output modules of remote I/O stations.</td><td>△</td><td>Unusable with A0J2H.
(Only remote I/O station information is valid for A2C.)</td></tr>
<tr><td>D9001</td><td>Fuse blow</td><td>Fuse blow module number</td><td>• Stores the module numbers corresponding to setting switch numbers or base slot numbers when fuse blow occurred.
<table>
<tr><th colspan="2">I/O Module for A0J2</th><th colspan="2">Extension Base Unit</th></tr>
<tr><th>Setting Switch</th><th>Stored Data</th><th>Base Unit Slot No.</th><th>Stored Data</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>2</td><td>1</td><td>6</td></tr>
<tr><td>2</td><td>3</td><td>2</td><td>7</td></tr>
<tr><td>3</td><td>4</td><td>3</td><td>8</td></tr>
<tr><td>4</td><td>5</td><td></td><td></td></tr>
<tr><td>5</td><td>6</td><td></td><td></td></tr>
<tr><td>6</td><td>7</td><td></td><td></td></tr>
<tr><td>7</td><td>8</td><td></td><td></td></tr>
</table></td><td>—</td><td>Dedicated to A0J2H.</td></tr>
<tr><td rowspan="2">D9002</td><td rowspan="2">I/O module verify error</td><td rowspan="2">I/O module verify error unit number</td><td>• If I/O modules, of which data are different from data entered, are detected when the power is turned on, the first I/O number of the lowest number unit among the detected units is stored in hexadecimal. (Storing method is the same as that of D9000.) To monitor the number by peripheral devices, perform monitor operation given in hexadecimal. (Cleared when all contents of D9116 to D9123 are reset to 0.)
• I/O module verify check is executed also to the modules of remote I/O terminals.</td><td>△</td><td>Unusable with A0J2H.
(Only remote I/O station information is valid for A2C.)</td></tr>
<tr><td>• If an I/O module, of which data is different from data entered, is detected when the power in turned on, the I/O number corresponding to the setting switch No. or base unit No. is stored. (Storing method is the same as that of D9001).
• In case of remote I/O station, (module I/O number/10H) + 1 is stored.</td><td>—</td><td>Dedicated to A0J2H.</td></tr>
</table>

Special Register List (Continue)

Number	Name	Description	Details	Applicable CPU	
D9003	SUM instruction detection bits	The number of bits detected by SUM instruction detection.	• The number of bits detected by execution of the SUM instruction are stored. in BIN code and updated every execution thereafter.	—	Dedicated to A0J2H.
＊1 D9004	MINI link master module error	Error detection status	• Error status of the MINI(S3) link detected on loaded AJ71PT32(S3) is stored. b15 to b8 b7 to b0 8 7 6 5 4 3 2 1 | 8 7 6 5 4 3 2 1 Bits which correspond to faulty AJ71PT32(S3) are turned on. Bits which correspond to the signals of AJ71PT32(S3), shown below, are turned on as the signals are turned on. · Hardware error (X0/X20) · MINI(S3) link error detection (X6/X26) · MINI(S3) link communication error (X7/X27)	—	Usable with AnA, A2AS and AnU.
＊1 D9005	AC DOWN counter	AC DOWN count	• 1 is added each time input voltage becomes 85% or less of rating while the CPU unit is performing operation, and the value is stored in BIN code.	○	Usable with all types of CPUs.
D9006	Battery low	Indicates the CPU module of which battery voltage is low.	• Bits which correspond to CPU of which battery is low are turned on in D9006, as shown below. B15 B3 B2 B1 B0 0 0 CPU A CPU B CPU C 0: Normal 1: Battery low	—	Dedicated to A3V.
＊1 D9008	Shelf-diagnostic error	Self-diagnostic error number	• When error is found as a result of self-diagnosis, error number is stored in BIN code.	○	Usable with all types of CPUs.
D9009	Annunciator detection	F number at which external failure has occurred	• When one of F0 to 255 is turned on by OUT F or SET F, the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. • D9009 can be cleared by RST F or LEDR instruction. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.	△	Unusable with A3, A3N, A3A, A73 and A3N board.
			• When one of F0 to 255 is turned on by OUT F or SET F, the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. • D9009 can be cleared by executing RST F or LEDR instruction or moving INDICATOR RESET switch on CPU front to ON position. If another F number has been detected, the clearing of D9009 causes the nest number to be stored in D9009.	—	Usable with A3, A3N, A3A, A73 and A3N board.

Special Register List (Continue)

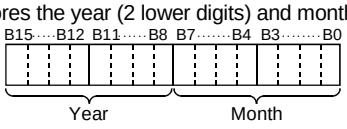
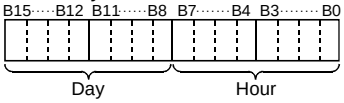
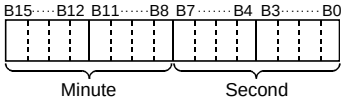
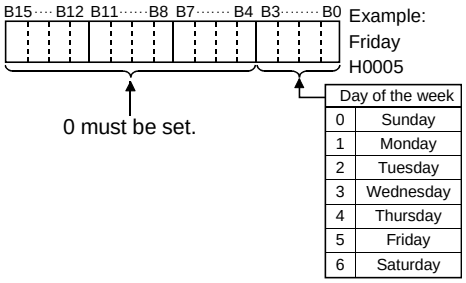
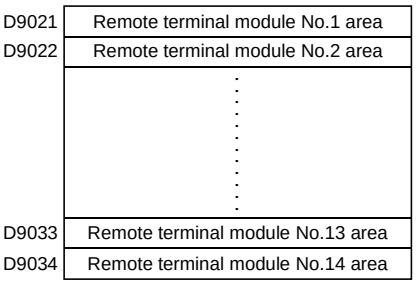
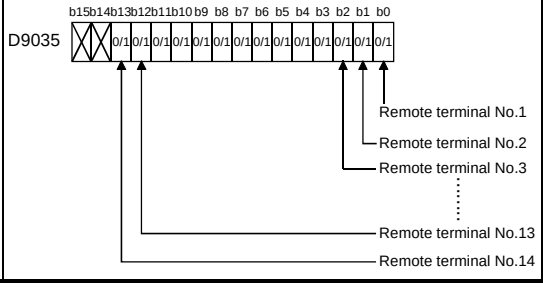
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9010</td><td>Error step</td><td>Step number at which operation error has occurred</td><td>• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Thereafter, each time operation error occurs, the contents of D9010 are renewed.</td><td>△</td><td>Unusable with A3H and A3M.</td></tr>
<tr><td>＊1
D9011</td><td>Error step</td><td>Step number at which operation error has occurred</td><td>• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Since storage into D9011 is made when M9011 changes from off to on, the contents of D9010 cannot be renewed unless M9011 is cleared by user program.</td><td>○</td><td>Usable with all types of CPUs.</td></tr>
<tr><td>D9014</td><td>I/O control mode</td><td>I/O control mode number</td><td>• The I/O control mode set is returned in any of the following numbers:
0. Both input and output in direct mode
1. Input in refresh mode, output in direct mode
3. Both input and output in refresh mode</td><td>△</td><td>Unusable with An, A3H and A3M.</td></tr>
<tr><td>D9015</td><td>CPU operating states</td><td>Operating states of CPU</td><td>• The operation states of CPU as shown below are stored in D9015.
 

＊ When the CPU is in RUN mode and M9040 is off, the CPU remains in RUN mode if changed to PAUSE mode.</td><td>○</td><td>Usable with all types of CPUs.</td></tr>
</table>

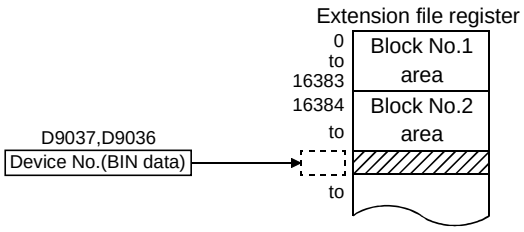
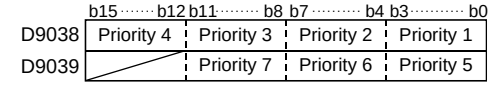
Special Register List (Continue)

Number	Name	Description	Details	Applicable CPU	
	ROM/RAM setting	0: ROM 1: RAM 2: E^2PROM	• Indicates the setting of memory select chip. One value of 0 to 2 is stored in BIN code.	—	Usable with A1 and A1N.
		0: Main program (ROM) 1: Main program (RAM) 2: Subprogram (RAM)	• Indicates which sequence program is run presently. One value of 0 to 2 is stored in BIN code. "2" is not stored when AnS, AnSH, A1FX, A0J2H, A2C, A2, A2N, A2A, A2AS and A2U is used.	△	Unusable with A1 and A1N
D9016	Program number	0: Main program (ROM) 1: Main program (RAM) 2: Subprogram 1 (RAM) 3: Subprogram 2 (RAM) 4: Subprogram 3 (RAM) 5: Subprogram 1 (ROM) 6: Subprogram 2 (ROM) 7: Subprogram 3 (ROM) 8: Main program (E^2PROM) 9: Subprogram (E^2PROM) A: Subprogram (E^2PROM) B: Subprogram (E^2PROM)	• Indicates which sequence program is run presently. One value of 0 to B is stored in BIN code.	—	Dedicated to AnU.
D9017	Scan time	Minimum scan time (per 10 ms)	• If scan time is smaller than the content of D9017, the value is newly stored at each END. Namely, the minimum value of scan time is stored into D9017 in BIN code.	○	Usable with all types of CPUs.
D9018	Scan time	Scan time (per 10 ms)	• Scan time is stored in BIN code at each END and always rewritten.	○	Usable with all types of CPUs.
D9019	Scan time	Maximum scan time (per 10 ms)	• If scan time is larger than the content of D9019, the value is newly stored at each END. Namely, the maximum value of scan time is stored into D9019 in BIN code.	○	Usable with all types of CPUs.
＊2 D9020	Constant scan	Constant scan time (Set by user in 10 ms increments)	• Sets the interval between consecutive program starts in multiples of 10 ms. 0: No setting 1 to 200: Set. Program is executed at intervals of (set value) × 10 ms.	△	Unusable with An.
D9021	Scan time	Scan time (1 msec unit)	• Scan time is stored and updated in BIN code after every END.	—	Usable with AnA, A2AS, AnU and QCPU-A (A Mode).
D9022	1 second counter	Counts 1 every second.	• When the PC CPU starts running, it starts counting 1 every second. • It starts counting up from 0 to 32767, then down to –32768 and then again up to 0. Counting repeats this routine.	—	Usable with AnA, A2AS, AnU and QCPU-A (A Mode).

Special Register List (Continue)

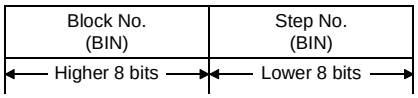
Number	Name	Description	Details	Applicable CPU	
＊2 D9025	Clock data	(Year, month)	• Stores the year (2 lower digits) and month in BCD.  Example: 1987,July H8707	△	Unusable with An, A3H, A3M, A3V, A2C and A0J2H.
＊2 D9026	Clock data	(Day, hour)	• Stores the day and hour in BCD.  Example: 31th,10 o'clock H3110	△	Unusable with An, A3H, A3M, A3V, A2C and A0J2H.
＊2 D9027	Clock data	(Minute, second)	• Stores the Minute and second in BCD.  Example: 35 minutes, 48 seconds H3548	△	Unusable with An, A3H, A3M, A3V, A2C and A0J2H.
＊2 D9028	Clock data	(, day of the week)	• Stores the day of the week in BCD.  Example: Friday H0005 Day of the week: 0 Sunday, 1 Monday, 2 Tuesday, 3 Wednesday, 4 Thursday, 5 Friday, 6 Saturday	△	Unusable with An, A3H, A3M, A3V, A2C and A0J2H.
D9021 D9022 D9023 D9024 D9025 D9026 D9027 D9028 D9029 D9030 D9031 D9032 D9033 D9034	Remote terminal parameter setting	1 to 61	• Sets the head station number of remote terminal modules connected to A2C and A52G. Setting is not necessarily in the order of station numbers. A2CCPUC24: 1 to 57 Other CPUs: 1 to 61 • Data configuration 	—	Usable with A2C and A52G.
D9035	Attribute of remote terminal module	0: MINI standard protocol 1: No protocol	• Sets attribute of each remote terminal module connected to A2C and A52G with 0 or 1 at each bit. 0: Conforms to the MINI standard protocol or remote terminal unit. 1: No-protocol mode of AJ35PTF-R2 • Data configuration 		

Special Register List (Continue)

Number	Name	Description	Details	Applicable CPU	
D9035	Extension file register	Use block No.	• Stores the block No. of the extension file register being used in BCD code.	—	Usable with AnA, A2AS, AnU and QCPU-A (A Mode)
D9036	Total number of stations	1 to 64	• Sets the total number of stations (1 to 64) of I/O modules and remote terminal modules which are connected to an A2C or A52G.	—	Usable with A2C and A52G.
D9036 D9037	For designation extension file register device numbers	The devise number used for getting direct access to each device for extension file register	• Designate the device number for the extension file register for direct read and write in 2 words at D9036 and D9037 in BIN data. Use consecutive numbers beginning with R0 of block No. 1 to designate device numbers. 	—	Usable with AnA, A2AS, AnU and QCPU-A (A Mode).
D9038 D9039	LED indication priority	Priority 1 to 4 Priority 5 to 7	• Sets priority of ERROR LEDs which illuminate (or flicker) to indicate errors with error code numbers. • Configuration of the priority setting areas is as shown below.  • For details, refer to the applicable CPUs User's Manual and the ACPU (Fundamentals) Programming manual.	—	Usable with A2C, AnS, AnSH, A1FX, A0J2H, A52G AnA, A2AS, AnU and QCPU-A (A Mode).
D9044	Sampling trace	Step or time during sampling trace	• Turned on/off with a peripheral device. At scanning..... 0 At time ..... Time (10 msec unit) Stores the value in BIN code.	△	Usable with A1 and A1N
D9049	SFC program execution work area	Expansion file register block number to be used as the work area for the execution of a SFC program.	• Stores the block number of the expansion file register which is used as the work area for the execution of a SFC program in a binary value. • Stores "0" if an empty area of 16K bytes or smaller, which cannot be expansion file register No. 1, is used or if M9100 is OFF.	—	Usable with AnN*, AnA*, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.
D9050	SFC program error code	Code number of error occurred in the SFC program	• Stores code numbers of errors occurred in the SFC program in BIN code. 0: No error 80: SFC program parameter error 81: SFC code error 82: Number of steps of simultaneous execution exceeded 83: Block start error 84: SFC program operation error		
D9051	Error block	Block number in which an error occurred.	• Stores the block number in which an error occurred in the SFC program in BIN code. In the case of error 83 the starting block number is stored.	—	Usable with AnN*, AnA*, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.

*: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-ll Programming Manual.

Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9052</td><td>Error step</td><td>Step number in which an error occurred.</td><td>• Stores the step number in which error 84 occurred in the SFC program in BIN code.
Stores "0" when errors 80, 81 and 82 occurred.
Stored the block starting step number when error 83 occurred.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>D9053</td><td>Error transfer</td><td>Transfer condition number in which an error occurred.</td><td>• Stores the transfer condition number in which error 84 occurred in the SFC program in BIN code.
Stored "0" when errors 80, 81, 82 and 83 occurred.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>D9054</td><td>Error sequence step</td><td>Sequence step number in which an error occurred.</td><td>• Stores the sequence step number of transfer condition and operation output in which error 84 occurred in the SFC program in BIN code.</td><td>—</td><td>Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G.</td></tr>
<tr><td>D9055</td><td>Status latch execution step number</td><td>Status latch execution step number</td><td>• Stores the step number when status latch is executed.
• Stores the step number in a binary value if status latch is executed in a main sequence program.
• Stores the block number and the step number if status latch is executed in a SFC program.
 
</td><td>—</td><td>Usable with AnA, A2AS, AnU and QCPU-A (A Mode).</td></tr>
<tr><td>D9060</td><td>Software version</td><td>Software version of internal system</td><td>Stores the software version of the CPU module's internal system in ASCII codes.
Example: Stores "41H" for version A.
Note) The software version of the internal system may be different from the version marked on the housing.
＊5: This function is available with the CPU of the following S/W versions or later.
<table><tr><th>CPU Type Name</th><th>Software Version</th></tr><tr><td>A2ACPU(P21/R21), A2ACPU-S1(P21/R21)</td><td>S/W version W (Manufactured in July, 1998)</td></tr><tr><td>A3ACPU(P21/R21)</td><td>S/W version X (Manufactured in July, 1998)</td></tr><tr><td>A2UCPU(S1), A3UCPU, A4UCPU</td><td>S/W version H (Manufactured in July, 1998)</td></tr><tr><td>A1SJHCPU, A1SHCPU, A2SHCPU</td><td>S/W version H (Manufactured in May, 1998)</td></tr><tr><td>A2USCPU(S1)</td><td>S/W version Y (Manufactured in July, 1998)</td></tr><tr><td>A2USHCPU-S1</td><td>S/W version E (Manufactured in July, 1998)</td></tr></table></td><td>△</td><td>Can be used only with AnU, A2US, or AnSH ＊5</td></tr>
</table>

＊: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-ll Programming Manual.

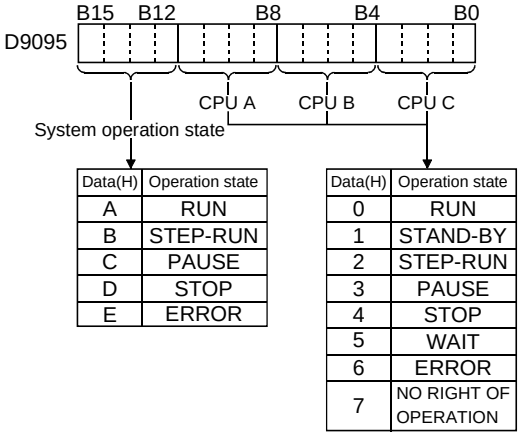
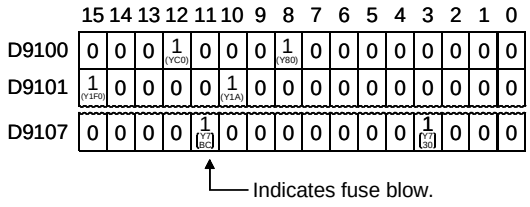
Special Register List (Continue)

Number	Name	Description	Details	Applicable CPU	
D9061	Communication error code	0: Normal 1: Initial data error 2: Line error	• Stores error code when M9061 is turned on (communication with I/O modules or remote terminal modules fails). • 1 ..... Total number of stations of I/O modules or remote terminal modules or number of retries is not normal. Initial program contains an error. • 2 ..... Cable breakage or power supply of I/O modules or remote terminal modules is turned off.	—	Usable with A2C and A52G.
D9068	Abnormal base module	Stores the bit pattern of the abnormal base module	Stores the bit pattern of the base module in abnormal condition. When basic base module is abnormal: Bit 0 turns ON. When 1st expansion base module is abnormal: Bit 1 turns ON. When 2nd expansion base module is abnormal: Bit 2 turns ON. ⋮ When 7th expansion base module is abnormal: Bit 7 turns ON.	—	Dedicated to QCPU-A (A Mode).
D9072	PC communication check	Data check by AJ71C24 (S3/S6/S8)	• In the loopback test mode of individual AJ71C24 (S3/S6/S8), the AJ71C24(S3/S6/S8) executes data write/read and communication check.	○	Usable with all types of CPUs.
D9075	Result of writing to standard ROM	Stores the status of writing to the standard ROM	Stores the status of writing to the standard ROM. 0: Writing enabled F1H: During RAM operation F2H: Writing to standard ROM disabled F3H: Failed to erase F4H: Failed to write FEH: Checking erasing FFH: During writing	—	Dedicated to QCPU-A (A Mode).
D9076	Status of writing to standard ROM	Stores the status of writing (enabled/disabled) to the standard ROM	Stores the status of writing (enabled/disabled) to the standard ROM. Statuses of DIP switch 3 and M9073 0: SW3 is OFF, M9073 is OFF/ON 1: SW3 is ON, M9073 is OFF 2: SW3 is ON, M9073 is ON	—	Dedicated to QCPU-A (A Mode).
D9077	Sequence accumulation time measurement	Accumulation time setting	• Stores the accumulation time used by M9077. Setting range: 1 to 255ms (Default: 5ms) * When the value other than 1 to 255 ms is designated, the value in D9077 is reset to 0.	—	Dedicated to QCPU-A (A Mode).

Special Register List (Continue)

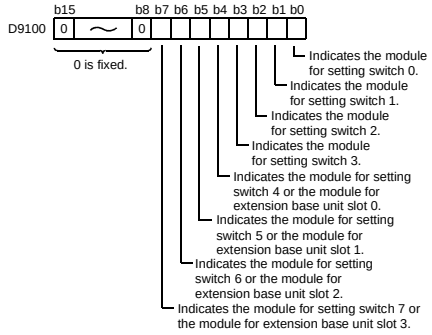
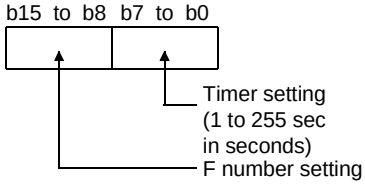
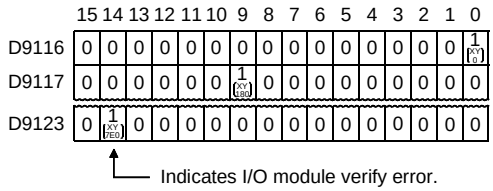
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9080</td><td>Number of executable CC-Link dedicated instructions</td><td>Stores the number of remaining CC-Link dedicated instructions being executable</td><td>Stores the number of remaining instructions (RIRD/RIWT/RISEND/RIRCV) being executable simultaneously at one scan.
(With QCUP-A or AnUCPU)
Number of remaining instructions being executable = 10 – Number of instructions executed simultaneously
(With AnSHCPU)
Number of remaining instructions being executable = 64 – Number of instructions executed simultaneously
＊6: This function is available with the CPU of the following S/W versions or later.
<table><tr><th>CPU Type Name</th><th>Software Version</th></tr><tr><td>Q02CPU-A, Q02HCPU-A, Q06HCPU-A</td><td rowspan="2">Available with all versions</td></tr><tr><td>A1SJHCPU, A1SHCPU, A2SHCPU</td></tr><tr><td>A2UCPU(S1), A3UCPU, A4UCPU</td><td>S/W version Q (Manufactured in July, 1999)</td></tr><tr><td>A2USCPU(S1)</td><td>S/W version E (Manufactured in July, 1999)</td></tr><tr><td>A2USHCPU-S1</td><td>S/W version L (Manufactured in July, 1999)</td></tr></table></td><td>△</td><td>Can be used only with AnU, A2US, QCPU-A (A Mode) or AnSH ＊6</td></tr>
<tr><td>D9081</td><td>Number of communication requests executed to remote terminal modules</td><td>0 to 32</td><td>• Stores the number of communication requests executed to remote terminal modules connected to AJ71PT32(S3), A2C and A52G.
• Subtracts 1 at completion of communication with a remote terminal module.</td><td>—</td><td>Usable with AnA, A2AS, QCPU-A (A Mode), AnU, A2C and A52G.</td></tr>
<tr><td>D9082</td><td>Final connected station number</td><td>Final connected station number</td><td>• Stores the final station number of I/O modules and remote terminal modules connected to A2C and A52G.</td><td>—</td><td>Usable with A2C and A52G.</td></tr>
<tr><td>D9085</td><td>Time check time</td><td>1 s to 65535 s</td><td>• Sets the time check time of the data link instructions (ZNRD, ZNWR) for the MELSECNET II.
• Setting range: 1 s to 65535 s (1 to 65535)
• Setting unit: 1 s
• Default value: 10 s (If 0 has been set, default 10 s is applied)</td><td>—</td><td>Usable with AnU, A2AS and QCPU-A (A Mode).</td></tr>
<tr><td>D9090</td><td>Microcomputer subroutine input data area head device number</td><td>Depends on the micro-computer program package to be used.</td><td>• For details, refer to the manual of each microcomputer program package.</td><td>△</td><td>Usable with AnA, A2AS, AnU and QCPU-A (A Mode).</td></tr>
<tr><td rowspan="3">D9091</td><td>Instruction error</td><td>Instruction error detail number</td><td>• Stores the detail code of cause of an instruction error.</td><td>—</td><td>Unusable with AnA, A2AS, AnU and QCPU-A (A Mode).</td></tr>
<tr><td>Microcomputer subroutine call error code</td><td>Depends on the micro-computer program package to be used.</td><td>• For details, refer to the manual of each microcomputer program package.</td><td>△</td><td>Unusable with AnA, A2AS, AnU and QCPU-A (A Mode).</td></tr>
<tr><td>SFC program detail error number</td><td>Detail error number of the error which occurr-ed in a SFC program</td><td>• Stores the detail error number of the error occurred in a SFC program in a binary value.</td><td>△</td><td>Unusable with AnA, A2AS, AnU and QCPU-A (A Mode).</td></tr>
<tr><td>＊2 ＊3
D9094</td><td>Changed I/O module head address</td><td>Changed I/O module head address</td><td>• Stores upper 2 digits of the head I/O address of I/O modules to be loaded or unloaded during online mode in BIN code.
Example) Input module X2F0 → H2F</td><td>—</td><td>Usable with AnN, A3V, AnA, A73, A2AS, AnU and QCPU-A (A Mode).</td></tr>
</table>

Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9095</td><td>Operation state of the A3VTS system and A3VCPU</td><td>Stores operation with 4 hexadecimal digits.</td><td>• Monitors operation state of the A3VTS system and the A3VCPU.
 
</td><td>—</td><td>Dedicated to A3V.</td></tr>
<tr><td>D9096</td><td>A3VCPU A Self-check error</td><td>Self-check error code</td><td>• Error code of self-check error on CPU A is stored in BIN code.
• Cleared when D9008 of CPU A is cleared.</td><td>—</td><td>Dedicated to A3V.</td></tr>
<tr><td>D9097</td><td>A3VCPU B Self-check error</td><td>Self-check error code</td><td>• Error code of self-check error on CPU B is stored in BIN code.
• Cleared when D9008 of CPU B is cleared.</td><td>—</td><td>Dedicated to A3V.</td></tr>
<tr><td>D9098</td><td>A3VCPU C Self-check error</td><td>Self-check error code</td><td>• Error code of self-check error on CPU C is stored in BIN code.
• Cleared when D9008 of CPU C is cleared.</td><td>—</td><td>Dedicated to A3V.</td></tr>
<tr><td>D9099</td><td>A3VTU Self-check error</td><td>Self-check error code</td><td>• Error code of self-check error on A3VTU is stored in BIN code.</td><td>—</td><td>Dedicated to A3V.</td></tr>
<tr><td>＊1 D9100
＊1 D9101
＊1 D9102
＊1 D9103
＊1 D9104
＊1 D9105
＊1 D9106
＊1 D9107</td><td>Fuse blown module</td><td>Bit pattern in units of 16 points of fuse blow modules</td><td>• Output module numbers (in units of 16 points), of which fuses have blown, are entered in bit pattern. (Preset output unit numbers when parameter setting has been performed.)
 

• Fuse blow check is executed also to the output module of remote I/O station.
(If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)</td><td>O</td><td>Usable with all types of CPUs
(Only remote I/O station information is valid for A2C.)</td></tr>
</table>

Special Register List (Continue)

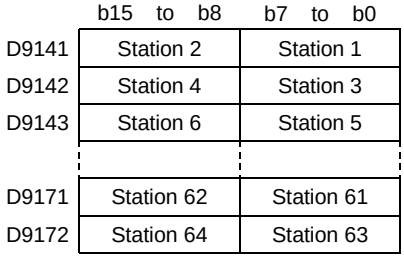
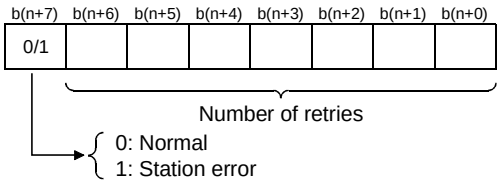
Number	Name	Description	Details	Applicable CPU	
＊1 D9100	Fuse blow module	Fuse blow module bit pattern	• Stores the output module number of the fuses have blown in the bit pattern. 	—	Dedicated to A0J2H.
＊2 D9108 ＊2 D9109 ＊2 D9110 ＊2 D9111 ＊2 D9112 ＊2 D9113 ＊2 D9114	Step transfer monitoring timer setting	Timer setting value and the F number at time out	• Sets value for the step transfer monitoring timer and the number of F which turns on when the monitoring timer timed out.  (By turning on any of M9108 to M9114, the monitoring timer starts. If the transfer condition following a step which corresponds to the timer is not established within set time, set annunciator (F) is tuned on.	—	Usable with AnN＊, AnA＊, AnU, A2AS, QCPU-A (A Mode), A2C, A0J2H, AnS, AnSH, A1FX and A52G
＊1 D9116 ＊1 D9117 ＊1 D9118 ＊1 D9119 ＊1 D9120 ＊1 D9121 ＊1 D9122 ＊1 D9123	I/O module verify error	Bit pattern in units of 16 points of verify error units	• When I/O modules, of which data are different from those entered at power-on, have been detected, the I/O unit numbers (in units of 16 points) are entered in bit pattern. (Preset I/O unit numbers when parameter setting has been performed.)  • I/O module verify check is executed also to remote I/O station modules. (If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)	○	Usable with all types of CPUs (Only remote I/O station information is valid for A2C.)
D9124	Annunciator detection quantity	Annunciator detection quantity	• When one of F0 to 255 (F0 to 2047 for AuA and AnU) is turned on by SET F 1 is added to the contents of D9124. When RST F or LEDR instruction is executed, 1 is subtracted from the contents of D9124. (If the INDICATOR RESET switch is provided to the CPU, pressing the switch can execute the same processing.) • Quantity, which has been turned on by SET F is stored into D9124 in BIN code. The value of D9124 is maximum 8.	○	Usable with all types of CPUs.

＊: Usable with AnN and AnA which are compatible with SFC.
For the AnN and AnA which are compatible with SFC, refer to the MELSAP-ll Programming Manual.

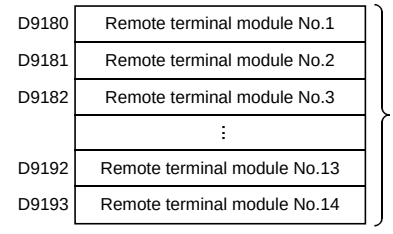
Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9125
D9126
D9127
D9128
D9129
D9130
D9131
D9132</td><td>Annunciator detection number</td><td>Annunciator detection number</td><td>• When one of F0 to 255 (F0 to 2047 for AuA and AnU) is turned on by SET F, F number, which has turned on, is entered into D9125 to D9132 in due order in BIN code.
• F number, which has been turned off by RST F, is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the preceding data registers.
• By executing LEDR instruction, the contents of D9125 to D9132 are shifted upward by one. (For A3N, A3HCPU, it can be performed by use of INDICATOR RESET switch on front of CPU module.)
• When there are 8 annunciator detections, the 9th one is not stored into D9125 to 9132 even if detected.
<table>
<tr><th></th><th>SET F50</th><th>SET F25</th><th>SET F99</th><th>RST F25</th><th>SET F15</th><th>SET F70</th><th>SET F65</th><th>SET F38</th><th>SET F110</th><th>SET F151</th><th>SET F210</th><th>LEDR</th><th></th></tr>
<tr><td>D9009</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td></tr>
<tr><td>D9124</td><td>0</td><td>1</td><td>2</td><td>3</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>8</td><td>8</td></tr>
<tr><td>D9125</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td></tr>
<tr><td>D9126</td><td>0</td><td>0</td><td>25</td><td>25</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>15</td></tr>
<tr><td>D9127</td><td>0</td><td>0</td><td>0</td><td>99</td><td>0</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>70</td></tr>
<tr><td>D9128</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>65</td></tr>
<tr><td>D9129</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>65</td><td>65</td><td>65</td><td>65</td><td>65</td><td>38</td></tr>
<tr><td>D9130</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>38</td><td>38</td><td>38</td><td>38</td><td>110</td></tr>
<tr><td>D9131</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>110</td><td>110</td><td>110</td><td>151</td></tr>
<tr><td>D9132</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>151</td><td>151</td><td>210</td></tr>
</table></td><td>○</td><td>Usable with all types of CPUs</td></tr>
<tr><td>D9133
D9134
D9135
D9136
D9137
D9138
D9139
D9140</td><td>Remote terminal card information</td><td>00: No I/O module or remote terminal module or initial communication impossible
01: Input module or remote terminal module
10: Output module</td><td>• Stores information of I/O modules and remote terminal modules connected to the A2C and A52G corresponding to station number.
• Information of I/O modules and remote terminal modules is for input, output and remote terminal module identification and expressed as 2-bit data.
00: No I/O module or remote terminal module or initial communication is impossible.
01: Input module or remote terminal module
10: Output module
• Data configuration
<table>
<tr><th></th><th>b15 b14</th><th>b13 b12</th><th>b11 b10</th><th>b9 b8</th><th>b7 b6</th><th>b5 b4</th><th>b3 b2</th><th>b1 b0</th></tr>
<tr><td>D9133</td><td>Station 8</td><td>Station 7</td><td>Station 6</td><td>Station 5</td><td>Station 4</td><td>Station 3</td><td>Station 2</td><td>Station 1</td></tr>
<tr><td></td><td>Station 16</td><td>Station 15</td><td>Station 14</td><td>Station 13</td><td>Station 12</td><td>Station 11</td><td>Station 10</td><td>Station 9</td></tr>
<tr><td></td><td>Station</td><td>Station</td><td>Station</td><td>Station</td><td>Station 20</td><td>Station 19</td><td>Station 18</td><td>Station</td></tr>
<tr><td></td><td>Station 56</td><td>Station 55</td><td>Station 54</td><td>Station 53</td><td>Station 52</td><td>Station 51</td><td>Station 50</td><td>Station 49</td></tr>
<tr><td>D9140</td><td>Station 64</td><td>Station 63</td><td>Station 62</td><td>Station 61</td><td>Station 60</td><td>Station 59</td><td>Station 58</td><td>Station 57</td></tr>
</table></td><td></td><td>Usable with A2C and A52G</td></tr>
</table>

Special Register List (Continue)

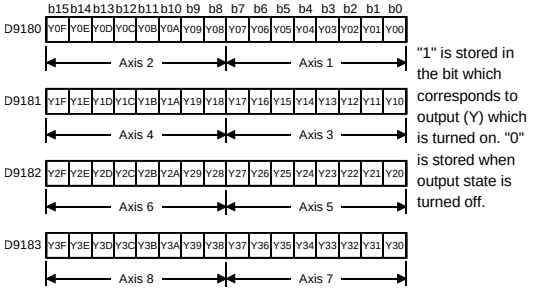
Number	Name	Description	Details	Applicable CPU	
D9141 D9142 D9143 D9144 D9145 D9146 D9147 D9148 D9149 D9150 D9151 D9152 D9153 D9154 D9155 D9156 D9157 D9158 D9159 D9160 D9161 D9162 D9163 D9164 D9165 D9166 D9167 D9168 D9169 D9170 D9171 D9172	Number of times of retry execution	Number of retries	• Stores the number of retries executed to I/O modules or remote terminal modules which caused communication error. (Retry processing is executed the number of times set at D9174.) • Data becomes 0 when communication is restored to normal. • Station number setting of I/O modules and remote terminal modules is as shown below.  • Retry counter uses 8 bits for one station.  * "n" is determined by station number of I/O module or remote terminal module. Odd number stations: b0 to b7 (n = 0) Even number stations: b8 to b15 (n = 8)	—	Usable with A2C and A52G.

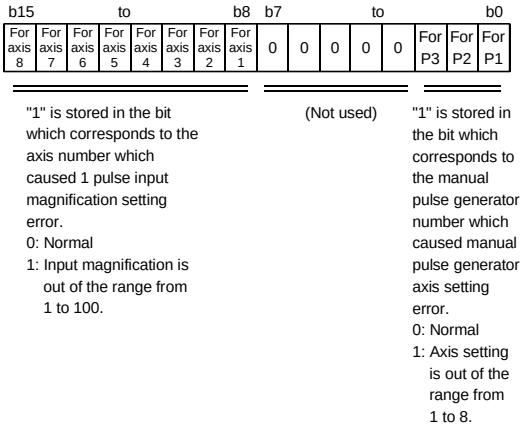
Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th colspan="3">Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td rowspan="4">D9173</td><td rowspan="4">Mode setting</td><td rowspan="4">0: Automatic online return enabled
1: Automatic online return disabled
2: Transmission stop at online error
3: Line check</td><td colspan="3">Mode setting</td><td rowspan="4">—</td><td rowspan="4">Usable with A2C and A52G.</td></tr>
<tr><td>0</td><td>Auto-matic online return enabled</td><td>• When an I/O module or a remote terminal module caused communication error, the station is placed offline.
• Communication with normal stations is continued.
• When a faulty station returned to normal, it is placed online.</td></tr>
<tr><td>1</td><td>Auto-matic online return disabled</td><td>• When an I/O module or a remote terminal module caused communication error, the station is placed offline.
• Communication with normal stations is continued.
• Though a faulty station returned to normal, communication is not restored unless the station module is restarted.</td></tr>
<tr><td>2</td><td>Trans-mission stop at online error</td><td>• When an I/O module or a remote terminal module caused communication error, communication with all stations is stopped.
• Though a faulty station returned to normal, communication is not restored unless the station module is restarted.</td></tr>
<tr><td>D9174</td><td>Setting of the number of retries</td><td>Number of retries</td><td colspan="3">• Sets the number of retries executed to I/O modules and remote terminal modules which caused communication error.
• Set for 5 times at power on.
• Set range: 0 to 32
• If communication with an I/O module or a remote terminal module is not restored to normal after set number of retries, such module is regarded as a faulty station.</td><td>—</td><td>Usable with A2C and A52G.</td></tr>
<tr><td>D9175</td><td>Line error retry counter</td><td>Number of retries</td><td colspan="3">• Stores the number of retries executed at line error (time out).
• Data becomes 0 when line is restored to normal and communication with I/O modules and remote terminal modules is resumed.</td><td>—</td><td>Usable with A2C and A52G.</td></tr>
<tr><td>D9180
D9181
D9182
D9183
D9184
D9185
D9186
D9187
D9188
D9189
D9190
D9191
D9192
D9193</td><td>Remote terminal module error number</td><td></td><td colspan="3">• Stores error code of a faulty remote terminal module when M9060 is turned on.
• The error code storage areas for each remote terminal module are as shown below.
 

• Error code is cleared in the following cases.
When the RUN key switch is moved from STOP to RUN.
(D9180 to D9183 are all cleared.)
When Yn4 of each remote terminal is set from OFF to ON.</td><td>—</td><td>Usable with A2C and A52G.</td></tr>
</table>

Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9180</td><td>Limit switch output state torage areas for axes 1 and 2</td><td rowspan="4">Bit pattern of limit switch function output state</td><td rowspan="4">• Stores output state of limit switch function.
 

"1" is stored in the bit which corresponds to output (Y) which is turned on. "0" is stored when output state is turned off.</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9181</td><td>Limit switch output state storage areas for axes 3 and 4</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9182</td><td>Limit switch output state storage areas for axes 5 and 6</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9183</td><td>Limit switch output state storage areas for axes 7 and 8</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9184</td><td>Cause of PCPU error</td><td>PCPU error code</td><td>• Stores error codes occurred at the PCPU in BIN code.
0: Normal
1: A73CPU hardware error
2: PCPU error
10: A70AF error
11: A70MDF error
12: A70MDF error
13: AY42 error</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9185</td><td>Servo amplifier connection data</td><td>Bit pattern of servo amplifier connection state</td><td>• Servo amplifier connection state is checked and the result is stored in the bit which corresponds to each axis number.
Connection state is continuously checked. Axes which changed from disconnected state to connected state are regarded as connected. But, axes which changed from connected state to disconnected state are still regarded as connected.
 
</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9187</td><td>Manual pulse generator axis setting error</td><td>Manual pulse generator axis setting error code</td><td>• Stores error code when the manual pulse generator axis setting error flag (M9077) is set in the bit each corresponds to each axis number.
 
</td><td>—</td><td>Dedicated to A73.</td></tr>
</table>

Special Register List (Continue)

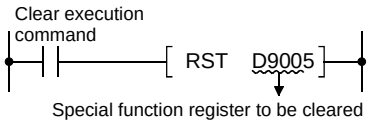
<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th><th colspan="2">Applicable CPU</th></tr>
<tr><td>D9188</td><td>Starting axis number at test mode request error</td><td>Starting axis number</td><td>• Stores axis number in the bit which corresponds to the axis which was running when a test mode request was given and test mode request error occurred.
b15 to b8 b7 to b0
0 0 0 0 0 0 0 0 | For axis 8 | For axis 7 | For axis 6 | For axis 5 | For axis 4 | For axis 3 | For axis 2 | For axis 1
(Not used)
"1" is stored when running.
"0" is stored when not running.</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9189</td><td>Error program number</td><td>Error program number</td><td>• Stores error servo program number (0 to 4095) when the servo program setting error flag (M9079) is set.</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9190</td><td>Data setting error</td><td>Data setting error number</td><td>• Stores error code which corresponds to the error setting item when the servo program setting error flag (M9079) is set.</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9191</td><td>Servo amplifier type</td><td>Bit pattern of the axis connected to a general-purpose servo amplifier</td><td>• Stores type of connected servo amplifier in the bit which corresponds to each axis number.
0: MR-SB is connected or not connected.
1: General-purpose servo amplifier is connected.
b15 to b8 b7 to b0
0 0 0 0 0 0 0 0 | For axis 8 | For axis 7 | For axis 6 | For axis 5 | For axis 4 | For axis 3 | For axis 2 | For axis 1
All 0
Type of servo amplifier set at each axis is stored with "0" or "1".</td><td>—</td><td>Dedicated to A73.</td></tr>
<tr><td>D9196
D9197
D9198
D9199</td><td>Faulty station detection</td><td>Bit pattern of the faulty station</td><td>• Bit which corresponds to faulty I/O module or remote terminal module is set (1).
(Bit which corresponds to a faulty station is set when normal communication cannot be restored after executing the number of retries set at D9174.)
• If automatic online return is enabled, bit which corresponds to a faulty station is reset (0) when the station is restored to normal.
• Data configuration
Address | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0
D9196 | Stasion 16 | Stasion 15 | Stasion 14 | Stasion 13 | Stasion 12 | Stasion 11 | Stasion 10 | Stasion 9 | Stasion 8 | Stasion 7 | Stasion 6 | Stasion 5 | Stasion 4 | Stasion 3 | Stasion 2 | Stasion 1
D9197 | Stasion 32 | Stasion 31 | Stasion 30 | Stasion 29 | Stasion 28 | Stasion 27 | Stasion 26 | Stasion 25 | Stasion 24 | Stasion 23 | Stasion 22 | Stasion 21 | Stasion 20 | Stasion 19 | Stasion 18 | Stasion 17
D9198 | Stasion 48 | Stasion 47 | Stasion 46 | Stasion 45 | Stasion 44 | Stasion 43 | Stasion 42 | Stasion 41 | Stasion 40 | Stasion 39 | Stasion 38 | Stasion 37 | Stasion 36 | Stasion 35 | Stasion 34 | Stasion 33
D9199 | Stasion 64 | Stasion 63 | Stasion 62 | Stasion 61 | Stasion 60 | Stasion 59 | Stasion 58 | Stasion 57 | Stasion 56 | Stasion 55 | Stasion 54 | Stasion 53 | Stasion 52 | Stasion 51 | Stasion 50 | Stasion 49
1: Error
0: Normal</td><td>—</td><td>Usable with A2C and A52G.</td></tr>
</table>

POINTS

(1) Special registers are cleared when the PC is switched off or the RESET switch is set to LATCH CLEAR or RESET. Data remains unchanged when the RUN key switch is set to STOP.

(2) Special registers marked ＊1 above are latched and their data will remain unchanged after normal status is restored.

(a) Method by user program
Insert the circuit shown at right into the program and turn on the clear execution command contact to clear the contents of register.



(b) Method by peripheral equipment
Set the register to "0" by changing the present value by the test function of peripheral equipment or set to "0" by forced reset. For the operation procedure, refer to the Instruction Manual for peripheral equipment.

(c) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

(3) Data is written to special registers marked ＊2 above in the sequence program.

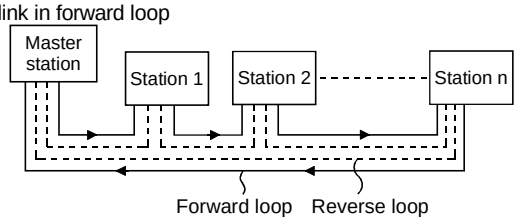
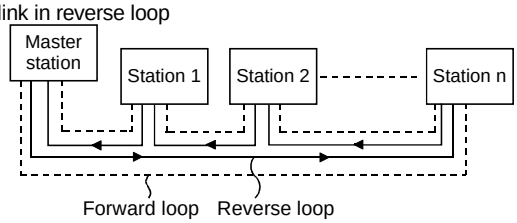
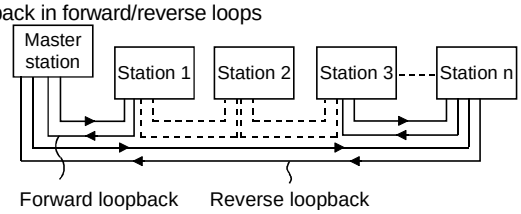
(4) Data is written to special registers marked ＊3 above in test mode of the peripheral equipment.

Appendix 2.4 Special registers for link

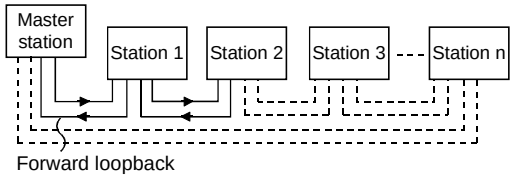
The link special register stores the result of any error, etc. which may occur during data communication as a numeric value.
By monitoring the link special register, any station number with an error or fault diagnosis can be read.
These special registers are applicable to all types of CPUs except the A3V.
For description of the special registers for link for the A3V, refer to the A3VTS Data Link System User's Manual.

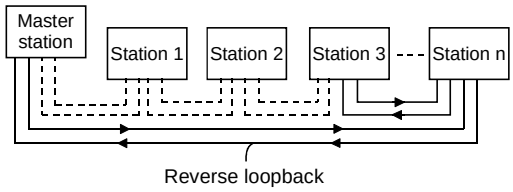
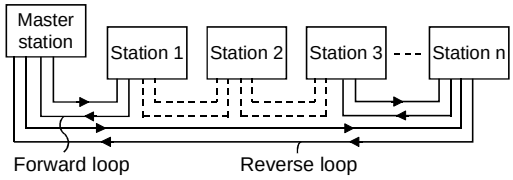
(1) Link special registers only valid when the host station is the master station

Link special Register

Number	Name	Description	Details
D9200	LRDP processing result	0: Normal 2: LRDP instruction setting fault 3: Corresponding station error 4: LRDP cannot be executed in the corresponding station	Stores the execution result of the LRDP (word device read) instruction • LRDP instruction setting fault: Faulty setting of the LRDP instruction constant, source, and/or destination • Corresponding station error: One of the stations is not communicating. • LRDP cannot be executed in the corresponding station: The specified station is a remote I/O station.
D9201	LWTP processing result	0: Normal 2: LWTP instruction setting fault 3: Corresponding station error 4: LWTP cannot be executed in the corresponding station	Stores the execution result of the LWTP (word device write) instruction. • LWTP instruction setting fault: Faulty setting of the LWTP instruction constant, source, and/or destination. • Corresponding station error: One of the stations is not communicating. • LWTP cannot be executed in the corresponding station: The specified station is a remote I/O station.
D9204 (Continue)	Link status	0: Data link in forward loop 1: Data link in reverse loop 2: Loopback in forward/reverse direction 3: Loopback in forward direction 4: Loopback in reverse direction 5: Data link impossible	Stores the present path status of the data link. • Data link in forward loop  • Data link in reverse loop  • Loopback in forward/reverse loops 

Link Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th></tr>
<tr><td>D9204</td><td>Link status</td><td></td><td>• Loopback in forward loop only
 

• Loopback in reverse loop only
 
</td></tr>
<tr><td>D9205</td><td>Loopback executing station</td><td>Station executing forward loopback</td><td rowspan="2">Stores the local or remote I/O station number at which loopback is being executed.
 

In the above example, 1 is stored into D9205 and 3 into D9206. If data link returns to normal status (data link in forward loop), values in D9205 and D9206 remain 1 and 3. Reset using sequence program or the RESET key.</td></tr>
<tr><td>D9206</td><td>Loopack executing station</td><td>Station executing reverse loopback</td></tr>
<tr><td>D9207</td><td>Link scan time</td><td>Maximum value</td><td rowspan="3">Stores the data link processing time with all local and remote I/O stations.
• Input (X) , output (Y) , link relay (B) , and link register (W) assigned in link parameters communicate with the corresponding stations every link scan.
• Link scan is a period of time during which data link is executed with all connected slave stations, independently of the sequence program scan time</td></tr>
<tr><td>D9208</td><td>Link scan time</td><td>Minimum value</td></tr>
<tr><td>D9209</td><td>Link scan time</td><td>Present value</td></tr>
<tr><td>D9210</td><td>Retry count</td><td>Total number stored</td><td>Stores the number of retry times due to transmission error.
Count stops at maximum of "FFFFH" .
RESET to return the count to 0.</td></tr>
<tr><td>D9211</td><td>Loop switching count</td><td>Total number stored</td><td>Stores the number of times the loop line has been switched to reverse loop or loopback.
Count stops at maximum of "FFFFH".
RESET to return the count to 0.</td></tr>
</table>

Link Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th></tr>
<tr><td>D9212</td><td>Local station operating status</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local station numbers which are in STOP or PAUSE mode.
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9212</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9213</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9214</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9215</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>When a local station is switched to STOP or PAUSE mode, the bit corresponding to the station number in the register becomes "1" .
Example : When station 7 switches to STOP mode, bit 6 in D9212 becomes "1" , and when D9212 is monitored, its value is "64 (40H) " .</td></tr>
<tr><td>D9213</td><td>Local station operating status</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9214</td><td>Local station operating status</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9215</td><td>Local station operating status</td><td>Stores the status of stations 49 to 64</td></tr>
<tr><td>D9216</td><td>Local station error detection</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local station numbers which are in error.
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9216</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9217</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9218</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9219</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>If a local station detects an error, the bit corresponding to the station number becomes "1".
Example : When station 6 and 12 detect an error, bits 5 and 11 in D9216 become "1", and when D9216 is monitored, its value is "2080 (820H)".</td></tr>
<tr><td>D9217</td><td>Local station error detection</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9218</td><td>Local station error detection</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9219</td><td>Local station error detection</td><td>Stores the status of stations 49 to 64</td></tr>
<tr><td>D9220</td><td>Local station parameter mismatched or remote station I/O assignment error</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local station numbers which contain mismatched parameters or of remote station numbers for which incorrect I/O assignment has been made.
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9220</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9221</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9222</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9223</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>If a local station acting as the master station of tier three detects a parameter error or a remote station contains an invalid I/O assignment, the bit corresponding to the station number becomes "1" .
Example: When local station 5 and remote I/O station 14 detect an error, bits 4 and 13 in D9220 become "1" , and when D9220 is monitored, its value is "8208 (2010H) " .</td></tr>
<tr><td>D9221</td><td>Local station parameter mismatched or remote station I/O assignment error</td><td>Stores the status of stations 17 to 32.</td></tr>
<tr><td>D9222</td><td>Local station parameter mismatched or remote station I/O assignment error</td><td>Stores the status of stations 33 to 48.</td></tr>
<tr><td>D9223</td><td>Local station parameter mismatched or remote station I/O assignment error</td><td>Stores the status of stations 49 to 64.</td></tr>
</table>

Link Special Register List (Continue)

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th></tr>
<tr><td>D9224</td><td>Initial communication between local or remote I/O stations</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local or remote station numbers while they are communicating the initial data with their relevant master station.
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9224</td><td>L/R 16</td><td>L/R 15</td><td>L/R 14</td><td>L/R 13</td><td>L/R 12</td><td>L/R 11</td><td>L/R 10</td><td>L/R 9</td><td>L/R 8</td><td>L/R 7</td><td>L/R 6</td><td>L/R 5</td><td>L/R 4</td><td>L/R 3</td><td>L/R 2</td><td>L/R 1</td></tr><tr><td>D9225</td><td>L/R 32</td><td>L/R 31</td><td>L/R 30</td><td>L/R 29</td><td>L/R 28</td><td>L/R 27</td><td>L/R 26</td><td>L/R 25</td><td>L/R 24</td><td>L/R 23</td><td>L/R 22</td><td>L/R 21</td><td>L/R 20</td><td>L/R 19</td><td>L/R 18</td><td>L/R 17</td></tr><tr><td>D9226</td><td>L/R 48</td><td>L/R 47</td><td>L/R 46</td><td>L/R 45</td><td>L/R 44</td><td>L/R 43</td><td>L/R 42</td><td>L/R 41</td><td>L/R 40</td><td>L/R 39</td><td>L/R 38</td><td>L/R 37</td><td>L/R 36</td><td>L/R 35</td><td>L/R 34</td><td>L/R 33</td></tr><tr><td>D9227</td><td>L/R 64</td><td>L/R 63</td><td>L/R 62</td><td>L/R 61</td><td>L/R 60</td><td>L/R 59</td><td>L/R 58</td><td>L/R 57</td><td>L/R 56</td><td>L/R 55</td><td>L/R 54</td><td>L/R 53</td><td>L/R 52</td><td>L/R 51</td><td>L/R 50</td><td>L/R 49</td></tr></table>The bit corresponding to the station number which is currently communicating the initial settings becomes "1" .
Example: When stations 23 and 45 are communicating, bit 6 of D9225 and bit 12 of D9226 become "1", and when D9225 is monitored, its value is "64 (40H)", and when D9226 is monitored, its value is "4096 (1000H)"</td></tr>
<tr><td>D9225</td><td>Initial communication between local or remote I/O stations</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9226</td><td>Initial communication between local or remote I/O stations</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9227</td><td>Initial communication between local or remote I/O stations</td><td>Stores the status of stations 49 to 64</td></tr>
<tr><td>D9228</td><td>Local or remote I/O station error</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local or remote station numbers which are in error.
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9228</td><td>L/R 16</td><td>L/R 15</td><td>L/R 14</td><td>L/R 13</td><td>L/R 12</td><td>L/R 11</td><td>L/R 10</td><td>L/R 9</td><td>L/R 8</td><td>L/R 7</td><td>L/R 6</td><td>L/R 5</td><td>L/R 4</td><td>L/R 3</td><td>L/R 2</td><td>L/R 1</td></tr><tr><td>D9229</td><td>L/R 32</td><td>L/R 31</td><td>L/R 30</td><td>L/R 29</td><td>L/R 28</td><td>L/R 27</td><td>L/R 26</td><td>L/R 25</td><td>L/R 24</td><td>L/R 23</td><td>L/R 22</td><td>L/R 21</td><td>L/R 20</td><td>L/R 19</td><td>L/R 18</td><td>L/R 17</td></tr><tr><td>D9230</td><td>L/R 48</td><td>L/R 47</td><td>L/R 46</td><td>L/R 45</td><td>L/R 44</td><td>L/R 43</td><td>L/R 42</td><td>L/R 41</td><td>L/R 40</td><td>L/R 39</td><td>L/R 38</td><td>L/R 37</td><td>L/R 36</td><td>L/R 35</td><td>L/R 34</td><td>L/R 33</td></tr><tr><td>D9231</td><td>L/R 64</td><td>L/R 63</td><td>L/R 62</td><td>L/R 61</td><td>L/R 60</td><td>L/R 59</td><td>L/R 58</td><td>L/R 57</td><td>L/R 56</td><td>L/R 55</td><td>L/R 54</td><td>L/R 53</td><td>L/R 52</td><td>L/R 51</td><td>L/R 50</td><td>L/R 49</td></tr></table>The bit corresponding to the station number with the error becomes "1"
Example: When local station 3 and remote I/O station 14 have an error, bits 2 and 13 of D9228 become "1", and when D9228 is monitored, its value is "8196 (2004H)".</td></tr>
<tr><td>D9229</td><td>Local or remote I/O station error</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9230</td><td>Local or remote I/O station error</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9231</td><td>Local or remote I/O station error</td><td>Stores the status of stations 49 to 64</td></tr>
<tr><td>D9232</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 1 to 8.</td><td rowspan="8">Stores the local or remote station number at which a forward or reverse loop error has occurred
<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>D9232</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R8</td><td colspan="2">L/R7</td><td colspan="2">L/R6</td><td colspan="2">L/R5</td><td colspan="2">L/R4</td><td colspan="2">L/R3</td><td colspan="2">L/R2</td><td colspan="2">L/R1</td></tr><tr><td>D9233</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R16</td><td colspan="2">L/R15</td><td colspan="2">L/R14</td><td colspan="2">L/R13</td><td colspan="2">L/R12</td><td colspan="2">L/R11</td><td colspan="2">L/R10</td><td colspan="2">L/R9</td></tr><tr><td>D9234</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R24</td><td colspan="2">L/R23</td><td colspan="2">L/R22</td><td colspan="2">L/R21</td><td colspan="2">L/R20</td><td colspan="2">L/R19</td><td colspan="2">L/R18</td><td colspan="2">L/R17</td></tr><tr><td>D9235</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R32</td><td colspan="2">L/R31</td><td colspan="2">L/R30</td><td colspan="2">L/R29</td><td colspan="2">L/R28</td><td colspan="2">L/R27</td><td colspan="2">L/R26</td><td colspan="2">L/R25</td></tr><tr><td>D9236</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R40</td><td colspan="2">L/R39</td><td colspan="2">L/R38</td><td colspan="2">L/R37</td><td colspan="2">L/R36</td><td colspan="2">L/R35</td><td colspan="2">L/R34</td><td colspan="2">L/R33</td></tr><tr><td>D9237</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R48</td><td colspan="2">L/R47</td><td colspan="2">L/R46</td><td colspan="2">L/R45</td><td colspan="2">L/R44</td><td colspan="2">L/R43</td><td colspan="2">L/R42</td><td colspan="2">L/R41</td></tr><tr><td>D9238</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R56</td><td colspan="2">L/R55</td><td colspan="2">L/R54</td><td colspan="2">L/R53</td><td colspan="2">L/R52</td><td colspan="2">L/R51</td><td colspan="2">L/R50</td><td colspan="2">L/R49</td></tr><tr><td>D9239</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td colspan="2">L/R64</td><td colspan="2">L/R63</td><td colspan="2">L/R62</td><td colspan="2">L/R61</td><td colspan="2">L/R60</td><td colspan="2">L/R59</td><td colspan="2">L/R58</td><td colspan="2">L/R57</td></tr></table>In the above table, "F" indicates a forward loop line and "R" a reverse loop line .The bit corresponding to the station number at which the forward or reverse loop error has occurred, becomes "1"
Example: When the forward loop line of station 5 has an error, bit 8 of D9232 become "1" , and when D9232 is monitored, its value is "256 (100H)" .</td></tr>
<tr><td>D9233</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 9 to 16</td></tr>
<tr><td>D9234</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 17 to 24</td></tr>
<tr><td>D9235</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 25 to 32</td></tr>
<tr><td>D9236</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 33 to 40</td></tr>
<tr><td>D9237</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 41to 48</td></tr>
<tr><td>D9238</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 49 to 56</td></tr>
<tr><td>D9239</td><td>Local or remote I/O station loop error</td><td>Stores the status of stations 57 to 64</td></tr>
<tr><td>D9240</td><td>Number of receive error detection times</td><td>Total number stored</td><td>Stores the number of times the following transmission errors have been detected:
CRC, OVER, AB. IF
Count is made to a maximum of FFFFH. RESET to return the count to 0.</td></tr>
</table>

(2) Link special registers only valid when the host station is a local station

Link Special Register List

<table>
<tr><th>Number</th><th>Name</th><th>Description</th><th>Details</th></tr>
<tr><td>D9243</td><td>Own station number check</td><td>Stores a station number. (0 to 64)</td><td>Allows a local station to confirm its own station number</td></tr>
<tr><td>D9244</td><td>Total number of slave stations</td><td>Stores the number of slave station</td><td>Indicates the number of slave stations in one loop.</td></tr>
<tr><td>D9245</td><td>Number of receive error detection times</td><td>Total number stored</td><td>Stores the number of times the following transmission errors have been detected: CRC, OVER, AB. IF
Count is made to a maximum of FFFFH. RESET to return the count to 0.</td></tr>
<tr><td>D9248</td><td>Local station operating status</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local station number which is in STOP or PAUSE mode.
<table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9248</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9249</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9250</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9251</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>The bit corresponding to the station number which is in STOP or PAUSE mode, becomes "1" .
Example: When local stations 7 and 15 are in STOP mode, bits 6 and 14 of D9248 become "1" , and when D9248 is monitored, its value is "16448 (4040H)" .</td></tr>
<tr><td>D9249</td><td>Local station operating status</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9250</td><td>Local station operating status</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9251</td><td>Local station operating status</td><td>Stores the status of stations 49 to 64</td></tr>
<tr><td>D9252</td><td>Local station error</td><td>Stores the status of stations 1 to 16</td><td rowspan="4">Stores the local station number other than the host, which is in error.
<table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>D9252</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>D9253</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>D9254</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>D9255</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>The bit corresponding to the station number which is in error, becomes "1" .
Example: When local station 12 is in error, bit 11 of D9252 becomes "1" , and when D9252 is monitored, its value is "2048 (800H) " .</td></tr>
<tr><td>D9253</td><td>Local station error</td><td>Stores the status of stations 17 to 32</td></tr>
<tr><td>D9254</td><td>Local station error</td><td>Stores the status of stations 33 to 48</td></tr>
<tr><td>D9255</td><td>Local station error</td><td>Stores the status of stations 49 to 64</td></tr>
</table>

Appendix 3 Peripheral Devices

(1) The following table shows whether the peripheral devices and system FD which are used by the conventional system can be used or not.

Model Name of the Peripheral Device	Model Name of the Software Package	Usable or Not	Usable Range	Model Name of the PC at the Startup
A6GPP/A6PHP	SW4GP-GPPAA	Usable	Device range of A3ACPU	A3A
	SW3GP-GPPA	Usable	Device range of A3HCPU	A3H
	Prior to SW2 -type	Not usable	————	————
A6HGP	SW3-HGPA	Usable	Device range of A3HCPU	A3H
	Prior to SW2 -type	Not usable	————	————
A8PU	————	Usable	Device range of A3ACPU	A2USH (displayed at the startup)
A7PU A7PUS	————	Usable	Device range of A3HCPU	A2USH (displayed at the startup)
A6WU	Software version "E" or later	Usable	Device range of A3ACPU	————
	Software version "D" or earlier	Not usable	————	————

(2) The compatibility of the conventional products (existing system products) and the new products (AnU-compatible products) are listed in the following table.

No.	Product Used to Write to the CPU	Product Used to Read from the CPU	Compatible
1	Conventional product (PC: A3A startup)	New Product (PC: A3A startup)	• All the data is compatible.
2	New Product (PC: A3A startup)	Conventional product (PC: A3A startup)	
3	Conventional product (PC: A3A startup)	New Product (PC: A3U startup)	• Because the model names of the PCs for write and read are different, the following things apply. 1 When the verification is executed after the readout, the verification fails. (The data is usable.) 2 The setting values (data stored in the CPU) of the sampling trace/status latch cannot be displayed. 3 When the network parameters are set in the new product, they cannot be displayed on the conventional product.
4	New Product (PC: A3U startup)	Conventional product (PC: A3A startup)	

POINT

Do not execute readout and the following operations to a conventional product from the QCPU-A in which the MELSECNET/10 network parameters have been set by the new product, because "LINK PARA.ERROR" (CPU error) will occur:

(a) Modifying and writing in the main sequence program area (memory capacity).

(b) Writing the readout parameters to another QCPU-A in the network system.

Appendix 4 Precautions When the Existing Sequence Programs Are Diverted for the QCPU-A

The precautions for diverting the sequence programs created for the A1SCPU and A2SCPU for the QCPU-A are explained.
The sequence programs created for the A2USCPU(S1) can directly be used for the QCPU-A.

POINTS

(1) The following three instructions created exclusively for the AnUCPU can be used by adding to the existing sequence program.
ZNWR instruction ····· For writing to word devices of the stations connected to the MELSECNET/10
ZNRD instruction ····· For reading from word devices of the stations connected to the MELSECNET/10
ZCOM instruction ····· MELSECNET/10 network refresh instruction

(2) All of the sequence programs for the A1SCPU and A2SCPU can be used.

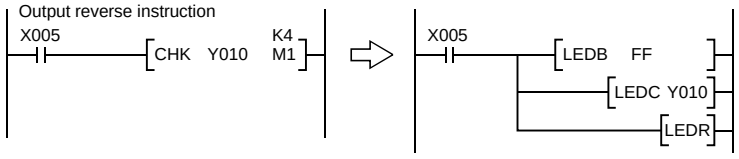
(3) The following instructions cannot be used by the QCPU-A as they cannot be used by the A2USCPU(S1). Please note, however, that the handling is different between the A2USCPU(S1) and QCPU-A when they are used mistakenly.

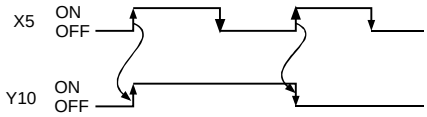
Item	QCPU-A, Q2USHCPU-S1	A2USCPU(S1)
LED, LEDC instruction	No error occurs.	"INSTRCT CODE ERR." occurs.
CHG instruction	Error code 13 occurs.	Error code 10 occurs.

Appendix 4.1 Instructions with different specifications

Modifications to the sequence program to use the instructions of different specifications are explained.
Basically, the instructions which are not listed in this section do not require modifications.

(1) CHK instruction.....Modifications are necessary when the A1SCPU and A2SCPU are used in the refresh method.

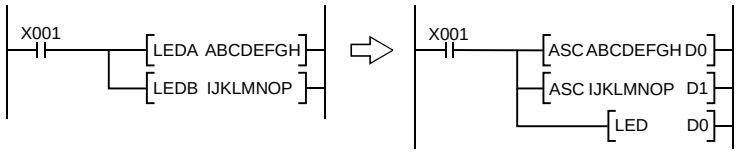




(2) DI/EI instruction.....Modifications are necessary when the special relay M9053 is ON.

- Enable and disable (EI, DI) of the link refresh is executable when M9053 is turned ON.
- Because the QCPU-A executes the link refresh by the END processing, the link refresh cannot be enabled and disabled while the sequence program is being executed.
- Modify the sequence program.

(3) LEDA/LEDB instruction



(4) SUB, SUBP instruction.....Unusable

- The SUB instruction cannot be used because the QCPU-A cannot store the microcomputer program.
- All of the contents which are processed by the microcomputer area need to be changed to the program using the dedicated instructions in order to be used by the QCPU-A.

Appendix 4.2 Special relays and special registers with different specifications

The QCPU-A does not use the following special relays and special registers.
Even though no error occurs when the following special relays and special registers exist in the diverted program (ignored), it is recommended that they are deleted from the program.

- M9010.....Turned ON when a operation error occurs and turned OFF when the error disappears.
- M9053.....Link refresh enable of the EI instruction /interrupt enable instruction of the interrupt program, DI instruction to the link refresh disable/interrupt disable instruction of the interrupt program.

Appendix 4.3 Parameter setting

The parameters set by the existing CPU can be used as is if the following items do not apply to them.

Setting Item	Description
Microcomputer program capacity	The microcomputer area of the QCPU-A is for the SFC only. "PARAMETER ERROR" occurs if a utility package of the microcomputer program is stored in the microcomputer area of the existing CPU.
Registering the model name of the module by the I/O assignment (By the system FD which is compatible with the QCPU-A)	When the AD57 module or AD57-S1 module is used in the existing system, the utility package of the SW□-AD57P is stored in the microcomputer program area. The QCPU-A system does not allow the AD57 or AD57-S1 to be loaded.

The following items are executed differently from the parameter setting of the existing CPU.

- Watchdog timer setting.....The setting time is ignored and processed by 200ms.
- Interrupt counter setting.....The interrupt counter set by the A1SCPU and A2SCPU are ignored and treated as a normal counter by the sequence program.

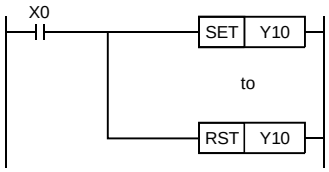
Appendix 4.4 I/O control method

The I/O control method of the QCPU-A is the refresh method (partial direct I/O depending on the instruction), and is different from that of the A1SCPU and A2SCPU. Therefore, pay attention to the input timing of the input (X) and the output timing of the output (Y).

(1) Program to process to pulses by the SET/RST instruction

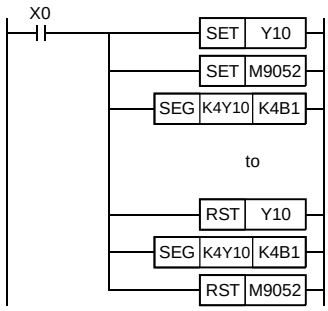
Program as follows in order for the QCPU-A to execute the pulse output to the outside by the SET/RST instruction while in the direct method of the A1SCPU and A2SCPU.

For direct method of the A1SCPU and A2SCPU

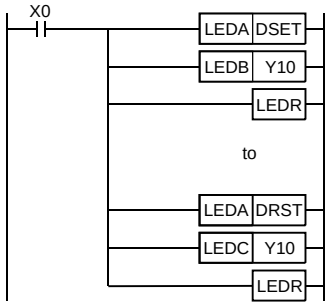


(a) When the instructions common to the ACPU are used:

For direct method of the QCPU-A



(b) When the instructions dedicated to the QCPU-A are used:



POINT

Use the program above in order to send the pulse signal output to the special function module when a special function module is used, such as the A1SD61-type high-speed counter module.

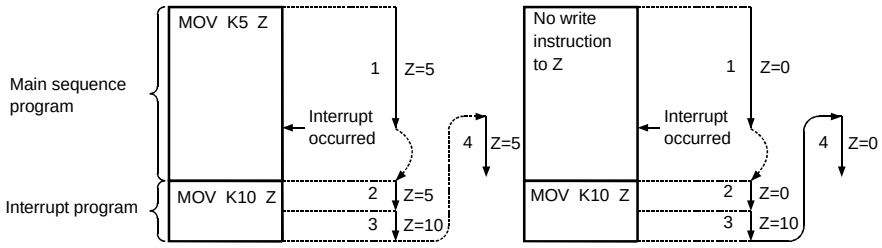
Appendix 4.5 Microcomputer program

The utility software packages and the microcomputer programs created by the user which are used by the A1SCPU and A2SCPU cannot be used by the QCPU-A because it does not have the microcomputer mode. (The microcomputer program area of the QCPU-A is for the SFC only.)
When the utility software packages or the microcomputer programs above are used, delete all of the SUB instructions (microcomputer program call) used for executing them from the sequence program.
When the following utility package is used, modify the program using instructions dedicated to the QCPU-A.

1 SW□-UTLP-FNO····· AnSH/AnACPU/AnUCPU Programming Manual (Dedicated Instruction) IB-66251
2 SW□-UTLP-PID····· AnACPU/AnUCPU Programming Manual (PID) IB-66258
3 SW□-AD57P
4 SW□-SIMA
5 SW□-UTLP-FDI
6 SW□-SAPA
} Unusable

Appendix 4.6 Processing of the index register

The index register of the QCPU-A is written over again to the value prior to the execution of the interrupt program when the processing is handed over to the main or sequence program even if the value was updated by the interrupt program.



Appendix 5 List of Instruction Processing Time

The following table shows the instruction processing time of QCPU-A (A mode).

(1) Sequence instructions

Instruction	Condition (Device)						Instruction Processing Time (μs)	
							QnCPU-A	QnHCPU-A
LD, LDI AND, ANI OR, ORI	X						0.079	0.034
	Y, M, L, S, B, F, T, C						0.079	0.034
OUT	Y	At no change (OFF → OFF, ON → ON)					0.158	0.068
		At change (OFF → ON, ON → OFF)					0.158	0.068
	M (except for special M) L S B	At no change (OFF → OFF, ON → ON)					0.158	0.068
		At change (OFF → ON, ON → OFF)					0.158	0.068
	Special M						0.316	0.136
	F	At no execution					1.11	0.480
		At execution					35.1	15.1
	T	Instruction execution time					0.158	0.068
		END	Time for no execution				0.088	0.037
			At execution	After time elapsed			1.80	0.774
				At addition	K		3.07	1.32
					D		3.31	1.42
	C	Instruction execution time					0.158	0.068
		END	Time for no execution				0.105	0.045
			At execution	At no counting			0.105	0.045
				After counting up			0.105	0.045
				At counting	K		1.67	0.720
					D		1.91	0.823
SET	Y	At no execution					0.158	0.068
		At execution	At no change (ON → ON)				0.158	0.068
			At change (OFF → ON)				0.158	0.068
	M, L S, B	At no execution					0.158	0.068
		At execution	At no change (ON → ON)				0.158	0.068
			At change (OFF → ON)				0.158	0.068

Instruction	Condition (Device)			Instruction Processing Time (μs)	
				QnCPU-A	QnHCPU-A
SET	Special M B	At no execution		0.316	0.136
		At execution		0.316	0.136
	F	At no execution		0.798	0.343
		At execution		35.1	15.1
RST	Y	At no execution		0.158	0.068
		At execution	At no change	0.158	0.068
			At change	0.158	0.068
	M, L S, B	At no execution		0.158	0.068
		At execution	At no change	0.158	0.068
			At change	0.158	0.068
	Special M B	At no execution		0.316	0.136
		At execution		0.316	0.136
	F	At no execution		0.798	0.343
		At execution		37.7	16.3
	T C	At no execution		0.561	0.242
		At execution		2.24	0.962
	W, A0, A1 V, Z	At no execution		0.561	0.242
		At execution		3.35	1.44
	R	At no execution		0.561	0.242
		At execution		1.66	0.715
NOP				0.079	0.034
FEND END	When M9084 is OFF			339	145
	When M9084 is ON			253	110
MC	Y	At no execution		0.482	0.208
		At execution		0.482	0.208
	M, LS, BF	At no execution		0.482	0.208
		At execution		0.482	0.208
MCR				0.237	0.101
PLS PLF	Y	At no execution		0.877	0.376
		At execution	ON	0.877	0.376
			OFF	0.877	0.376
	L, B, F	At no execution		0.877	0.376
		At execution	ON	0.877	0.376
			OFF	0.877	0.376

Instruction	Condition (Device)		Instruction Processing Time (μs)	
			QnCPU-A	QnHCPU-A
SFT SFTP	Y	At no execution	0.561	0.242
		At execution	1.75	0.755
	M, L, B, F	At no execution	0.561	0.242
		At execution	1.75	0.755
MPS			0.079	0.034
MRD			0.079	0.034
MPP			0.079	0.034
CJ	Without index qualification		2.72	1.17
	With index qualification		2.72	1.17
SCJ	Without index qualification		2.72	1.17
	With index qualification		2.72	1.17
JMP			2.72	1.17
CALL	Without index qualification		6.81	2.93
	With index qualification		6.81	2.93
CALLP	Without index qualification		6.81	2.93
	With index qualification		6.81	2.93
RET			2.79	1.20
EI			1.19	0.514
DI			1.27	0.548
IRET			1.36	0.586
SUB	Without index qualification			
	With index qualification			
SUBP	Without index qualification			
	With index qualification			
CHG	When M9084 is OFF			
	When M9084 is ON			
FOR			2.31	0.997
NEXT			3.19	1.38
STOP				

(2) Basic instructions

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
LD=		1.67	0.721
AND=		1.27	0.546
OR=		1.76	0.758
LDD=		4.50	1.94
ANDD=		3.48	1.50
ORD=		4.43	1.91
LD<>		1.92	0.829
AND<>		1.28	0.553
OR<>		1.76	0.758
LDD<>		4.26	1.84
ANDD<>		3.49	1.51
ORD<>		4.18	1.80
LD>		1.92	0.829
AND>		1.28	0.553
OR>		1.76	0.758
LDD>		4.26	1.84
ANDD>		3.49	1.51
ORD>		4.18	1.80
LD>=		1.92	0.829
AND>=		1.28	0.553
OR>=		1.76	0.758
LDD>=		4.26	1.84
ANDD>=		3.49	1.51
ORD>=		4.18	1.80
LD<		1.92	0.829
AND<		1.28	0.553
OR<		1.76	0.758
LDD<		4.26	1.84
ANDD<		3.49	1.51
ORD<		4.18	1.80
LD<=		1.92	0.829
AND<=		1.28	0.553
OR<=		1.76	0.758
LDD<=		4.26	1.84
ANDD<=		3.49	1.51
ORD<=		4.18	1.80

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
+ S D		1.11	0.480
+P S D		1.11	0.480
D+ S D		1.60	0.688
D+P S D		1.60	0.688
+ S1 S2 D		1.27	0.548
+P S1 S2 D		1.27	0.548
D+ S1 S2 D		1.83	0.790
D+P S1 S2 D		1.83	0.790
- S D		1.11	0.480
-P S D		1.11	0.480
D- S D		1.60	0.688
D-P S D		1.60	0.688
- S1 S2 D		1.27	0.548
-P S1 S2 D		1.27	0.548
D- S1 S2 D		1.83	0.790
D-P S1 S2 D		1.83	0.790
* S1 S2 D		1.36	0.586
* P S1 S2 D		1.36	0.586
D* S1 S2 D		7.97	3.43
D*P S1 S2 D		7.97	3.43
/ S1 S2 D		4.38	1.89
/P S1 S2 D		4.38	1.89
D/ S1 S2 D		14.4	6.20
D/P S1 S2 D		14.377	6.20
INC		0.798	0.344
INCP		0.798	0.344
DINC		0.956	0.412
DINCP		0.956	0.412
DEC		0.798	0.344
DECP		0.798	0.344
DDEC		0.956	0.412
DDECP		0.956	0.412
B+ S D		2.55	1.10
B+P S D		2.55	1.10
DB+ S D		13.6	5.86
DB+P S D		13.6	5.86
B+ S1 S2 D		5.58	2.40
B+P S1 S2 D		5.58	2.40
DB+ S1 S2 D		12.4	5.32
DB+P S1 S2 D		12.4	5.32

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
B- S D		2.47	1.07
B-P S D		2.47	1.07
DB- S D		12.7	5.48
DB-P S D		12.7	5.48
B- S1 S2 D		5.58	2.40
B-P S1 S2 D		5.58	2.40
DB- S1 S2 D		11.6	4.99
DB-P S1 S2 D		11.6	4.99
B* S1 S2 D		5.58	2.40
B*P S1 S2 D		5.58	2.40
DB* S1 S2 D		35.5	15.3
DB*P S1 S2 D		35.5	15.3
B/ S1 S2 D		4.38	1.89
B/P S1 S2 D		4.38	1.89
DB/ S1 S2 D		24.7	10.7
DB/P S1 S2 D		24.7	10.7
BCD		1.19	0.51
BCDP		1.19	0.51
DBCD		5.18	2.23
DBCDP		5.18	2.23
BIN		1.19	0.51
BINP		1.19	0.51
DBIN		2.39	1.03
DBINP		2.39	1.03
MOV		0.482	0.208
MOVP		0.482	0.208
DMOV		1.27	0.548
DMOVP		1.27	0.548
XCH		1.11	0.480
XCHP		1.11	0.480
DXCH		1.61	0.722
DXCHP		1.61	0.722
CML		0.956	0.412
CMLP		0.956	0.412
DCML		1.27	0.548
DCMLP		1.27	0.548
BMOV S D n	n=96	28.7	12.4
BMOVP S D n	n=96	28.7	12.4
FMOV S D n	n=96	12.7	5.48
FMOVP S D n	n=96	12.7	5.48

(3) Application instructions

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
WAND S D		1.11	0.480
WANDP S D		1.11	0.480
DAND		5.18	2.23
DANDP		5.18	2.23
WAND S1 S2 D		3.03	1.30
WANDP S1 S2 D		3.03	1.30
WOR S D		1.11	0.480
WORP S D		1.11	0.480
DOR		5.18	2.23
DORP		5.18	2.23
WOR S1 S2 D		3.03	1.30
WORP S1 S2 D		3.03	1.30
WXOR S D		1.11	0.480
WXORP S D		1.11	0.480
DXOR		5.18	2.23
DXORP		5.18	2.23
WXOR S1 S2 D		3.03	1.30
WXORP S1 S2 D		3.03	1.30
WXNR S D		1.19	0.514
WXNRP S D		1.19	0.514
DXNR		5.98	2.58
DXNRP		5.98	2.58
WXNR S1 S2 D		3.11	1.34
WXNRP S1 S2 D		3.11	1.34
NEG		3.43	1.48
NEGP		3.43	1.48

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
ROR n	n=5	2.31	0.997
RORP n	n=5	2.31	0.997
RCR n	n=5	2.55	1.10
RCRP n	n=5	2.55	1.10
ROL n	n=5	2.31	0.997
ROLP n	n=5	2.31	0.997
RCL n	n=5	2.55	1.10
RCLP n	n=5	2.55	1.10
DROR n	n=5	4.38	1.89
DRORP n	n=5	4.38	1.89
DRCR n	n=5	4.78	2.06
DRCRP n	n=5	4.78	2.06
DROL n	n=5	3.99	1.72
DROLP n	n=5	3.99	1.72
DRCL n	n=5	4.78	2.06
DRCLP n	n=5	4.78	2.06
SFR D n	n=5	1.99	0.86
SFRP D n	n=5	1.99	0.86
BSFR D n	n=5	11.6	4.99
BSFRP D n	n=5	11.6	4.99
DSFR D n	n=5	7.49	3.23
DSFRP D n	n=5	7.49	3.23
SFL D n	n=5	1.91	0.82
SFLP D n	n=5	1.91	0.82
BSFL D n	n=5	11.1	4.80
BSFLP D n	n=5	11.1	4.80
DSFL D n	n=5	8.77	3.78
DSFLP D n	n=5	8.77	3.78
SER S1 S2 n	n=5	13.2	5.67
SERP S1 S2 n	n=5	13.2	5.67

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
SUM		5.98	2.58
SUMP		5.98	2.58
DSUM		13.6	5.59
DSUMP		13.6	5.59
DECO S D n	n=2	11.1	4.80
DECOP S D n	n=2	11.1	4.80
SEG		2.55	1.10
ENCO S D n	n=2	15.2	6.54
ENCOP S D n	n=2	15.2	6.54
BSET D n	n=5	3.82	1.65
BSETP D n	n=5	3.82	1.65
BRST D n	n=5	3.82	1.65
BRSTP D n	n=5	3.82	1.65
UNI S D n	n=4	12.4	5.32
UNIP S D n	n=4	12.4	5.32
DIS S D n	n=4	9.96	4.29
DISP S D n	n=4	9.96	4.29
ASC		1.36	0.586
FIFW		18.0	3.44
FIFWP		7.98	3.44
FIFR		27.5	11.8
FIFRP		27.5	11.8
LRDP n1 S D n2	n2=1	33.0	27.4
	n2=32	33.0	27.4
LWTP n1 S D n2	n2=1	34.9	29.0
	n2=32	54.6	45.3
RFRP n1 n2 D n3	n3=1	14.5	12.0
	n3=32	14.5	12.0
RTOP n1 n2 S n3	n3=1	15.5	12.9
	n3=32	15.5	12.9

Instruction	Condition (Device)	Instruction Processing Time (μs)	
		QnCPU-A	QnHCPU-A
WDT		1.99	0.858
WDTP		1.99	0.858
CHK	When the number of conditional contacts is 1	13.2	5.67
	When the number of conditional contacts is 50	500	216
	When the number of conditional contacts is 100	997	430
	When the number of conditional contacts is 150	1495	644
SLT	Device memory only	4555	1744
	Device memory + R (8K points)	6123	2259
SLTR		2.63	1.13
STRA		1.99	0.858
STRAR		1.99	0.858
STC		0.956	0.412
CTC		0.956	0.412
DUTY		5.58	2.40
PR		29.5	12.7
PRC		14.7	6.35
CHK			
LED			
LEDA			
LEDB			
LEDR		41.8	18.0
FROM FROMP	n3 = 1, X, Y	180	143
	n3 = Other than 1, X, or Y	170	141
	n3 = 112, X, Y	1117	761
	n3 = Other than 1000, X, or Y	3346	3161
DFRO DFROP	n3 = 1, X, Y	184	154
	n3 = Other than 1, X, or Y	175	152
	n3 = 56, X, Y	875	741
	n3 = Other than 500, X, or Y	3321	3157
TO TOP	n3 = 1, X, Y	173	93.7
	n3 = Other than 1, X, or Y	173	93.3
	n3 = 112, X, Y	751	441
	n3 = Other than 1000, X, or Y	3126	3055
DTO DTOP	n3 = 1, X, Y	181	101
	n3 = Other than 1, X, or Y	184	101
	n3 = 56, X, Y	694	441
	n3 = Other than 500, X, or Y	3122	3060

(4) Dedicated instructions

Category	Instruction Name	Condition	Instruction Processing Time (μs)	
			QnCPU-A	QnHCPU-A
Direct processing instruction	DOUT		17.8	7.66
	DSET		17.6	7.59
	DRST		17.6	7.59
Structured program instruction	IX		20.3	8.27
	IXEND		3.35	1.44
	BREAK		24.3	10.5
	FCALL		21.9	9.44
	CHK		2.95	1.27
	CHKEND		1.11	0.48
Data operation instruction	DSER	1 point	47.6	20.5
		5 point	51.1	22.0
		96 point	137	59.1
	SWAP		14.8	6.36
	DIS	1-bit designation	44.2	19.0
		1-, 4-, 8-, 12-, and 15-bit designation	55.8	24.0
	UNI	1-bit designation	44.6	19.2
		1-, 4-, 8-, 12-, and 15-bit designation	57.3	24.7
	TEST		28.7	12.4
	DTEST		29.1	121
I/O operation instruction	FF		16.1	6.92
	KEY		46.5	20.0
BCD type real number processing instruction	BSQR		54.6	23.5
	BDSQR		51.0	22.0
	BSIN		23.9	10.3
	BCOS		24.7	10.7
	BTAN		24.7	10.7
	BASIN		33.5	14.4
	BACOS		33.8	14.6
	BATAN		38.7	16.7
Floating-point type real number processing instruction	INT		37.4	16.1
	DINT		38.2	16.5
	FLOAT		37.4	16.1
	DFLOAT		41.5	17.9
	ADD		288	109
	SUB		292	110
	MUL		276	104
	DIV		452	171
	RAD		223	84.1
	DEG		204	77.1

Category	Instruction Name	Condition	Instruction Processing Time (μs)	
			QnCPU-A	QnHCPU-A
Floating-point type real number processing instruction	SIN		4252	1056
	COS		2613	1126
	TAN		2639	1137
	ASIN		4662	2009
	ACOS		4642	2000
	ATAN		3522	1518
	SQR		1901	819
	EXP		2379	1025
	LOG	log1	486	209
		log10	2160	931
Character-string processing instruction	BINDA		27.1	11.8
	DBINDA		97.2	41.9
	BINHA		29.5	12.7
	DBINHA		35.1	15.1
	BCDDA		34.6	14.9
	DBCDDA		41.0	17.7
	DABIN		82.8	35.7
	DDABIN		124	53.6
	HABIN		30.2	13.0
	DHABIN		41.5	17.9
	DABCD		32.3	13.9
	DDABCD		46.2	19.9
	COMRD		40.2	17.3
	LEN	1 character	26.7	11.5
		96 character	99.2	42.8
	STR		53.8	23.2
	DSTR		115	49.6
	VAL		94.1	40.5
	DVAL		168	72.3
	ASC	1 character	59.4	25.6
		96 character	300	129
	HEX	1 character	57.8	24.9
		96 character	312	134
	SMOV	1 character	33.5	14.4
		96 character	131	56.3
	SADD	1 character + 1 character	74.5	32.1
		96 characters + 96 characters	318	137
	SCMP	1 character	40.7	17.5
		96 character	189	81.6

Category	Instruction Name	Condition	Instruction Processing Time (μs)	
			QnCPU-A	QnHCPU-A
Character-string processing instruction	WTOB	1 byte	48.6	20.9
		96 byte	101	43.6
	BTOW	1 byte	46.2	19.9
		96 byte	84.1	36.2
Data operation instruction	LIMIT		33.8	14.6
	DLIMIT		35.1	15.1
	BAND		88.8	15.6
	DBAND		34.6	14.9
	ZONE		33.5	14.4
	DZONE		34.3	14.8
Clock instruction	DATERD		17.1	7.37
	DATEWR		19.1	8.24
Expansion file register instruction	RSET		16.6	7.15
	BMOVR	1 point	44.5	19.1
		96 point	59.9	25.7
	BXCHR	1 point	50.4	21.6
		96 point	80.9	34.6
	ZRRD		5.68	2.41
	ZRWR		5.66	2.42
	ZRRDB		5.91	2.54
	ZRWRB		6.14	2.64
Data link instruction	LRDP		54.9	23.5
	LWTP		54.9	23.5
	RFRP		61.3	26.2
	RTOP		54.9	25.8
MD61 (S1) instruction	PVWR1		111	84.4
	PVWR2		111	84.5
	SVWR1		118	91.2
	SVWR2		118	91.4
	PVRD1		112	82.2
	PVRD2		113	82.6

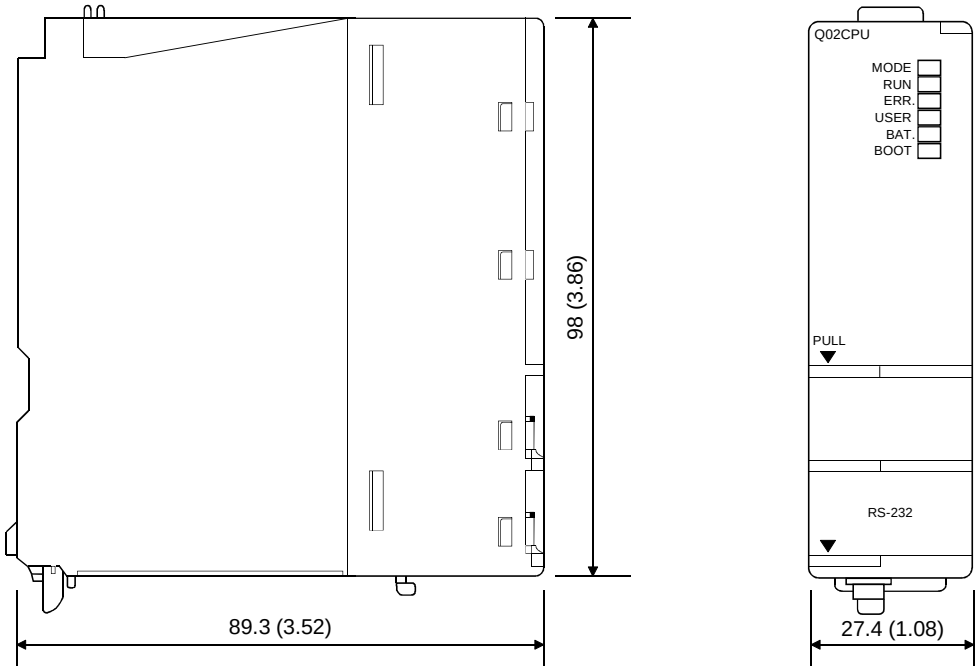
Category	Instruction Name	Condition	Instruction Processing Time (μs)	
			QnCPU-A	QnHCPU-A
AJ71UC24 instruction	PRN	2 words	265	220
		96 words	647	537
	PR	2 words	167	139
		96 words	694	576
	INPUT	100 words	441	366
	SPBUSY		45.9	38.1
	SPCLR		42.1	34.9
AJ71PT32-S3 instruction	INPUT (Operating box)		189	157
	PRN AJ35PTF-R2	1 character	243	202
		96 character	626	519
	PR AJ35PTF-R2	1 character	240	199
		96 character	535	444
	INPUT AJ35PTF-R2	96 character	345	287
	MINI	FROM/TO instruction: 1	76.5	63.5
		FROM/TO instruction: 16	491	407
	MINIERR		41.1	34.1
	SPBUSY		69.8	58.0
	SPCLR		84.2	69.9
Data link instruction	ZCOM		34.0	14.6
	ZNRD		86.2	29.7
	ZNWR		87.3	29.7
	ZNFR		65.2	27.9
	ZNTO		65.4	28.0
CC-Link dedicated instruction	RLPA	1 station	0.173	0.116
		64 station	0.600	0.500
	RRPA	1 point	0.192	0.150
		4096 point	0.192	0.171
	RIFR	1 point	0.217	0.153
		4096 point	13.3	12.3
	RITO	1 point	0.277	0.220
		4096 point	12.8	12.7
	RIRD	1 point	0.326	0.340
		480 point	0.315	0.300
	RIWT	1 point	0.298	0.350
		480 point	1.75	1.68
	RISEND	1 point	0.337	0.320
		480 point	1.17	1.10
	RIRCV	1 point	0.361	0.301
		480 point	0.370	0.380
1ms-timer setting instruction	ZHTIME		5.42	2.33

Appendix 6 Dimensions

The dimensions of QCPU-A and the base module are shown below:

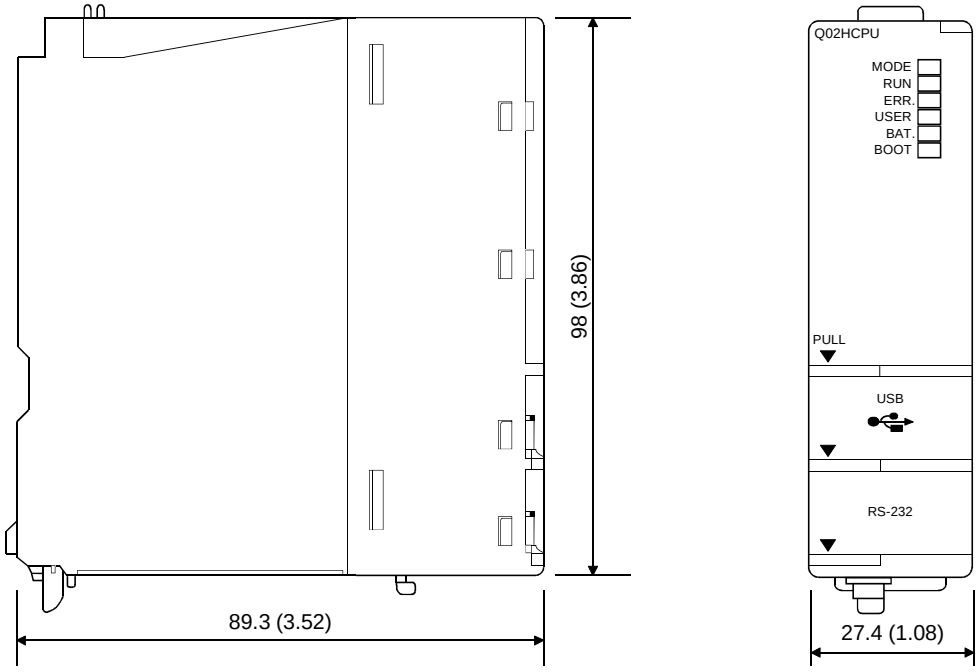
Appendix 6.1 Dimensions of CPU module

(1) Q02CPU-A



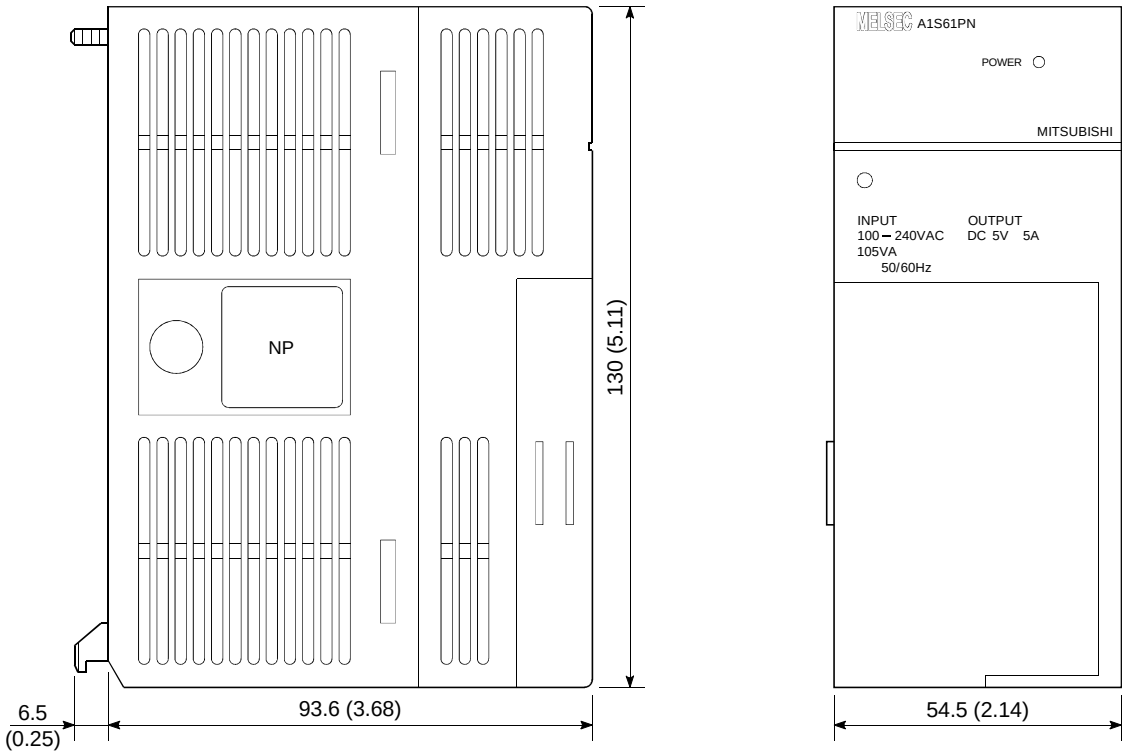
Unit: mm (inch)

(2) Q02HCPU-A, Q06HCPU-A



Unit: mm (inch)

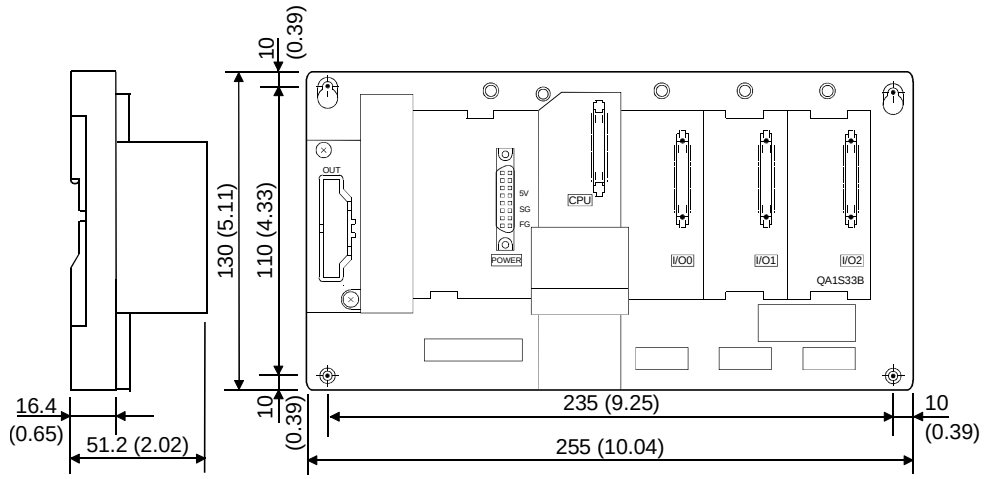
Appendix 6.2 Power supply modules



Unit: mm (inch)

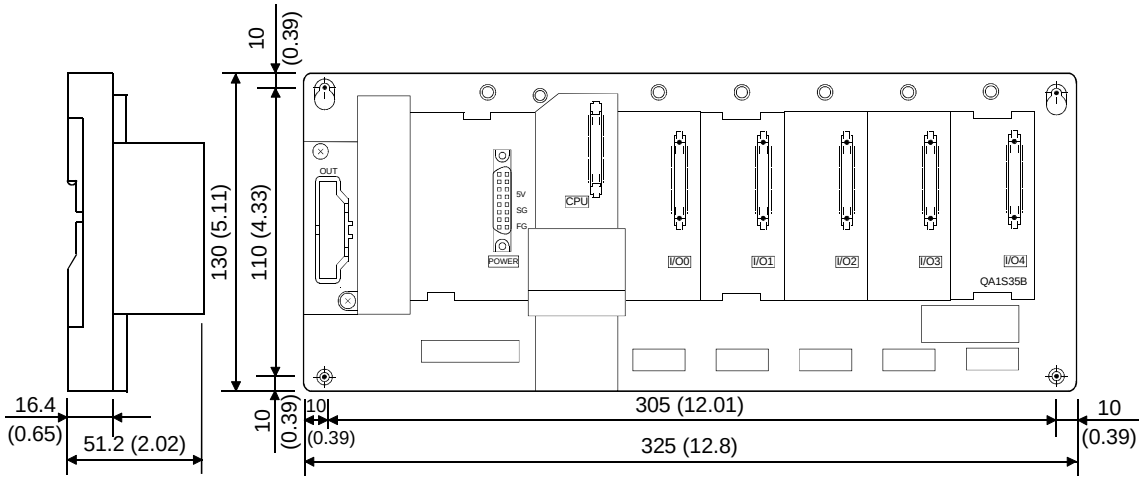
Appendix 6.3 Dimensions of base module

(1) Basic base module (QA1S33B)



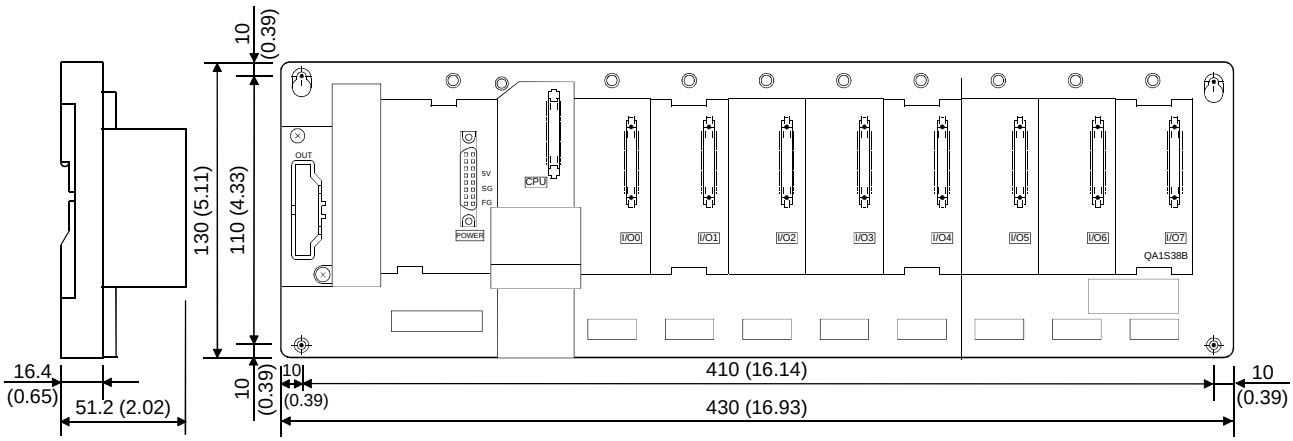
Unit: mm (inch)

(2) Basic base module (QA1S35B)



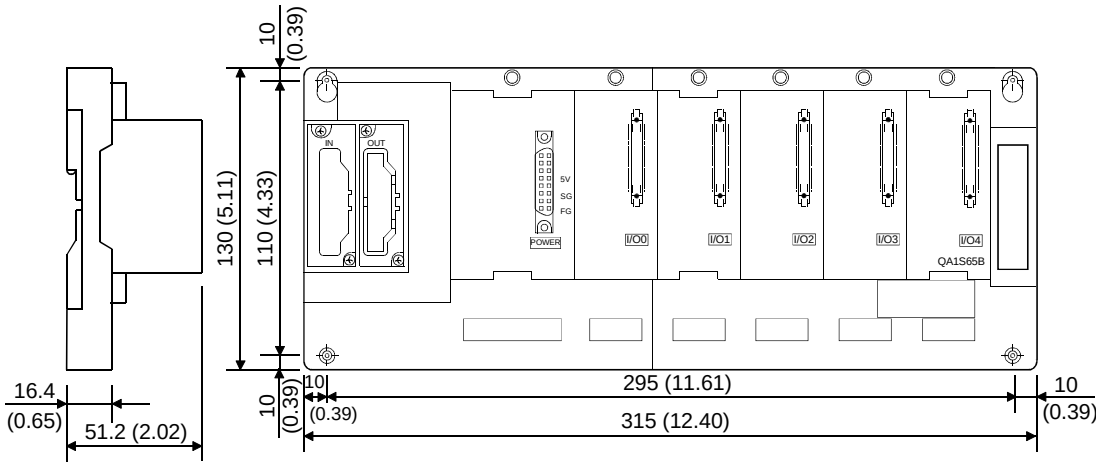
Unit: mm (inch)

(3) Basic base module (QA1S38B)



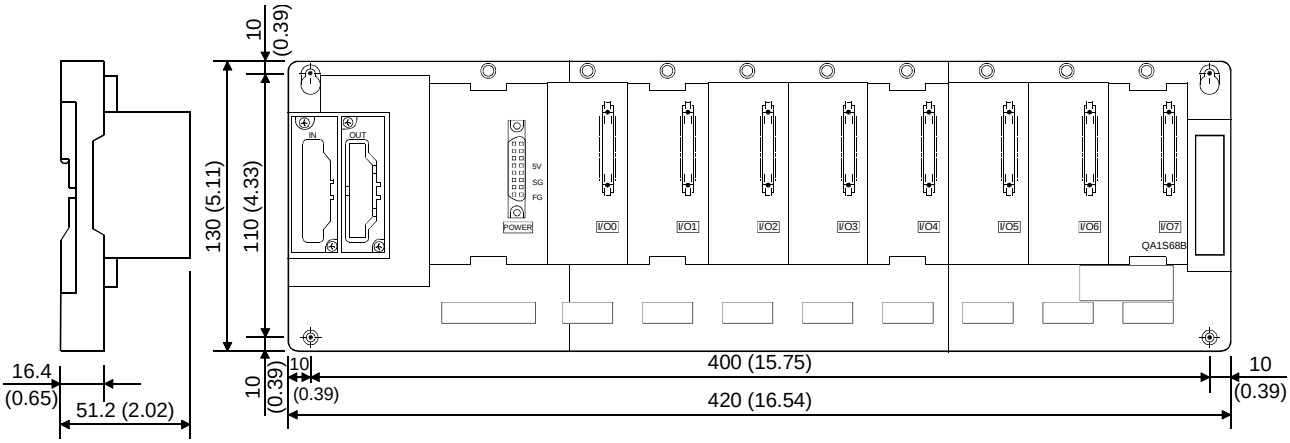
Unit: mm (inch)

(4) Expansion base module (QA1S65B)



Unit: mm (inch)

(5) Expansion base module (QA1S68B)



Unit: mm (inch)

MEMO

WARRANTY

Please confirm the following product warranty details before starting use.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the dealer or Mitsubishi Service Company. Note that if repairs are required at a site overseas, on a detached island or remote place, expenses to dispatch an engineer shall be charged for.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found to not be the responsibility of Mitsubishi or the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not possible after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of chance loss and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to damages caused by any cause found not to be the responsibility of Mitsubishi, chance losses, lost profits incurred to the user by failures in Mitsubishi products, damages and secondary damages caused from special reasons regardless of Mitsubishi's expectations, compensation for accidents, and compensation for damages to products other than Mitsubishi products and other duties.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.

(2) The Mitsubishi general-purpose programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for each Japan Railways company or the Department of Defense shall be excluded from the programmable logic controller applications.

Note that even with these applications, if the user approves that the application is to be limited and a special quality is not required, application shall be possible.

When considering use in aircraft, medical applications, railways, incineration and fuel devices, manned transport devices, equipment for recreation and amusement, and safety devices, in which human life or assets could be greatly affected and for which a particularly high reliability is required fin terms of safety and control system, please consult with Mitsubishi and discuss the required specifications.

QCPU-A(A Mode)

User's Manual

MODEL	QCPU-A(A)-U-SHO-E
MODEL CODE	13JR10
SH(NA)-080065-B(0003)MEE	

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100-8310 TELEX : J24532 CABLE MELCO TOKYO
NAGOYA WORKS : 1-14 , YADA-MINAMI 5 , HIGASHI-KU, NAGOYA , JAPAN