V8600A

CMOS, 5 Volt-only Voice Synthesizer Module

FEATURES

- High speech quality, unlimited vocabulary
- Converts any ASCII text into speech automatically
- Add/modify messages by simply editing a text file
- Requires only a single +5 V supply and speaker
- User programmable greeting and default settings
- Flexible exception dictionary support
- 2 KB input buffer
- Software control of all voice parameters
- Real-time and pre-recorded playback of sound files
- Three-voice musical tone generator
- Dual sinusoidal generator
- DTMF (Touch-Tone) dialer
- CMOS design – TTL compatible inputs and outputs
- Low power:
  - 110 mW typ active
  - 5 mW typ idle
  - 250 µW typ standby
- Three built-in interfaces:
  - Microprocessor bus
  - Asynchronous serial port
  - Parallel printer port

APPLICATIONS

Robotics
Talking OCR systems
Talking e-mail/telecommunications
Remote diagnostic reporting
Industrial controllers
Electronic test and measurement
Security and warning systems
Aids for the orally or visually disabled

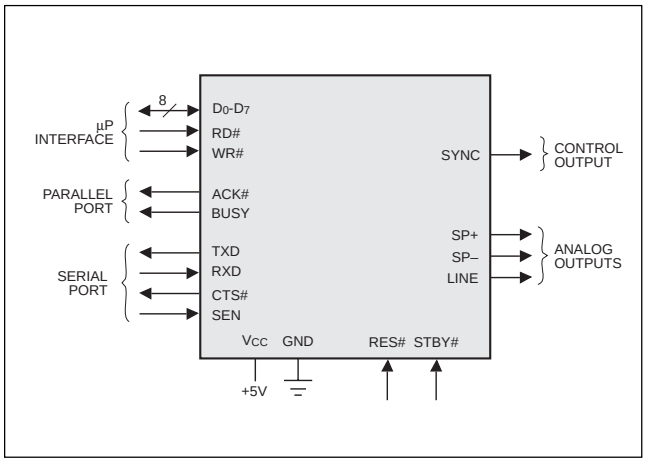
GENERAL DESCRIPTION

The V8600A is a full-featured voice synthesizer based on RC Systems' DoubleTalk RC8650 chipset. The V8600A automatically converts plain English ASCII text into a high quality male voice. Only a 5 V power supply and speaker are needed for operation.

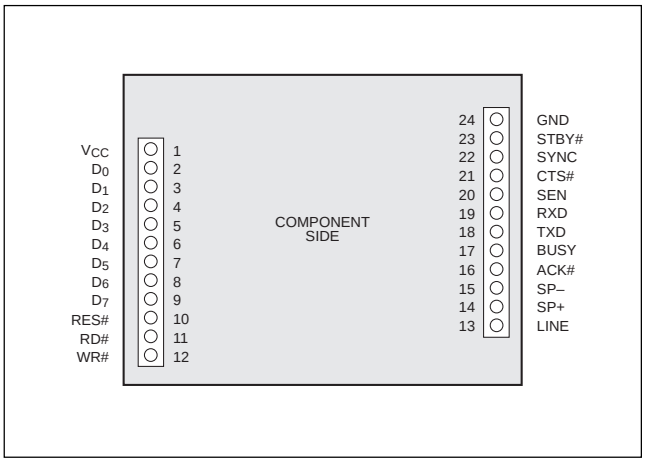
The V8600A is designed to be piggy-backed onto a host PCB, such as a system's controller board, via two 12-pin headers. An eight bit bidirectional data bus and read/write control pins enable the V8600A to be easily interfaced to virtually any microprocessor bus. Stand-alone applications are also possible with the V8600A's built in printer and serial ports.

For additional information about using and programming the V8600A, please refer to the *DoubleTalk RC8650 Chipset User's Manual*, available from http://www.rcsys.com.

LOGIC SYMBOL



PIN CONFIGURATION



PIN DEFINITIONS

VCC *Power Supply Voltage* (+5 V ±10%).

D0-D7 *Data Bus* (input/output, active High, 3-state). These pins form an eight bit bidirectional data bus between the V8600A and the host. When WR# is Low, the Data Bus is placed in the input mode (host→V8600A). When RD# is Low, the bus is placed in the output mode (V8600A→host). When RD# is High, the Data Bus is held in the high-impedance state.

RES# *Reset* (input, active Low). A Low on this pin forces a hardware reset: speech production is immediately halted, the input buffer is cleared and the status flags and voice parameters (volume, speed, pitch, etc.) are reset to their power-up states.

As shown in the Block Diagram, the V8600A contains an internal power-on reset (POR) circuit, allowing the Reset pin to be left unconnected in most applications. Because the POR circuit drives the Reset pin through a 47K resistor, it will not contend with external circuitry connected to the Reset pin. *Caution*: If external voltages are present on one or more of the V8600A's pins before V_{CC} is applied (therefore exceeding the maximum V_{IH} rating), the internal POR circuit may not operate reliably. In this case, RES# must be driven from an external source.

RD# *Read* (input, active Low). This pin is used to transfer V8600A status information to the host via the Data Bus. A Low gates the status onto the Data Bus and turns on the output drivers. RD# contains an internal pull-up resistor and may be left unconnected.

WR# *Write* (input, active Low). This pin is used to transfer data to the V8600A via the Data Bus. The contents of the Data Bus are written to the V8600A at the rising edge of Write. WR# contains an internal pull-up resistor and may be left unconnected.

LINE *Line* (output, analog). This pin supplies a low-level audio signal suitable for connection to an external low pass filter/power amplifier circuit. The output amplitude is a function of both the volume control setting and Volume command. LINE can also be used as a remote volume control input (see "Application Example – Remote Volume Control").

SP+, SP– *Speaker* (output, analog). These pins provide a filtered, differential audio signal capable of driving 500 mW into an 8 ohm speaker. The output power is a function of both the volume control setting and Volume command. The SP+ output is AC-coupled, allowing ground-referenced loads to be connected between SP+ and ground (at one-fourth the power, however, since the effective output voltage is cut in half). Both pins go into a high-impedance state when the V8600A is idle or asleep.

ACK# *Acknowledge* (output, active Low). This pin produces a 9 µs low-going pulse after each successful write operation over the Data Bus. If the input buffer becomes full as a result of the last write operation, the Acknowledge pulse will not occur until room becomes available. ACK# is inactive when using the serial port.

BUSY *Busy* (output, active High). This pin is Low when the V8600A is able to accept data from the host. BUSY goes High momentarily after each write operation over the Data Bus, acknowledging receipt of each character. If the input buffer becomes full as a result of the last write operation, BUSY will remain High until room becomes available.

TXD *Transmit Data* (output, active High). This pin transfers serial data to the host, least significant bit (LSB) first.

RXD *Receive Data* (input, active High). The V8600A receives serial data from the host on this pin, LSB first. RXD contains an internal pull-up resistor and may be left unconnected.

SEN *Serial Enable* (input, active High). This pin is used to enable the optional RS-232 transceiver chip on the V8600A PCB (see "RS-232 transceiver option"). Setting this pin Low will power-down the transceiver chip, reducing overall power consumption. SEN may be left unconnected if the transceiver option is not installed.

CTS# *Clear to Send* (output, active Low). This pin is Low when the V8600A is able to accept data from the host. CTS# goes High momentarily after a character is received via the RXD pin, acknowledging receipt of each character. If the input buffer becomes full as a result of the last character received, CTS# will remain High until room becomes available.

SYNC *Sync* (output, active High). This pin is normally High when the V8600A is active (producing output). It can be used to control external devices, such as a transmitter or telephone DAA. SYNC is driven by the on-board RC8650's TS pin; thus its polarity and state can be programmed with the RC8650's TS Pin Control command. Refer to the *DoubleTalk RC8650 Chipset User's Manual* for further details.

STBY# *Standby* (input, active Low). This is a dual function pin that can be used to put the V8600A in Standby mode or initialize its internal memory.

Driving STBY# Low for 250 ms or longer causes the V8600A to enter Standby mode. All port handshake lines are driven to their false ("not ready") states, and the V8600A draws minimum current (50 µA typ). During standby, the V8600A is not able to respond to any input pin except STBY# and RES#. Returning STBY# High causes the V8600A to enter Idle mode (1 mA typ drain); the handshake lines are re-asserted and the V8600A is able to accept input again. If the V8600A entered standby due to a Sleep Timer event, driving this pin Low for 250 *ns* or longer then High will return the V8600A to Idle mode.

If the V8600A is not in Standby mode, driving STBY# Low for less than 250 ms initializes the V8600A's internal memory. Any exception dictionary loaded and/or greeting message is erased, and all voice parameters are reset to their factory default settings. The V8600A then announces its version number via the Speaker and Line pins.

In order to maintain backward compatibility with the V8600, STBY# contains a "dynamic" pull-up resistor. If STBY# is not used, it may be left unconnected. If STBY# is used to enter Standy mode, the internal pullup resistor is automatically disconnected from the pin during standby to reduce overall current drain. STBY# must be *driven* High to exit Standby mode; it should not be allowed to float. The pullup resistor is automatically reconnected once Idle mode has been re-established.

GND *Ground* (ground reference). This pin must be connected to system ground.

FUNCTIONAL DESCRIPTION

The V8600A is a complete, self-contained text-to-speech system. It can be interfaced to a microprocessor bus like a static RAM or I/O port, connected directly to a PC's parallel printer port, or, with appropriate signal conditioning, to an RS-232 serial port.

Operating the V8600A is simply a matter of writing (or "printing," if connected to a printer port) the text that is to be spoken to the V8600A. Software commands that control voice attributes, such as speed and pitch, are issued the same way, allowing them to be embedded in text for dynamic control of the speech output.

Refer to the V8600A Block Diagram for the following functional description.

Data Register. This is an eight bit register into which ASCII text, commands, tone generator and PCM data are written from the parallel Data Bus D_0-D_7. A host microprocessor can write data to this register by placing the data on the Data Bus and asserting the WR# signal. Data is latched on the rising (trailing) edge of WR#.

Status Register. This eight bit register contains the V8600A status flags. The host can read this register over the Data Bus by asserting the RD# signal.

Serial Port. The Serial Port provides a bidirectional link between the V8600A and serial devices, such as a computer's RS-232 port. This allows the V8600A to be remotely located, such as in a stand-alone synthesizer. The Serial Port operates with 8 data bits, 1 or more stop bits, no parity, and any standard baud rate between 300 and 115200 bps. The V8600A determines which baud rate to use by measuring the duration of the shortest High or Low period of the first character received on the RXD pin. The baud rate can also be optionally "strapped," using three jumpers on the V8600A PCB. See "Fixed baud rate option" for details.

Controller. The controller is responsible for processing text and commands from the host and converting input text into speech. Tone generation and I/O port flow control are also performed by the controller.

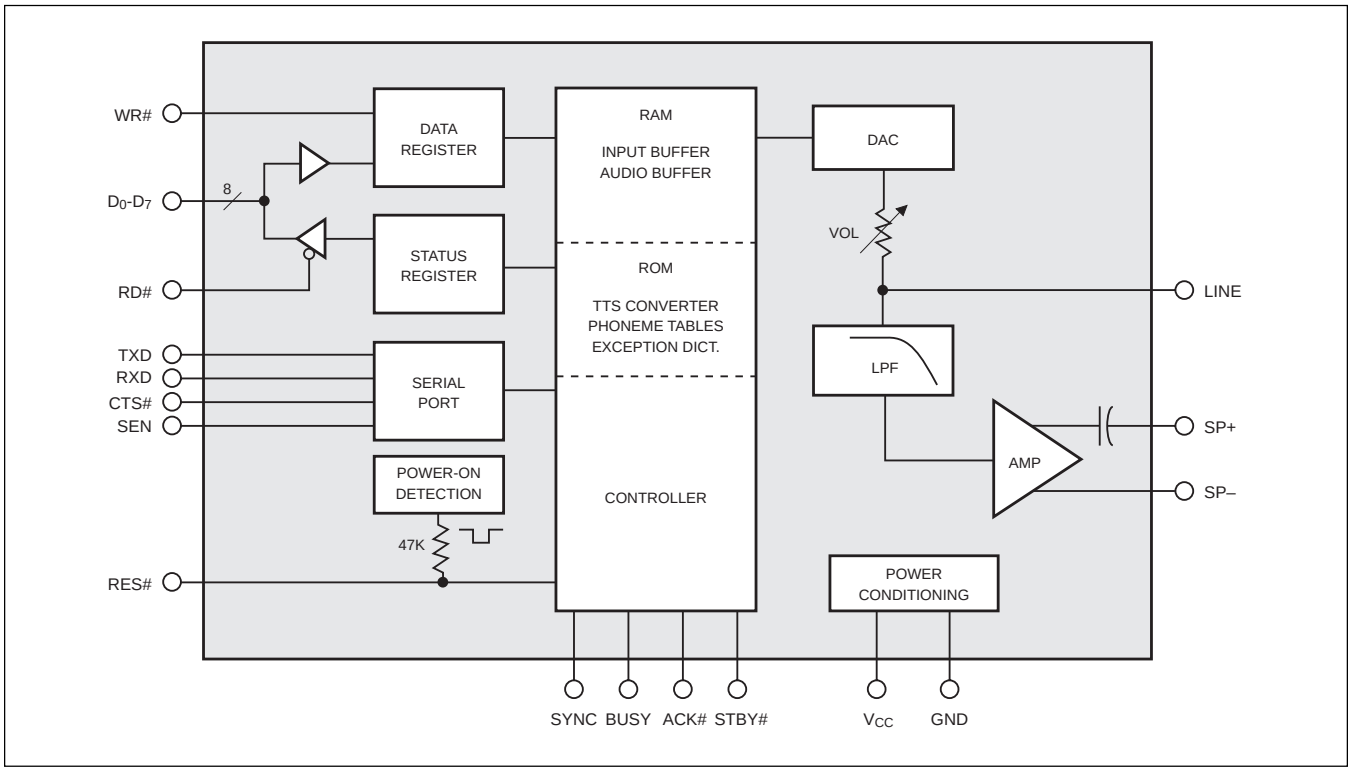
ROM. The ROM contains the internal operating system and text-to-speech algorithms. Some of the ROM is re-writable and used for storing pre-recorded PCM encoded speech, user dictionary and custom settings.

RAM. A 4K x 8 volatile static RAM provides storage for the input text buffer, and a 1K audio sample buffer for the DAC and tone generators. Approximately 2K bytes are available for the input buffer.

DAC, LPF. An eight bit digital to analog converter converts the digital speech samples from the Controller into a low level analog signal, which is presented to the input of an antialiasing, four-pole low pass filter (LPF). The filter cutoff frequency is nominally 3.5 kHz.

Amp. The amplifier takes the smoothed signal from the LPF and boosts the power to a level sufficient to drive an 8 ohm speaker. High efficiency and noise rejection are achieved with the bridge-tied-load output configuration.

BLOCK DIAGRAM

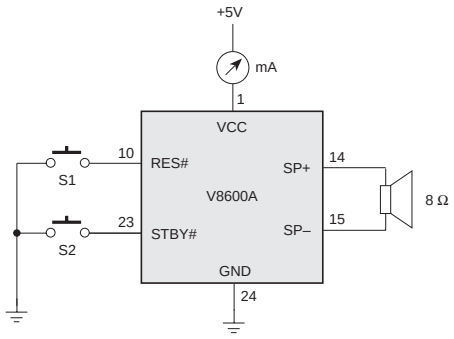


ABSOLUTE MAXIMUM RATINGS†

Supply voltage, V_{CC} . . . . . –0.3 V to +6.5 V
DC input voltage, V_I . . . . . –0.3 V to V_{CC} + 0.3 V
Operating temperature, T_A . . . . . 0°C to +70°C
Storage temperature, T_S . . . . . –55°C to +125°C

†Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEST CIRCUIT



Pressing S1 then S2 for < 0.25 sec causes message to be spoken

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input voltage, Low	–0.3		0.8	V	
V_{IH}	Input voltage, High	2.8		V_{CC} + 0.3	V	
V_{HYR}	Input hysterisis, RES#	0.2		1.8	V	
V_{OL}	Output voltage, Low					
	D_0-D_7			0.3	V	I_{OL} = 6 mA
	All other outputs			0.5	V	I_{OL} = 2 mA
V_{OH}	Output voltage, High					
	D_0-D_7	V_{CC} – 0.5			V	I_{OH} = –6 mA
	All other outputs	V_{CC} – 0.5			V	I_{OH} = –2 mA
I_{IL}	Input current, Low					
	D_0-D_7			–10	µA	V_I = 0 V
	All other inputs			–120	µA	V_I = 0 V
I_{IH}	Input current, High			10	µA	V_I = V_{CC}
I_{OZ}	Output leakage current, D_0-D_7			±5	µA	V_I = 0 to V_{CC}
R_L	Output load impedance, SP+, SP–	8			Ω	
P_{OUT}	Speaker peak output power			500	mW	R_L = 8 Ω
I_{CC}	Supply current					All outputs open;
	Active		22	55	mA	all inputs = V_{CC}
	Idle		1	3	mA	
	Sleep/Standby		50	100	µA	

AC CHARACTERISTICS

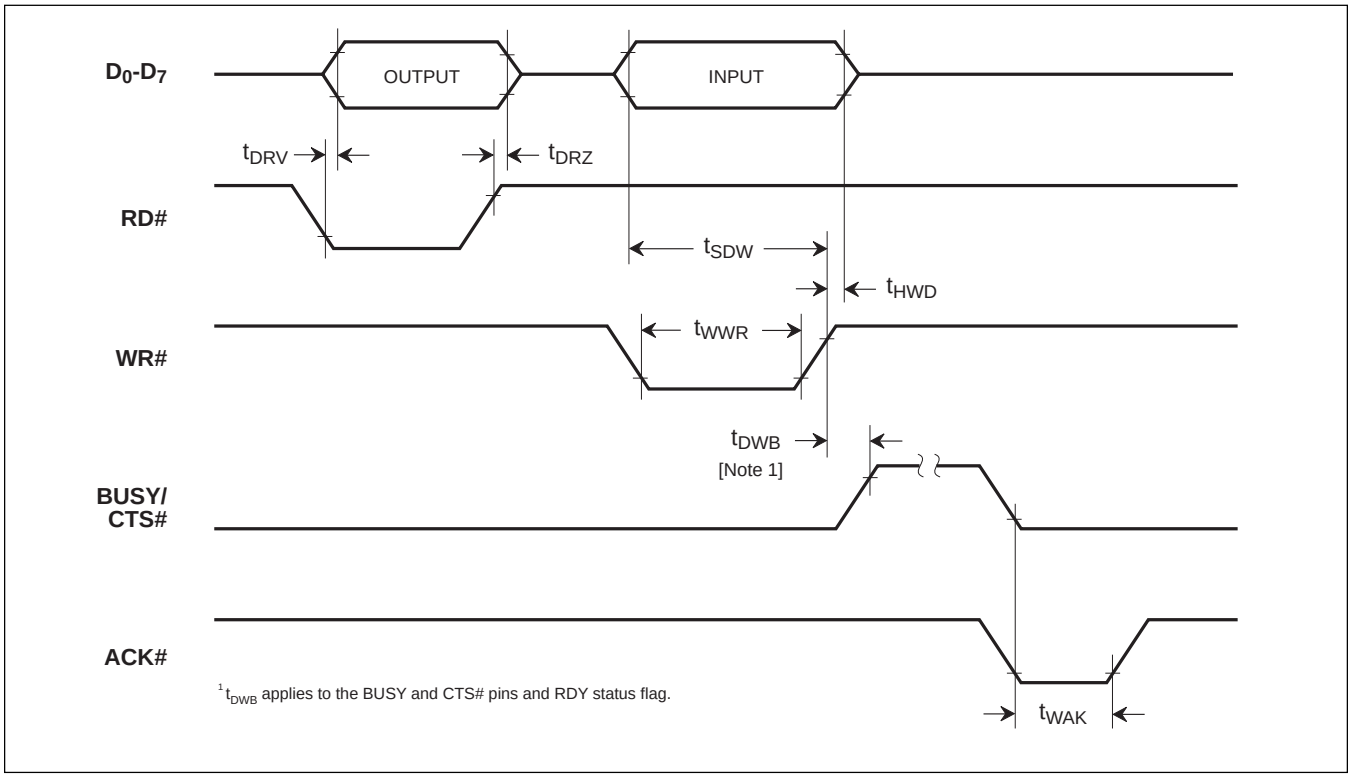
T_A = 0°C to +70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{DRV}	RD#↓ to Data valid delay		25	61	ns	
t_{DRZ}	RD#↑ to Data float delay		23	61	ns	
t_{SDW}	Data setup to WR#↑ delay	25			ns	
t_{HWD}	Data hold from WR#↑ delay	5			ns	
t_{WWR}	WR# pulse width	250			ns	
t_{DWB}	WR#↑ to BUSY↑, CTS#↑ delay			15	µs	Note 1
t_{WAK}	ACK# pulse width		9		µs	
t_{WRS}	RESET# pulse width	3			µs	After V_{CC} stable [2]
t_{DRR}	RESET# recovery delay			2	ms	Note 3

[1] Applies to the BUSY and CTS# pins and RDY status flag.
[2] Reset timings apply only when Reset is driven from an external source. The V8600A contains an internal power-on reset circuit, thus Reset may be left unconnected.
[3] V8600A performs internal initialization; all logic outputs will be floating (except ACK#, which will be High) and the status flags undefined. Do not attempt to send data to the V8600A during this period.

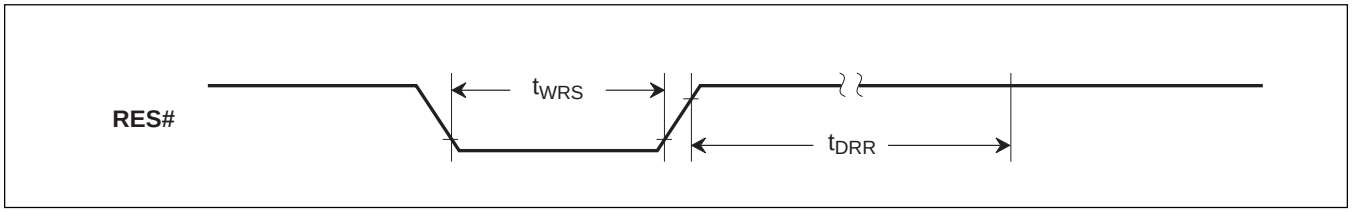
TIMING DIAGRAMS

Read/Write



TIMING DIAGRAMS, CONT'D

Reset



INTERFACING THE V8600A

The V8600A includes microprocessor bus, printer, and serial interfaces. Detailed schematics illustrating their uses are shown in the Application Examples.

Microprocessor Bus Interface

In the microprocessor bus configuration, the V8600A is connected to the microprocessor in the same manner as a static RAM. The microprocessor's read and write signals control all transactions with the V8600A over the system data bus. The CS# signal is derived from the system's address decoding logic. The V8600A can also be mapped into the system's I/O space in a similar manner.

Prior to each write to the V8600A, the host processor should read the V8600A's status by performing a read operation (RD# = Low). The definition of each status bit is described below.

V8600A Status Bits

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	SYNC	SYNC	RDY	AF	AE	STBY	0

SYNC. The SYNC bit has the same meaning as the SYNC pin. When set to 1, it means that the V8600A is producing output. SYNC drops to 0 immediately after output has ceased.

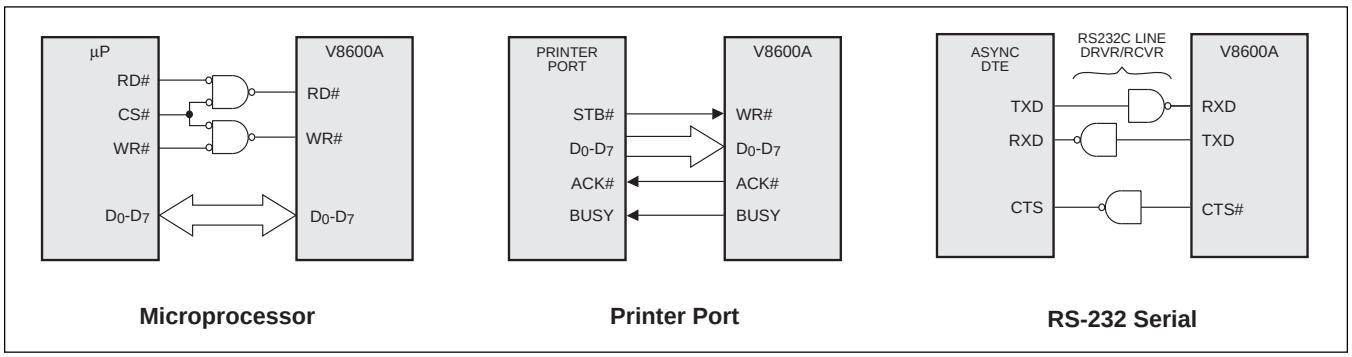
RDY. The RDY bit has the opposite meaning of the BUSY pin. When RDY is set to 1, the V8600A is ready to accept data. RDY drops to 0 momentarily after each write operation over the Data Bus, acknowledging receipt of each character.

AF. This bit is set to 1 when less than 100 bytes are available in the input buffer, indicating that the buffer is almost full. AF is always 0 in the PCM modes and when using the musical tone generator.

AE. This bit is set to 1 when less than 100 bytes are remaining in the input buffer, indicating that the buffer is almost empty. AE is always 1 in the PCM modes and when using the musical tone generator.

STBY. This bit is set to 1 when the V8600A is in Standby mode.

TYPICAL INTERFACES

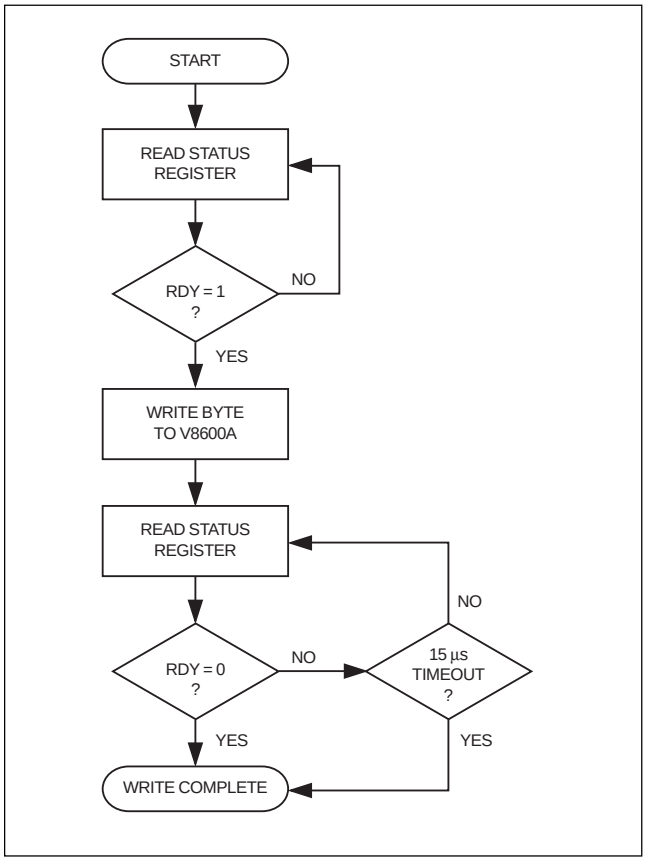


The flowchart below illustrates the recommended method of writing data to the V8600A's microprocessor interface. This method should be used for writing all types of data, including text, commands, tone generator and real time audio data.

Note from the AC Characteristics that the V8600A can take up to 15 µs (t_{DWB}) for each byte to be accepted. Because of this, it is imperative that the driver wait for RDY to drop to 0 after each byte is written. The reason for this is to avoid overwriting the byte just written the next time the routine is called, which can result in the loss of data. Waiting for RDY to drop to 0 ensures that it will not falsely show that the V8600A is ready for another byte the next time the output routine is called.

If a system interrupt can occur while waiting for RDY to become 0, or if RDY cannot otherwise be checked at least once every 8 µs, a software timeout should be enforced to avoid hanging up in the wait loop. The time RDY stays 0 is relatively short (8 µs min.) and can be missed if interrupted. The timeout should be at least 15 µs, which is the maximum time for RDY to drop to 0 after writing a byte of data. In non time-critical applications, the output routine could simply delay 15 µs or longer before exiting, without checking for RDY = 0 at all.

MICROPROCESSOR DRIVER FLOWCHART



Printer Interface

In the printer port configuration, the STB# output from the PC's printer port connects directly to the V8600A's WR# pin. The V8600A's ACK# and BUSY outputs serve as handshaking signals with the PC. It is not usually necessary to utilize both handshaking signals, as they essentially convey the same information (BUSY is used by convention). In this configuration, the host PC simply prints the ASCII text to be spoken to the V8600A.

Serial Interface

The V8600A's asynchronous serial port enables the V8600A to be used with a microprocessor or PC's communications port. This port operates with 8 data bits, 1 or more stop bits and no parity. Baud rate selection can be either automatic or jumper selectable. In this configuration, the host system simply outputs the ASCII text to be spoken to the V8600A.

Because the V8600A's serial port I/O pins operate at TTL levels, the addition of (at most) two RS-232 line drivers and one receiver will be necessary if the host system operates at RS-232 voltage levels. Numerous 5 V-only transceiver chips are available that generate the ±10 V RS-232 voltage levels from the system's +5 V supply. See "RS-232 transceiver option" for more information.

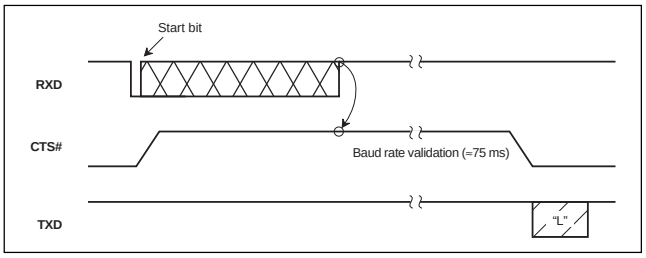
Baud rate detection

The V8600A includes an automatic baud rate detection mechanism, enabling it to operate at any standard baud rate between 300 and 115200 bps. The baud rate is determined from the first character received on the RXD pin, based on the shortest High or Low period detected in the input stream. This period is assumed to be the bit rate of the incoming data.

In order for the V8600A to determine the incoming baud rate, there must be at least one isolated "1" or "0" in the input character. The CR character, 0Dh, is recommended for locking the V8600A's baud rate. The character is not otherwise processed by the V8600A; it is discarded.

If the measured bit period corresponds with a valid baud rate, the V8600A transmits the ASCII character "L" on the TXD pin, providing acknowledgment of lock acquisition.

BAUD RATE DETECTION TIMING



Note: The measurement cycle ends when there have been no High-to-Low nor Low-to-High transitions on the RXD pin for at least 75 ms. Consequently, the V8600A will ignore any data sent to it for a period of 75 ms after the "lock-on" character has been received. The CTS# pin is driven High during this time, and the acknowledgment character is not transmitted until the V8600A is actually ready to accept data.

Fixed baud rate option

If automatic baud rate detection is not desired, the baud rate may be set via jumpers JP1, JP2, and JP3 on the V8600A PCB. The accompanying table lists the jumper connections for all of the V8600A's supported baud rates.

Note: The copper trace connecting jumper pins 1-2 must first be cut on the PCB, if that jumper is to be changed to pins 2-3. For example, to set the baud rate to 9600, cut the trace connecting JP2 pins 1 and 2 and install a jumper between pins 2 and 3.

RS-232 transceiver option

The V8600A's serial port operates at 0/+5 V levels, which is directly compatible with most microcontroller and microprocessor serial ports. If an RS-232 connection is required, such as to a PC's communications port, an RS-232 transceiver is required to convert the 0/+5 V levels of the V8600A to the ±10 V voltage levels of the RS-232 port. The transceiver may be located on the board to which the V8600A is mounted, or on the V8600A PCB itself.

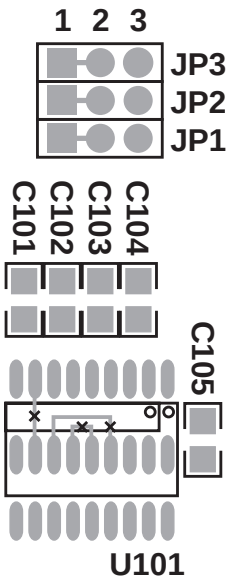
The V8600A supports four of the more popular RS-232 transceiver chips. The industry standards MAX202 or MAX232A are the most economical choices, but neither can be shut down through the V8600A's SEN pin. For power-sensitive applications the MAX222 or MAX242 should be used, because they can be shut down via the SEN pin. All transceiver chips require that C101 through C105 be installed.

SPEAKER CONSIDERATIONS

An often taken-for-granted component of voice synthesis systems is the speaker. Considering how greatly the overall sound quality can be affected by the size and quality of the speaker used, it is usually prudent to test several different speakers under actual operating conditions, before making a final selection. Medium-size (3" to 5") speakers are ideal for speech reproduction, while smaller speakers (such as the common 2" garden-variety type) suffer from lack of sufficient bass response to accurately reproduce the speech signal. If room permits in your application, use a high-quality speaker with good low-end response. Adding baffling around the speaker can also help.

Don't overlook the Tone control (*n*X command) built into the V8600A. If you must use a small speaker, setting the Tone to the bass setting (0X) can help pick up the slack of the poor low-end response of the speaker.

PCB SERIAL PORT OPTIONS



C101 through C105 are 0.1 µF 0805 ceramic chip capacitors. U101 may be a MAX202/232A (SO-16 narrow package) or MAX222/242 (SO-18 wide package). *Copper tracks marked with "X" must be cut before installing U101.*

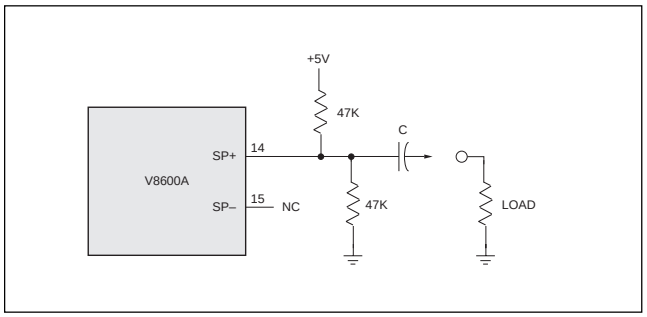
JP3	JP2	JP1	Baud Rate
2-3	2-3	2-3	300
2-3	2-3	1-2	600
2-3	1-2	2-3	1200
2-3	1-2	1-2	2400
1-2	2-3	2-3	4800
1-2	2-3	1-2	9600
1-2	1-2	2-3	19200
1-2	1-2	1-2	Automatic (default)

APPLICATION EXAMPLES

Driving Single-Ended Loads

Single-ended (ground-referenced) loads may be driven directly from the V8600A's SP+ pin. However, a noticeable "click" may be present when speech begins and ends. The circuit shown here will help minimize this effect by keeping the SP+ pin biased at $V_{CC}/2$. The value of C will depend on the impedance of the load—100 µF minimum for 8 ohm loads.

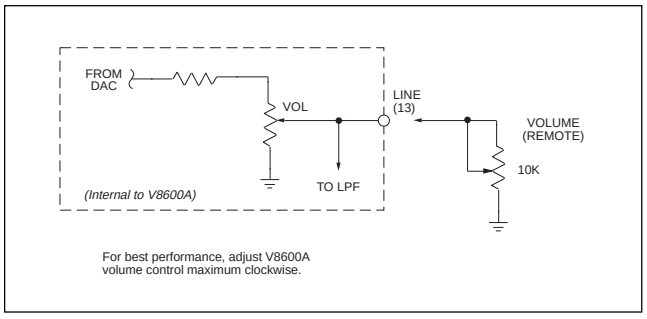
DRIVING SINGLE-ENDED LOADS



Remote Volume Control

Although the V8600A has no provision for an off-board volume control, one can be used by connecting a 10K pot between the Line pin and ground. For maximum dynamic range, the V8600A volume control should be adjusted fully clockwise.

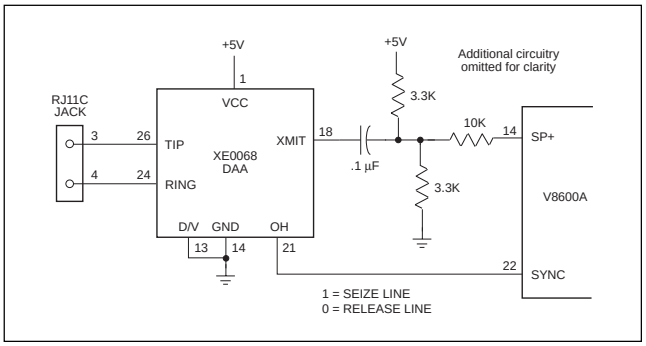
REMOTE VOLUME CONTROL



Phone Line Interface

This is a suggested circuit for applications requiring connection to a telephone line. The XE0068 is an FCC Part 68 approved telephone line interface, available from Xecom (408 945-6640). The PCB layout should employ power and ground planes to minimize coupling of switching noise in the audio path.

PHONE LINE INTERFACE

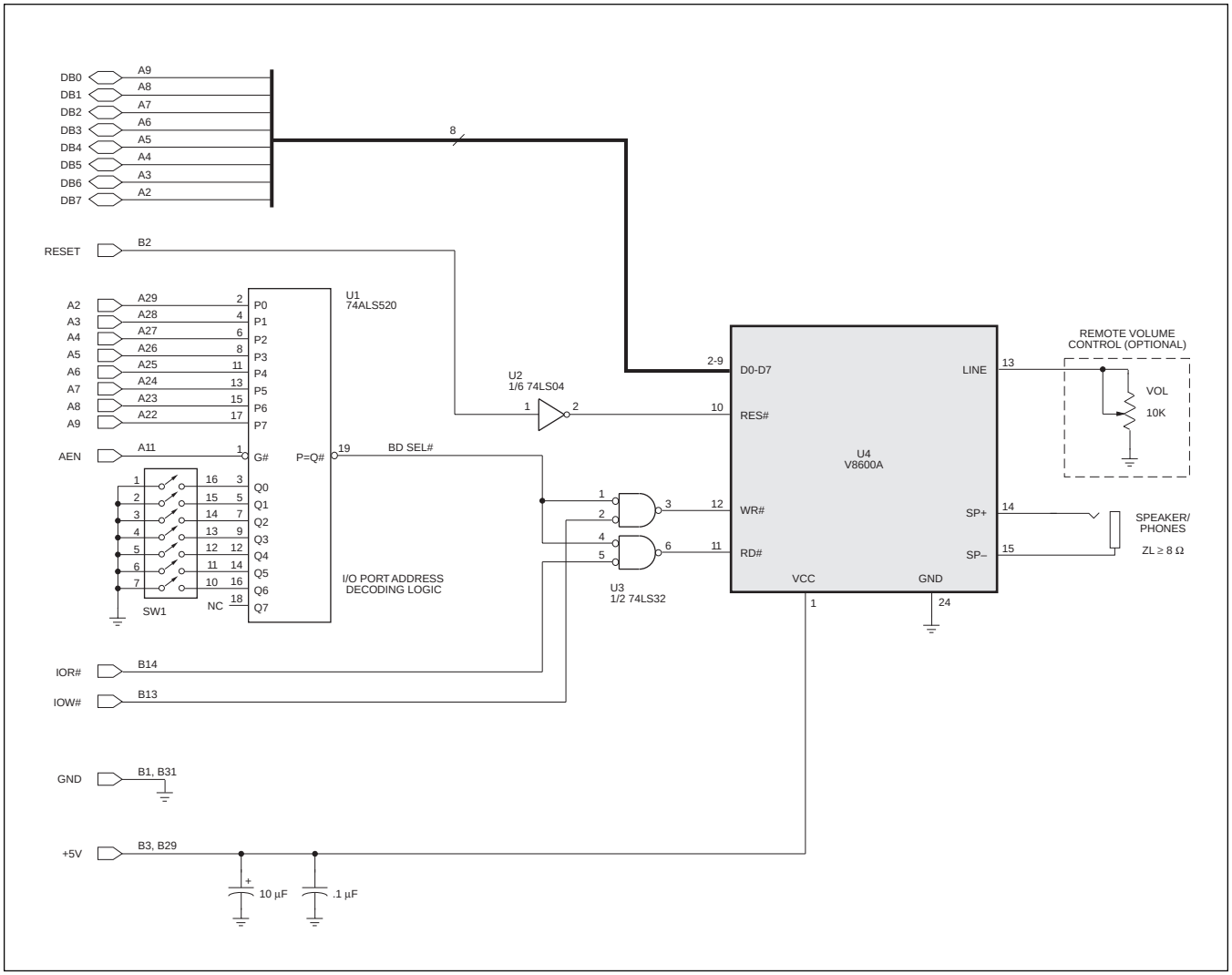


APPLICATION EXAMPLES, CONT'D

ISA Bus Synthesizer

A PC-compatible (ISA bus) synthesizer can be constructed using the V8600A and a small amount of glue logic. In this implementation, the board is mapped into the system as an IO port. Switch bank SW1 selects the I/O address the board will use.

ISA BUS SYNTHESIZER



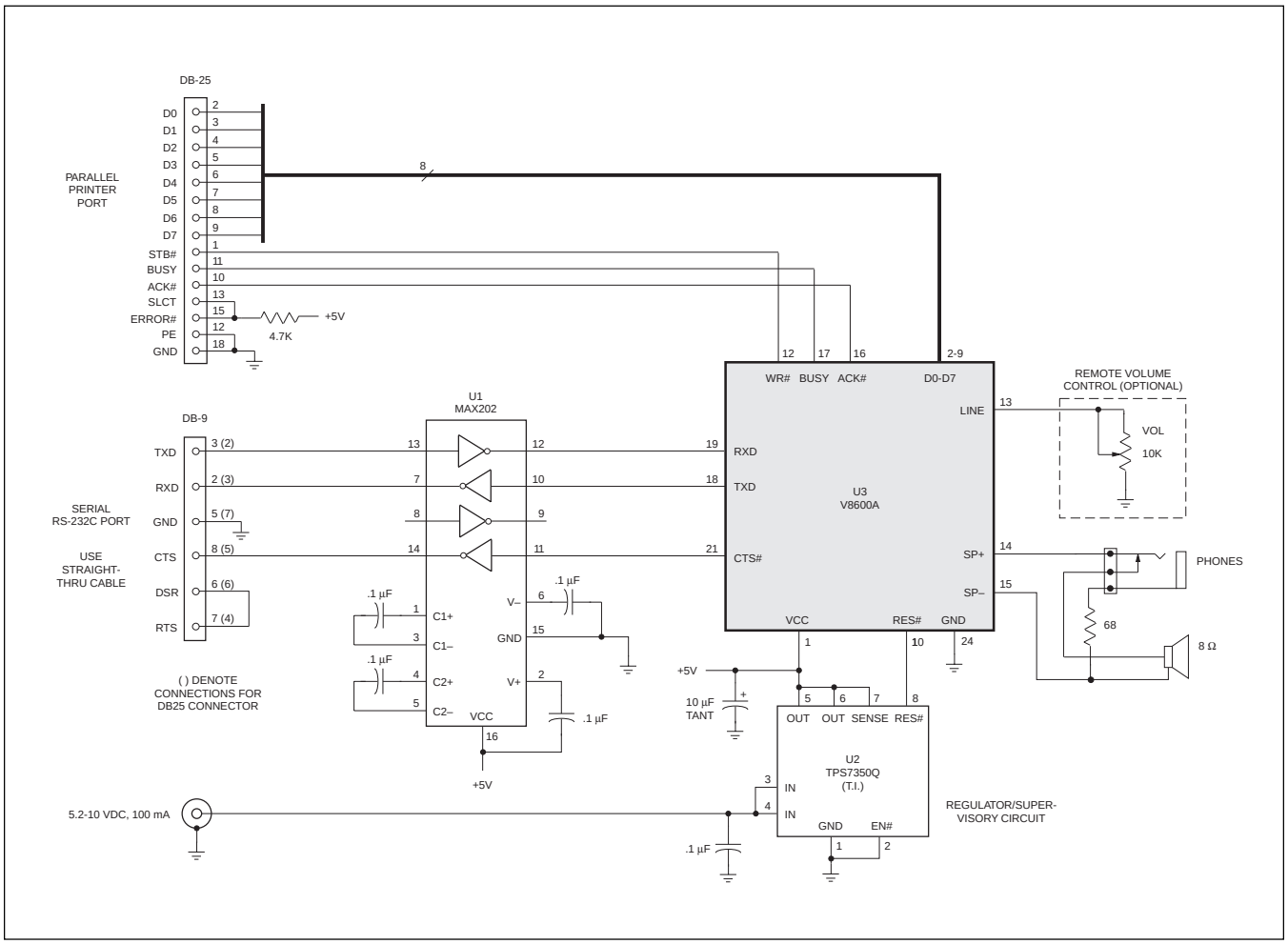
APPLICATION EXAMPLES, CONT'D

Stand-Alone Synthesizer

This circuit shows how a complete stand-alone synthesizer can be constructed using only the V8600A and two inexpensive support chips—a MAX202 (a low cost version of the industry standard MAX232) to convert the serial RS-232C signal levels to and from TTL levels, and a Texas Instruments TPS7350Q to provide the regulated +5 V supply and system reset signal. The synthesizer can be connected to virtually any source via the serial or parallel ports provided. Because the TPS7350Q has very low quiescent current and dropout voltage (35 mV at 100 mA), and constantly monitors the output voltage, this circuit is ideal for battery-powered applications.

The 68 ohm resistor at the headphone jack provides balance between relative speaker volume and headphone volume. It also improves headphone S/N ratio, provides short-circuit protection, and gives wider, useful dynamic range of the volume control.

STAND-ALONE SYNTHESIZER

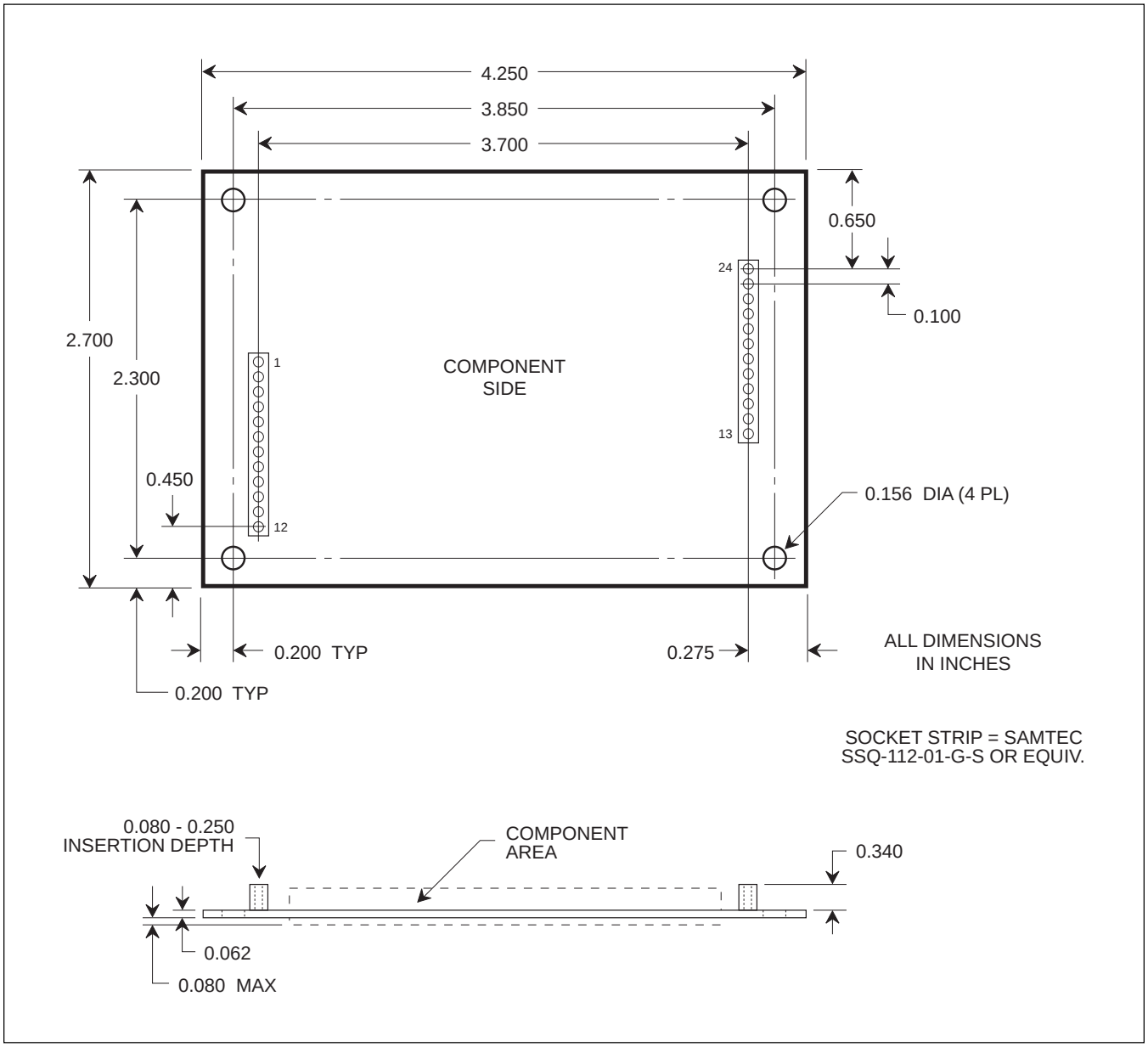


MECHANICAL DATA

All connections to the V8600A are made through two standard 12-pin socket strips. The socket strips mate with any of the popular 0.025" square post headers with 0.100" center pin spacing. The posts generally can be of any height necessary to provide clearance between the V8600A and components on the host PCB. All socket contacts are gold plated.

The V8600A may be secured to the host board with self-locking nylon standoffs or threaded spacers at the four corner mounting hole locations.

MODULE DIMENSIONS



COMPARISON OF THE V8600A AND V8600/V8601

Item		V8600A	V8600/V8601
I/O pins	Pin 23	STBY#: multifunction standby/test	TEST: perform self-test
	Pin 22	SYNC: set/clear/automatic; programmable polarity	SYNC: automatic, active High only
	Pin 21	Renamed CTS# (Clear to Send)	DTR# (Data Terminal Ready)
	Pin 20	SEN (Serial Enable)	DSR# (Data Set Ready)
Memory	Input buffer	2.0K	V8600: 2.7K V8601: 26K
	Exception dictionary	16K non-volatile (*Note:* internal format of dictionary has changed; V8600 dictionaries must be recompiled)	V8600: 2.7K volatile (shared with input buffer) V8601: 26K non-volatile (shared with input buffer)
	User-settable defaults	Non-volatile, user-definable default settings and greeting message	V8600: none V8601: default settings only
	Recorded sound	Up to 130 seconds	None
Baud rate selection		Automatic, programmable or jumper-selectable	Automatic only
RS-232 transceiver		External or on-board	External only
Performance†		Significantly more responsive; entire voice speed range increased	
Status obtainable via serial port†		Speech start = “s” Speech stop = “t” Buffer almost empty (<100 bytes) = “e” Buffer almost full (>1900 bytes) = “f” Baud rate lock confirmation = “l” Sleep mode confirmation = “p”	Speech start = “B” Speech stop = “E” Baud rate lock confirmation = “L” Sleep mode confirmation = “S”
Parameter high/low limits		Wrap or saturate (programmable)	Wrap only
Sleep mode	Enter	Sleep timer or STBY# pin	Sleep timer only
	Exit	RES# or STBY# pins	RES# pin only
Power supply tolerance		5 V ±10%	5 V ±5%
Supply current (typ)	Active	22 mA	48 mA
	Idle	1 mA	15 mA
	Sleep	50 µA	50 µA
Upgrades/updates		Via PC serial port	Must replace EPROM

† In V8600 Compatibility Mode (the default), the V8600A uses the V8600 speed range and status responses.

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