CM47-M66 BOARD USER MANUAL

OVERVIEW

This manual describes how to set up, configure, and utilize CM47-M66. The following topics are addressed in this manual.

— The minimum system requirements to use CM47-M66.
— References to the background and related documentation
— A list of terms used in this Manual
— A description for CopperMagic ADSL chipset
— Block architecture of the CM47-M66.
— A description of other key components
— How to connect a CM47-M66 to your PC
— How to configure a CM47-M66 as an ATU-R
— How to configure an Evaluation Kit's RS-232C serial port for different baud rates
— How to connect a power supply to the CM47-M66
— How to cable Evaluation Kit components
— How to download the Evaluation software to the CM47-M66
— How to test ADSL modem functions like bridge function or gateway functions

MINIMUM SYSTEM REQUIREMENTS

USER PC FOR THE CM47-M66

The requirements for monitoring the operation of CM47-M66 on a PC are

— Pentium processor running at 75MHz or faster
— Microsoft Window 95 operation system or window 98 operating system
— 20MB RAM and 20MB free disk space
— One available UART serial port (Support up to 38,400 baud.)
— VGA graphics monitor and adapter
— Microsoft compatible pointing device
— LAN card (10 or 100BaseT type)

CM47-M66 REFERENCE BOARD

The requirements for operating CM47-M66 are

— AC110~220V Power source and DC+5V out, power adapter
— One CM47-M66 and ADSL CO-side equipment such as DSLAM and RAS (Remote access server)
— Two 10/100BaseT LAN cables
— One RS-232C cables

POWER ADAPTER

— AC Power Input: 110/220V free voltage
— DC Power output: +5V DC regulated voltage, 2A

BACKGROUND AND RELATED DOCUMENTS

ITU G.992.1: G.DMT -1999

ITU G.992.2: G.Lite –1999

ANSI T1.413 issue2

DEFINITIONS, ABBREVIATIONS, AND ACRONYMS

ADC	Analog to digital converter
ADSL	Asymmetric digital subscriber loop
AFE	Analog front end
ATM	Asynchronous transmission mode
ATU	ADSL transceiver unit
ATU-C	ATU at the central office
ATU-R	ATU at the remote end
BSP	Board support package
CM (CopperMagic)	Samsung DSL chipset trademark
CO	Central office, see also ATU-C
DAC	Digital to analog converter
DMT	Discrete multi-tone
Downstream	The transport of data in the ATU-C to ATU-R direction
Embedded software	Software running on the Samsung ADSL chipset (CopperMagic) evaluation board
eoc	Embedded operations channel
EVB	Evaluation board
FDM	Frequency division multiplexing
FEC	Forward error correction
flash memory	Memory that does not need continuous power to retain its contents
FPGA	Field programmable gate array
frequency spectrum	Frequency distribution of all signals that are used during a transmission over a certain line
gain	Transmitted power of the transceiver
host port	Port on the CM47-M66 to which you make a serial connection to PC, enabling an application on the PC to communicate with the CM47/M66
HPI	Host port interface
HyperTerminal	Terminal access program available on windows 95 systems
IC	Integrated circuit
image	Another name for a file that resides in memory or can be copied from one medium to another, for example, from a CD-ROM disk to flash memory
line attenuation	Decrease in the power of a signal across a line
line simulator	Equipment that simulates various (U)ADSL line conditions
loop back	Diagnostic test in which a signal being transmitted is sent back to the receiver
MAC	Media access controller
makefile	Used to compile the coppermagic chipset control software
Mbps	Millions of bits per second
MII	Media independent interface

DEFINITIONS, ABBREVIATIONS, AND ACRONYMS (Continued)

PLL	Phased locked loop
pSOS	Real time operating system from ISI
RAM	Random access memory
PCB	Printed circuit board
ROM	Read only memory
RS-232	Serial communications standard developed for connecting DTE and DCE devices
RT	Remote Terminal, refers to a residence or business connected to a telco. central office. See also ATU-R
RTOS	Real Time Operating System
SNR	Signal-to-noise ratio; ratio of the signal received to the noise or undesired signal, usually expressed in decibels
subcarrier	A user as ADSL broadband access carrier
transceiver	Communication device capable of transmitting and receiving data
UART	Universal Asynchronous Receiver and Transmitter)
upstream	Direction from an ADSL transceiver unit at a remote terminal to an ADSL transceiver unit at a central office
UADSL	Universal ADSL
USB	Universal serial bus
UTOPIA bus	Universal test and operations physical interface ATM (UTOPIA) bus
VCXO	Voltage controlled X-tal (crystal) oscillator
Zh	Hybrid matching impedance network
Zin	Termination impedance network

COPPERMAGIC CHIPSET

CM47-M66 Board is a reference design for ITU-T's G.DMT (G.992.1) compliant external modem and supports to develop an external modem using Samsung CopperMagic chipset which is composed of S5N8947 16/32-bit RISC micro-controller, S5N8950 G.DMT (Discrete Multi-Tone) chip and S5N8951 AFE (Analog front end) chip. This is a cost effective CPE solution for the high speed Internet access ADSL network environment. The followings are some brief descriptions for the Samsung CopperMagic chipset.

S5N8947 16-/32-RISC MCU

S5N8947, 16-/32-bit RISC (ARM7TDMI) micro-controller is cost effective, high performance micro-controller solution for ADSL modem or gateway. The S5N8947 is designed as an integrated Ethernet controller for use in a managed communication hubs and routers. The S5N8947 also provides ATM layer SAR (Segmentation and Re-assembly) function with UTOPIA (the Universal Test & Operations PHY Interface for ATM) Level 2 Interface and Full-rate USB function.

Fearture

- 8-Kbyte unified cache
- SAR (Segmentation and Reassembly)
- UTOPIA (the Universal Test & Operations PHY Interface for ATM) Interface
- 2-channel Ethernet MAC with MII interface
- Full-rate USB controller
- 2-CH GDMA (General Purpose Direct Memory Access)
- UART (Universal Asynchronous Receiver and Transmitter)
- 3 programmable 32bits Timers
- Watchdog timer
- 18 Programmable I/O ports
- Interrupt controller
- I^2C controller
- SPI (Serial Peripheral Interface)
- PCMCIA memory and I/O master modes
- Built-in PLLs for System/USB
- Cost effective JTAG-based debug solution
- Boundary scan
- 3.3V I/Os and 1.8V core operating voltage
- Operating Frequency Up to 72MHz
- 208 LQFP Package

S5N8950 G.DMT DMT CHIP

The S5N8950 is a complete ATM-based rate adaptive G.DMT and G.Lite ADSL solution with an Analog Front-End (S5N8951). The S5N8950 provides all the digital functions such as ATM TC, FEC Codec with interleave/de-interleaver, adaptive QAM codec, FFT/IFFT, equalizers, digital filters and so on. There are four interfaces for direct connection to ATM systems, serial interface for non-ATM applications, 14-bit ADC/DAC interface, and host interface for general CPUs like Intel or Motorola.

Features

- Fully compliant to ITU-T G.DMT, G.Lite and G.hs
- FDM based DMT Line Coding
- Data rate: Up to 10 Mbps for Downstream and 1 Mbps for Upstream.
- Reach: 5.4Km (18Kft) on 26AWG
- Rate Adaptive Modem (Steps of 32Kbps)
- Reed-Solomon Forward Error correction with interleaver.
- Frequency and Time Domain Equalizer.
- Support Fast Retraining Function
- Support Network Management Function
- Support Power Management Function
- Host interface (Intel/Motorola) and ATM (UTOPIA-L2) / non-ATM interface
- 0.18μm, 1.8V CMOS Technology
- Operating Temperature: -40°C to 85°C
- Package type: 176-LQFP

S5N8951 G.DMT AFE CHIP

The S5N8951 (ATU-R & ATU-C) is Analog Front End IC designed for DMT based universal ADSL (Asymmetric Digital Subscribe Line) modems with 0.35μm fully CMOS technology.

It has 25.875 – 138kHz Upstream channel and 142.312 – 1104kHz bandwidth Downstream channel. The S5N8951 includes AGC, LPF, ADC, DAC. The AGC has 42dB gain 0.4dB step in RX mode and -24dB gain 2dB step in TX mode with 12bit/8bit control bit. Anti alias LPF has 1104kHz passband frequency in TX path and 138kHz in RX path. Samsung ADSL AFE chip provides 14bit ADC at 4.416M sample rates and 14bit 4.416MHz DAC.

A 10-bit DAC support VCXO control for timing recovery. The VCXO is generates 35.328MHz. clock PLL-locked with ATI-C Modem.

Features

— Integrated Analog Front End (AFE) for ADSL, ATU-R and ATU-C
— Up to 1104kHz/s down stream and 138kHz/s upstream channel
— 14-bit 4.416MHz/s ADC
— 14-bit 4.416MHz DAC
— 5th-order Low Pass Anti-alias Filter TX/RX paths
— RX: 42dB 0.4dB Step Gain Range with 12-bit control signal
— TX: -24dB 2dB Step Gain Range with 8-bit control signal
— 10-bit 4kHz VCXO DAC
— Fully 0.35um CMOS Technology
— 3.3V Power Supply Operation
— -40°C to 85°C Operating Temperature
— 0.4W Power consumption
— 100TQFP Package

FUNCTIONAL BLOCK DIAGRAM OF CM47-M66

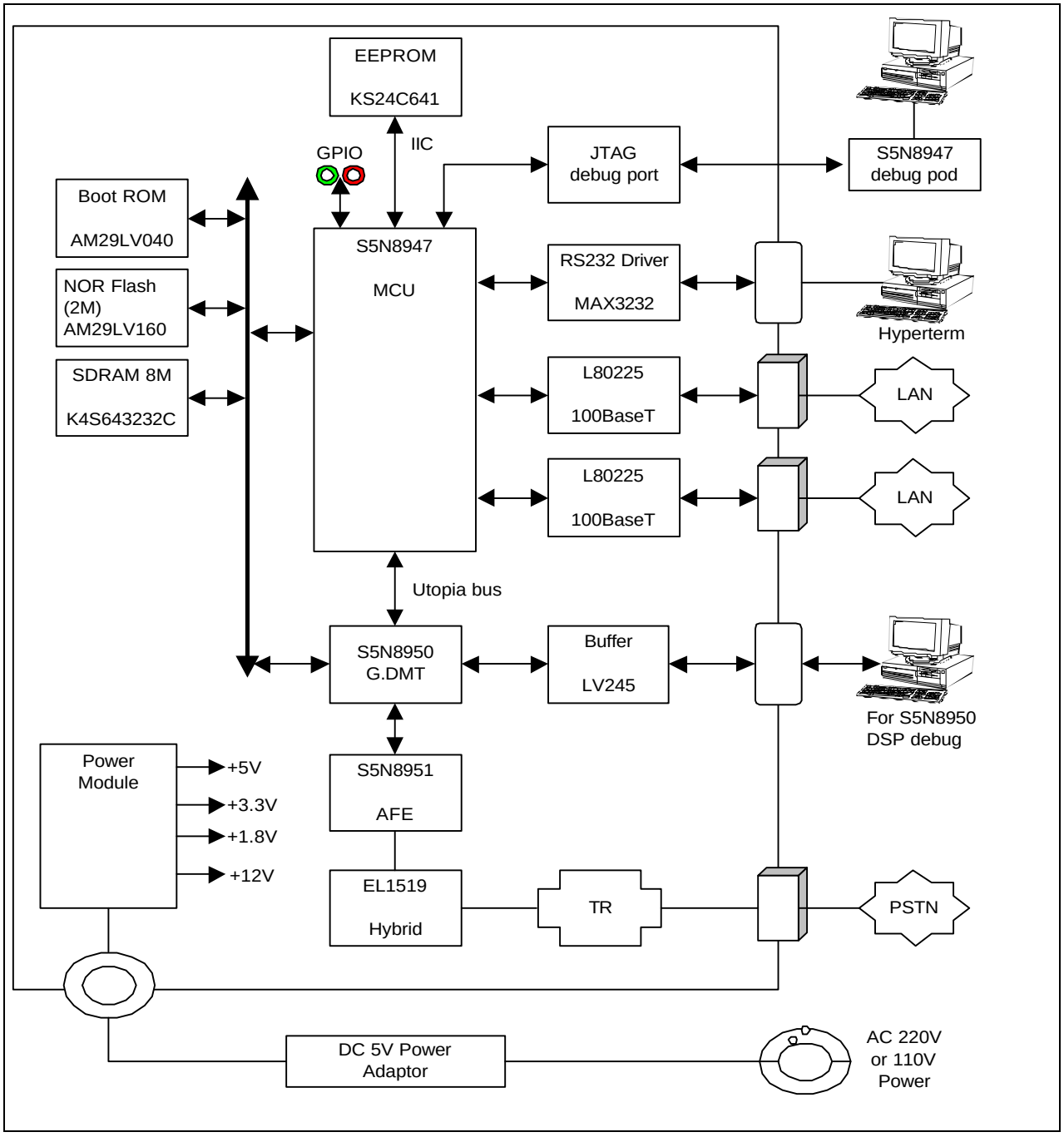


Figure 1. A functional Block Diagram of CM47-M66

OTHER COMPONENTS OF THE CM47-M66

L80225

The L80225 Ethernet interface transceiver made by LSI LOGIC supports 10/100BASE-T Twisted Pair(TP) interface media connections through external isolation transformers. It provides a Media Independent Interface (MII) for easy attachment to 10/100 MAC. The 80225 Ethernet transceiver is easy to connect to the Ethernet MAC contained in the S5N8947 device through MII interface signals without any glue logic.

MAX3232 (SP3232ACN) RS232C INTERFACE

The CM47-M66 Board are controlled and configured by the host PC for the software development. The communications between PC and the Board occurs across the RS232C port.

EL7512C HIGH-FREQUENCY PWM STEP-UP REGULATOR

The EL7512C is a high frequency step-up DC:DC regulator operated at fixed frequency PWM mode. With 1 A MOSFET, it can deliver up to 600mA output current at up to 90% efficiency. The adjustable switching frequency is up to 1.2MHz, making it ideal for DSL applications. So it is used as 12V generator at CM47_M66.

EL1519C LINE DRIVER

The EL1519C contains two wide-band high-voltage drivers. It is used for DMT line driving device in CM47-M66 board. It is designed to drive 15Vp-p signal at 2Mhz into a 200 load differentially with very low distortion. Both amplifiers are of the current-feedback type, giving high slew rates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

K4S643232C SDRAM

The K4S643232C is 64Mbits synchronous high data rate DRAM organized as 4x512Kwords by 32bits.

AM29LV160 FLASH MEMORY

The AM29LV160 is word-wide Flash memory that is16-Mbit densities. They are high-performance memories arranges as 1M words of 16 bits or 2M(1M) byte of 8bits. This data is grouped in thirty-two 64-Kbyte blocks that can be erased, locked and unlocked in system. This product specifically designed for 3 V systems.

AM29LV040 FLASH ROM

The AM29LV040 is a 4Mbit, 3.3 volt-only Flash memory organized as 512Kbyte of 8bits. The 512Kbytes of data are divided into eight sectors of 64Kbytes each. This device is offered in 32-pin PLCC packages. In the CM47-M66 board, there is a 32-pin PLCC socket for this device.

HOW TO CONNECT CM47-M66

FEATURES OF THE CM47-M66

The CM47-M66 provides a complete and convenient evaluation platform for the ADSL application that uses the CopperMagic transceiver.

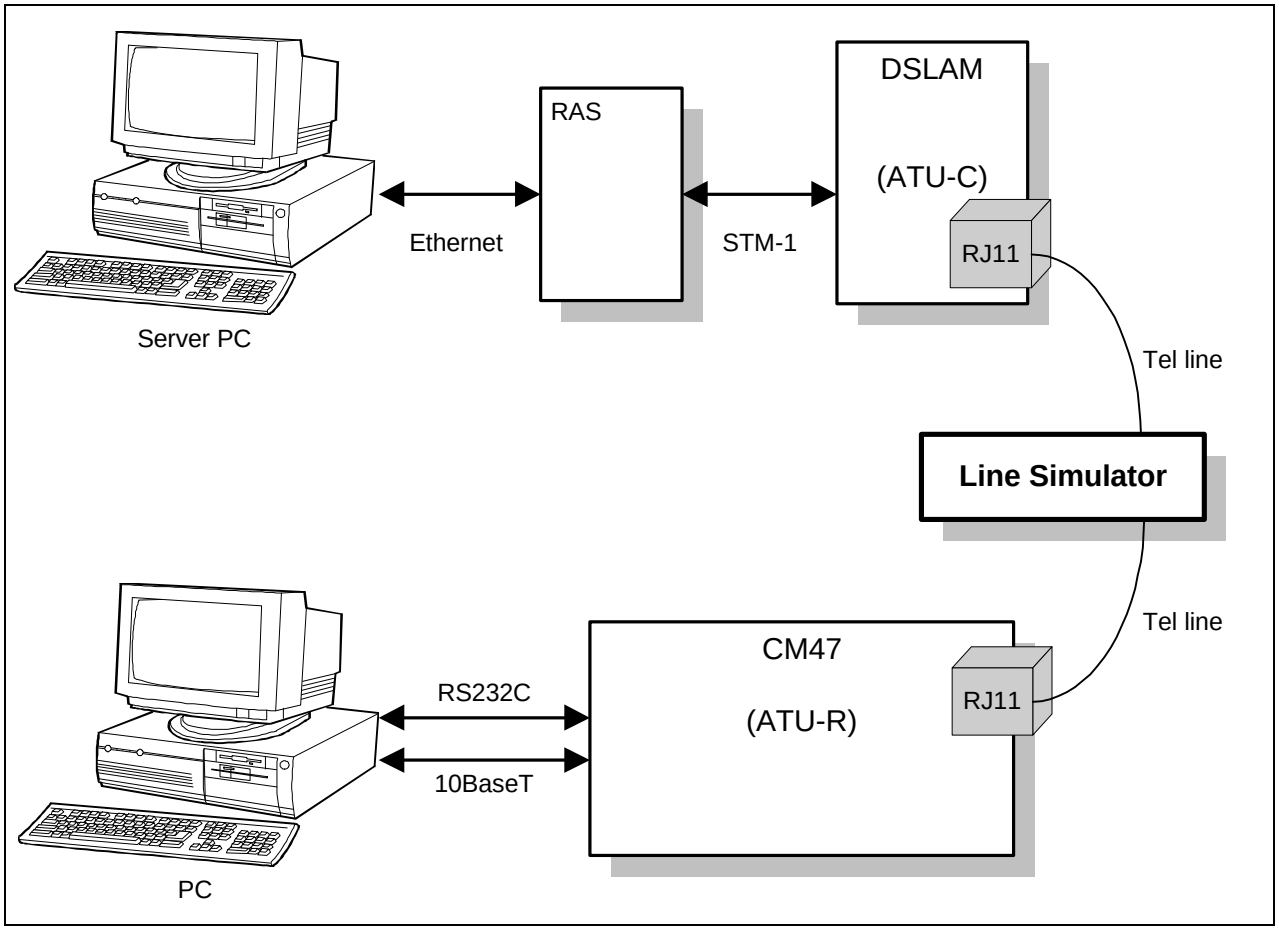


Figure 2. Lab. Test Configuration of CM47-M66 Kit

This diagram describes how S5N8947, S5N8950 and S5N8951 work in the network environment, monitors operation of the chipset, and shows how to apply to the requirement of vendor. We have to prepare for a simple network emulation environment using DSLAM, RAS, server PC and RT modem kit (CM47-M66). The RT modem kit makes a role as a network bridge or a broadband access gateway. The detailed protocol stack is described in the following figures. So both of the server PC and client PC can access each other and Internet through the network of the laboratory. However this network bridge couldn't work well when the data rate of the LAN exceeds the data rate of the ADSL channel. In this case, the evaluation kits has to process the protocol layers so that overflow of any data buffer might not occur. Therefore you must check the condition of the local network bandwidth before we install this evaluation kit.

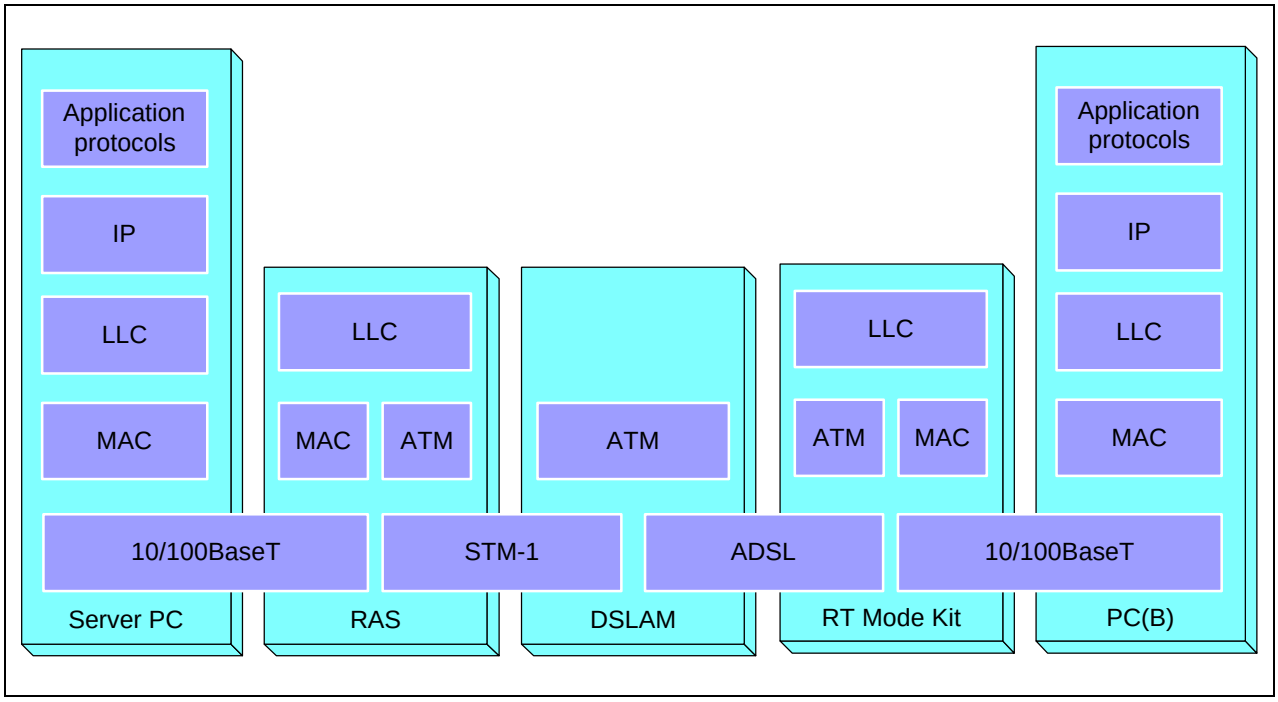


Figure 3. The End-to-End Protocol for the RFC2684 (RFC1483) Bridge Test

In this CM47-M66, the RFC2684 (RFC1483) bridge code is possible to provide. Other gateway solutions such as PPPoE and PPPoA with NAT, PAT and DHCP functions based on the VxWorks THG are prepared for ready to support customers. But the source code is not possible to provide. If you want to get it, please contact WindRiver.

SETUP ACTIVITIES

CHECK PACKING LIST

Check the packaging list delivered with the CM47-M66, to make sure you received all components of the CM47-M66 RT modem kit

- CM47-M66: 1
- DC5V/2A, Power Adapter: 1
- RS232C cable: 1
- Tel line: 1
- Ethernet cable: 1

CONFIGURING THE CM47-M66 KIT

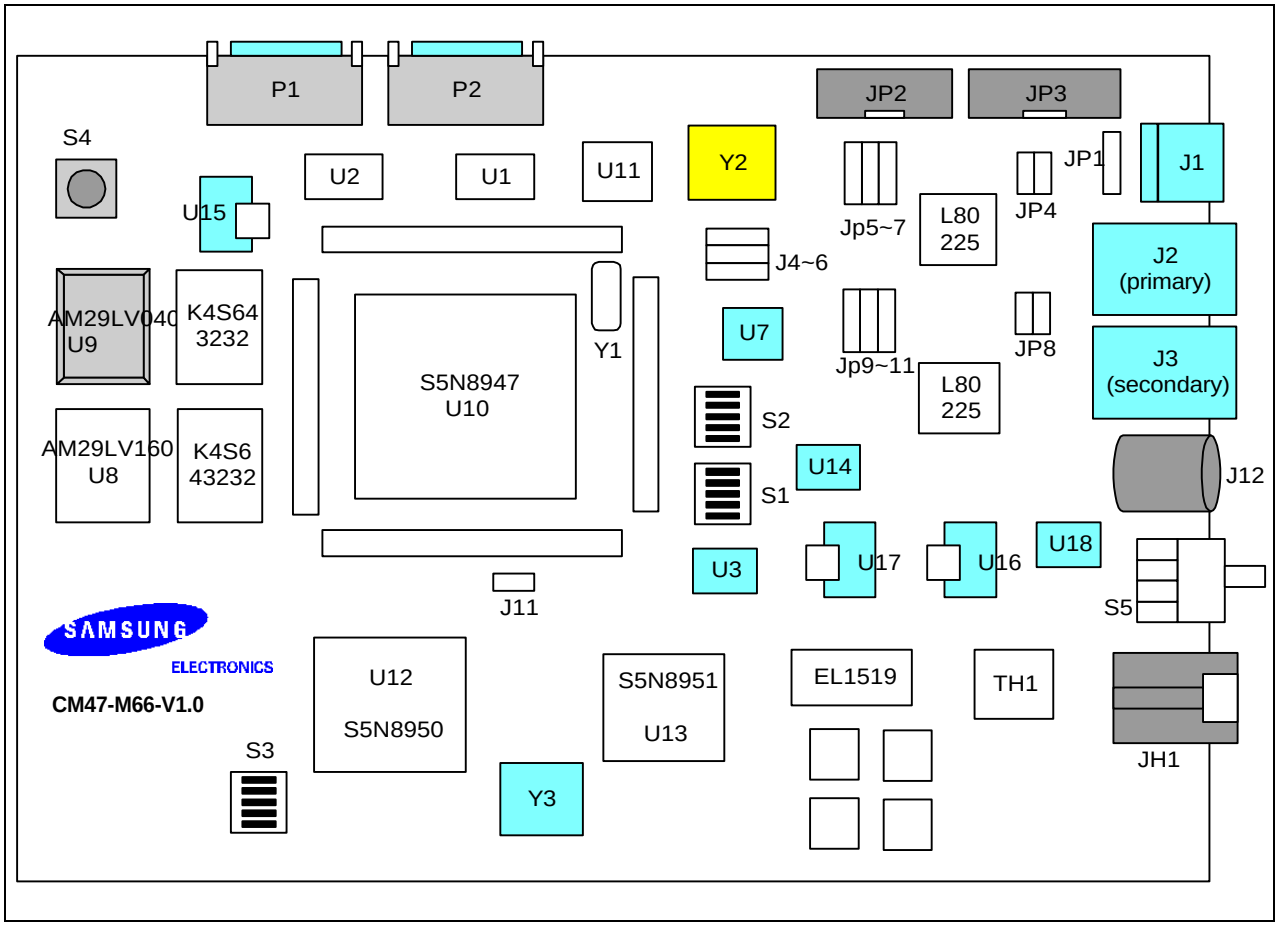


Figure 4. The Locations of the Key Components on the CM47-M66

DIP SWITCH CONFIGURATION

The CM47-M66 provides five switches (see S1~3 and JP4,5,6 and J11 in Figure 4) for configuring some operation options. Typically, the switch positions should be left in the default configuration as shipped. If alternate operation settings are required, refer to the followings.

S5N8950 DMT Chip Debug Mode (Position 3~6 of S3)

Position 5 and 6 of S3 is used for chip test mode**, so you have to keep the position 5 connected and position 6 open when you are testing in normal operation.** And the position 3 and 4 of S3 is used for the DMT debug mode selection. When you are testing in normal operation, **you must keep the position 3 open and the position 4 connected**. Please refer to the following table for more detail information.

NOTE

Position 1 of s3 is not used.

Table 1. DMT Operation Mode Selection

Mode	Position 3 of S3	Position 4 of S3	Position 5 of S3	Position 6 of S3	Remarks
Reset mode	Connect	Connect	Connect	Open	DMT reset
Normal mode	Open	Connect	Connect	Open	Normal operation
Debug mode	Connect	Open	Connect	Open	JTAG debug for DSP
Self-test mode	Open	Open	Connect	Open	Only for chip test

Bus Mode of S5N8950 (Position 2 of S3)

Position 2 of S3 must be connected. (This means Motorola MC68000 bus mode)

The bus configuration of host processor in demo program is set to motorola bus mode.

UTOPIA Address Set (J11)

The S5N8947 provides only 2bits of UTOPIA Address signals but the S5N8950 has 5bits of UTOPIA address signals. So it is possible to set the upper 3bits (UTO_ADD[2-4] signals in circuit diagram) of UTOPIA Address to all 1, like “111” or all 0, like “000” using J11. The default setting is all 0. So you have to connect the position 1 and 2 of J11.

MCU Operating Clock Mode (J4-5)

Using jumper J4 and J5, the operating clock frequency of S5N8947 is selected. It is recommended to use 66MHz or 66MHz-clock mode. Direct clock mode is possible to operate the MCU but it is impossible to use USB function block except 48MHz operation. However, there are some constraints on using 72MHz- clock mode and 66MHz-clock mode. It must be kept within 40pF load capacitance of Address and Data bus of S5N8947 to run S5N8947 on 72MHz. And It is also must be kept within 60pF load capacitance of the bus to run S5N8947 on 66MHz.

Table 2. MCU Operating Clock Mode

Clock Mode	J4: TMODE	J5: CLKSEL	Remarks
66MHz	Connect 2-3 position	Connect 2-3 position	Using Y1 or Y2 12Mhz clock source
72MHz	Connect 1-2 position	Connect 2-3 position	Using Y1 or Y2 12HHz clock source
Direct clock	Connect 2-3 position	Connect 1-2 position	Using U11 Oscillator, cannot use USB function

MCU Function Mode Selection (J6)

S5N8947 provides two kinds of operating configuration such as 2 MAC operating configuration and 1 MAC and PCMCIA operating configuration. But it is not possible to use these two operating configurations at the same time. So, you have to select the operating mode using FMODE pin of S5N8947 or selecting J6 jumper.

Table 3. MCU Function Mode Selection

S5N8947 Operating Mode	J6: FMODE Pin	Remarks
2 MAC operating mode	Connect 1-2 position (High)	
1MAC operating mode	Connect 2-3 position (Low)	

It is strictly required to check the DIP switches S1 and S2 are set to On state when 2nd MAC is used. Also it is required to check the DIP switch S1 and S2 are set to OFF state when PCMCIA or other GPIO port is used instead of 2nd MAC.

— It is also possible to design PCMCIA using external I/O access and GPIO signals when using 2 MAC operating mode.

PHY (80225) Jumper Setting (JP5~7, JP9~11)

Table 4. PHY Jumper Setting

Jumper	Description	Connect 1-2 Potion (Low)	Connect 2-3 Potion (High)
JP5,JP9(2nd PHY)	SPEED	10Mbps	100Mbps
JP6,JP10(2nd PHY)	AutoNegotiation	AutoNegotiation Off	AutoNegotiation On
JP7,JP11(2nd PHY)	Duplex	Half Duplex	Full Duplex

MCU-2nd PHY Connection DIP Switch (S1 and S2)

If these switches are on state, the GPIO pins of S5N8947 are connected with MII interface signals of L80255 Ethernet PHY. Therefore it is required to keep these switches OFF state when CM47-M66 reference board is operating on 1 MAC operating mode

INSTALLING THE CM47-M66 SOFTWARE

INTRODUCTION

The CM47-M66 uses the pSOS real time operating system (RTOS) to control the CopperMagic chipset and other devices. The operating system must be updated by downloading a pSOS image during the following circumstances:

— A new version release of CopperMagic evaluation control software.

— The CopperMagic evaluation control software becomes corrupted.

Download the CopperMagic Evaluation Software

Verify if the Cabling was Completed

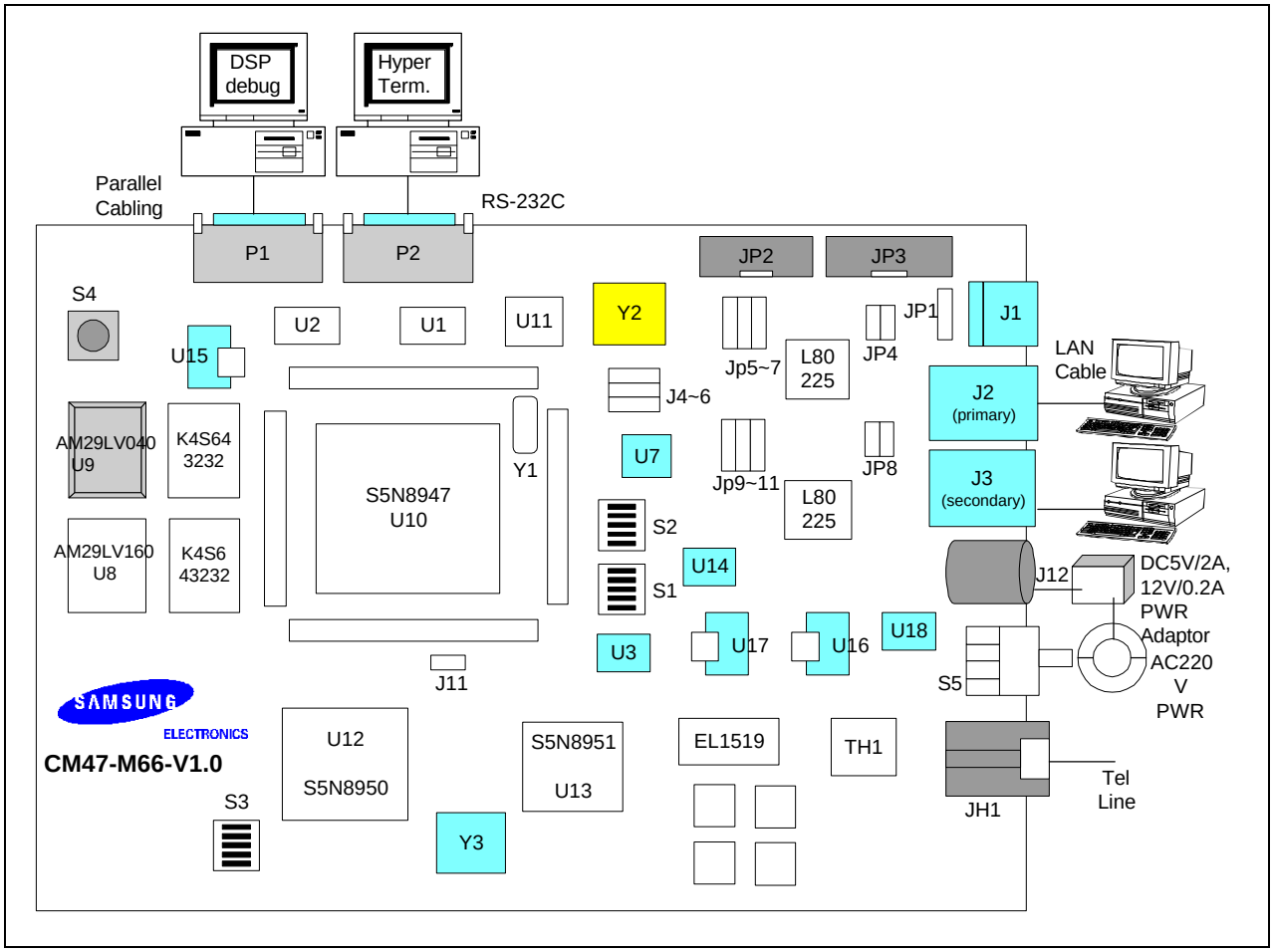


Figure 5. Cabling Diagram to Get Ready to Enable the CM47-M66

J1: USB Jack for USB connectivity. (Now we are preparing USB modem solution).

J2: 10/100BaseT LAN Jack. If you want to connect PC directly you have to use flat cable J2 connector of CM47-M66 board is network type Ethernet connector. This port is primary Ethernet interface.

J3: 10/100BaseT LAN Jack. If you want to connect PC directly you have to use flat cable.
J3 connector of CM47-M66 board is network type Ethernet connector. This port is secondary Ethernet interface.

P1: RS232C Connector for console.

P2: Teaklite DSP (inside S5N8950) debug connector. It is needed to equip with Teaklite debug environment in your PC if you try to debug the S5N8950.

J12: Power Jack. It requires DC 5V/2A Power Adaptor.

JH1: Tel line jack.

Check the Figure 5 and verify if the CopperMagic Evaluation Kit is ready to test and download the CopperMagic Evaluation Software.

Enable your PC Communication Software

Any serial terminal emulation software may be used to communicate with the CM47-M66. The following procedure uses HyperTerminal, which comes with Windows 95/98 or Windows NT. The CM47-M66 will communicate at 38,400baud rate, eight bits, no parity, one stop bit, no flow control with default mode.

Connect your Power Adapter to CM47-M66

Now you are ready to test and turn on your power supply, then the CM47-M66 starts to run and display the following message to your HiperTerminal window.

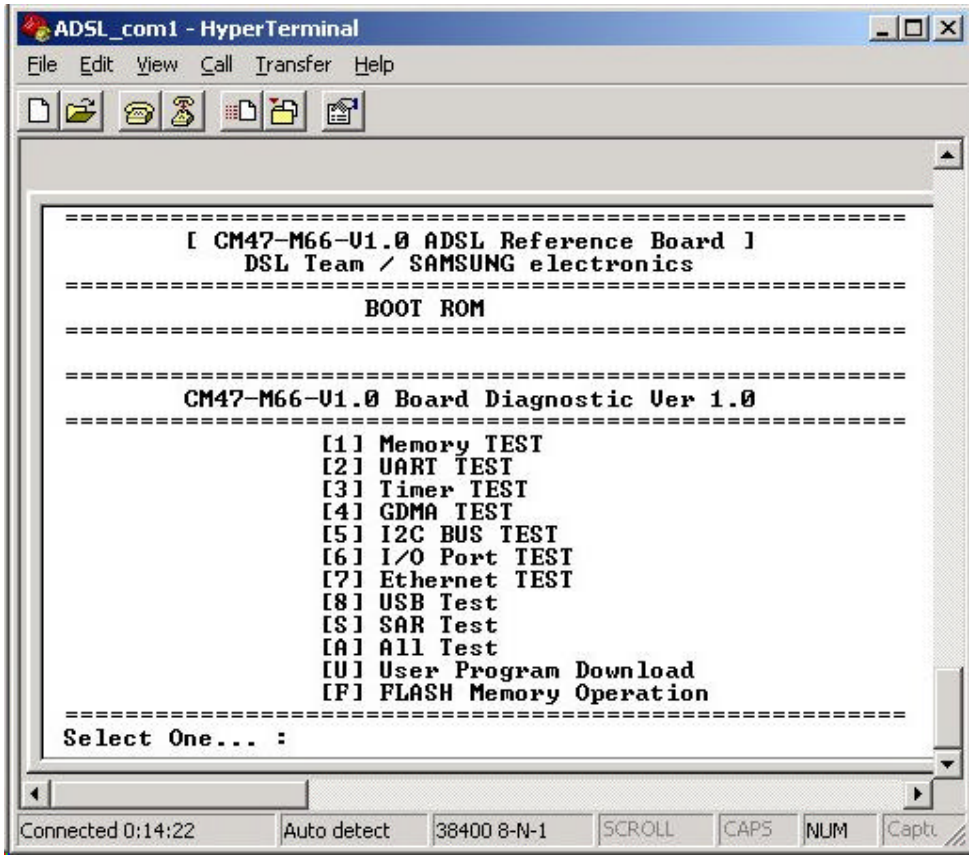


Figure 6. Hyperterminal Window Display When Initializing CM47 Reference Board

STARTING THE COPPERMAGIC EVALUATION SOFTWARE

Now, we are going to start running the G.DMT Modem. Check the connection between CO DSLAM and RT modem kit before running the kit. Let us review the details of the initialization procedure between CO DSLAM and RT kit.

CM47: PPPoE Solution (Remote Access Network Environment)

If you are equipped with remote access server (RAS) environment like below figure, you can access Internet or other WAN network using PPPoE protocol solution or other protocol solutions.

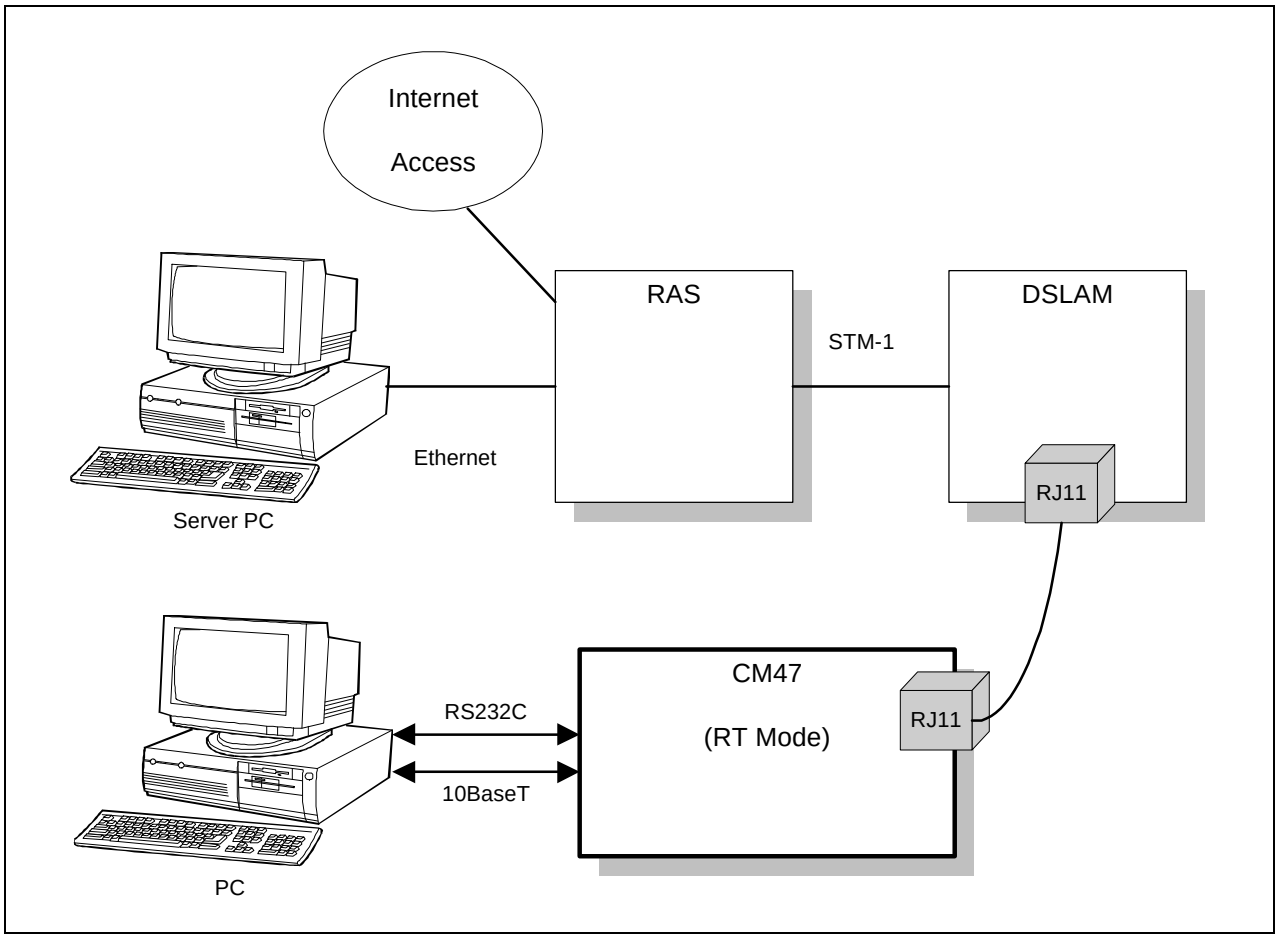


Figure 7. ADSL Network Enviornment

DIAGNOSTIC PROGRAM DESCRIPTION

Main Menu

If you finished the installation, turn on the power switch on the CM47-M66 board. Then the following message appears at the hyper-terminal window.

```
=========================================================
      [CM47-M66-V1.0 ADSL Reference Board]
           DSL Team / SAMSUNG electronics
=========================================================
BOOT ROM  (ver 1.0)
=========================================================
=========================================================
S5N8947 Emulation Board Diagnostic Ver 1.0
=========================================================
[1] Memory TEST
[2] UART TEST
[3] Timer TEST
[4] GDMA TEST
[5] I2C BUS TEST
[6] I/O Port TEST
[7] Ethernet TEST
[8] USB Test
[S] SAR Test
[A] All Test
[U] User Program Download
[F] Flash Memory Operation
=========================================================
Select One...
```

If you want to test, select the menu.

Memory TEST

This message appears if you key-in [1] and press enter key.

```
--------------------------------
      Memory Test Menu
--------------------------------
  [1] Memory Read
  [2] Memory Write
  [3] Read & Write
  [4] R/W Long-Run Test(Sequential)
  [Q] Exit Memory Test
--------------------------------
Select One..
```

Please refer to the following description about the above test menu

[1] Memory Read: This test will request ‘start address’ and ‘word size’. If you key-in any value you want to read, the result data appears on your hyper-terminal window.

[2] Memory Write: This test will request ‘start address’, ‘word size’ and data that you want to write. If you key-in any value, the S5N8947 MCU writes the data to the memory area. And you will check the result by [1] test again. By the way, you must keep the start address larger than ‘0x1000050’. (ex. 0x1500000)

[3] Read & Write: This rest will access some dedicated area repeatedly and check if any memory access errors occurs. It will take some minutes. After finishing the test, If ‘Memory W/R TEST SUCCEEDED!!’ message come, the memory test means OK.

[4] R/W Long-Run Test (Sequential): This test will repeat the [3] test until you press Reset Button at CM47 board.

UART TEST

```
================================================
    UART TEST MENU
================================================
  [1] View Current UART Configuration
  [2] Change UART Configuration
  [3] Set Baud Rate
  [4] UART Tx Interrupt Test
  [5] UART Rx Interrupt Echo Test
  [Q] EXIT UART Test
================================================
Select One (ESC to Return To MAIN MENU)
```

Please refer to the following description about the above test menu.

[1] View Current UART Configuration: This test shows the UART configuration register contents.

```
This is UART_0
>> Current UART_0 registers' values <<
########################################
      ULCON0      :     0x3
      UCON0       :     0xd
      USTAT0      :     0x10
      UTXBUF0     :     0x0
      URXBUF0     :     0x31
      UBRDIV0     :     0x390
########################################
Press Anykey To Return To Top MENU...
```

[2] Change UART Configuration: This test modifies the UART configuration register values. But the UART is now used to communicate with the present Hyper-terminal window. So if you change any registers in this test, you can't monitor the operation. I recommend you not to modify any registers.

[3] Set Baud Rate: I recommend you not to test this. In this 'Diagnostic program' it is fixed to 38400bps.

[4] UART Tx Interrupt Test: The display on your hyper-terminal message means the UART Tx Interrupt works well.

[5] UART Rx Interrupt Echo Test: This test will echo what you key-in. So you can see on your Hyper-terminal what you key-in.

Timer TEST

```
---------------------------------
     Timer Test Menu
---------------------------------
  [1] Run Timers
  [2] Test TOUT0/1/2
  [3] Test Watch-dog Timer
  [4] View Timer Configuration
  [Q] Exit Timer Test
---------------------------------

Select One..
```

Please refer to the following description about the above test menu.

[1] Run Timers: This test will request ‘Timer 0, Timer1 and Timer 2’s interval’. Then if you key-in the values, run the timers and terminates the timers after 10 times of timer interrupts. You can check the interval difference between the three timers (Timer0, Timer1 and Timer2).

[2] Test TOUT0/1/2: This test is similar to [1] test except that the Timer0 time interval is half of the Timer1 time interval.

[3] Test Watch-dog Timer: this test is the watch-dog timer test.

[4] View Timer Configuration: this test shows the values of timer register.

GDMA TEST

```
---------------------------------
     GDMA Test Menu
---------------------------------
  [1] Memory to Memory
  [2] Memory to UART
  [3] UART to Memory
  [4] Loopback GDMA(GDMA0 -> UART -> GDMA1)
  [5] View GDMA Configuration
  [Q] Exit GDMA Test
---------------------------------

Select One...
```

Please refer to the following description about the above test menu.

[1] Memory to Memory: Memory to Memory GDMA function test. In this function, there are two memory areas. The one is the source memory area to be transferred and the other is the destination memory area. The contents of the memory are assigned in the code. User's option is selecting transfer width (byte / half-word / word). After transfer, It compares the destination area with the source area and gives user a message whether the transfer is successful.

[2] Memory to UART: Memory to UART GDMA function test. In this function there is a memory area which is going to be transferred to UART. User fills this area with specific data and transfers this area to UART byte by byte. User can see the byte data displayed in the console window.

[3] UART to Memory: UART to Memory GDMA function test. After fills UART Rx buffer with specific data, transfer to memory.

[4] Loopback GDMA (GDMA0 -> UART -> GDMA1): Loopback GDMA test. GDMA0 → UART(Tx Buffer) → UART(Rx Buffer) → GDMA1.

[5] View GDMA Configuration: shows the values of GDMA specific registers.

I²C BUS TEST

This message appears if you key-in [5] and press enter key.

```
-------------------------------------
      IIC Test Memu
-------------------------------------
  [1] IIC Page Write Test(INT)
  [2] IIC Sequential Read Test(INT)
  [3] IIC Read/Write Test(INT)
  [4] IIC Page Write Test(POLL)
  [5] IIC Sequential Read Test(POLL)
  [6] IIC Read/Write Test(POLL)
  [7] IIC Byte random R/W Test
  [8] IIC Loopback test(INT)
  [9] IIC configuration view
  [Q] Quit IIC Test
-------------------------------------
 Select One..
```

[1] IIC Page Write Test (INT): IIC write test by interrupt

[2] IIC Sequential Read Test (INT): IIC read test by interrupt

[3] IIC Read/Write Test (INT): IIC Read/Write test program by interrupt method

[4] IIC Page Write Test (POLL): IIC Write test program by polling method

[5] IIC Sequential Read Test (POLL): IIC read test by polling

[6] IIC Read/Write Test (POLL): IIC Read/Write test program by polling method

[7] IIC Byte random R/W Test: IIC Write one byte of data to a given address of EEPROM

[8] IIC Loopback Test (INT): IIC read/write Loopback test

[9] IIC Configuration view: Shows IIC related register value

I/O Port TEST

This message appears if you key-in [6] and press enter key.

```
-----------------------------------------------
     IO Port Test Menu
-----------------------------------------------
  [1] IO Port Read (port[0..7])
  [2] IO Port Write (port[0..7])
  [3] External Interrupt Test (port[5..11])
  [4] View Configuration
  [5] IOPDATA Read (Input mode)
  [Q] Exit IO Port Test
-----------------------------------------------
Select One..
```

This test is not suitable in this board because it is hard to monitor the operation of GPIO pins. If you are willing to do this test in spite of these difficulties, you have to use Oscilloscope to monitor output port and use some jumper to test input port.

[1] IO Port Read (port[0..7]): Shows the I/O Port.

[2] IO Port Write (port[0..7]): In CM47-M66 board, I/O Ports 0 through 7 has just Test Header. If you write or read I/O port[0..7], you can monitor it using the Test Header pins.

[3] External Interrupt Test (port[5..11]): This test is not possible in CM47-M66.

[4] View Configuration: Shows the values of I/O Port specific registers.

[5] IOPDATA Read (Input mode): You can configure the I/O Ports as inputs or outputs with configuring the IOPMOD register. In this menu function, I/O Ports [12..15] are set as input.

Ethernet TEST

In the 'Diagnostic program' main menu, select [7] (Ethernet TEST).

```
=========================================================
            Ethernet TEST MENU
=========================================================
      [1] Ethernet0 TEST
      [2] Ethernet1 TEST
      [3] Ethernet to Ethernet Bridge TEST
      [Q] Exit Ethernet TEST
=========================================================
Select One... :
```

[1] Ethernet0 TEST (Ethernet1 TEST method is same as Ethernet0 TEST)

```
+-------------------------------------------------------------------+
|    >>>>> MAC0 Block Diagnostic Program <<<<<                      |
+-------------------------------------------------------------------+
| Capture & Show Ethernet Frame                          - [C]      |
| MAC Loopback Test                                      - [L]      |
| Transfer Ethernet Frame                                - [T]      |
| Receive Ethernet Frame                                 - [R]      |
| Other MAC Function Test                                - [O]      |
| Change & View MAC Configuration                        - [V]      |
| MAC Initialization                                     - [I]      |
| Quit Ethernet Test                                     - [Q]      |
+-------------------------------------------------------------------+

Select Test Item :
```

Please refer to the following description about the above test menu.

[C] Capture & Show Ethernet Frame

If you key-in 'C' and press Enter key, the following message come out on your hyper-terminal window.

```
+-------------------------------------------------------------------+
|    ***** Capture & ShowFrame MAC0 Frame *****                     |
+-------------------------------------------------------------------+
| Capture All MAC Frame to Buffer Full                    - [A]     |
| Capture My MAC Address Frame                            - [M]     |
| Capture Broadcast Frame                                 - [B]     |
| Capture Control Frame                                   - [C]     |
| Capture Matched Destination Address                     - [D]     |
| Show Captured MAC Frame                                 - [S]     |
| Quit Show & Capture                                     - [Q]     |
+-------------------------------------------------------------------+

Select Test Item :
```

[L] MAC Loopback Test

If you key-in 'L' and press Enter key, the following message come out on your Hyper-terminal window.

```
+-------------------------------------------------+
|          ***** MAC0 LoopBack Test *****         |
+-------------------------------------------------+
| MAC Internal LoopBackTest                 - [I] |
| MAC - PHY LoopBackTest(Without Collision) - [L] |
| MAC - PHY LoopBackTest(WithCollision)     - [C] |
| Physical Ethernet LoopBackTest(External)  - [E] |
| Polling LoopBackTest                      - [P] |
| All LoopBackTest(Without Physical LoopBack) - [A] |
| Quit MAC LoopBack Test                    - [Q] |
+-------------------------------------------------+

Select Test Item :
```

[I] MAC Internal LoopBackTest

```
Select Test Item : I
$$$ Enter Number of Loopback Test : 1
** Total Mismatch Frame is 0
 >>>>> Error Report <<<<<
 +- MAC Tx Err Count (Good:180) -+
    ExColl: 0, Defered: 0, Paused: 0, Under : 0
    Defer : 0, NoCarri: 0, SQE   : 0, LatCol: 0
    TxPar : 0, TxHalt : 0
 +- MAC Rx Err Count -+
    CtlRcd: 0, 10Stat : 0, Allign: 0, CRCErr: 0
    OverFl: 0, LongErr: 0, RxPar : 0, RxHalt: 0
 +- BDMA Tx Err Count -+
    BTxNull: 0, BTxNOwn: 0, BTxEmpty: 0
 +- BDMA Rx Err Count (RxCnt:180) -+
    BRxNull: 0, BRxNOwn: 0, BRxOvr: 0
 +- Missed Error Count : 0
 >>>>> Error Occurred Time <<<<<
*** Press any key to Continue
```

[T] Transfer Ethernet Frame

```
+-----------------------------------------------------------------+
|          ***** Transfer MAC Frame *****                        |
+-----------------------------------------------------------------+
| Transfer Single MAC Frame                              - [S] |
| Transfer Multiple MAC Frame                            - [M] |
| Transfer Control Frame                                 - [C] |
| Quit MAC Transfer Test                                 - [Q] |
+-----------------------------------------------------------------+

Select Test Item :
```

[S] Transfer Single MAC Frame: Transmit a single MAC frame

```
Select Test Item : s
   $$ Select Transmit(T) or Quit(Q) ? t
   $$ Select Transmit(T) or Quit(Q) ? t
   $$ Select Transmit(T) or Quit(Q) ? q
   >>>>> Error Report <<<<<
   +- MAC Tx Err Count (Good:2) -+
      ExColl: 0, Deferred: 0, Paused: 0, Under : 0
      Defer : 0, NoCarri: 0, SQE   : 0, LatCol: 0
      TxPar : 0, TxHalt : 0
   +- MAC Rx Err Count -+
      CtlRcd: 0, 10Stat : 0, Allign: 0, CRCErr: 0
      OverFl: 0, LongErr: 0, RxPar : 0, RxHalt: 0
   +- BDMA Tx Err Count -+
      BTxNull: 0, BTxNOwn: 0, BTxEmpty: 0
   +- BDMA Rx Err Count (RxCnt:0) -+
      BRxNull: 0, BRxNOwn: 0, BRxOvr: 0
   +- Missed Error Count : 0
   >>>>> Error Occurred Time <<<<<
```

[M] Transfer Multiple MAC Frame

```
Select Test Item : m
[T0:0]Tx count value(Decimal)-> 10
 >>>>> Error Report <<<<<
 +- MAC Tx Err Count (Good:10) -+
     ExColl: 0, Defered: 0, Paused: 0, Under : 0
     Defer : 0, NoCarri: 0, SQE   : 0, LatCol: 0
     TxPar : 0, TxHalt : 0
 +- MAC Rx Err Count -+
     CtlRcd: 0, 10Stat : 0, Allign: 0, CRCErr: 0
     OverFl: 0, LongErr: 0, RxPar : 0, RxHalt: 0
 +- BDMA Tx Err Count -+
     BTxNull: 0, BTxNOwn: 0, BTxEmpty: 0
 +- BDMA Rx Err Count (RxCnt:0) -+
     BRxNull: 0, BRxNOwn: 0, BRxOvr: 0
 +- Missed Error Count : 0
 >>>>> Error Occurred Time <<<<<
```

[R] Receive Ethernet Frame: (…)

[O] Other MAC Function Test

```
+-------------------------------------------------+
|        ***** Other MAC Function Test *****      |
+-------------------------------------------------+
| BDMA Buffer Test                          - [B] |
| MAC Rx FIFO                               - [R] |
| MAC Tx Halt Request Test                  - [H] |
| MDC On Test                               - [M] |
| MDC Off Test                              - [O] |
| MAC Register View & Change                - [A] |
| PHY Register View & Change                - [I] |
| PHY MII Station Management Test           - [P] |
| Quit Other MAC Function Test              - [Q] |
+-------------------------------------------------+
Select Test Item : b
>>>  BDMA Tx/Rx and CAM Buffer Test <<<
>>   BDMA Tx Buffer Test ....    Ok.
>>   BDMA Rx Buffer Test ....    Ok.
>>   CAM Read/Write Test ....    Ok.
Press any key to Continue MAC Test

Select Test Item : r
BDMA FIFO : 8x
BDMA FIFO : 8x
BDMA FIFO : 8x
Press any key to Continue MAC Test

Select Test Item : h
>>>  MAC Tx Halt Request Test  <<<

>> Select (Q)uit or (T)x 2 Frame  : t
[101] Size : 1514
[101] Size : 165
>> Select (Q)uit or (T)x 2 Frame  : q

>>>>> [Ethernet0] Error Report <<<<<
+- Ethernet[0] MAC Tx Err Count (Good:2) -+
   ExColl: 0, Defered: 0, Paused: 0, Under : 0
   Defer : 0, NoCarri: 0, SQE   : 0, LatCol: 0
   TxPar : 0, TxHalt : 0
+- Ethernet[0] BDMA Rx Err Count (RxCnt:0) -+
   BRxNull: 0, BRxNOwn: 0, BRxOvr: 0
+- Ethernet[0] MAC Rx Err Count -+
   CtlRcd: 0, 10Stat : 0, Allign: 0, CRCErr: 0
   OverFl: 0, LongErr: 0, RxPar : 0, RxHalt: 0
+- Ethernet[0] BDMA Tx Err Count -+
   BTxNull: 0, BTxNOwn: 0, BTxEmpty: 0
+- Ethernet0 Missed Error Count : 0
+- Ethernet0 BDMA Owner Count : 0
+- Ethernet0 Send Packet Count : 0
Press any key to Continue MAC Test
```

```
Select Test Item : p
>>>>> PHY0 Station Management Reg Read <<<<
1. CNTL REG          (0x3000) : 1000
2. STATUS REG        (0x7809) : 7809
3. ID REG1           (0x00F0) : 0016
4. ID REG2           (0x00F0) : f880

Press any key to Continue MAC Test
```

[V] Change & View MAC Configuration

[I] MAC Initialization: Menu for Re-initializing

USB TEST

If you want to test USB function you have to prepare USB cable and install USB driver on your PC. In the test notebook PC, the USB test program is located at C:\Util\8947usb\exe.

Installment of USB Driver

— Prepare a PC with USB port and Windows 98. Then install the USB driver if it has not installed.
* In the test notebook PC, the USB driver program is at C:\Util\8947usb\sys.

— In the 'Diagnostic program' main menu, select [8](USB TEST) If you can see the following message '[USB_Diag_Log]: Suspend Mode', connect the USB cable between PC (USB host) and CM47 board (USB device).

a. After handshaking process, this message will be appeared on your Hyper-terminal window.

```
MCU >> Standard Type Interrupt
MCU >> Set Configuration
```

At this time, if the USB driver doesn't installed in your PC, 'New hardware found' pop-up window will come out and request to select USB driver for your USB device. Then you select the folder 'C:\Util\8947usb\sys' and file 'Bulkusb.inf'.

b. Let us check if the USB driver is installed correctly. Open the 'System registered information' window from the 'Control Panel'. Find 'Device manager' folder → USB controller → SAMSUNG S5N8947 USB Test. If there is no icon of '?' or '!', then the USB driver is installed correctly. If you can see the icon '?' or '!', then delete the device and repeat the installment procedure.

USB Test Procedure

a. Open the MS-DOS window on your USB host PC.

b. Move to the folder where USB test program is. (ex. C:\Util\8947usb\exe).

c. Key-in 'bulk34' and press [enter] key and you can see the test program guide.

(ex) Bulk34 –w (byte length) –r (byte length) –c (loop count) → Endpoint 3, 4 test.
(ex) Int12 –w (byte length) –r (byte length) –c (loop count) → Endpoint 1, 2 test.

d. If you want to test endpoint3, 4 with 10 byte data, Key-in 'bulk34 –w 10 –r 10 ' and press [enter] key.

e. Then you can see the test result on your MS-DOS window.

SAR TEST

In the 'Diagnostic program' main menu, select [S] (SAR TEST).

```
=========================================================
  [ SAR Diagnostic Program ]
---------------------------------------------------------
> MAIN MENU
---------------------------------------------------------
  [1] Configure SAR/UTOPIA/PHY Registers
  [2] Configure SAR Connection Memory
  [3] Open New Connection
  [4] View SAR Register & Opened-Connection Information
  [5] Internal LoopBack Test
  [6] External LoopBack Test
  [7] Reset with Current Connection Memory Configuration
  [8] Predefined Connection
  [9] MAC <-->SAR
  [D] Change Debug Level
  [F] Aging Test
  [T] Traffic Shaper Test
  [Q] Quit
=========================================================
Select one... :
```

[1] Configure SAR Registers: You can change SAR configuration register setting.

NOTE

If you want to test 'External Loopback Test' and monitor UTOPIA bus signals, you have to select KS8950 (16bit access) device as an ATM PHY. The followings show you the way.

Press **'1'** to configure SAR/UTOPIA/PHY registers at the above menu.

```
-------------------------------------------------------------------------------
[1] Select SAR Clock                      [2] Select UTOPIA Clock
[3] Enter TIME OUT BASE                   [4] Enter Clock Ratio value
[5] Endian Selection                      [6] Tx/Rx Payload Alignment Selection
[7] External/Internal Connection Memory   [8] CAM/ VP lookup Selection
[9] Enable/Disable Utopia                 [A] Select Utopia Level
[B] Select Phy No                         [C] Select Utopia Output Delay
[D] Select Utopia TX CLAV Timeout         [E] Select Utopia TX DISCARD Timeout
[F] Cache Toggle
[P] Select Phy
[S] Save new configuration
[U] Update configuration register
[V] View configuration register
[Q] Quit
-------------------------------------------------------------------------------
Select one... : p
```

Press 'P' to select PHY.

```
-------------------------------------------------------
 > Select PHY.
-------------------------------------------------------
   [0] IDT ATM25
   [1] KS8950 (8 BIT ACCESS)
   [2] KS8950 (16 BIT ACCESS)
   [3] KS8944
-------------------------------------------------------
Select one... : 2
```

Press '2' to write data with 16-bit unit.

[2] Configure SAR Connection Memory Registers: You can change SAR connection memory setting.

[3] Open New Connection: Open new ATM VPCI channel. (Assign VPI, VCI value as you want)

[4] View SAR Register & Opened-Connection Information.: Display SAR internal register & show the opened VPCI channel.

[5] Internal LoopBack Test.: SAR internal loop-back test.

```
=======================================================
      [ Loop Back Test - internal loopback ]
=======================================================
  [1] Select a Channel
  [2] Select Transmit Packet Size(Max: 0x2ff0)
  [3] Select Transmit Packet Pattern
  [4] Send a Packet
  [Q] Quit
-------------------------------------------------------
- You have to Select Channel Number at first...
-------------------------------------------------------
-------------------------------------------------------
> Select Channel Number to View or Send Packet
-------------------------------------------------------
  Select a Channel from following open channel lists.
  - Open Channel Lists :
[0] VP=0, VC=3, PORT=0, PCR=7000000, AAL=AAL5 SEM, CBR
-------------------------------------------------------
Enter Channel Number : 0
```

At this time, you have to select one among the above open channel list. And key-in the value like the above message and press [enter] key.

Then you can see the following message.

```
=========================================================
       [ Loop Back Test - internal loopback ]
=========================================================
 [1] Select a Channel
 [2] Select Transmit Packet Size(Max: 0x2ff0)
 [3] Select Transmit Packet Pattern
 [4] Send a Packet
 [Q] Quit
---------------------------------------------------------
Select one... : 2
---------------------------------------------------------
> Select Transmit Packet Size ( Default Size : 0x500 )

---------------------------------------------------------
Enter Tx Packet Size... : 0x100

 [3] Select Transmit Packet Pattern.
---------------------------------------------------------
> Select Transmit Packet Pattern ( 0x0 ~0xff - Default Pattern : 0x0 )
---------------------------------------------------------
Enter Tx Packet Pattern... : 0x0

 [4]Send a Packet. : Send a frame as you defined at [1]~[4].
Tx: 0x100 Bytes, VPI: 0, VCI:3, PORT:0, PTI:0  **** Rx: OK
```

If the above message come out in your hyper-terminal window, the SAR loop-back operation is OK. (This message come out as many as you selected at [4]menu.)

[6] External LoopBack Test: The test method is same with ‘Internal Loopback Test’.

[7] Reset with Current Connection Memory Configuration: Display SAR connection memory.

[8] Predefined Connection: Configure predefined connection.

[9] MAC < - - > SAR: MAC to SAR bridge test.

In order to do this test, ATM PHY device should work well. But the Samsung ADSL chipset is not working at this test. So it is impossible to do this test at this menu. However you can do this test by selecting [F] menu (Flash memory operation) at main menu. The ADSL modem function code is stored at the flash memory. You can also modifiy the ADSL modem code by selecting [U] menu (User program downloading) at main menu. Please refer to ‘CM47 Reference Board G.dmt link Setup’ chapter about more detail explanation.

ALL TEST

This test is for quick test of S5N8947 operation. The following message comes out when all of the tests are successful.

```
$$ Enter test count to perform : 1
================================================
 TEST #1
================================================
>> SAR TEST---------------------[O.K]
>> MAC0 TEST--------------------[O.K]
>> Memory TEST------------------[O.K]
>> GDMA TEST--------------------[O.K]
>> IIC BUS TEST-----------------[O.K]
>> IO Port TEST-----------------[O.K]
>> Timer TEST-------------------[O.K]
================================================
>> S5N8947 FULL TEST DONE(1 times) WITH 0 ERRORs.. <<
```

CM47 Reference Board G.dmt Link Set-up

[U] User Program Downloading

Select *"User Program Download"* with typing '**u**' at the cursor and you will see the message below.

```
-------------------------------------------
     SYSTEM INFORMATION
-------------------------------------------
  ROM0 BASE    : 0x       0
  ROM1 BASE    : 0x  200000
  DRAM BASE    : 0x 1000000
-------------------------------------------
 ## Input Download Area Address (default:0x1000050) : 0x
```

Just press Enter. If you want to change the download start address, you have to re-burn your ROM after changing *"ROMOPTS"* in makefile.

```
=========================================================
            DownLoad User's Program to DRAM
=========================================================
                [x] Using Xmodem
                [s] Using SFTP
                [q] Exit
=========================================================
Select One... :
```

[x] Using Xmodem

Select *"Using Xmodem"* with typing '**x**' at the cursor and you will see the message below.

```
$$ Waiting for User Program .....

 * Please Select Menu on your Hyper Terminal
 => Transfer => Send file
 => Browse File => Choose protocol you seleted
 => Browse File => Choose File name
```

Click the *"send file"* in pull-down menu of Hyperterminal and you will see the windows below. And then, search the ***"ram.bin(User File)"*** file in your working directory. At last, select the Xmodem protocol.

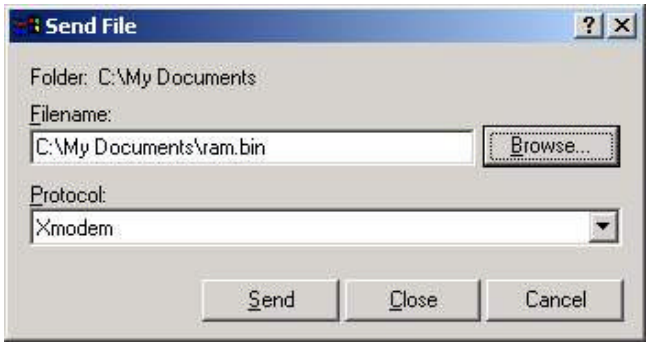


Figure 8. Hyperterminal Window Display when Click the Send File in Pull-down Menu

Click “Send” button, and then ***“ram.bin (User File)”*** file send.

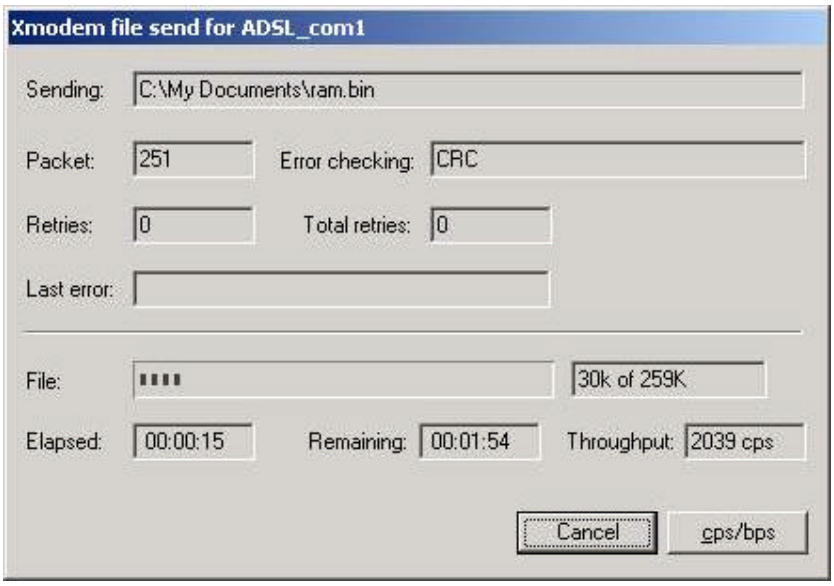


Figure 9. Hyperterminal Window Display when Xmodem File Send

After completing downloading and CRC checking following message appears at HyperTerminal window.

```
$$ Waiting for User Program .....
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC OK !
$$ CRC Check Ok ..

-----------------------------------------------
          Start  User's  Program
-----------------------------------------------
   [s]  Start Program
   [q]  Exit
-----------------------------------------------
Select Test Item : s
$$ Now, User program will be started.
```

Press **'s'** key and your program will start running.

[s] Using SFTP

Open a DOS window and run Sftp as a format below.

sftp < com port # > < file name >

Ex) sftp 1 ram.bin

Following message asks you if you want to change downloading baud rate. Just press **'n'.**

The downloading procedure starts and the progress shown with '#' mark.

After completing downloading and CRC checking following message appears at HyperTerminal window.

```
$$ Waiting for User Program ..... Ok.
$$ CRC Check Ok ..

-----------------------------------------------
          Start  User's  Program
-----------------------------------------------
   [s]  Start Program
   [q]  Exit
-----------------------------------------------
Select Test Item : s
$$ Now, User program will be started.
```

Press **'s'** key and your program will start running.

[F] FLASH Memory Operation

Select *"FLASH Memory Operation"* with typing 'f' at the cursor and you will see the message below.

```
-----------------------------------------
      Flash Operation Menu
-----------------------------------------
  [0] Erase Whole Flash memory
  [1] Erase Flash Region 0
  [2] Erase Flash Region 1
  [3] Program Flash Regions
  [4] Execute Program in Region 0
  [5] Execute Program in Region 1
  [Q] Return To Main Menu
-----------------------------------------
Select One...
```

If you want to download the User Program at Flash,

First, you have to select ' ***3*** ' for Program the Flash Memory, so you will see the message below.

Second, you have to select Region 0 or Region 1.

```
-----------------------------------------------
      Flash Operation Menu
-----------------------------------------------
  [0] Erase Whole Flash memory
  [1] Erase Flash Region 0
  [2] Erase Flash Region 1
  [3] Program Flash Regions
  [4] Execute Program in Region 0
  [5] Execute Program in Region 1
  [Q] Return To Main Menu
-----------------------------------------------
Select One..3
Select Region to program (0/1, 'Q' to avoid)...0

=========================================================
           DownLoad User's Program to DRAM
=========================================================
                [x] Using Xmodem
                [s] Using SFTP
                [q] Exit
=========================================================
Select One... :
```

Third, you have to select one among the above menu table.

[x] Using Xmodem

Select *"Using Xmodem"* with typing '**x**' at the cursor and you will see the message below.

```
$$ Waiting for User Program .....

 * Please Select Menu on your Hyper Terminal
 => Transfer => Send file
 => Browse File => Choose protocol you seleted
 => Browse File => Choose File name
```

"Flash Memory Operation" method is same as "User Program Downloading".

Click the "send file" in pull-down menu of Hyperterminal. (see Figure 8) And then, search the "ram.bin (User File)" file in your working directory and select the Xmodem protocol.

Click "Send" button, and then ***"ram.bin (User File)"*** file send.(see Figure 9)

[s] Using SFTP

Open a DOS window and run Sftp as a format below.

sftp < com port # > < file name >
Ex) sftp 1 ram.bin

Following message asks you if you want to change downloading baud rate. Just press **'n'**.

The downloading procedure starts and the progress shown with '#' mark.

After completing downloading and CRC checking following message appears at HyperTerminal window.

```
>> Please send the image file to UART..
>> CRC is OK..
>> Download file to DRAM Succeeded..

Copying the code to Flash, please wait..
## Flash Update Completed!!!
Programming Region 0 Succeded !!
Press Anykey to Return to Main Menu..
```

Just press Enter or select **'f'** item use bold character, you will see the following Menu Table.

```
Select One... : f
  ---------------------------------
        Flash Operation Menu
  ---------------------------------
   [0] Erase Whole Flash memory
   [1] Erase Flash Region 0
   [2] Erase Flash Region 1
   [3] Program Flash Regions
   [4] Execute Program in Region 0
   [5] Execute Program in Region 1
   [Q] Return To Main Menu
  ---------------------------------
    Select One..4

  >> Copying Code from Region 0 to DRAM, please wait.........
  ## Press Anykey to Start Flash Code..
  %  PPPoE Enable mode  %
      VPI = 0 ,  VCI = 32
   MBR = 8
   PCR = 778240
   >> Do you want to change the values?[y/n]n
   Tc Reset Setup value -> 253
   Tc Reset Setup value -> 253
   Tc Reset Setup value -> 253
   Tc Reset Setup value -> 253
   [root] - Shell Initialization
   [root] - EtherRx Initialization
   [root] - Sar Initialization
   [root] - DMT Initialization

   -------------------------------
    Welcome to Samsung UADSL World
   -------------------------------
   ADSL RT+> DMTPllClockSet
   DMT Parameters is setting to default values
   eocTask(s) is(are) created.

   Code Size    = 28540(word)

   s-MP_BOOT_SOD : 1
   s-DSL_DSP_ON  : 1

   Now, DSP is ON!!!

   Now, MP.BOOT.sod is ON!!!
   DSL_DSP_ON : 1
   DSL_HOST_ON : 1
   MP_BOOT_DL_FLAG0 : 1
   MP_BOOT_DL_FLAG1 : 1
   Downloaded Word Count: 28540
```

```
 e-MP_BOOT_SOD : 0
 e-DSL_DSP_ON  : 1

 DL_STATUS   : 0

 ...Downloading is finished...0
DSP code starts...
DSP Handshake starts...0x0
DSP Training starts...
DSP Channel analysis starts...
DSP Messgae exchange starts...
DSP Link succeeded...

-------------------------------------------------------------------------------
ATU-R Current VPI / VCI :  0  /  32
*** NEAR-END ***
VENDOR ID       : 0     REVISION NUMBER :       SERIAL NUMBER   :
-------------------------------------------------------------------------------
                          Downstream         Upstream
-------------------------------------------------------------------------------
Noise SNR Margin     :      6 dB              0 dB
Net/Max Data Rate    :    928/ 1088 Kbps    544/ 608 Kbps
Parity bytes (RF/RI) :      0/16              0/8
Data Frames  (S)     :      4                 8
Interleave Depth (D) :     16                 1
-------------------------------------------------------------------------------
Current Power State  : L0
Initial AGC :   151,   Final AGC :   139,   Peak Value : 12592
Maximum downstream data rate :  1280 kbps
[TC] TC Asic Initialization
CURRENT PCR value : 544000
OK! Rx/Tx Starts..
```

CM47 Reference Board T1.413 Link setup

```
ADSL RT+> cfgbd

-------------------------------------------------------
         DMT Configuration & Board Test Menu
-------------------------------------------------------
 0. Quit Test   (DSP goes to idle state.)

 1. ADSL STANDARD    ->     0) G.DMT
    1) G.LITE               2) T1.413
    -> T1.413 Command Ex. : 1#2<Enter>

 2. DSP Test Request ->     0) DSP Abort
    1) Host Memory Test     2) DSP Download
    3) DSP Disconnect       4) DI Loopback
    5) TC Loopback          6) Pilot Tx
    7) Reverb Tx            8) Medley Tx
    -> Pilot Tx Command Ex. : 2#6<Enter>

 3. Modem Restart       (Link setup starts.)

 4. Set MinSnrMargin : 0x06 ~ 0x0f
    -> Command Ex. : 4#6<Enter>
-------------------------------------------------------
1#2
DMT Configuration & Board Test ends.

ADSL Modem state is now startup.
ADSL RT+> DSP Link fails...
Tx State : R-QUIET2,
Rx State : C-PILOT1-DETECTION
tx_state_id : 101, rx_state_id : 101
tx_duration : 8000, rx_duration : 7999
DSP T1.413 starts...0x1
DSP Training starts...
DSP Channel analysis starts...
DSP Messgae exchange starts...
DSP Link succeeded...

-------------------------------------------------------------------------------
ATU-R Current VPI / VCI :  0  /  32
*** NEAR-END ***
VENDOR ID       : 0     REVISION NUMBER :       SERIAL NUMBER   :
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
                          Downstream         Upstream
-------------------------------------------------------------------------------
Noise SNR Margin     :      5 dB              0 dB
Net/Max Data Rate    :    928/ 1088 Kbps    480/ 544 Kbps
Parity bytes (RF/RI) :      0/16              0/8
```

```
Data Frames  (S)     :      4                 8
Interleave Depth (D) :     16                 1
------------------------------------------------------------------------------
Current Power State  : L0
Initial AGC :   126,   Final AGC :   143,   Peak Value : 12984
Maximum downstream data rate :  1280 kbps
[TC] TC Asic Initialization
CURRENT PCR value : 480000
OK! Rx/Tx Starts..
```

APPENDIX A

Table A-1. Samsung ADSL Modem Command List

PWD	Display Current Working Directory
CLRSCR	Clear The Screen
HELP	Display Command usage
LS	Display All Commands
DATE	Get The Current Date/Time
SETTIME	Change The Current Date/Time
DM	Display Memory
PM	Patch Memory
CM	Compare Memory
SH	Show modem operation status
PHY	Show PHY status
MAC	MAC Test
SAR	SAR+MAC Test
CONN	Read Connection memory
SRESET	SAR Reset
SSTART	SAR Start
START	Start Rx Tx
TCSTAT	Show TC cell count
INITTC	Initialize TC Registers
RESETTC	Reset TC
RESETTCSAR	Reset & Init TC & SAR Reset
SETVPVC	Set VP, VC Value
SETPCRMBR	Set PCR, MBR Value
SETSNR	Set Downstream SNR Margin
INITSYS	InitSys
TCINIT	RESETTC and INITTC
SARINIT	SAR START and RxTxAllSTART
ETST	COMMANDS for EOC Tx/Rx TEST
CLRCOUNTER	Clear Counters
CFGBD	Configure and test DMT Modem
LST	Line Status view
STPV	Showtime Primitive Verbose mode toggle
SDM	Set/Show DSP Memory
FW	Firmware View

NOTES

APPENDIX B

CM47-M66-V1.0

SCHEMATIC AND BOARD LAYOUT

The CM47-M66 board schematics consist of eight pages. The content of each page is briefly described below.

PAGE 1: S5N8951

— S5N8951
— Hybrid module

PAGE 2: EXTERNAL INTERFACE

— USB
— UART
— JTAG
— S5N8950 JTAG
— I^2C EEPROM

PAGE 3: EXTERNAL PHY

— 10/100Mbps two Ethernet Interfaces (MII)
— Physical Interface: PHY, Magnetic
— RJ45 adaptor side pin configuration RJ45

PAGE 4: FLASH ROM

— Two boot ROM sockets
— ROM data size is configured by B0SIZE[1:0] select resistor
— Flash ROM support

PAGE 5: MCU

— S5N8947
— Probe header
— Mode select jumper
— System clock

PAGE 6: S5N8950

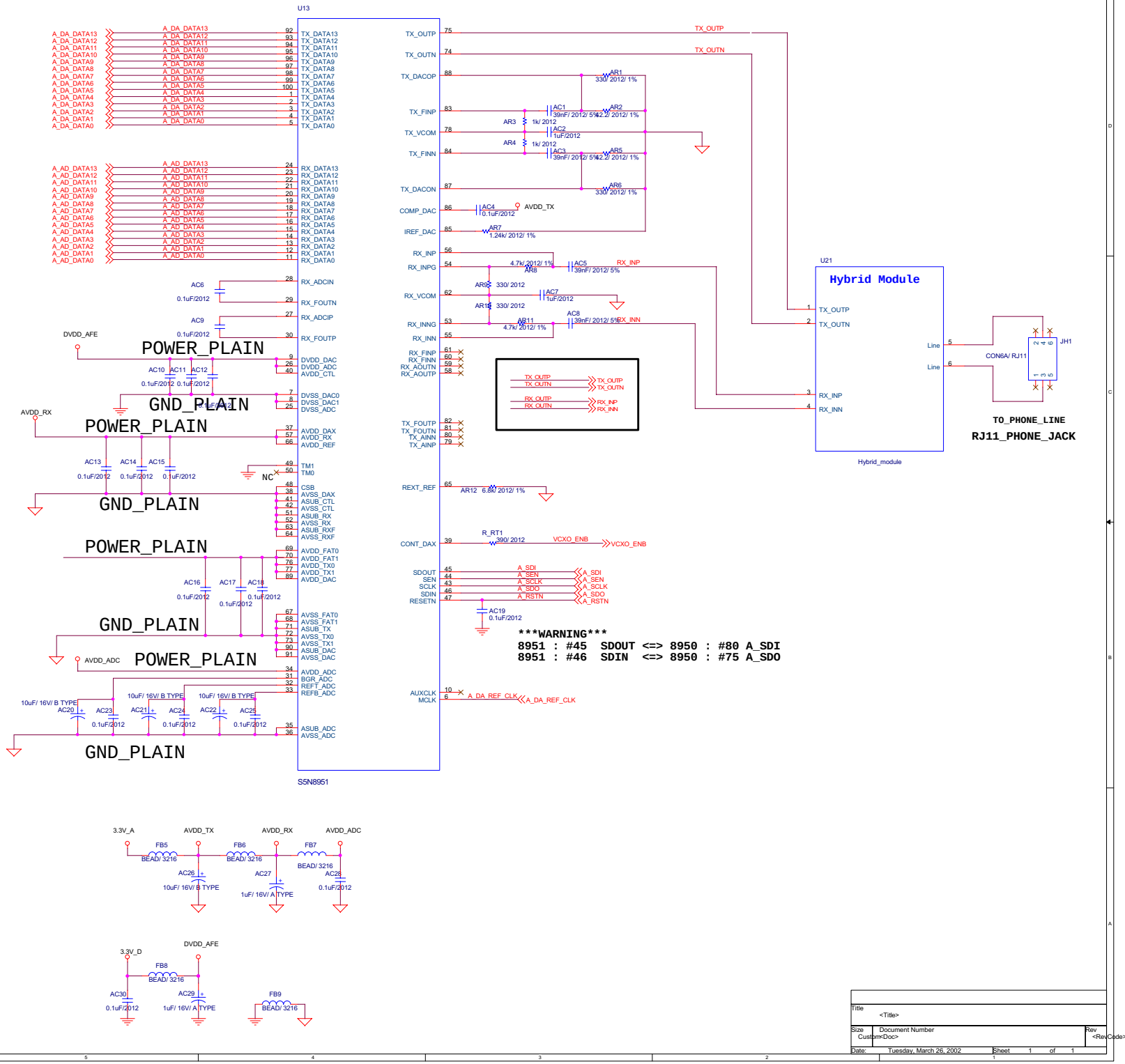
— S5N8950
— DMT clock
— Dying gasp

PAGE 7: POWER

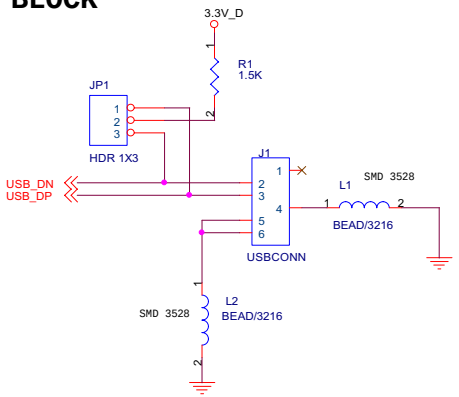
— Reset
— System control (B0SIZE, BIG/LITTLE Endian)
— Power

PAGE 8: SDRAM

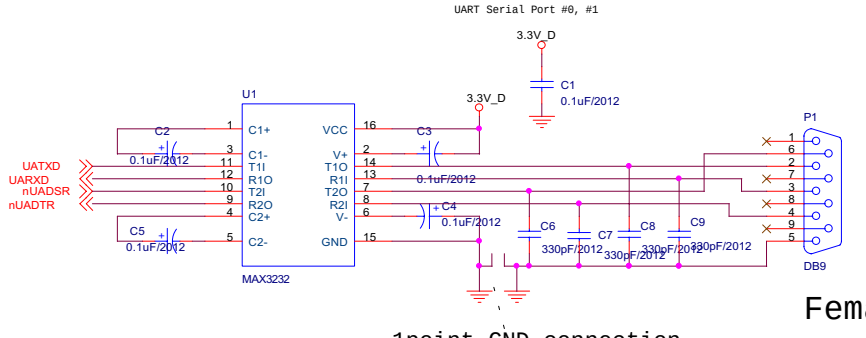
— 2M × 32 SDRAM


U13
S5N8951
U21
Hybrid Module
Hybrid_module
TO_PHONE_LINE
RJ11_PHONE_JACK
CON6A/ RJ11
JH1
POWER_PLAIN
GND_PLAIN
DVDD_AFE
AVDD_RX
AVDD_ADC
NC
WARNING
8951 : #45 SDOUT <=> 8950 : #80 A_SDI
8951 : #46 SDIN <=> 8950 : #75 A_SDO
3.3V_A
AVDD_TX
AVDD_RX
AVDD_ADC
3.3V_D
DVDD_AFE
Title
<Title>
Size
Custom
Document Number
<Doc>
Rev
<RevCode>
Date:
Tuesday, March 26, 2002
Sheet
1
of
1

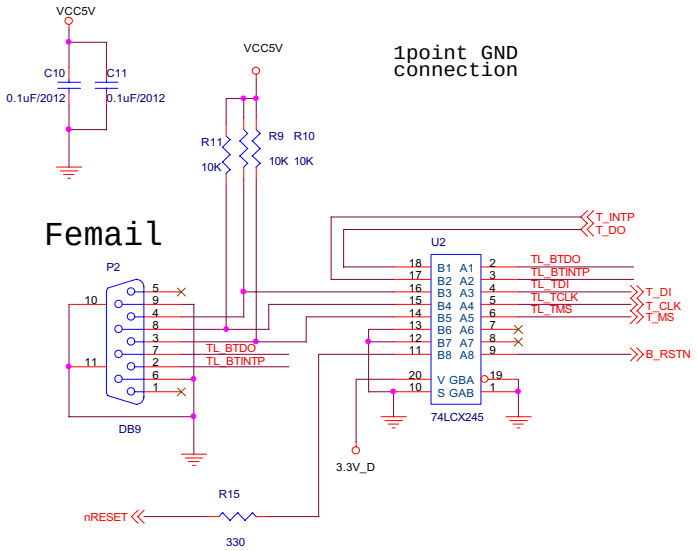
USB INTERFACE BLOCK



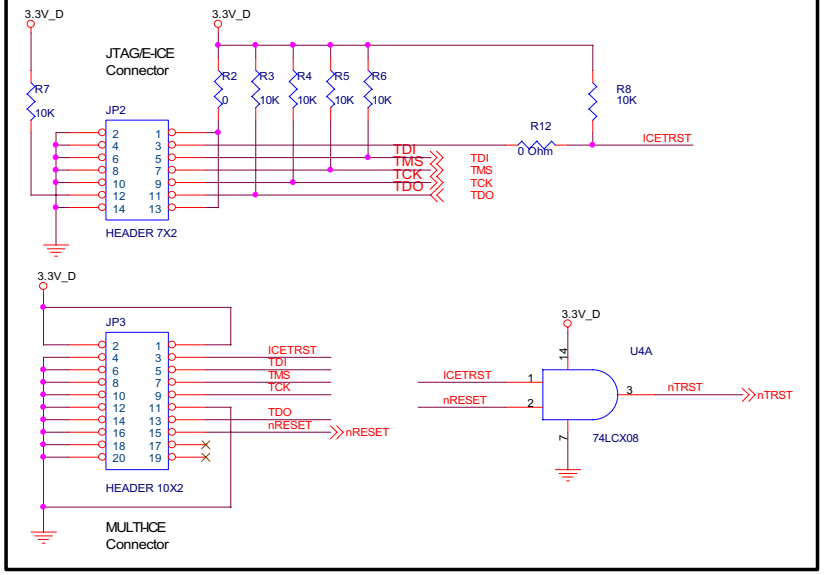
UART INTERFACE BLOCK FOR 8947.



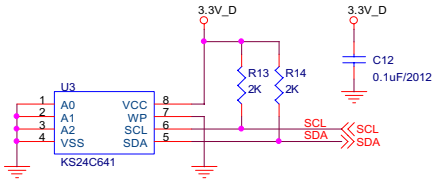
KS8950 JTAG INTERFACE



JTAG INTERFACE



IIC EEPROM



Title	EXTERNAL INTERFACE	
Size: Custom<Doc>	Document Number	Rev: 0.9
Date: Tuesday, March 26, 2002	Sheet 2 of 8	

MAC INTERFACE

MDC
MDIO
COL
RXD[3..0]
RX_DV
RX_CLK
RX_ERR
TX_CLK
TXD[3..0]
TX_EN
TX_ERR
CRS

nRESET

SECOND MAC INTERFACE

nECS3
sMDIO
SPIMISO
PP12
PP13
PP14
PP15
PP7
sRX_CLK
PP17
UCLK
PP4
PP5
PP6
nECS2
SPIMOSI
SPICLK
PP11

EXTERNAL PHY CLOCK

3.3V_D
L3
BEAD/3216
C22
0.1uF/2012
U7
NC
VDD
GND
OUT
OSC(25MHz)
R41
22
PHY_CLK

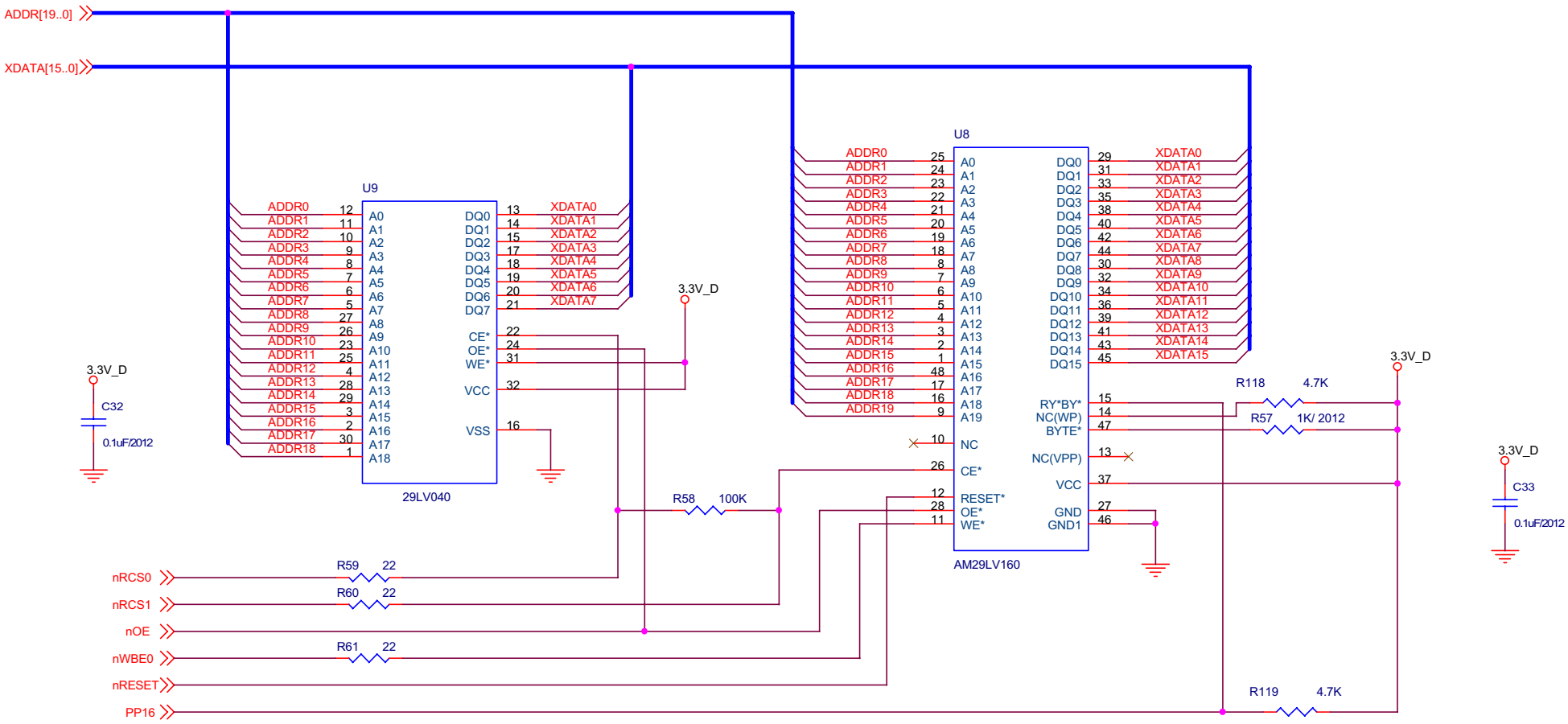
ETHERNET2 TEST S/W

S1
SW DIP-8
S2
SW DIP-8

Using PCMCIA module,
disconnect these two switches

U5
U6
80255
JP4
HEADER 2X2
JP8
HEADER 2X2
JP5
JP6
JP7
JP9
JP10
JP11
HEADER 3
J2
J3
RJ45_SCH7H5
R-PACK/75
R-PACK4.7K
R-PACK22
BEAD 2012
FB1
FB2
GND_RJ45
GND_80255

Title	EXTERNAL PHY
Size	Document Number: Custom<Doc>
Rev	0.9
Date:	Tuesday, March 26, 2002
Sheet	3 of 8



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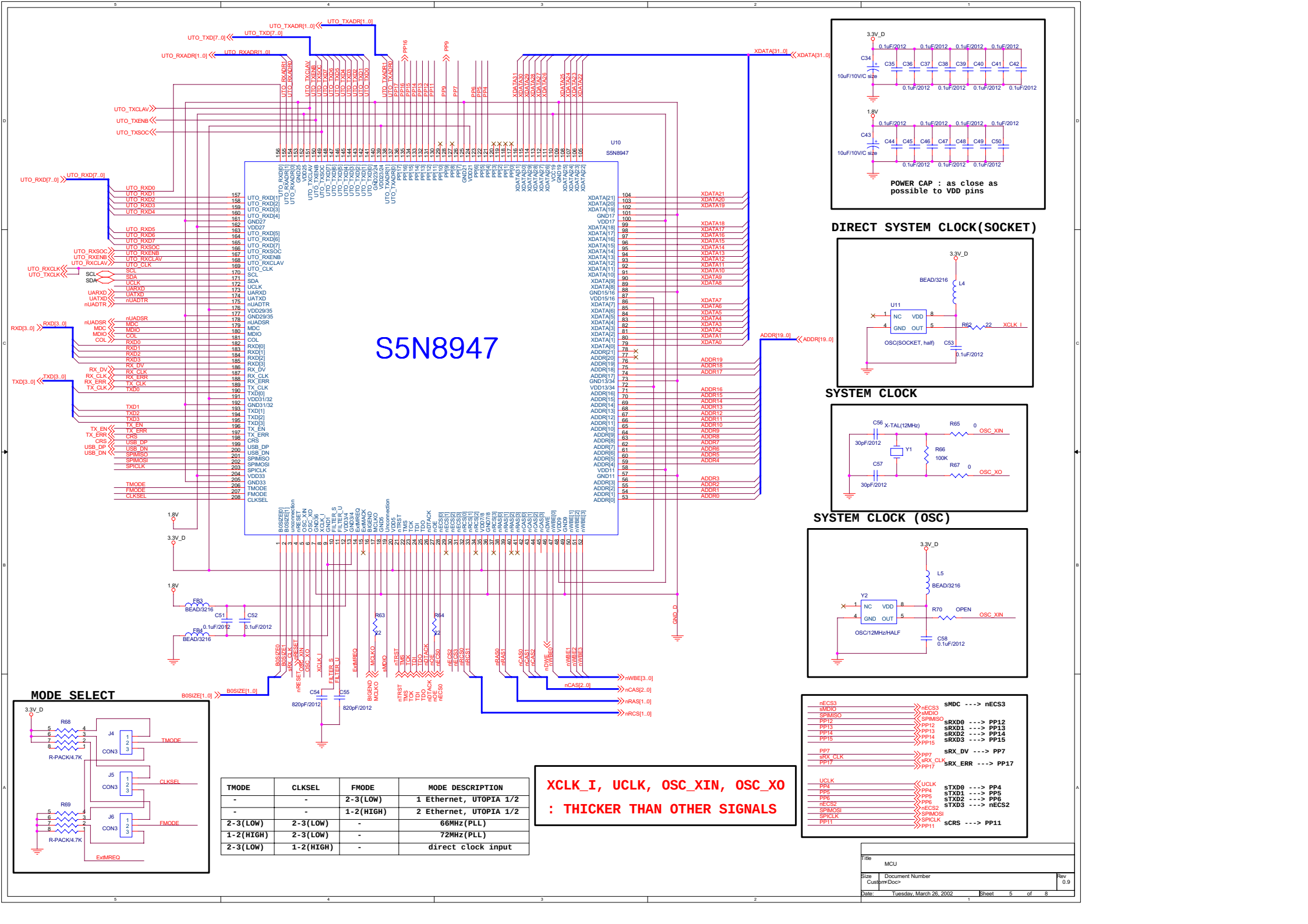
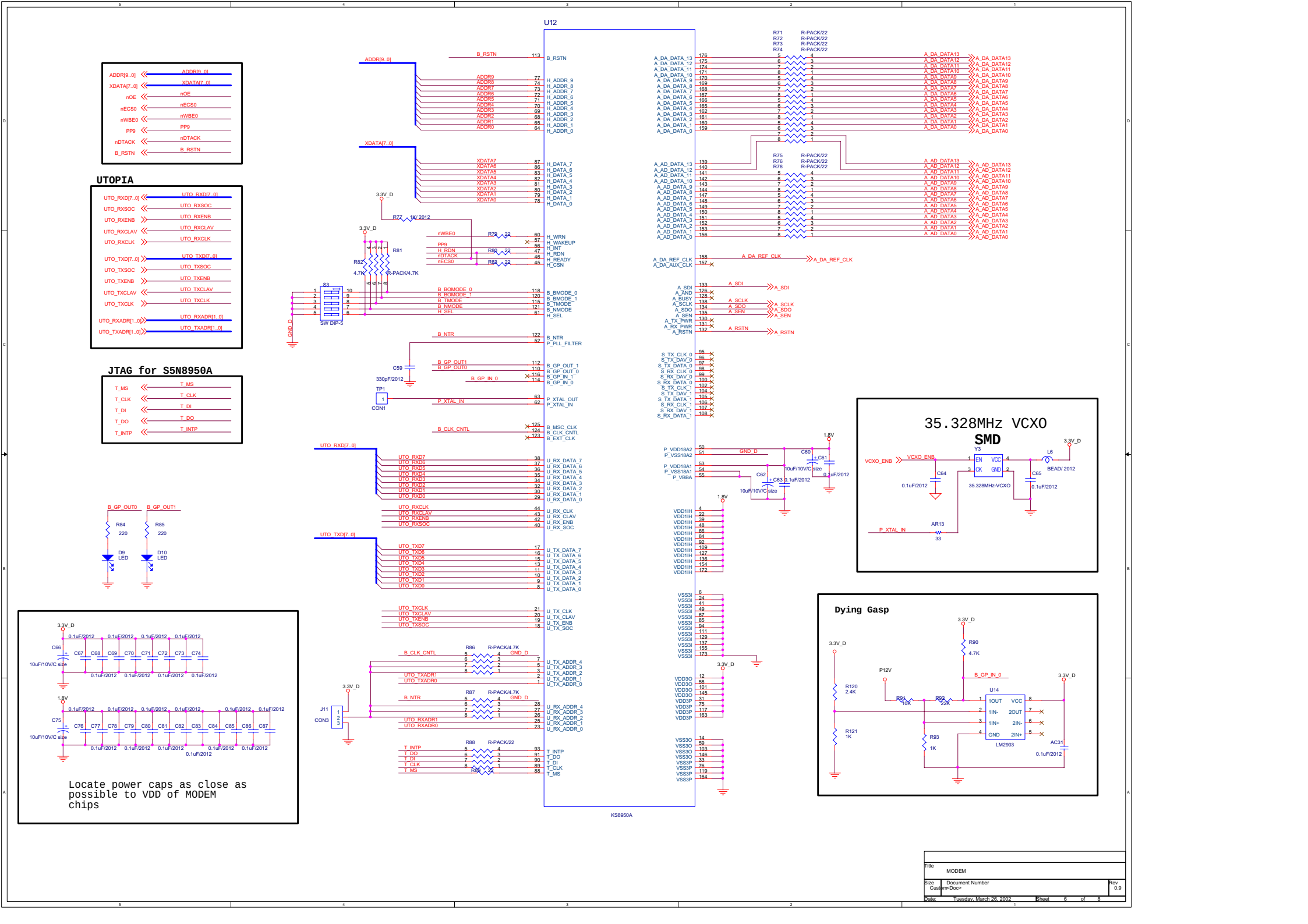
Size: Custom<Doc>	Document Number	Rev: 0.9
Date: Tuesday, March 26, 2002	Sheet 4 of 8	



TMODE	CLKSEL	FMODE	MODE DESCRIPTION
-	-	2-3(LOW)	1 Ethernet, UTOPIA 1/2
-	-	1-2(HIGH)	2 Ethernet, UTOPIA 1/2
2-3(LOW)	2-3(LOW)	-	66MHz(PLL)
1-2(HIGH)	2-3(LOW)	-	72MHz(PLL)
2-3(LOW)	1-2(HIGH)	-	direct clock input

Title	MCU
Size	Document Number: Custom<Doc>
Rev	0.9
Date:	Tuesday, March 26, 2002
Sheet	5 of 8


U12
ADDR[9..0]
XDATA[7..0]
UTOPIA
UTO_RXD[7..0]
UTO_RXSOC
UTO_RXENB
UTO_RXCLAV
UTO_RXCLK
UTO_TXD[7..0]
UTO_TXSOC
UTO_TXENB
UTO_TXCLAV
UTO_TXCLK
UTO_RXADR[1..0]
UTO_TXADR[1..0]
JTAG for S5N8950A
T_MS
T_CLK
T_DI
T_DO
T_INTP
B_RSTN
nWBE0
PP9
nDTACK
nECS0
nOE
H_RDN
H_WRN
H_WAKEUP
H_INT
H_READY
H_CSN
H_ADDR_9
H_ADDR_8
H_ADDR_7
H_ADDR_6
H_ADDR_5
H_ADDR_4
H_ADDR_3
H_ADDR_2
H_ADDR_1
H_ADDR_0
H_DATA_7
H_DATA_6
H_DATA_5
H_DATA_4
H_DATA_3
H_DATA_2
H_DATA_1
H_DATA_0
3.3V_D
R77 1K/ 2012
R81
R82
4.7K
R-PACK/4.7K
S3
SW DIP-5
GND_D
B_BOMODE_0
B_BOMODE_1
B_TMODE
B_NMODE
H_SEL
B_NTR
P_PLL_FILTER
C59
330pF/2012
B_GP_OUT1
B_GP_OUT0
B_GP_IN_0
TP1
CON1
P_XTAL_IN
P_XTAL_OUT
B_CLK_CNTL
B_MSC_CLK
B_CLK_CNTL
B_EXT_CLK
U_RX_DATA_7
U_RX_DATA_6
U_RX_DATA_5
U_RX_DATA_4
U_RX_DATA_3
U_RX_DATA_2
U_RX_DATA_1
U_RX_DATA_0
U_RX_CLK
U_RX_CLAV
U_RX_ENB
U_RX_SOC
U_TX_DATA_7
U_TX_DATA_6
U_TX_DATA_5
U_TX_DATA_4
U_TX_DATA_3
U_TX_DATA_2
U_TX_DATA_1
U_TX_DATA_0
U_TX_CLK
U_TX_CLAV
U_TX_ENB
U_TX_SOC
R86 R-PACK/4.7K
GND_D
U_TX_ADDR_4
U_TX_ADDR_3
U_TX_ADDR_2
U_TX_ADDR_1
U_TX_ADDR_0
J11
CON3
R87 R-PACK/4.7K
U_RX_ADDR_4
U_RX_ADDR_3
U_RX_ADDR_2
U_RX_ADDR_1
U_RX_ADDR_0
R88 R-PACK/22
T_INTP
T_DO
T_DI
T_CLK
T_MS
R71 R-PACK/22
R72 R-PACK/22
R73 R-PACK/22
R74 R-PACK/22
A_DA_DATA_13
A_DA_DATA_12
A_DA_DATA_11
A_DA_DATA_10
A_DA_DATA_9
A_DA_DATA_8
A_DA_DATA_7
A_DA_DATA_6
A_DA_DATA_5
A_DA_DATA_4
A_DA_DATA_3
A_DA_DATA_2
A_DA_DATA_1
A_DA_DATA_0
R75 R-PACK/22
R76 R-PACK/22
R78 R-PACK/22
A_AD_DATA_13
A_AD_DATA_12
A_AD_DATA_11
A_AD_DATA_10
A_AD_DATA_9
A_AD_DATA_8
A_AD_DATA_7
A_AD_DATA_6
A_AD_DATA_5
A_AD_DATA_4
A_AD_DATA_3
A_AD_DATA_2
A_AD_DATA_1
A_AD_DATA_0
A_DA_REF_CLK
A_DA_AUX_CLK
A_SDI
A_AND
A_BUSY
A_SCLK
A_SDO
A_SEN
A_TX_PWR
A_RX_PWR
A_RSTN
S_TX_CLK_0
S_TX_DAV_0
S_TX_DATA_0
S_RX_CLK_0
S_RX_DAV_0
S_RX_DATA_0
S_TX_CLK_1
S_TX_DAV_1
S_TX_DATA_1
S_RX_CLK_1
S_RX_DAV_1
S_RX_DATA_1
P_VDD18A2
P_VSS18A2
P_VDD18A1
P_VSS18A1
P_VBBA
GND_D
C60
C61
10uF/10V/C size
0.1uF/2012
C62
C63
VDD1IH
VSS3I
VDD3O
VDD3P
VSS3O
VSS3P
1.8V
3.3V_D
35.328MHz VCXO
SMD
Y3
VCXO_ENB
C64
0.1uF/2012
35.328MHz-VCXO
C65
L6
BEAD/ 2012
AR13
33
P_XTAL_IN
Dying Gasp
P12V
R90
4.7K
R120
2.4K
R121
1K
R91
10K
R92
22K
R93
1K
U14
LM2903
1OUT
VCC
1IN-
2OUT
1IN+
2IN-
GND
2IN+
AC31
0.1uF/2012
B_GP_IN_0
B_GP_OUT0
B_GP_OUT1
R84
220
R85
220
D9
LED
D10
LED
C66
C67
C68
C69
C70
C71
C72
C73
C74
C75
C76
C77
C78
C79
C80
C81
C82
C83
C84
C85
C86
C87
Locate power caps as close as possible to VDD of MODEM chips
KS8950A
Title
MODEM
Size
Document Number
Custom<Doc>
Rev
0.9
Date:
Tuesday, March 26, 2002
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of
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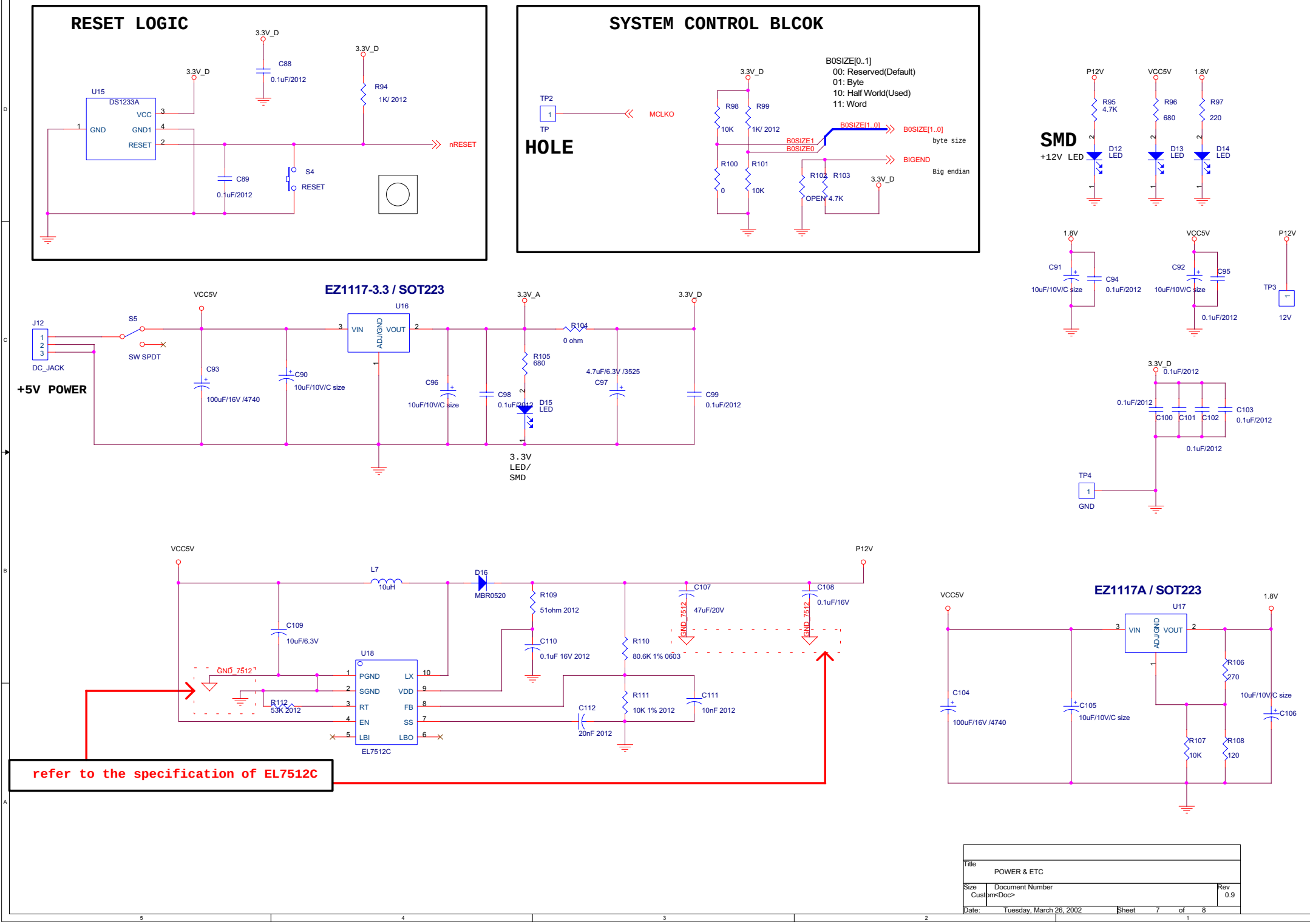
RESET LOGIC
U15
DS1233A
VCC
GND
GND1
RESET
3.3V_D
C88
0.1uF/2012
R94
1K/ 2012
C89
0.1uF/2012
S4
RESET
nRESET
SYSTEM CONTROL BLCOK
TP2
TP
MCLKO
HOLE
R98
10K
R99
1K/ 2012
R100
0
R101
10K
B0SIZE[0..1]
00: Reserved(Default)
01: Byte
10: Half World(Used)
11: Word
B0SIZE1
B0SIZE0
B0SIZE[1..0]
byte size
BIGEND
Big endian
R102
OPEN
R103
4.7K
SMD
+12V LED
P12V
VCC5V
1.8V
R95
4.7K
R96
680
R97
220
D12
LED
D13
LED
D14
LED
EZ1117-3.3 / SOT223
U16
VIN
ADJ/GND
VOUT
J12
DC_JACK
S5
SW SPDT
+5V POWER
VCC5V
C93
100uF/16V /4740
C90
10uF/10V/C size
C96
10uF/10V/C size
C98
0.1uF/2012
3.3V_A
R104
0 ohm
R105
680
D15
LED
4.7uF/6.3V /3525
C97
3.3V_D
C99
0.1uF/2012
3.3V
LED/
SMD
C91
10uF/10V/C size
C94
0.1uF/2012
C92
10uF/10V/C size
C95
0.1uF/2012
TP3
12V
3.3V_D
0.1uF/2012
C100
C101
C102
C103
0.1uF/2012
TP4
GND
VCC5V
L7
10uH
D16
MBR0520
P12V
C109
10uF/6.3V
R109
51ohm 2012
C110
0.1uF 16V 2012
R110
80.6K 1% 0603
C107
47uF/20V
C108
0.1uF/16V
GND_7512
U18
PGND
SGND
RT
EN
LBI
LX
VDD
FB
SS
LBO
EL7512C
R112
53K 2012
R111
10K 1% 2012
C111
10nF 2012
C112
20nF 2012
refer to the specification of EL7512C
EZ1117A / SOT223
U17
C104
100uF/16V /4740
C105
10uF/10V/C size
R106
270
R107
10K
R108
120
C106
10uF/10V/C size
Title
POWER & ETC
Size
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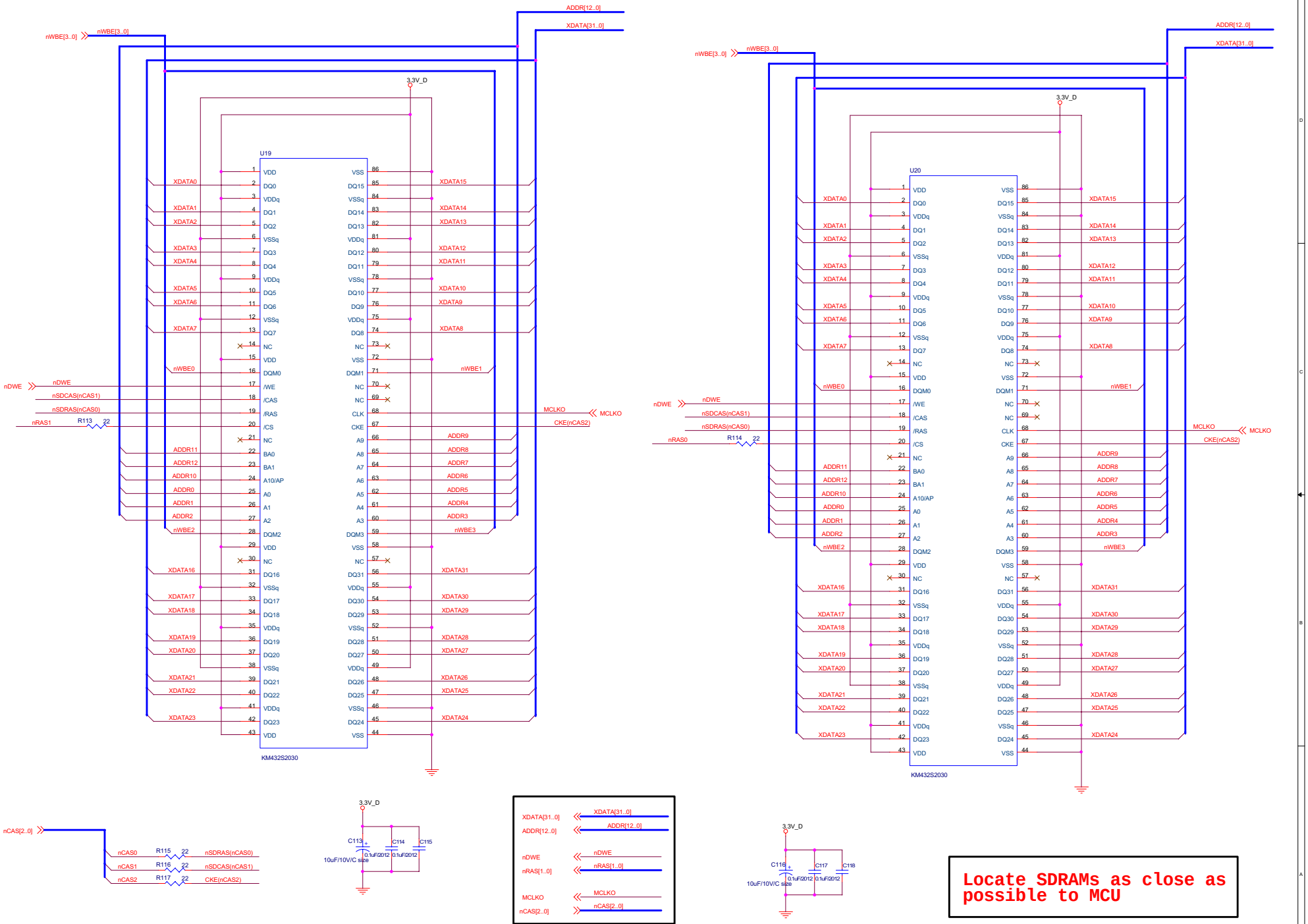

Title	SDRAM	
Size C	Document Number <Doc>	Rev 0.9
Date: Tuesday, March 26, 2002	Sheet 8 of 8	