

# **ART2768**

## **User's Manual**



**Beijing ART Technology Development Co., Ltd.**

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## Chapter 1 Overview

ART2768 is an arbitrary waveform generator card based on PC104 bus, can be connected to the computer's PC104 interface to constitute the laboratory, product quality inspection center and other areas of data acquisition, waveform analysis and processing system. And also can constitute industrial process monitoring system. Its main applications are:

- Electronic Product Quality Testing
- Signal acquisition
- Process Control
- Servo Control

### Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.

Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- Art2768 Data Acquisition Board
- ART Disk
  - a) user's manual (pdf)
  - b) drive
  - c) catalog
- Warranty Card

### DA Arbitrary Waveform Output Function

- Converter Type: DAC7641
- Output Range: 0~5V, 0~10V, ±5V, ±10V
- Resolution: 16-bit
- Output Point Rate (Frequency): up to 1MHz (1us/point). software adjustable, adjustable range: 0.01Hz ~ 1MHz
- Number of Channels: 4
- Trigger Source : software trigger source, hardware analog trigger source (ATR), hardware digital trigger source (DTR)
- Trigger Level: 0 ~ 10V
- Trigger Direction (TriggerDir): negative trigger, positive trigger, either positive or negative trigger
- Clock Source: internal clock and external (software selectable)
- Memory Depth: each channel is 256K word (point) RAM Memory
- Data Transmission: program mode
- DA Set-up Time: 10μs (0.003% accuracy)
- Non-linear Error: ±3LSB (maximum)
- Output error (full-scale): ±2LSB
- Operating Temperature Range: 0°C ~ +50°C
- Storage Temperature Range: - 20°C ~ +70°C

## Digital Input

- Channel No.: 4-channel
- Electric Standard: TTL compatible
- High Voltage:  $\cong 2\text{V}$
- Low Voltage:  $\cong 0.8\text{V}$

## Digital Output

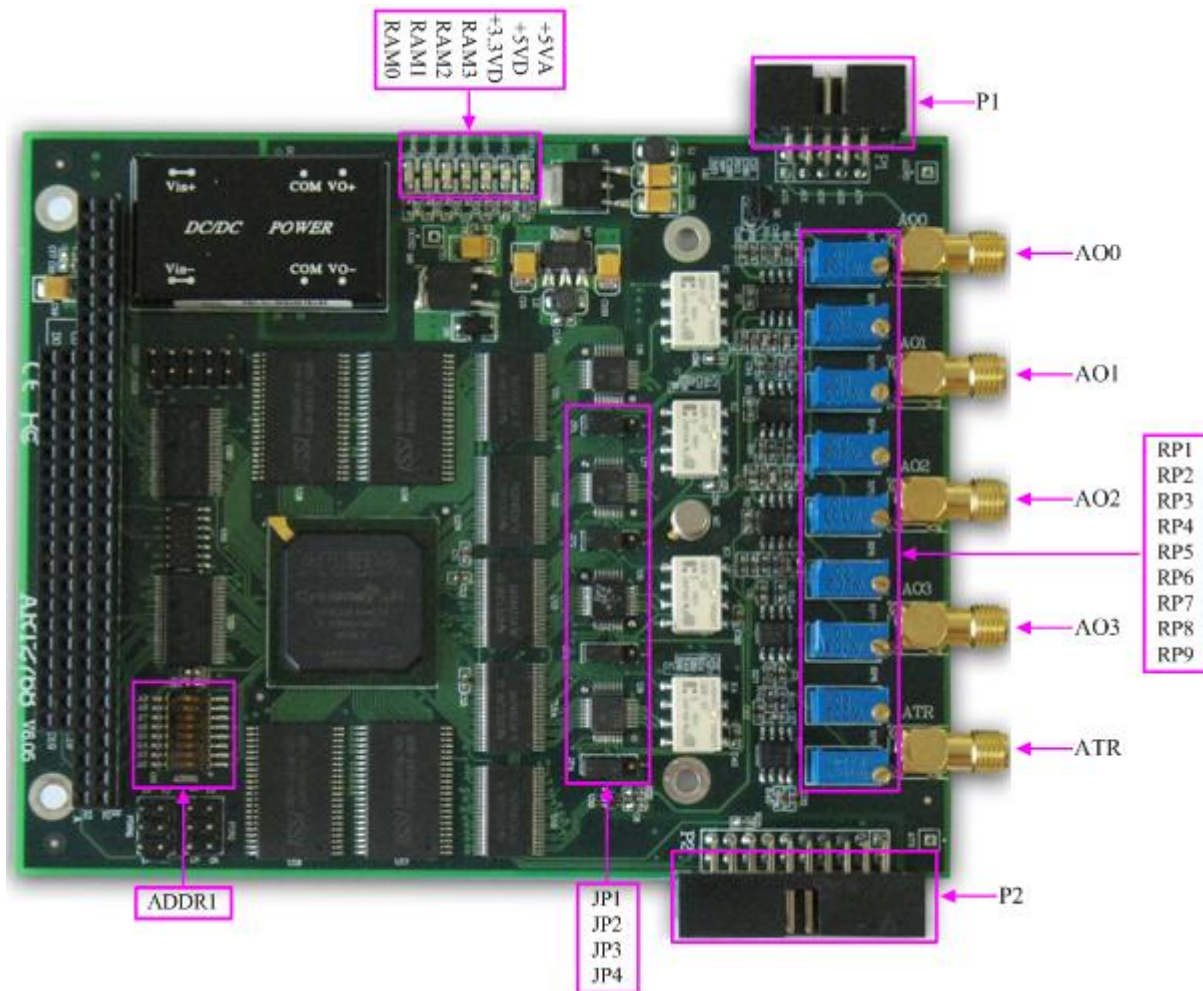
- Channel No.: 4-channel
- Electrical Standard: TTL compatible
- High Voltage:  $\cong 3.8\text{V}$
- Low Voltage:  $\cong 0.44\text{V}$
- Power-on Reset

## Other Features

- On-board Clock Oscillator: 40MHz
- Dimension: 102mm (L) \* 127mm (W) \* 16mm (H)

## Chapter 2 Components Layout Diagram and a Brief Description

### 2.1 The Main Component Layout Diagram



### 2.2 The Function Description for the Main Component

#### 2.2.1 Signal Input and Output Connectors

- P1: Analog signal output connector
- P2: Digital signal input/output connector
- AO0: Analog output interface
- AO1: Analog output interface
- AO2: Analog output interface
- AO3: Analog output interface
- ATR: Analog trigger signal input interface

## 2.2.2 Potentiometer

RP1: AO0 analog output zero-point adjustment

RP2: AO0 analog output full-scale adjustment

RP3: AO1 analog output zero-point adjustment

RP4: AO1 analog output full-scale adjustment

RP5: AO2 analog output zero-point adjustment

RP6: AO2 analog output full-scale adjustment

RP7: AO3 analog output zero-point adjustment


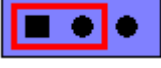
RP8: AO3 analog output full-scale adjustment

RP9: ATR trigger level adjustment

## 2.2.3 Jumper

JP1, JP2, JP3, JP4: AO0 ~ AO3 analog output signal reset selection, when the 2-3 pins of the jumpers corresponding to the channels are shorted, the range reset to the 0 code value (0x000), when 1-2 pins are shorted, reset to the middle code value of the range (0x800).

Corresponds to the DA range, the reset value selection as follows:

JP1, JP2, JP3, JP4	0~5V	0~10V	±5V	±10V
	0V	0V	-5V	-10V
	2.5V	5V	0V	0V

PIRQ, PDRQ: reserved

## 2.2.4 Board Base Address Selection

ADDR1: board base address DIP switches. Board base address can be set to binary code which from 200H to 3F0H be divided by 16, board base address defaults 300H, will occupy the base address of the date of 44 consecutive I/O addresses. Switch No. 3, 4, 5, 6, 7, 8 correspond to address bits A4, A5, A6, A7, A8, A9 are the base address of selector switch, Switch No.1, 2 are reserved bits.

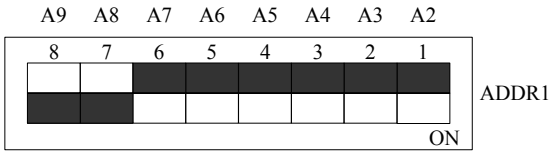
Board base address selection is as follows: when the ADDR1 switches dial to "ON" that means the high virtual is 1, the switch to the other side means the low virtual value is 0.

Base address configuration methods

Address bit	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X is configurable bit	unused	unused	x	x	x	x	x	x	x	0	0	0
	The third hex bits			The second hex bits				The first hex bits				

Note: in the table, the bit which is labeled "0" is a fixed value, only the bit that labeled "x" can be changed by the ADDR1.

For example, the default base addresses is 300H, A8, A9= "ON", shown as the following:



Common base address

Adr	ADDR1	Adr	ADDR1
200H		210H	
220H		230H	
240H		250H	
260H		270H	
280H		290H	
2A0H		2B0H	
2C0H		2D0H	

2E0H		2F0H	
300H		310H	
320H		330H	
340H		350H	
360H		370H	
380H		390H	
3A0H		3B0H	
3C0H		3D0H	
3E0H		3F0H	



## 2.2.5 Indicator

+5 VA: +5V analog power indicator

+5 VD: +5V digital power indicator

+3.3 VD: +3.3V digital power indicator

RAM3: AO3 analog output channel RAM status indicator

RAM2: AO2 analog output channel RAM status indicator

RAM1: AO1 analog output channel RAM status indicator

RAM0: AO0 analog output channel RAM status indicator

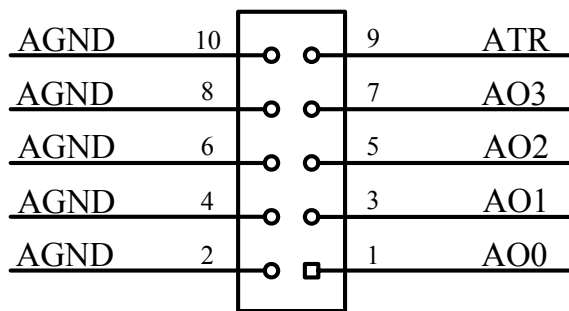
## Chapter 3 Signal Connectors

### 3.1 Analog Input/Output Interface

ART2768 has five signal interface, AO0, AO1, AO2, AO3, and ATR signal port, AO0, AO1, AO2, AO3 are analog output ports of the 4 channels DA, corresponding to the AO0 ~ AO3 pins of the P1, ATR is analog trigger signal input port, corresponding to the ATR pin of the P1.

### 3.2 Analog Signal Connector

P1: 10-pin definition

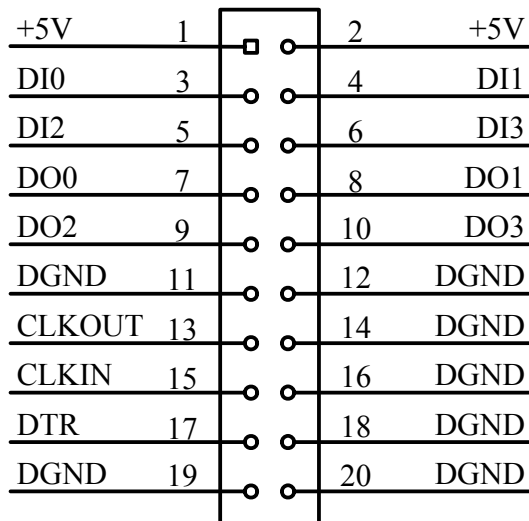


Pin definition

Signal Name	Type	Definition
AO0~AO3	Output	Analog output pins
ATR	Input	Analog trigger signal input port
AGND	GND	Analog ground

### 3.3 Digital Input/Output Connector

P2: 20-pin definition

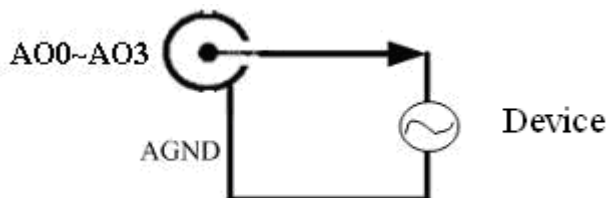


## Pin definition

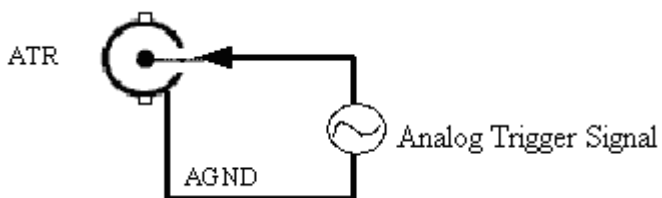
Signal Name	Type	Definition
CLKIN	Input	External clock input pin
CLKOUT	Output	Internal clock output pin
DTR	Input	External digital trigger signal input pin
+5V	PWR	+5V power output pin
DGND	GND	Digital ground
NC		NC

## Chapter 4 Connection Ways for Input and Output

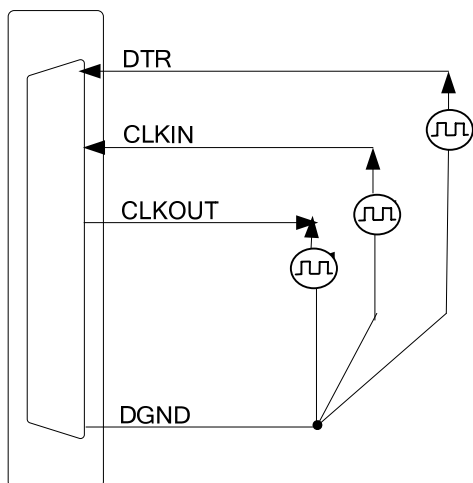
### 4.1 Analog Output Connection



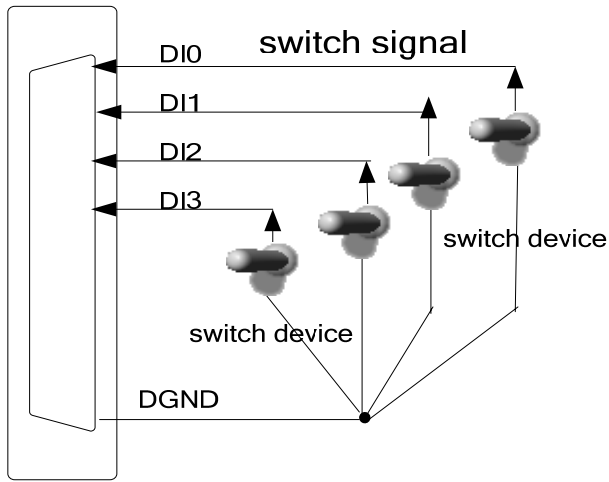
### 4.2 External Trigger Signal (ART) Connection



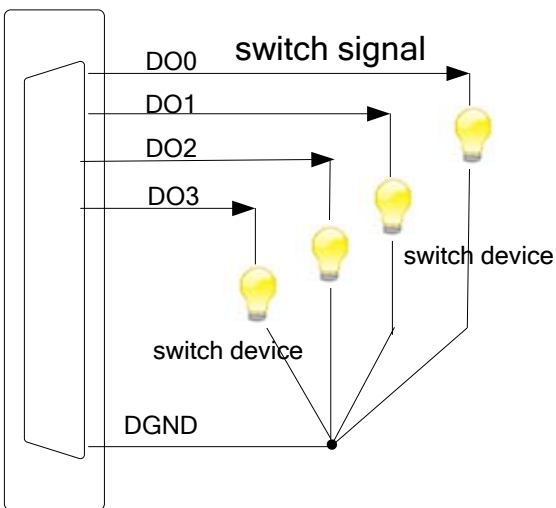
### 4.3 Clock input/Output and Digital Trigger Signal Connection



### 4.4 Digital Signal Input Connection



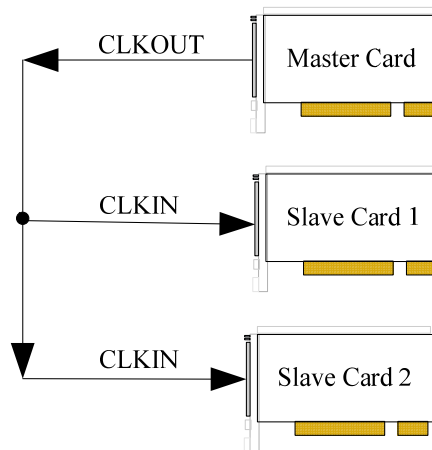
### 4.5 Digital Signal Output Connection



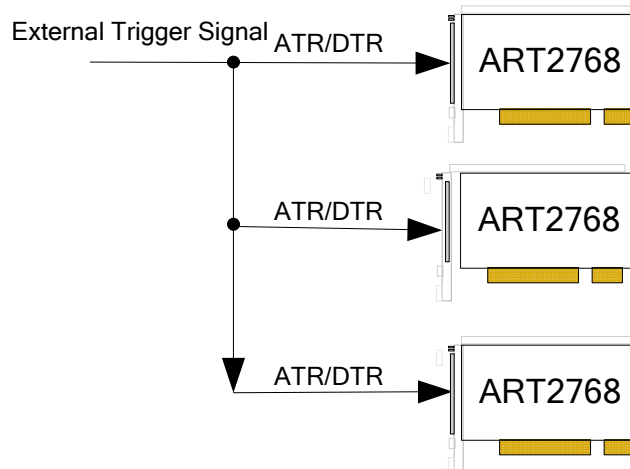
## 4.6 Methods of Realizing the Multi-card Synchronization

Three methods can realize the synchronization for the ART2768, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.

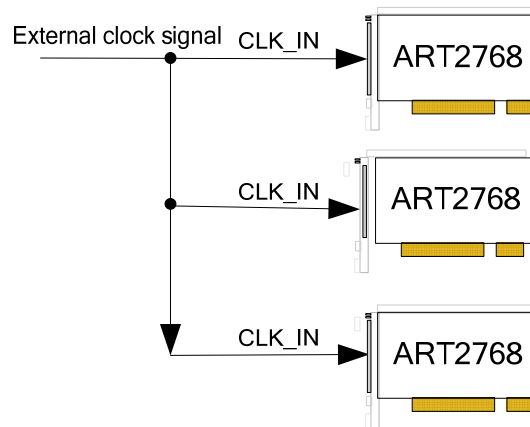


When using the common external trigger, please make sure all parameters of different ART2768 are the same. At first, configure hardware parameters, and use analog or digital signal triggering (ATR or DTR), then connect the signal that will be sampled by ART2768, input triggering signal from ART pin or DTR pin, then click “Start Sampling” button, at this time, ART2768 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



When using the common external clock trigger, please make sure all parameters of different ART2768 are the same. At first, configure hardware parameters, and use external clock, then connect the signal that will be sampled by ART2768, input trigger signal from ART pin or DTR pin, then click “Start Sampling” button, at this time, ART2768 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the

common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:



## Chapter 5 The Instruction of the DA Trigger Function

### 5.1 DA Internal Trigger Mode

When DA is in the initialization, if the DA hardware parameter DAPara. TriggerSource= ART2768\_TRIGMODE\_SOFT, we can achieve the internal trigger acquisition. In this function, calling the InitDeviceDA function to initial the device, then wait EnableDeviceDA function to start DA, DA immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the DA work pulse is decided by the sampling frequency.

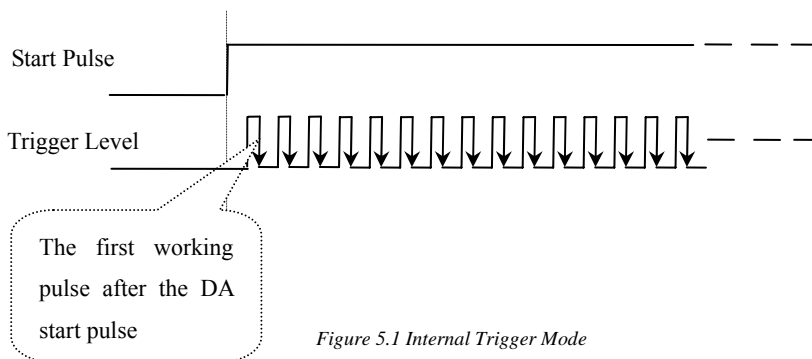


Figure 5.1 Internal Trigger Mode

### 5.2 DA External Trigger Mode

When DA is in the initialization, if the DA hardware parameter DAPara. TriggerSource= ART2768\_TRIGSRC\_ATR, we can achieve the ATR trigger acquisition, if DAPara. TriggerSource=ART2768\_TRIGSRC\_DTR, we can achieve the DTR trigger acquisition. In this function, calling the InitDeviceDA function to initial the device, then wait EnableDeviceDA function to start DA, DA will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source includes the DTR (Digital Trigger Source) and ATR (Analog Trigger Source).

#### 5.2.1 ATR Trigger

Analog trigger source uses the analog signal which can change in a certain range. The trigger source signal provided by the ATR and the analog trigger level are into the comparator simultaneously, and the do high-speed analog comparison in the comparator, generate a comparison expected result (Result) to trigger DA (see below). Analog trigger signal decided by the voltage that output by the serial D/A. The analog trigger source signal effective range is LVTTTL, it can be achieved through the computer writes the serial number to the D/A, the software function is SetDevTrigLevelDA ().



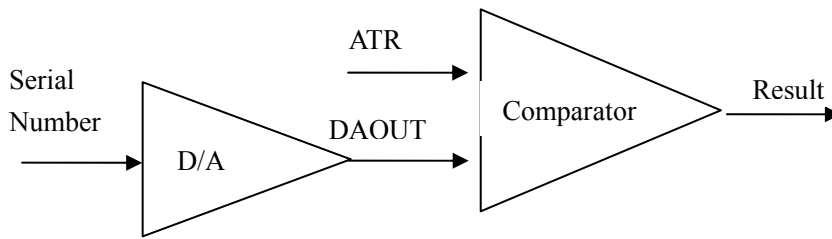


Figure 5.2 Analog Comparator

When `DAPara.TriggerDir = ART2768_TRIGDIR_POSITIVE`, it is positive trigger, that is, when ATR trigger source signal changes from smaller than trigger level to higher than trigger level, DA immediately into the conversion process, in this case, its follow-up changes have no effect on DA acquisition, unless the user re-initialize the AD.

When `DAPara.TriggerDir = ART2768_TRIGDIR_NEGATIVE`, it is negative trigger, it is triggered in the opposite direction with the positive, but the others are the same as the positive trigger. See the Figure 5.3:

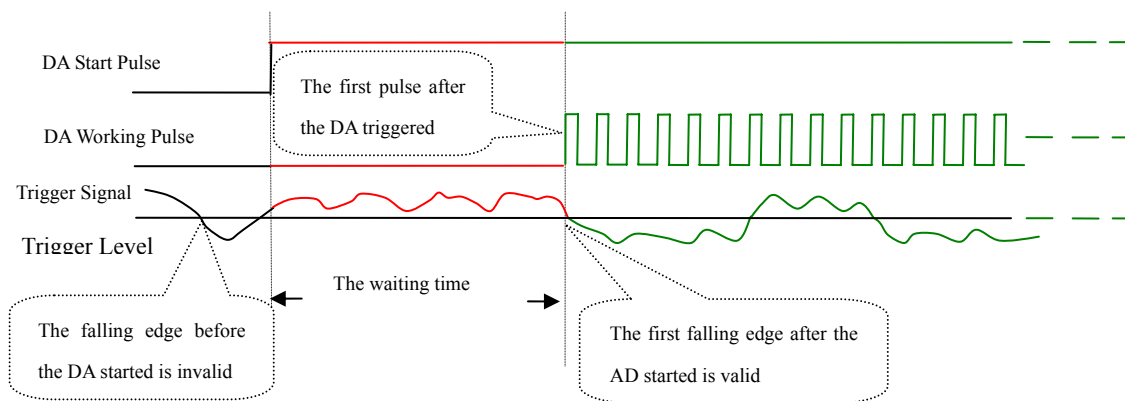


Figure5.3 Falling Edge Trigger

When `DAPara.TriggerDir = ART2768_TRIGDIR_POSIT_NEGAT`, choose the trigger mode as rising or falling edge trigger. As long as the trigger sources signal across the trigger level, it will trigger DA immediately. The follow-up changes have no effect on DA acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

## 5.2.2 DTR Trigger

`DAPara.TriggerDir = ART2768_TRIGDIR_NEGATIVE`, that is negative trigger. When the trigger signal changes from the high-level to low-level (falling edge signal), it will generate a trigger event, DA immediately into the conversion process, and its follow-up changes have no effect on DA acquisition.

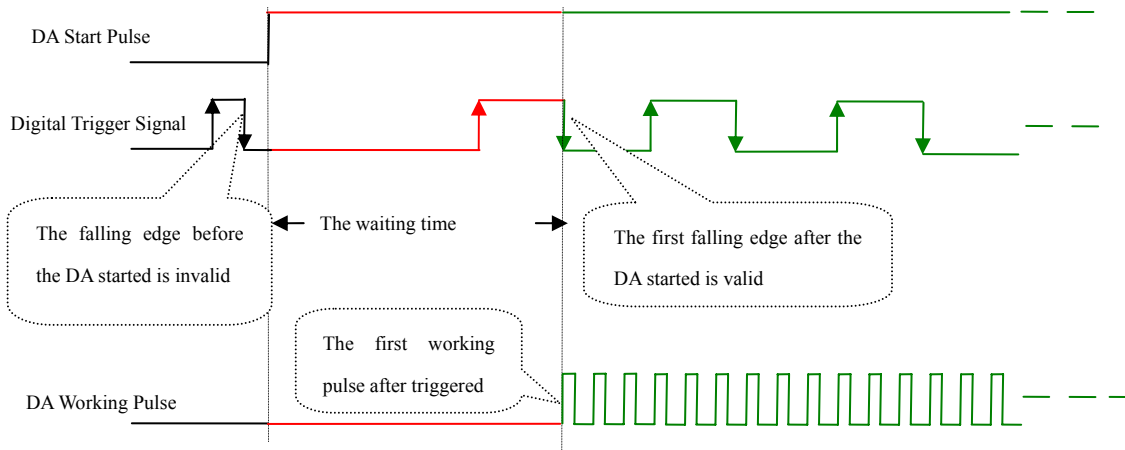


Figure5.4 Falling Edge Trigger

DAPara.TriggerDir = ART2768\_TRIGDIR\_POSITIVE, that is positive trigger. When the trigger signal changes from the low-level to high-level (rising edge signal), it will generate a trigger event, DA immediately into the conversion process, and its follow-up changes have no effect on DA acquisition.

When ADPara.TriggerDir = ART2768\_TRIGDIR\_POSIT\_NEGAT, choose the trigger mode as rising or falling edge trigger. As long as the trigger sources signal appear high-level or low-level (rising edge or falling edge), it will trigger DA immediately. The follow-up changes have no effect on DA acquisition. This function can be used in the case that the acquisition will occur if the exoteric signal changes.

## ***Chapter 6 Methods of using Internal and External Clock Function***

### **6.1 Internal Clock Function**

Internal clock function use the clock signal that generated by the on-board clock oscillator to trigger DA conversion (ie, DA refresh clock). The clock of the waveform data that stored in the RAM is generated on-board logic control circuit, and according to the user specified frequency divided by the number, the max clock is the same as the trigger DA frequency, the min clock is the 65535 times of the DA trigger frequency, in this case, we can achieve slow playback the waveform in the RAM. To use the internal clock function, the hardware parameters `DAPara.ClockSouce = ART2768_CLOCKSRC_IN` should be installed in the software. The frequency of the clock in the software depends on the hardware parameters `DAPara.Frequency`. For example, if `Frequency = 100000`, that means the speed of read waveform is 100KHz, but the DA's refresh clock unchanged , it is still 40MHz.

### **6.2 External Clock Function**

External clock function uses the external clock signal to trigger the DA. The clock signal is provided by the CLKIN pin. To use the external clock function, the hardware parameters `DAPara.ClockSouce = ART2768_CLOCKSRC_OUT` should be installed in the software. The clock frequency depends on the external clock frequency. In external clock mode, both the read waveform data clock and DA refresh frequency are the same as external.

## Chapter 7 Address Allocation Table

ART2768 register address as follows:

Base address +0 x0 write control address	Base address+0x2 write data	Base address+0x2 read data
0x0000	Read back	DA0_MODE control word, the low 7-bit effective
0x0001	Read back	DA0 frequency control word (16bit)
0x0002	Read back	DA0 enable signal D15 = 0: disable DA0 convert D15 = 1: start DA0 to convert (if use the external trigger, need to wait for the trigger signal to start DA). = 0: allow users to access RAM0, = 1: disable users do any operation of the RAM0.
0x0003	Reserved	Reserved
0x0004	Read back	The current low 16-bit offset address of the RAM0
0x0005	Read back	The current high 2-bit offset address of the RAM0 (data low 2-bit)
0x0006	Read DA0 data from the RAM0	Write the data will be converted by the DA0 to the RAM0 (16-bit)
0x0007	Read back	Low 16-bit of the loop start address
0x0008	Read back	High 2-bit of the loop start address (data low 2-bit)
0x0009	Read back	The cycle end address low 16-bit
0x000a	Read back	The cycle end address high 2-bit (data low 2-bit)
0x000b	Read back	The number of cycles (= 0 indicates an infinite loop)
0x000c	Read back	Single point immediate output DA0 data (16-bit)
0x000d	Read back	Reset RAM0 output location to the cycle starting location
0x000e	Read back	DA0 polarity setting: = 0: unipolar, = 1: bipolar
0x000f	Read back	DA0 gain setting: = 0: single gain, = 1: double gain
0x0010	Read back	DA1_MODE control word, the low 7-bit effective
0x0011	Read back	DA1 frequency control word (16-bit)
0x0012	Read back	DA1 enable signal D15= 0: disable DA1 conversion D15= 1: start DA1 conversion ((if use the external trigger, need to wait for the trigger signal to start DA). = 0: allow users access to RAM1, = 1: disable users do any operation of the RAM1.
0x0013	Reserved	Reserved
0x0014	Read back	The current low 16-bit offset address of the RAM1
0x0015	Read back	The current high 2-bit offset address of the RAM1 (data low 2-bit)
0x0016	Read DA0 data from the RAM1	Write the data will be converted by the DA1 to the RAM1 (16-bit)

0x0017	Read back	Low 16-bit of the loop start address
0x0018	Read back	High 2-bit of the loop start address (data low 2-bit)
0x0019	Read back	The cycle end address low 16-bit
0x001a	Read back	The cycle end address high 2-bit (data low 2-bit)
0x001b	Read back	The number of cycles (= 0 indicates an infinite loop)
0x001c	Read back	Single point immediate output DA1 data (16-bit)
0x001d	Read back	Reset RAM0 output location to the cycle starting location
0x001e	Read back	DA1 polarity setting: = 0: unipolar, = 1: bipolar
0x001f	Read back	DA1 gain setting: = 0: single gain, = 1: double gain
0x0020	Read back	DA2_MODE control word, the low 6-bit effective
0x0021	Read back	DA2 frequency control word (16-bit)
0x0022	Read back	DA2 enable signal D15= 0: disable DA2 conversion D15= 1: start DA2 conversion ((if use the external trigger, need to wait for the trigger signal to start DA). = 0: allow users access to RAM2, = 1: disable users do any operation of the RAM2.
0x0023	Reserved	Reserved
0x0024	Read back	The current low 16-bit offset address of the RAM2
0x0025	Read back	The current high 2-bit offset address of the RAM2 (data low 2-bit)
0x0026	Read DA0 data from the RAM2	Write the data will be converted by the DA2 to the RAM2 (16-bit)
0x0027	Read back	Low 16-bit of the loop start address
0x0028	Read back	High 2-bit of the loop start address (data low 2-bit)
0x0029	Read back	The cycle end address low 16-bit
0x002a	Read back	The cycle end address high 2-bit (data low 2-bit)
0x002b	Read back	The number of cycles (= 0 indicates an infinite loop)
0x002c	Read back	Single point immediate output DA2 data (16-bit)
0x002d	Read back	Reset RAM2 output location to the cycle starting location
0x002e	Read back	DA2 polarity setting: = 0: unipolar, = 1: bipolar
0x001f	Read back	DA2 gain setting: = 0: single gain, = 1: double gain
0x0030	Read back	DA3_MODE control word, the low 6-bit effective
0x0031	Read back	DA3 frequency control word (16-bit)
0x0032	Read back	DA3 enable signal D15= 0: disable DA3 conversion D15= 1: start DA3 conversion ((if use the external trigger, need to wait for the trigger signal to start DA). = 0: allow users access to RAM3, = 1: disable users do any operation of the RAM3.
0x0033	Reserved	Reserved
0x0034	Read back	The current low 16-bit offset address of the RAM3
0x0035	Read back	The current high 2-bit offset address of the RAM3

		(data low 2-bit)
0x0036	Read DA3 data from the RAM2	Write the data will be converted by the DA3 to the RAM3 (16-bit)
0x0037	Read back	Low 16-bit of the loop start address
0x0038	Read back	High 2-bit of the loop start address (data low 2-bit)
0x0039	Read back	The cycle end address low 16-bit
0x003a	Read back	The cycle end address high 2-bit (data low 2-bit)
0x003b	Read back	The number of cycles (= 0 indicates an infinite loop)
0x003c	Read back	Single point immediate output DA3 data (16-bit)
0x003d	Read back	Reset RAM3 output location to the cycle starting location
0x003e	Read back	DA3 polarity setting: = 0: unipolar, = 1: bipolar
0x003f	Read back	DA3 gain setting: = 0: single gain, =1: double gain
0x0040	4-ch digital input	4-ch digital output
0x0041	Read back	Analog trigger level low 8-bit
0x0042	Version: [D15: D0]: firmware version	Invalid
0x0043	Version: [D7: D0]: hardware version [D15: D8]: Reserved	Invalid

## Chapter 8 Notes and Warranty Policy

### 8.1 Notes

In our products' packing, user can find a user manual, a Art2768 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using Art2768, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of Art2768 module.

### 8.2 Analog Signal Output Calibration

In the manual, we introduce how to calibrate ART2768 in  $\pm 5V$  input range; calibrations of other input ranges are similar.

1. Connect the ground both of the digital voltmeter and P1 connector, the input port of the voltmeter connects with the DA which need to be calibrated.
2. Zero-point Calibration: run ART2768 advanced program under Windows, select AO0 channel, the DA output is set to 0, adjust the potentiometer RP1 to make AO0 channel output 0V. Adjust the potentiometer RP3, RP5, RP7 to make AO1~ AO3 output 0V.
3. Full-scale Calibration: run ART2768 advanced program under Windows, select AO0 channel, the DA output is set to 65535, by adjusting the potentiometer RP2 to make AO0 output 4999.84mV, and by adjusting the potentiometer RP4, RP6, RP8 to make AO1~ AO3 output 4999.84mV.
4. Trigger Level Calibration: When use the trigger function, the user can set the trigger level 0~10V, by adjusting the potentiometer RP9, measure the ATR test point that outside the on-board BNC5 interface, to make the measured trigger level be the same as the trigger level that be set.
5. Repeat steps above until meet the requirement.

### 8.3 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: [www.art-control.com](http://www.art-control.com).
2. All ART products come with a limited two-year warranty:
  - The warranty period starts on the day the product is shipped from ART's factory
  - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
  - Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated

software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.



# Products Rapid Installation and Self-check

## Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button **【driver installation】** ; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

## Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

## Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.