3GBit/s Digital Automotive Pixel Link Transmitter

INAP378TAQ

The INAP378TAQ together with the INAP378RAQ receiver offers the next generation high speed digital serial link for CAMERA applications. It provides a DC-balanced, AC coupled low latency, point-to-point link over shielded twisted pair (STP) cables. Its scalable physical layer provides bandwidth of up to 3 GBit/s at lowest EMI. The INAP378TAQ supports popular automotive image sensor solutions with video resolutions such as 1280x800 pixels and refresh rates of up to 45fps. The device offers a parallel video interface for support of up to 16 color bits + 2 control bits. Software adjustable driver characteristics and configurable operating modes allow the transmission of 1.5 GBit/s at distances of up to 25m over a single pair of wires. In addition to the video transmission the INAP378TAQ provides completely independent Full Duplex Communication channels. Using the internal AShell protocol, data transfers are protected by error detection and retransmission mechanisms.

Additionally, the link is optimized to carry low latency GPIO signals for reset or synchronization purposes.

Applications:

- Round View Camera Systems
- Stereo Camera Systems
- Rear View Camera Systems
- Automotive Driver Assistance
- Surveillance Systems
- Inspection Systems

Features:

- 500 MBit/s, 1 GBit/s, 1.5 GBit/s and 3 GBit/s sustained downstream link bandwidth for video data rates up to 2591 MBit/s
- up to 187.5 MBit/s upstream link bandwidth
- Configurable video interface
  - openLDI compliant LVDS interface (18 or 24 Bit)
  - Parallel Bulk Data Mode (10,12,18 Bit)
- Video resolutions up to HD resolutions
- Full duplex AShell communication channel
  - Data CRC protection and correction
- SPI slave interface
- I²C Master interface
- GPIOs for direct signalling and camera synchronization support
- I²S Audio interface
  - supports 16/24/32 Bit word length
  - supports up to 192kHz sampling
  - TDM support for up to 8 channels
- Diagnostic Features:
  - Built-In PRBS Generator
  - Embedded diagnostics
- Up to 25m distance at 1.5 GBit/s

Package:

- 92 pin aQFN

Temperature/Quality:

- -40°C to +85°C
- AEC-Q100

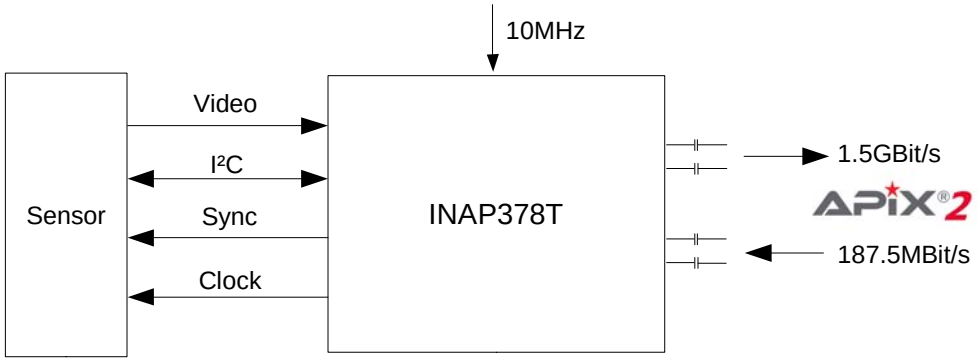


Figure 1: Application example

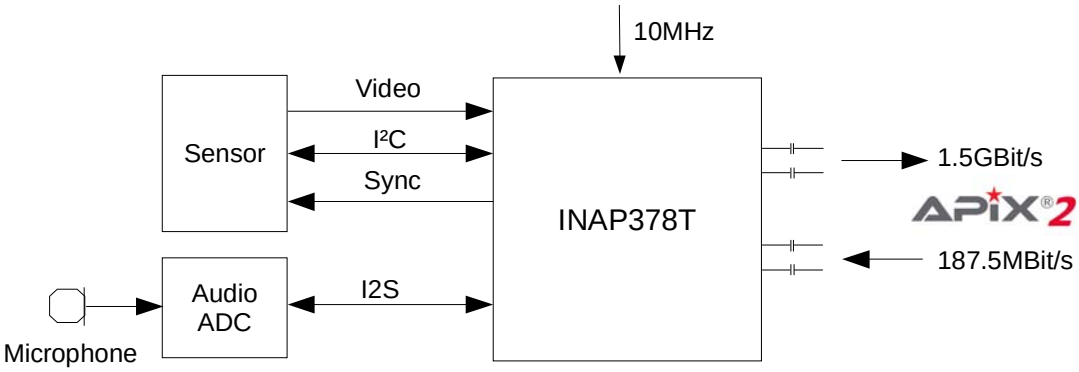


Figure 2: Application example for camera with audio

1.0 Block diagram

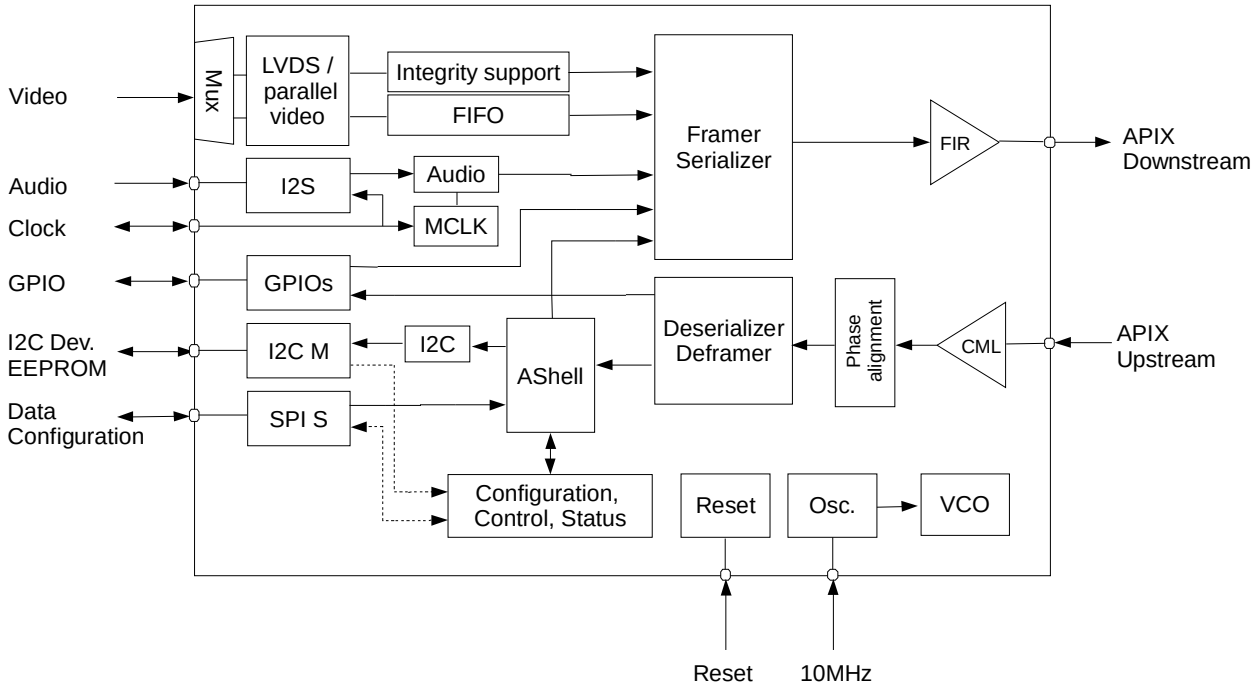


Figure 1-1: Block diagram

2.0 Electrical Characteristics

All values in this section are based on preliminary characterization. Final values will be available after product qualification.

2.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{DVDD}, V_{DVDD_XTAL}, V_{AVDD_LD}	-0.5	5.0	V	
Input Voltage	V_{VDD}, V_{AVDD}, V_{AVDD_LVDS}, V_{VDD_XTAL}	-0.5	3.0	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Storage Temperature	T_{stg}	-55	+150	° C	
Max Soldering Temperature	T_{SLD} / T_{SLD}		260	° C	40 seconds maximum
ESD Protection HBM JEDEC JESD22/A114		-3	+3	kV	R_D=1.5kΩ, C_S=100pF
ESD Protection CDM EIA/JEDEC JESD22/C101		-1	+1	kV	
ESD Protection MM EIA/JEDEC JESD22-A115A		-200	+200	V	

Table 2-1: Absolute maximum ratings

2.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Digital Core supply, Oscillator supply	V_{VDD}, V_{VDD_XTAL}	1.71	1.8	1.89	V	
Digital IO Supply, Digital Oscillator supply	V_{DVDD}, V_{DVDD_XTAL}	3.0	3.3	3.6	V	
CML PHY supply voltage, VCO supply	V_{AVDD}, V_{AVDD_VCO}	1.71	1.8	1.89	V	
CML IO supply	V_{AVDD_LD}	1.8	3.3	3.6	V	
LVDS PLL & Core supply	$V_{AVDD\_LVDS\_PLL}$, V_{AVDD_LVDS}	1.71	1.8	1.89	V	
Ambient Temperature	T_a	-40	-	+105	° C	

Table 2-2: Recommended operating conditions

2.3 Electrical Characteristics

2.3.1 Serial Interface

The INAP378TAQ downstream serial interface offers a flexible serial interface, with configurable pre-emphasis and digital filter structure. Data dependent deterministic jitter components, mainly introduced by ISI due to cable attenuation, can be compensated by pre-emphasis and equalization. Therefore only periodic and random jitter components are considered.

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Effective serial bit rise and fall time	$t_{rf\_ser\_effective}$	75	140	-	ps	
CML Drive current	I_{out_dwn}	tbd	-	-	mA	

Table 2-3: Downstream interface characteristics (SDOUT+, SDOUT-)

Parameter	Symbol	Min.	Max.	Units	Note
Differential input voltage range	V_{diff_in}	± 50	± 500	mV	
Serial input common mode range	V_{cmm_SDIN}	GND +0.7V + (V_{diff_in}/2)	V_{AVDD} +0.5V - (V_{diff_in}/2)	V	

Table 2-4: Upstream interface characteristics (SDIN+,SDIN-)

2.3.2 Supply Current

Parameter	Symbol	Typ.[a]	Max.	Unit	Comment
Digital Core & Oscillator Supply current	$I_{VDD} + I_{VDD\_XTAL}$	51	120	mA	
Digital IO & Oscillator Supply Current	$I_{DVDD} + I_{DVDD\_XTAL}$	3	50	mA	
LVDS Core & PLL Supply Current	$I_{AVDD\_LVDS} + I_{AVDD\_LVDS\_PLL}$	-	30	mA	
CML PHY Supply Current	I_{AVDD}	82	190	mA	see Figure 2-9
VCO Supply Current	I_{AVDD_VCO}	5	15	mA	
CML IO Supply Current	I_{AVDD_LD}	2	95	mA	see Figure 2-9

Table 2-5: Supply current

a. Bulk data with 95MHz pixel clock and 5m cable settings at 1.5GBit/s

2.3.3 Pixel Interface

The INAP378TAQ‘s pixel interface can be configured to parallel RGB or LVDS inputs. For further informations please refer to the INAP378TAQ user manual.

2.3.3.1 RGB Interface

Parameter	Description	Test Condition	Min.	Max.	Units
V_{IH}	Input High Voltage		2.0	V_{DVDD}	V
V_{IL}	Input Low Voltage		0	0.8	V
I_{IH}	Input High Current [a]	Vin = V_{DVDD}	-10	10	µA
I_{IL}	Input Low Current [a]	Vin = 0 V	-10	10	µA
V_{OH}	Output High Voltage	IOH= -3mA	2.4	-	V
V_{OL}	Output Low Voltage	IOL= 3mA	-	0.4	V

Table 2-6: RGB characteristics

a. input with Schmitt Trigger (current feedback of ~100µA)

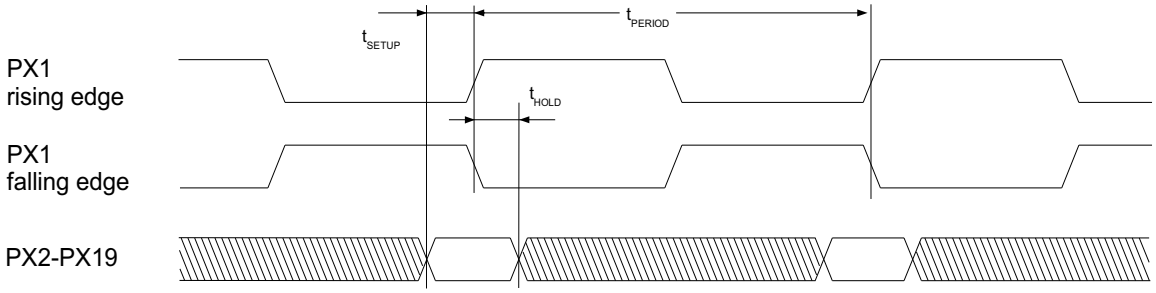


Figure 2-1: RGB Interface Timing

The capturing edge of pixel clock can be set to rising or falling. For further information please refer to the INAP378TAQ user manual. $f_{PIXEL\_CLOCK} = 1/t_{PERIOD}$. All values specified for T_A=25°C.

Parameter	Description	Test Condition	Min.	Max.	Units
f_{PIXEL_CLOCK}	Pixel Clock Input Frequency		5	120	MHz
t_{SETUP}	Setup Time Pixel Data To Pixel Clock	slew rate 2V/ns	2	-	ns
t_{HOLD}	Hold Time Pixel Data to Pixel Clock	slew rate 2V/ns	1	-	ns

Table 2-7: RGB Interface timing

2.3.3.2 LVDS Interface

LVDS interface according to TIA/EIA644 specification. Exceptions are listed at table 1-8.

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
V_{OD}	|Change to V_{OD}|	-	50	mV
V_{OS}	|Change to V_{Os}|	-	50	mV
I_{SA}	Short Circuit Current	-	24	mA
I_{IN}	Input Current	-	20	µA
V_{TH}	Receiver Threshold Voltage	-	+100	mV
V_{IN}	Input Voltage Range	0	1.8	V
f_{LVDS_CLK}	LVDS Clock Frequency	5	80	MHz

Table 2-8: LVDS interface exceptions to TIA/EIA644 specification

2.3.4 Data Interface

2.3.4.1 General Characteristics

The following characteristics are valid for SPI, GPIO, I²S and I²C functionality. The pins I2C_SCL/INBOUND_TS and I2C_SD/OUTBOUND_TS are open drain outputs and require external pull up circuitry. All values specified for T_A=25°C.

Parameter	Symbol	Test Condition	Min.	Max.	Units
Input High Voltage	V_{IH}		2.0	V_{DVDD}	V
Input Low Voltage	V_{IL}		0	0.8	V
Pull Down Current [a]	I_{IH_PD}	Vin = V_{DVDD}	30	120	µA
Input High Current	I_{IH}	Vin = V_{DVDD}	-10	10	µA
Input Low Current	I_{IL}	Vin = 0 V	-10	10	µA
Output High Voltage [b]	V_{OH}	IOH= -3mA, Figure 2-10	2.4	-	V
Output Low Voltage	V_{OL}	IOL= 3mA, Figure 2-10	-	0.4	V
Output Rise Time [b]	t_{RO}	C_L=5pF	-	2.6	ns
Output Fall Time [b]	t_{FO}	C_L=5pF	-	2.1	ns

Table 2-9: General IO Characteristics

a. pins with internal pull down to GND
b. not relevant for open drain outputs

2.3.4.2 SPI Slave Interface timing

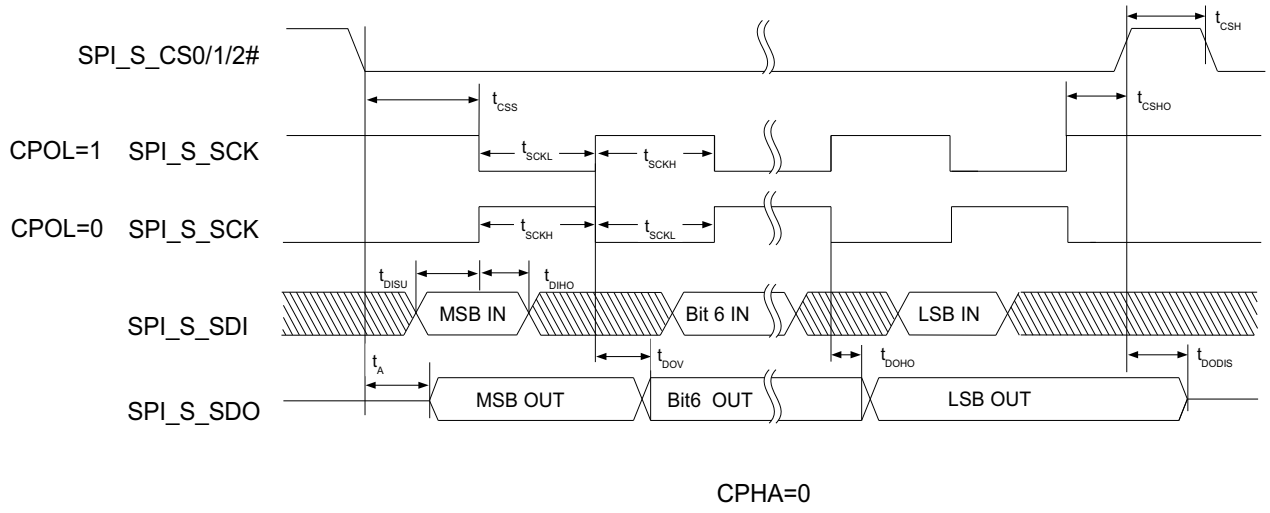


Figure 2-2: SPI Slave Timing Diagram (CPHA=0)

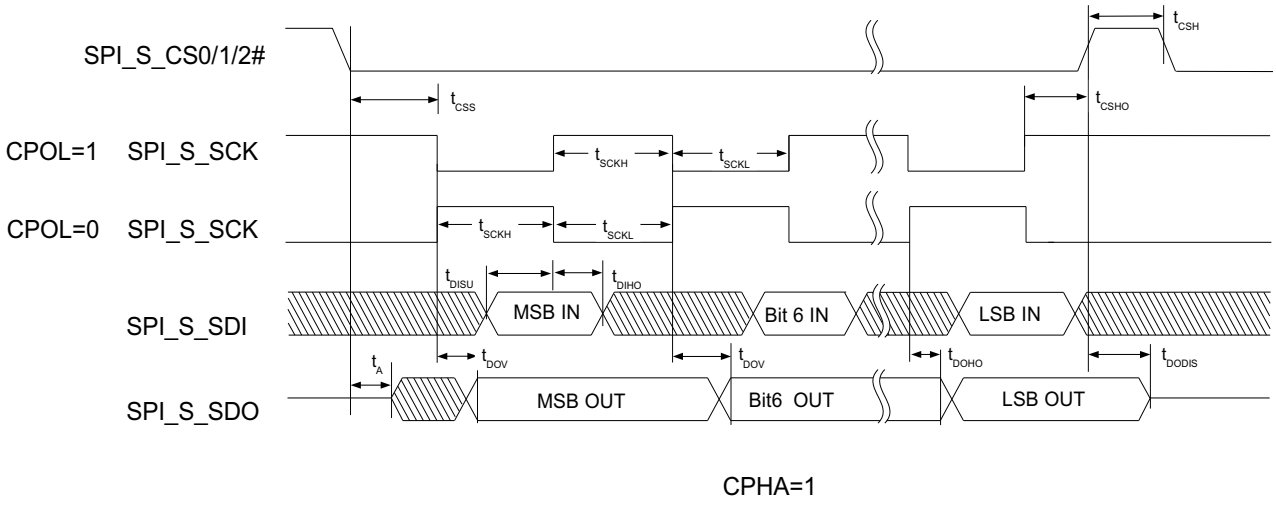


Figure 2-3: SPI Slave Timing Diagram (CPHA=1)

The SPI Slave interface can be flexible configured with the parameters cfg_spi_s_cpol, cfg_spi_s_cpha. For further informations please refer to the INAP375T user manual.

Core clock frequency for APIX1 Mode = 125MHz and for APIX2 Mode = 187.5MHz. All values specified for T_A=25°C. $t_{SCK} = 1/f_{SCK}$.

		APIX1 Mode		APIX2 Mode		
Parameter	**Description**	**Min.**	**Max.**	**Min**	**Max**	**Units**
f_{SCK}	SCK Clock Frequency	-	11	-	15	MHz
t_{SCKH}	SCK High Time	45	-	33	-	ns
t_{SCKL}	SCK Low Time	45	-	33	-	ns
t_{CSH}	CS# High Time	20	-	15	-	ns
t_{CSS}	CS# Setup Time	1/2 t_{SCK}	-	1/2 t_{SCK}	-	ns
t_{CSHO}	CS# Hold Time	50	-	34	-	ns
t_{DISU}	Data In Setup Time	16	-	12	-	ns
t_{DIHO}	Data in Hold Time	16	-	12	-	ns
t_{DOV}	Data Output Valid	-	40	-	29	ns
t_{DOHO}	Data Output Hold Time	8	-	5	-	ns
t_{DODIS}	Data Output Disable Time	-	50	-	45	ns
t_A	Data Access Time	20	-	15	-	ns

Table 2-10: SPI Slave Interface characteristics (Read Access)

		APIX1 Mode		APIX2 Mode		
Parameter	**Description**	**Min.**	**Max.**	**Min**	**Max**	**Units**
f_{SCK}	SCK Clock Frequency	-	31	-	41	MHz
t_{SCKH}	SCK High Time	1/2 t_{SCK}	-	1/2 t_{SCK}	-	ns
t_{SCKL}	SCK Low Time	1/2 t_{SCK}	-	1/2 t_{SCK}	-	ns
t_{CSH}	CS# High Time	20	-	15	-	ns
t_{CSS}	CS# Setup Time	1/2 t_{SCK}	-	1/2 t_{SCK}	-	ns
t_{CSHO}	CS# Hold Time	50	-	34	-	ns
t_{DISU}	Data In Setup Time	16	-	12	-	ns
t_{DIHO}	Data In Hold Time	16	-	12	-	ns

Table 2-11: SPI Slave Interface characteristics (Write Only Access)

2.3.4.3 I²C Interface timing

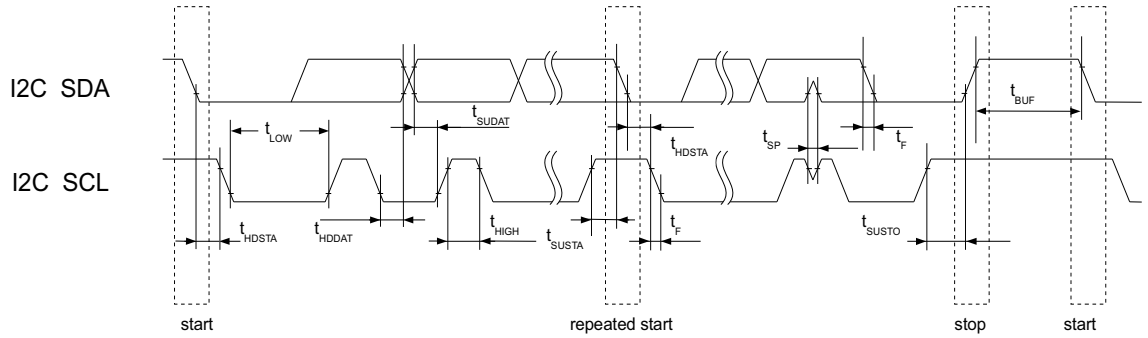


Figure 2-4: I2C Timing Diagram

The I2C timings depend on the accuracy of the external 10MHz reference clock and are therefore listed as typical values. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency Standard Mode Fast Mode	-	-	 100 400	kHz
t_{HIGH}	SCL High Time Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{LOW}	SCL Low Time Standard Mode Fast Mode	-	 6.0 1.5	-	µs
t_{HDSTA}	Hold Time (repeated) START conditon Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{HDDAT}[a]	Data Hold Time Standard Mode Fast Mode	-	 4.0 1.0	-	µs
t_{SUDAT}	Data Setup Time Standard Mode Fast Mode	-	 2.0 0.5	-	µs
t_{SUSTA}	Setup Time for repeated START conditon Standard Mode Fast Mode	-	 6.03 1.58	-	µs

Table 2-12: I2C Interface characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t_{SUSTO}	Setup Time for STOP conditon Standard Mode Fast Mode	-	 4.03 1.08	-	µs
t_{BUF}	Bus Free Time Standard Mode Fast Mode	-	 10.0 2.5	-	µs
t_f	fall time of SDA and SCL Standard Mode Fast Mode[b]	-	-	 300 300	ns
t_{SP}	pulse width of spike supression Standard Mode Fast Mode[c]	-	-	 - 50	ns

Table 2-12: I2C Interface characteristics

a. max. valid time (t_{VD}) non-applicable, since device stretches the LOW period (t_{LOW}) of the SCL signal
b. output buffers without slope control for falling edges, use series resistors to slow down falling egdes if needed
c. valid for SCL signal, no spike supression on SDA signal

2.3.4.4 RESET and Boot Strap timing

The INAP378TAQ offers several boot strap pins to define, how the device will come up and check for a configuration after boot up or hardware reset. The correct boot strap selection is necessary for proper operation of the INAP378TAQ. For more information please refer to the INAP378TAQ user manual.

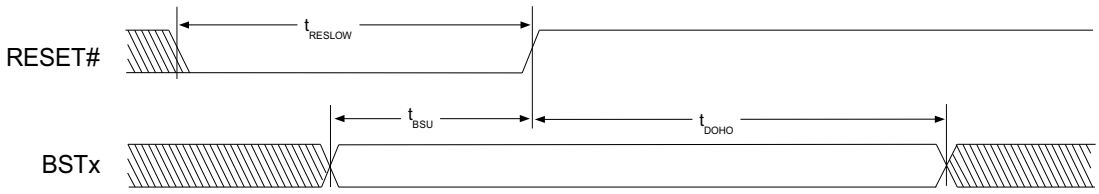


Figure 2-5: Reset and Boot Strap Timing Diagram

For a valid Reset Low Time (t_{RESLOW}) all supply voltages needs to be stable in the operating condition. At reset release (rising edge of RESET#) a stable reference clock is required. All values specified for T_A=25°C.

Parameter	Description	Min.	Typ.	Max.	Units
t_{RESLOW}	Reset Low Time	1	-	-	ms
t_{BSU}	Boot Strap In Setup Time	0	-	-	ns
t_{BHO}	Boot Strap in Hold Time	500	-	-	ns

Table 2-13: Boot Strap Reset Timing

2.3.4.5 GPIO Interface

2.3.4.5.1 GPIO Interface Downstream

The GPIO interface is only available in APIX2 mode. At transmitter side GPIO data input ports are sampled asynchronously and transmitted to configurable GPIO output ports at receiver side. Sampling frequency can be flexible configured using parameters GPIO Bandwidth (gpio_bw_dwn) and GPIO halved (gpio_bw_div). For further information please refer to the INAP378TAQ user manual. All values specified for T_A=25°C.

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Sampling Frequency.	Unit
3 GBit/s	1	high	off	26.768	MHz
3 GBit/s	1	low	off	6.696	MHz
3 GBit/s	1	high	on	13.393	MHz
3 GBit/s	1	low	on	3.348	MHz
3 GBit/s	2	high	off	13.393	MHz
3 GBit/s	2	low	off	3.348	MHz
3 GBit/s	2	high	on	6.696	MHz
3 GBit/s	2	low	on	unsupported	MHz
1.5 GBit/s	1	high	off	26.768	MHz
1.5 GBit/s	1	low	off	6.696	MHz
1.5 GBit/s	1	high	on	13.393	MHz
1.5 GBit/s	1	low	on	3.348	MHz
1.5 GBit/s	2	high	off	13.393	MHz
1.5 GBit/s	2	low	off	3.348	MHz
1.5 GBit/s	2	high	on	6.696	MHz
1.5 GBit/s	2	low	on	unsupported	MHz
1 GBit/s	1	high	off	17.857	MHz
1 GBit/s	1	low	off	4.468	MHz
1 GBit/s	1	high	on	8.929	MHz
1 GBit/s	1	low	on	2.232	MHz
1 GBit/s	2	high	off	8.929	MHz
1 GBit/s	2	low	off	2.232	MHz
1 GBit/s	2	high	on	4.464	MHz
1 GBit/s	2	low	on	1.116	MHz

Table 2-14: GPIO Interface Downstream

Downstream Bandwidth	GPIO ports	GPIO Bandwidth	GPIO halved	Sampling Frequency.	Unit
500 MBit/s	1	high	off	17.857	MHz
500 MBit/s	1	low	off	4.468	MHz
500 MBit/s	1	high	on	8.929	MHz
500 MBit/s	1	low	on	2.232	MHz
500 MBit/s	2	high	off	8.929	MHz
500 MBit/s	2	low	off	2.232	MHz
500 MBit/s	2	high	on	4.464	MHz
500 MBit/s	2	low	on	1.116	MHz

Table 2-14: GPIO Interface Downstream

2.3.4.5.2 GPIO interface upstream

Transmitter GPIO upstream interface outputs GPIO data coming from either one or two APIX2 receiver devices. Output frequency can be configured using parameter GPIO Bandwidth (gpio_bw_up). For further informations please refer to the INAP375T user manual. All values specified for T_A=25°C.

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
1	187.5 MBit/s	1	high	13.39	MHz
1	187.5 MBit/s	1	low	3.35	MHz
1	187.5 MBit/s	2	high	13.39	MHz
1	187.5 MBit/s	2	low	3.35	MHz
1	62.5 MBit/s	1	high	4.46	MHz
1	62.5 MBit/s	1	low	1.12	MHz
1	62.5 MBit/s	2	high	4.46	MHz
1	62.5 MBit/s	2	low	1.12	MHz
2	187.5 MBit/s	1	high	6.69	MHz
2	187.5 MBit/s	1	low	3.35	MHz
2	187.5 MBit/s	2	high	6.96	MHz
2	187.5 MBit/s	2	low	3.35	MHz
2	62.5 MBit/s	1	high	2.23	MHz

Table 2-15: GPIO Interface Upstream

Number of Rx	Upstream Bandwidth	GPIO ports	GPIO Bandwidth	Maximum Output frequency	Unit
2	62.5 MBit/s	1	low	1.12	MHz
2	62.5 MBit/s	2	high	2.23	MHz
2	62.5 MBit/s	2	low	1.12	MHz

Table 2-15: GPIO Interface Upstream

2.3.4.6 Sideband Interface

2.3.4.6.1 Sideband Interface Downstream

The Sideband interface is only available in APIX1 mode. At transmitter side sideband data input ports are sampled asynchronously and transmitted to the corresponding output ports at receiver side. All values specified for T_A=25°C.

Downstream Bandwidth	Sampling frequency	Units
1 GBits/s	13.89	MHz
500 MBits/s	6.94	MHz

Table 2-16: Sideband Interface Downstream

2.3.4.6.2 Sideband Interface Upstream

Transmitter Sideband interface outputs sideband data coming from receiver side. All values specified for T_A=25°C.

Upstream Bandwidth	Maximum output frequency	Units
62.5 MBits/s	10.41	MHz
31.25 MBits/s	5.21	MHz

Table 2-17: Sideband Interface Upstream

2.3.4.7 I²S Audio Interface

f_{BCK} = 1 / t_{PERIOD}. All values specified for T_A=25°C.

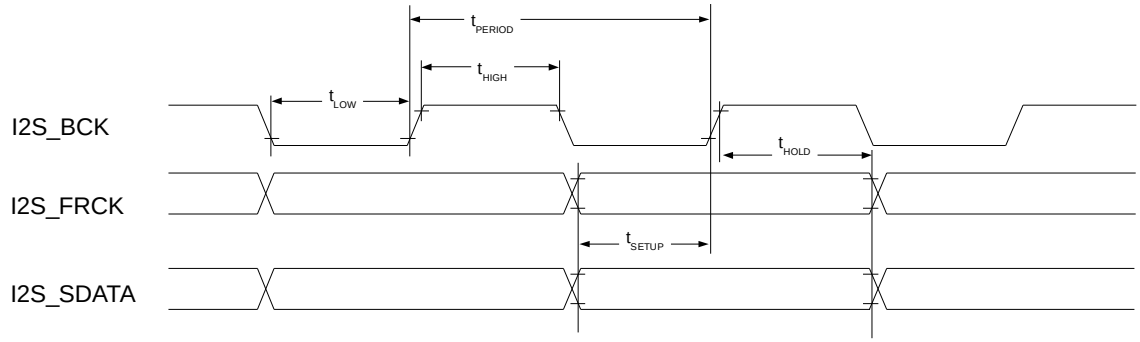


Figure 2-6: I2S Audio Interface Timing Diagram

Parameter	Description	Min	Max	Units
f_{BCK}	I2S_BCK frequency	0.75	26.78	MHz
t_{HIGH}	I2S_BCK high time	7	-	ns
t_{LOW}	I2S_BCK low time	7	-	ns
t_{SETUP}	Setup time	2	-	ns
t_{HOLD}	Hold time	7	-	ns

Table 2-18: I2S Audio Interface Timing

2.3.4.8 MCLK clock output

The granularity of the frequency output of MCLK is definded by pulse width. For further informations please refer to the INAP378TAQ user manual. All values specified for T_A=25°C.

Parameter	Description	Min	Max	Units
f_{MCLK_OUT}	MCLK output frequency	2.953	187.5	MHz

Table 2-19: MCLK output frequency range

2.3.5 Reference Clock

The INAP378TAQ requires an external clock source like a crystal or oscillator, acting as reference for the internal PLL.

Parameter	Description	Min.	Typ.	Max.	Unit
f_{ref_osc}	Nominal Reference Frequency	-	10	-	MHZ
F_{TOL}	Frequency Tolerance	-100	-	+100	ppm
ESR_{XTAL}	Equivalent Series Resistance	-	-	80	Ohm
	Drive Level	see Table 2-21			

Table 2-20: Reference clock requirements

The INAP378TAQ core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal. Alternatively a stable 10 MHz clock signal (3.3V CMOS TTL) can be directly connected to XTAL_IN with XTAL_OUT left open. Figure 2-7 shows a typical crystal design required for the oscillator circuit. The values for C1, C2 and R1 need to be selected to match the oscillation requirements of the crystal Q1.

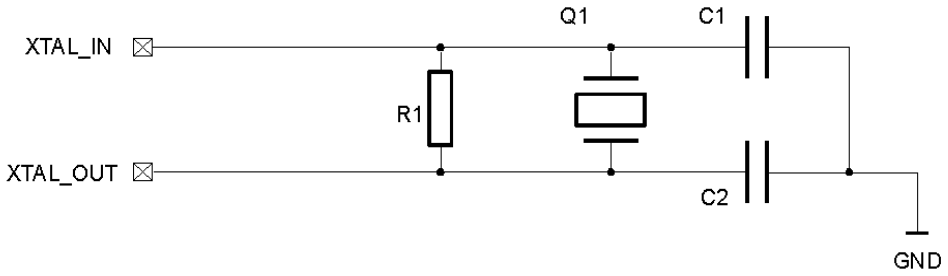


Figure 2-7: Crystal clock schematic example

For resonance at the correct frequency, the crystal needs to be loaded with its specified load capacitance C_L, which is the value of capacitance used in conjunction with the oscillation unit. The INAP378TAQ oscillator provides some of the load with internal capacitance which is specified within the range of 10pF to 12.5pF. The remainder is generated by the external capacitors and tuning capacitors labeled C1 and C2.

The load capacitance CL can be calculated from CL = Cint + C1//C2. E.g. selecting C1 and C2 with 15pF, CL can be calculated to CL = 12.5pF + 7.5pF = 20pF.

The crystal needs to be able to withstand the power dissipation, produced by the INAP378TAQ. The power dissipation depends on the ESR of the crystal and is reflected by the maximum drive level of the crystal. Table 2-21 illustrates the power dissipation of the INAP378TAQ and therefore the minimum drive level capabilities of the crystal at different crystal ESR levels.

Crystal ESR	INAP378TAQ Power dissipation / Minimum crystal drive level	Unit
30	77	µW
50	121	µW
80	179	µW

Table 2-21: Minimum Drive level

2.3.6 Power Up Sequencing

To avoid high IO currents, 1.8V supply voltages have to ramp before 3.3V supply on power-up. On power-down, 3.3V supply have to be powered down before 1.8V. On power-up all supply voltages have to rise steadily from GND level up to the VCC_{MIN} level without turn to negative direction. The ramping times must be within the limits as specified in Table 2-22. All 1.8V supplies have to be ramped up simultaneously starting from GND according Figure 1-13. Reset has to be held low until all supplies reached recommended operating conditions.

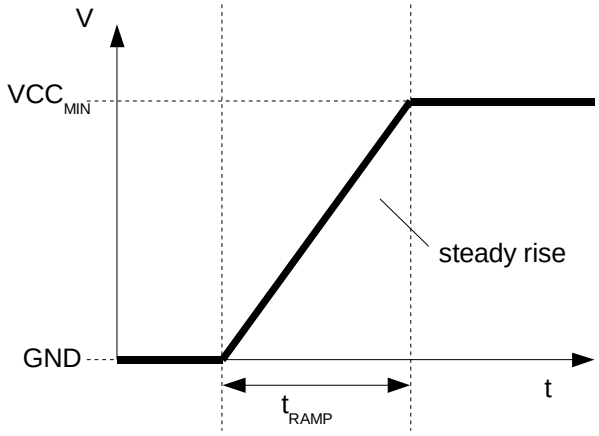


Figure 2-8: Steady voltage ramp-up

The INAP378TAQ tolerates the supplies to be ramped simultaneously. To avoid high IO currents, 1.8V supplies should ramp before 3.3V on power-up. On power-down, 3.3V should be powered down before 1.8V. The ramping times must be within the limits as specified in Table 2-22.

Supply	Ramp-Up time	
	Min	Max
All supplies	50µs	10ms

Table 2-22: Power supply ramping requirements

2.4 Typical Operating Characteristics

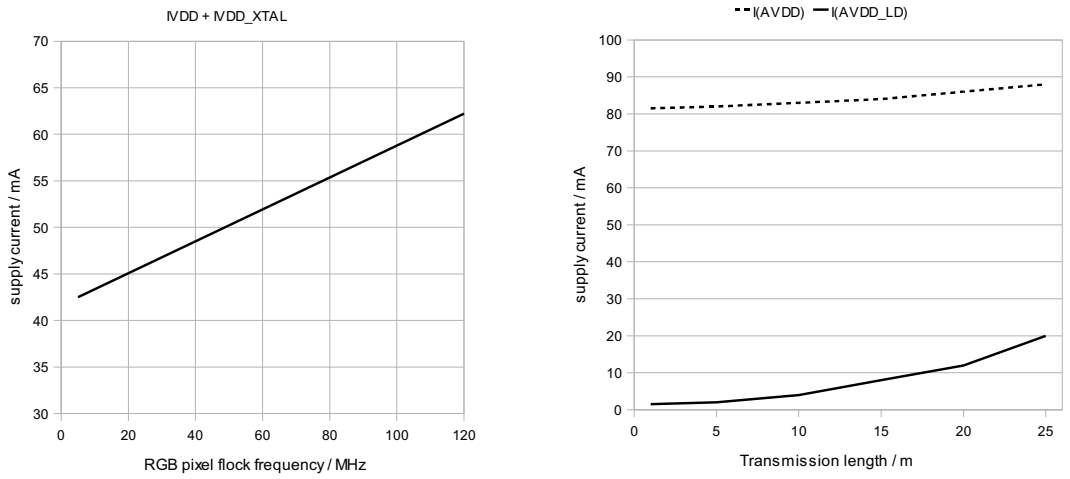


Figure 2-9: typical supply current characteristics (1.5GBit/s)

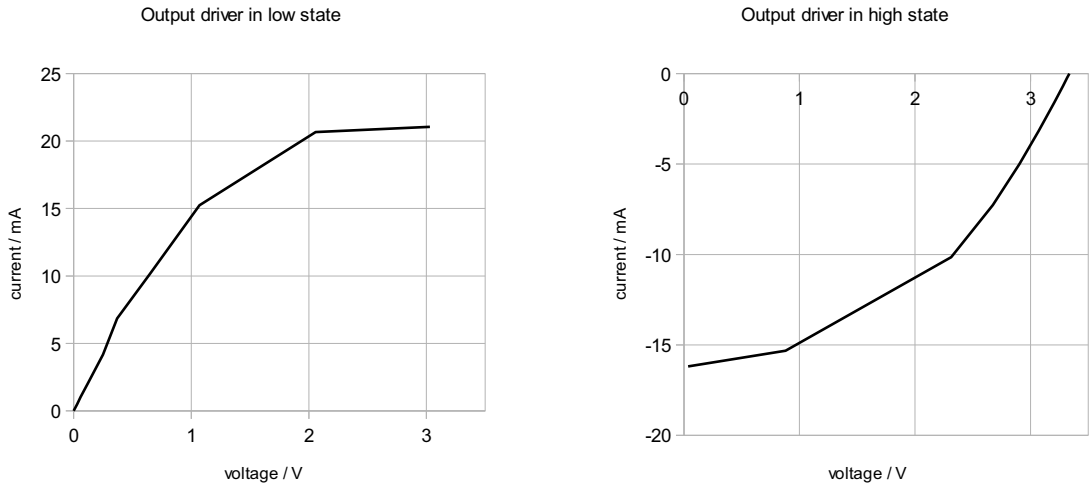


Figure 2-10: Typical device I-V curve for 3.3V data interface IO under nominal condictions

3.0 Pin Description

Signal Name	Pin #	Type	Description
PX[19:1] [a]	C1,D4,B2,A1, T3,K1,K2,M1, P1,L1,L2,J2, J1,R6,T5,R5, T6,T7,N8	I	Video Interface pins
BST5	R9	I/O [b]	BST5: Boot strap option 5 input
BST2	T10	I/O [b]	BST2: Boot strap option 2 input
SPI_S_SDO/ BST3	T11	I/O [b]	SPI_S_SDO: SPI Slave Data Output BST3: Boot strap option 3 input
SPI_S_SDI	N10	I [c]	SPI Slave Data Input
SPI_S_SCK	R11	I [c]	SPI Slave Serial Clock Input
SPI_S_STALL/ BST4	T12	I/O [b]	SPI_S_STALL: High: SPI Slave not ready or buffer full Low: SPI Slave ready to receive data BST4: Boot strap option 4 input
SPI_S_CS0#/ SBDWN_DATA0	T14	I [c]	SPI_S_CS0#: SPI Slave Chip-select 0 Input (Data channel 0) SBDWN_DATA0: APIX1 Downstream data input 0
SPI_S_CS1#/ SBDWN_DATA1	P16	I [c]	SPI_S_CS0#: SPI Slave Chip-select 1 input (Data channel 1) SBDWN_DATA1: APIX1 Downstream data input 1
SPI_S_CS2#	M15	I [c]	SPI Slave Chip-select 2 input (Configuration)
SPI_S_MB0/ SBUP_DATA0/ BST1	M16	I/O [b]	SPI_S_MB0: SPI Slave mailbox 0 output SBUP_DATA0: APIX1 Upstream data output 0 BST1: Boot strap option 1 input
SPI_S_MB1/ SBUP_DATA1/ BST6	L13	I/O [b]	SPI_S_MB1: SPI slave mailbox 1 output SBUP_DATA1: APIX1 Upstream data output 1 BST6: Boot strap option 6 input
I²C_SCL	L15	I/O [d]	I²C_SCL: I²C Clock output
I²C_SD	L16	I/O [b]	I²C_SD: I²C Data pin
SD_UP_IN_P	K16	I [e]	Serial Link, Upstream Serial Link Input from RX
SD_UP_IN_N	J13	I [e]	Serial Link, Upstream Serial Link Input from RX
SD_DWN_OUT_N	G15	O [e]	Serial Link, Downstream Serial Link output to RX
SD_DWN_OUT_P	F16	O [e]	Serial Link, Downstream Serial Link output to RX
XTAL_IN	B12	I	10MHz Oscillator input

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
XTAL_OUT	A12	O	10MHz Oscillator output
I2S_MCLK	A9	I/O	I2S Interface, Master Clock input/output
I2S_SDATA	A10	I [c]	I2S Interface, Data input
I2S_FRCK	A11	I [c]	I2S Interface, Frame clock input
I2S_BCK	B10	I [c]	I2S Interface, Bit clock input
GPIO1/SBDWN_CLK	B8	I/O	GPIO1: General purpose I/O SBDWN_CLK: Sampling clock output for SBDWN_DATA[1:0] (APIX1 Mode) DEBUG Interface : Debug Output Pin1
GPIO0/SBUP_CLK	A8	I/O	GPIO0: General purpose I/O SBUP_CLK: Sampling clock output for SBUP_DATA[1:0] (APIX1 Mode) DEBUG Interface : Debug Output Pin0
STATUS	A7	O	STATUS: Device status output
RESET#	D7	I [f]	Reset
DVDD	F1,T1,A3,F2, M2,B5,R7,N7, R12	Power	Digital I/O power supply
AVDD_LVDS_PLL	G2	Power	LVDS PLL power supply
VDD	H2,R10,K15, D9	Power	Core supply
AVDD_LVDS	R8,B6,A6	Power	LVDS I/O power supply
AVDD_LD	E15,F15,E16	Power	Serial Link I/O Power supply
AVDD	H13,A14,C16	Power	Serial Link core power supply
AVDD_VCO	H15	Power	Serial Link VCO Power supply
VDD_XTAL	B11	Power	10MHz Oscillator core supply
DVDD_XTAL	D10	Power	10MHz Oscillator digital supply
GND_XTAL	*D11*	GND	10MHz Oscillator Ground

Table 3-1: Pin description

Signal Name	Pin #	Type	Description
GND	E2,E1,G1,H1, R2,N4,T8,N9, N11,F13,G16, H16,J16,J15, K13,D6,A5, B9	GND	Ground
Exposed PAD (EP)	-	GND	must be connected to GND-plane
TEST	B7	I [c]	reserved, pull down external over 100kOhm to GND

Table 3-1: Pin description

a. 100Ohm termination between n and p lines required in case pins are used as LVDS. See INAP378T user manual for further information on the videe interface
b. boot strap pins are sampled on hardware reset and need to be pulled to a defined value. See INAP378T user manual for the functional description.
c. with internal pull-down
d. n-channel open drain
e. CML interface
f. schmitt trigger input

3.1 Reset

The pin RESET# triggers an asynchronous reset (active low) and can be activated any time. This reset erases all configuration settings. Please see Table 3-2 for the status of all pins during reset.

Signal Name	Pin #	Reset State	Functional State
PX[19:1]	C1,D4,B2,A1,T3,K1,K2,M1,P1,L1, L2,J2, J1,R6,T5,R5,T6,T7,N8	Input	Input
BST5	R9	Input	Output
BST2	T10	Input	Output
SPI_S_SDO/BST3	T11	Input	Output
SPI_S_SDI	N10	Input	Input
SPI_S_SCK	R11	Input	Input
SPI_S_STALL/ BST4	T12	Input	Output
SPI_S_CS0#/ SBDWN_DATA0	T14	Input	Input
SPI_S_CS1#/ SBDWN_DATA1	P16	Input	Input
SPI_S_CS2#	M15	Input	Input

Table 3-2: Reset States

Signal Name	Pin #	Reset State	Functional State
SPI_S_MB0/ SBUP_DATA0/ BST1	M16	Input	Output
SPI_S_MB1/ SBUP_DATA1/ BST6	L13	Input	Output
I²C_SCL	L15	Tri-State	Tri-State / Output
I²C_SD	L16	Tri-State	Tri-State / Input / Output
I2S_MCLK	A9	Tri-State	Tri-State / Input / Output
I2S_FRCK	A11	Input	Input
I2S_SDATA	A10	Input	Input
I2S_BCK	B10	Input	Input
GPIO1/SBDWN_CLK	B8	Input	Input / Output
GPIO0/SBUP_CLK	A8	Input	Input / Output
STATUS	A7	Output	Output

Table 3-2: Reset States

4.0 Package Information

4.1 Pinout Diagram

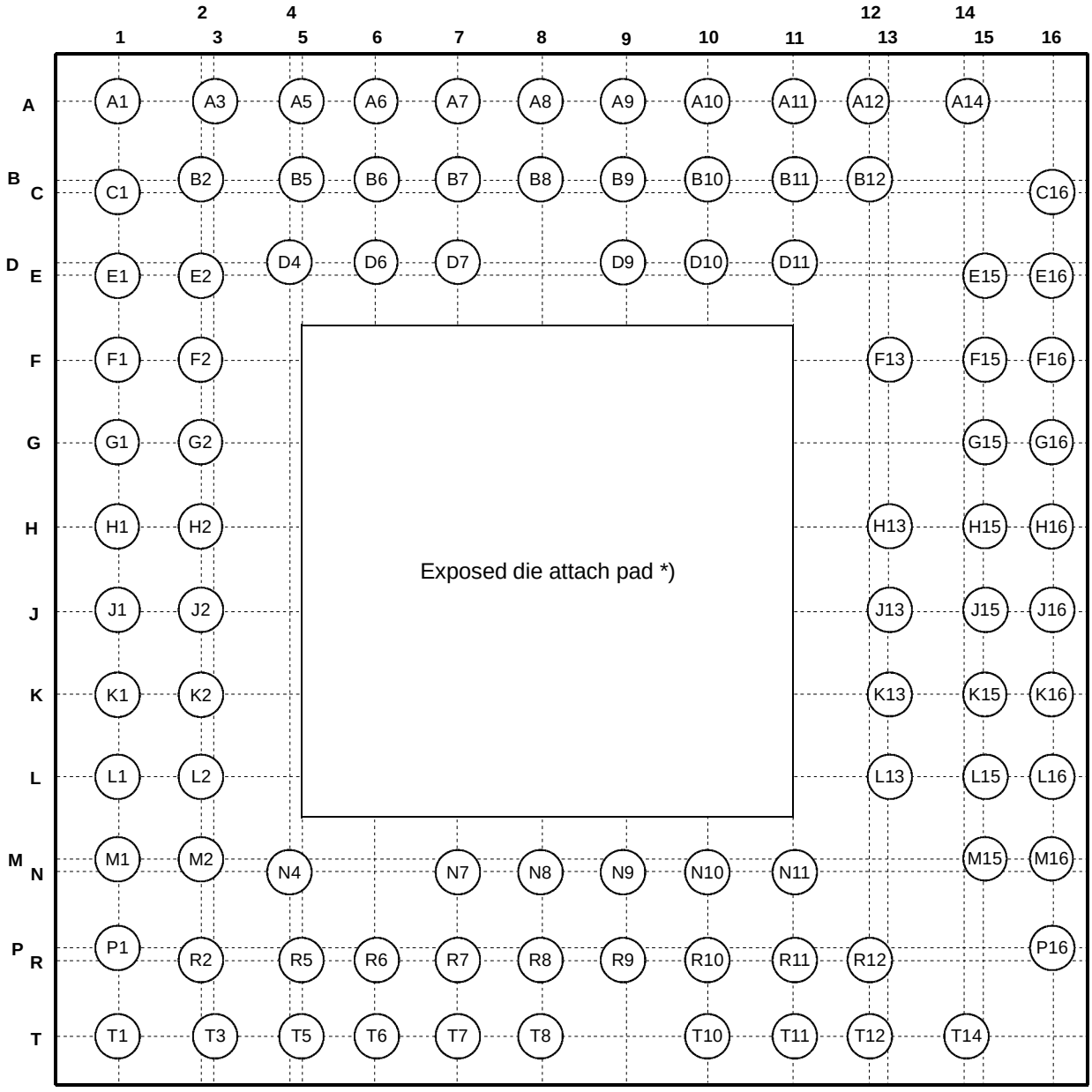


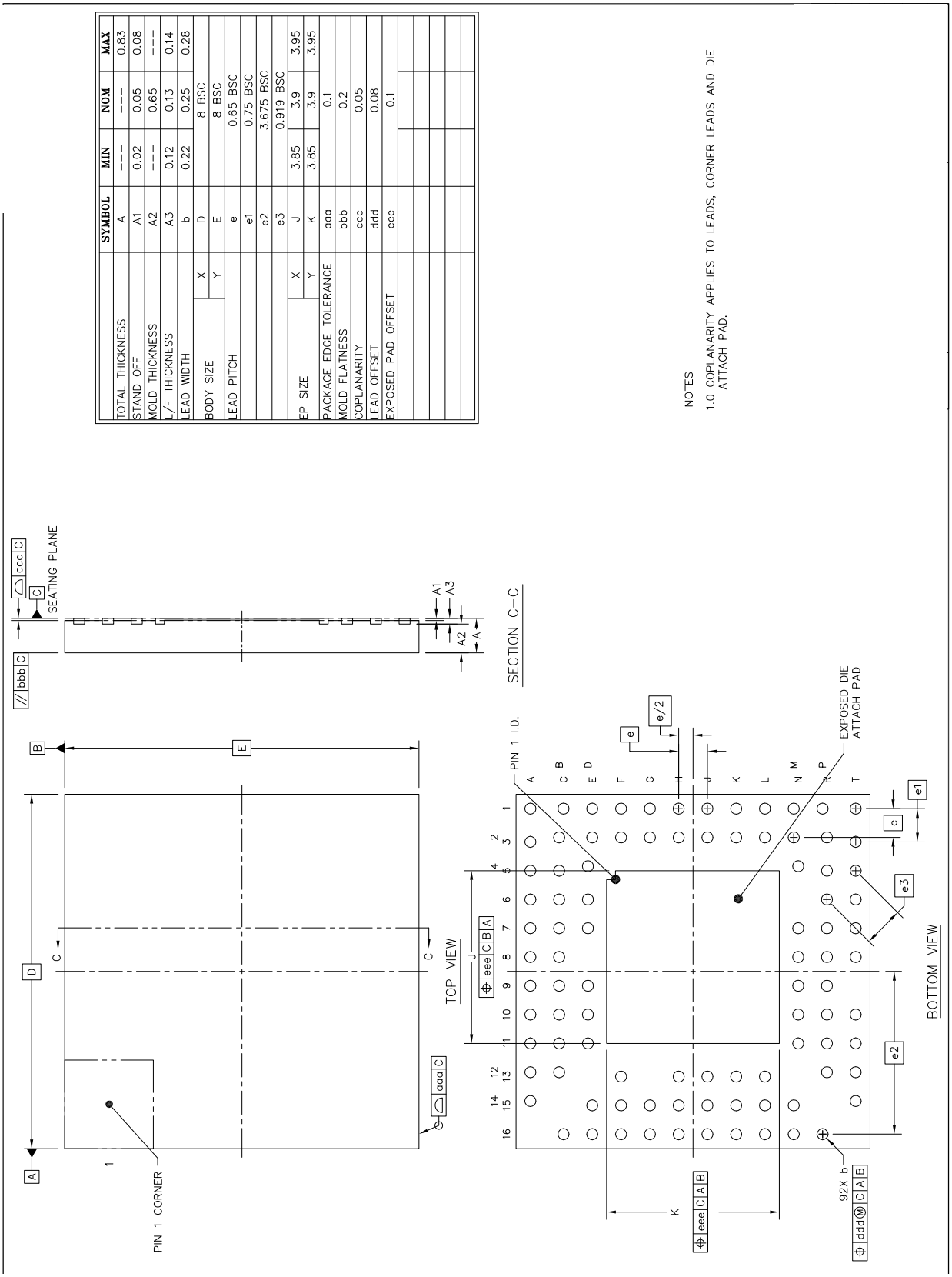
Figure 4-1: Pinout diagram, Top View, 92pin aQFN

* Exposed PAD connect to GND-plane

4.2 Package Dimensions

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.83
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.12	0.13	0.14
LEAD WIDTH		b	0.22	0.25	0.28
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.65 BSC	
		e1		0.75 BSC	
		e2		3.675 BSC	
		e3		0.919 BSC	
EP SIZE	X	J	3.85	3.9	3.95
	Y	K	3.85	3.9	3.95
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.2	
COPLANARITY		ccc		0.05	
LEAD OFFSET		ddd		0.08	
EXPOSED PAD OFFSET		eee		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.



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