80C186EB/80C188EB AND 80L186EB/80L188EB EMBEDDED MICROPROCESSORS SPECIFICATION UPDATE

Release Date: April, 1997
Order Number: 272897-002

The 80C186EB/80C188EB and 80L186EB/80L188EB embedded microprocessors may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Such errata are not covered by Intel's warranty. Current characterized errata are available on request.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-7641

or call 1-800-879-4683
or visit Intel's website at http:\\www.intel.com

CONTENTS

REVISION HISTORY

Rev. Date	Version	Description
04/01/97	002	Changed stepping information for item 9 in Errata Table.
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
80C186EB/80C188EB Microprocessor User's Manual	270830-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80x186EB/80x188EB microprocessor product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	B0	B1			
1	x	x	x	8	NoFix	INTx/INTAx
2	x	x	x	15	NoFix	Powerdown Mode on the 80C18xEB
3	x	x	x	15	NoFix	NMI Entering Powerdown Mode on 80C18x EA/EB/EC
4	x			18	Fixed	ONCE Mode
5	x			19	Fixed	RESIN# Hysterisis
6	x			19	Fixed	SINT1
7	x			19	Fixed	INTA# Bus Cycles
8	x			20	Fixed	Clock Unit
9	x	x		20	Fixed	Ipd not fully operational

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	003			Changes to the *80C186EB/80C188EB Microprocessor User's Manual*

IDENTIFICATION INFORMATION

Markings

80x186EB/80x188EB microprocessors may be identified electrically according to device type and stepping. Refer to the data sheet for instructions on how to obtain the identifier number.

A-step

A-step production devices can be identified in two ways:

1. The product is marked with a 9-character alphanumeric Intel FPO number underneath the product code number. For A-step EB devices, the ninth character is “A”, or it may be absent (i.e., no ninth character). Refer to the datasheet for the exact location of the FPO number.
2. There is a STEPID register which may be examined through software. For A-step devices, the register contains a value of 01H.

B-step

There are two B-step devices:

- B0-Step Silicon with two functional anomalies
- B1-Step Silicon with one functional anomaly

A B0-Step device can be identified as follows:

1. The product is marked with a 9-character alphanumeric Intel FPO number underneath the product code number.

   For B0-Step devices, the ninth character is “B”. Refer to the data sheet to determine the exact location of the FPO number.

A B1-Step device can be identified as follows:

2. The product is marked with a 9-character alphanumeric Intel FPO number underneath the product code number.

   For B0-Step devices, the ninth character is “C”. Refer to the data sheet to determine the exact location of the FPO number.

Both B-step devices have a STEPID register which may be examined through software. The STEPID register can help differentiate an A-step device (STEPID=01H) from a B-step device (STEPID=02H). However, the STEPID cannot be used to differentiate between B0-Step and B1-step devices since both contain the same value.

ERRATA

1. INTx/INTAx

PROBLEM: An internal problem with the Interrupt Control Unit is cascade mode can cause no acknowledge cycle on the INTA1# line after an interrupt on INT1 or on INTA0# after an interrupt on INT0.

There are two cases. Problem 1: Interrupt 1 is configured in cascaded mode and a higher priority interrupt exists. Problem 2: Interrupt 0 is configured in cascaded mode and interrupt 1 is higher priority.

Problem 1:

An interrupt acknowledge for INT1 is not generated on INTA1#. If two interrupts are in cascade mode, the interrupt acknowledge is generated on INTA0#

Condition:

Another interrupt of higher priority occurs after the decision is made to service Interrupt 1 but before the expected acknowledge cycle on INTA1#.

Configuration:

1. Master Mode
2. INT1 is in Cascade mode and enabled.
3. An Interrupt of higher priority than INT1 is enabled (DMA, Timers, INT lines, Serial, etc.).

Problem 2:

An interrupt acknowledge for INT0 is not generated on INTA0#. If two interrupts are in cascade mode, the interrupt acknowledge is generated on INTA1#.

Condition:

Interrupt 1, configured as higher priority than interrupt 0, occurs after the decision is made to service Interrupt 0 but before the expected acknowledge cycle on INTA0#.

Configuration:

1. Master Mode
2. INT0 is in Cascade mode and enabled.
3. INT1 is enabled and higher priority than INT0.

Problem 1 Description

Note: In the cases below, the interrupt controller has already decided to service the INT1 interrupt before the higher priority interrupt occurs.

Correct operation of the device acknowledges the interrupt on INTA1# after an interrupt on INT1. Normally, this occurs even if there is a higher priority interrupt after INT1 but before the acknowledge (Figure 1).

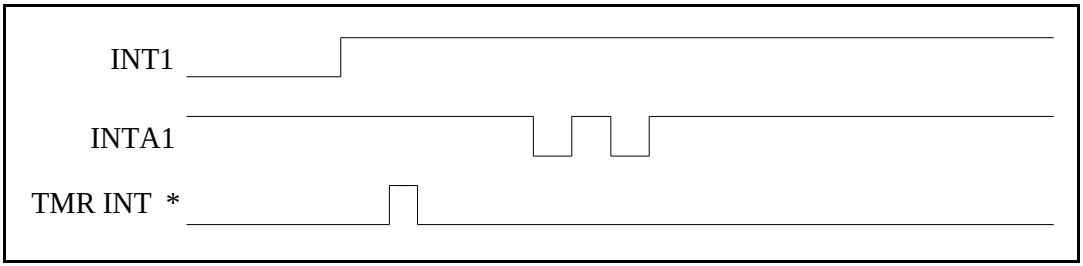

Figure 1. Correct INT1 Acknowledge Sequence with Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, INT0, or INT2.

The errata occurs when a higher priority interrupt occurs between INT1 and its expected acknowledge. The processor completes internal interrupt acknowledge cycles as seen on the status lines but no acknowledge cycle is sent on the INTA1# output (Figure 2).

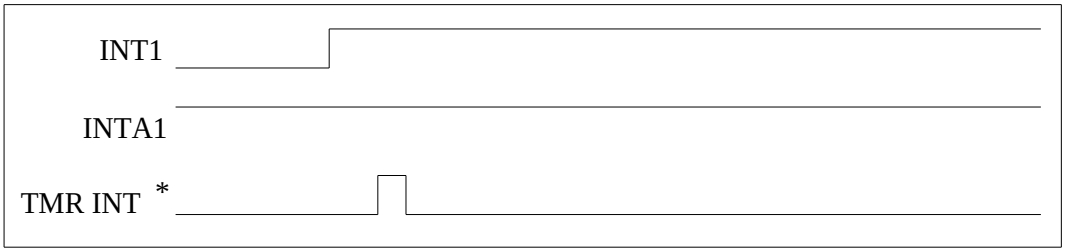

Figure 2. Incorrect INT1 Acknowledge Sequence with Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, INT0, or INT2.

If INT0 and INT1 are configured in cascade mode and a higher priority interrupt occurs between INT1 and its expected acknowledge, then the acknowledge will appear on INTA0# instead (Figure 3).

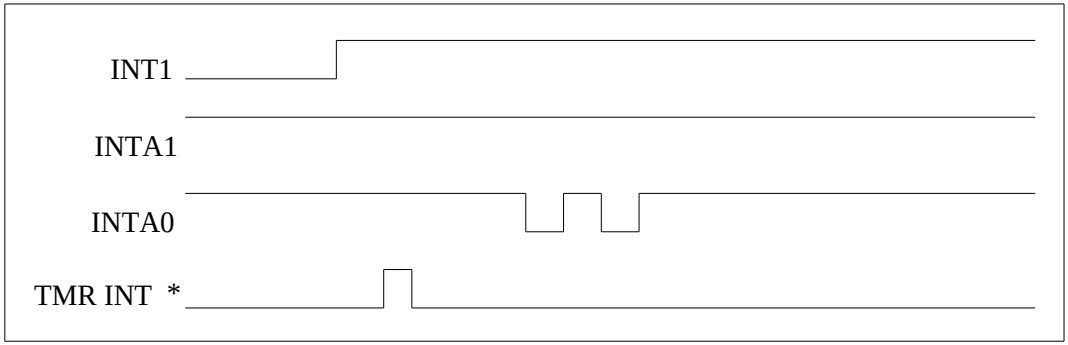

Figure 3. INT0 And INT1 Acknowledge Failure due to Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, or INT0.

Problem 2 Description

Note: In the cases below, the interrupt controller has already decided to service the INT0 interrupt before the higher priority INT1 occurs.

Correct operation acknowledges INT0 on INTA0#. Normally, this occurs even if there is a higher priority INT1 after INT0 but before the acknowledge (Figure 4).

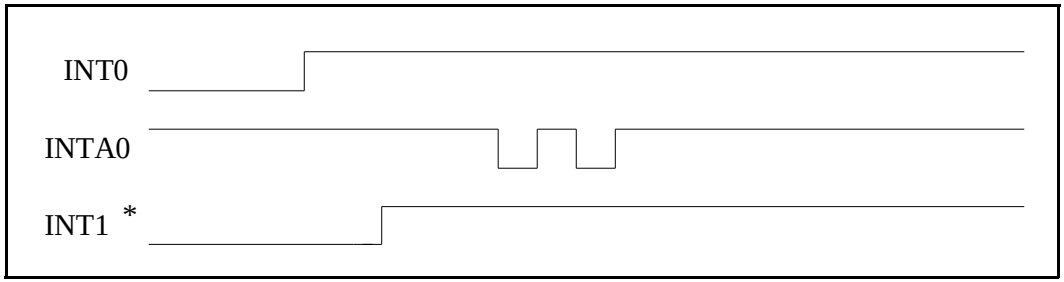

Figure 4. Correct INT0 Acknowledge Operation with a Simultaneous INT1

*Note: INT1 is the only interrupt that causes the errata to occur.

The errata occurs when INT1, which is higher priority than INT0, occurs between INT0 and its expected acknowledge. The processor completes internal interrupt acknowledge cycles as seen on the status lines but no acknowledge cycle is sent on the INTA0# output (Figure 5).

Figure 5. Incorrect INT0 Acknowledge Operation with a Simultaneous INT1

*Note: This problem occurs only if INT1 is higher priority than INT0.

If INT0 and INT1 are configured in cascade mode and the higher priority INT1 occurs between INT0 and its expected acknowledge, then the acknowledge will appear on INTA1# instead of INTA0# (Figure 6).

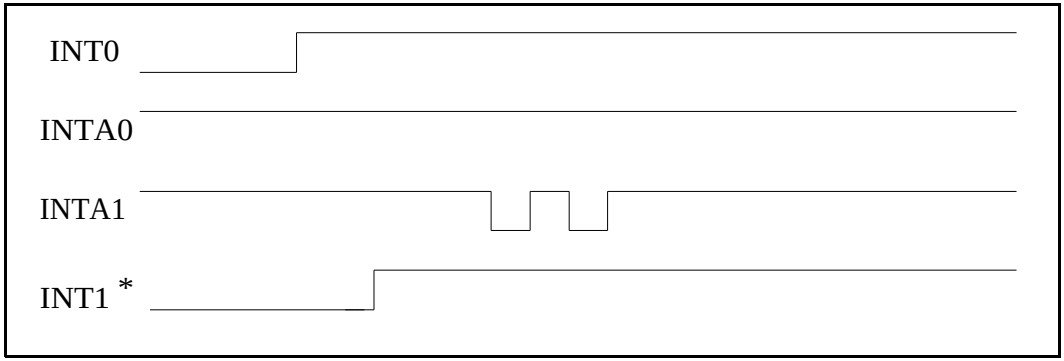

Figure 6. INT0 and INT1 Acknowledge Failure Due to the Higher Priority INT1

*Note: This problem occurs only if INT1 is higher priority than INT0.

IMPLICATION: If two cascaded interrupt controllers are used, the interrupt acknowledge can be sent to the wrong controller. This can cause no acknowledge cycle on the INTA1# line after an interrupt on INT1 or on INTA0# after an interrupt on INT0.

In a system with a single external interrupt controller, the errata will cause no acknowledge to be sent on the INTA# output. Internally, the device still functions normally, only the state of the output pin is incorrect. The Interrupt Request Register and Interrupt Service Register will operate normally.

The 186 will still run two back-to back interrupt acknowledge cycles. If the external interrupt controller does not receive the two interrupt acknowledge pulses, it will never drive the interrupt type onto the data bus. Therefore, the 186 will read an invalid interrupt type.

Software Workaround:

	CONDITION	WORKAROUND
1.	Only INT1 is configured in cascade mode and is lower priority than at least one other interrupt.	Use only INT0 in cascade mode instead, or make INT1 the highest priority interrupt, or use hardware workaround.
2.	INT1 and INT0 are both in cascade mode.	Use only one interrupt in cascade mode, or use hardware workaround.
3.	Only INT0 is configured in cascade mode and is lower priority than INT1.	Make INT0 higher priority than INT1, or use hardware workaround.

Table 1. Software Workarounds for Problem 1

Master Mode	Cascade Mode	INT1 Priority vs. any other interrupt	INTA1 Problem	INTA0 Problem	Workaround
Yes	INT0 and INT1	N/A	Yes	Yes	Use only one interrupt line in cascade mode or H/W workaround
Yes	INT1 only	Lower	Yes	No	Change to INT0 or make INT1 highest priority
Yes	INT1 only	Higher	No	No	N/A
Yes	INT0 only	N/A	No	Yes	See Table 2
No	N/A	N/A	No	No	N/A

Table 2. Software Workarounds for Problem 2

Master Mode	Cascade Mode	INT0 Priority vs. any INT1	INTA0 Problem	INTA1 Problem	Workaround
Yes	INT0 and INT1	N/A	Yes	Yes	Use only one interrupt line in cascade mode or H/W workaround
Yes	INT0 only	Lower	Yes	No	Make INT0 highest priority
Yes	INT0 only	Higher	No	No	N/A
Yes	INT1 only	N/A	No	Yes	See Table 1
No	N/A	N/A	No	No	N/A

Hardware Workaround

1. Pull data bus lines 0 to 7 to a known value (using pull-up resistors) to force a defined value on the bus when the errata occurs.

   These resistors will pull the floated bus to 0FFH during the 186 interrupt acknowledge cycle. A type 255 interrupt will be read from the bus and executed. An interrupt service routine for a type 255 interrupt should be included in the software. This solution allows a graceful recovery from the errata condition. If the current design uses interrupt type 255, the resistors can be selectively connected to V_{CC} or Ground to define an unused interrupt type.
2. Program cascaded interrupt inputs on the 186 to be level sensitive; otherwise, the 186 does not recognize that the interrupt is still active.
3. Write a simple service routine for the interrupt type defined in step 1.

   Now that the system has recovered from the errata, the original interrupts must be serviced. The higher priority interrupt will execute next. Finally the interrupt request from the external interrupt controller must be serviced.
4. Write a simple service routine for an 8259 interrupt 7 (only for cases with two external interrupt controllers).

   In systems with two external interrupt controllers. When the errata occurs because of a higher priority internal interrupt, the wrong INTA# signal will become active. If an 8259 receives an acknowledge and no interrupt is present, it assumes a spurious interrupt occurred and issues an interrupt 7. The service routine for this interrupt must be included in the software.
5. Issue non-specific End of Interrupt commands in INT0 and INT1 service routines (only for cases with two external interrupt controllers).

   The situation where the interaction between INT0 and INT1 causes the errata is a special case. This situation will occur as just described, the INTA# pulse will be issued to the wrong 8259. In this situation, the interrupt input to the wrong 8259 is active when the acknowledge occurs. The acknowledged 8259 will drive its interrupt type onto the bus, and the CPU will service that interrupt. The only difficulty is what happens internally to the 186. The incorrect Interrupt Request and Service Bits have been set. To recover from this, the interrupt service routine must issue a non-specific End of Interrupt command. At this point, the wrong interrupt has been serviced correctly and because the interrupt inputs are configured to be level sensitive, the initial interrupt is now serviced.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

2. Powerdown Mode on the 80C18xEB

PROBLEM: When entering Powerdown or Idle modes on the 80C18xEB, the address/data pins AD015:0 float instead of being driven to zero. This is unlike the 80C186EA/XL/EC where the AD015:0 are driven to zero.

IMPLICATION: Operation is different from that of the 80C186EA/XL/EC.

WORKAROUND: Powerdown Mode Functionality

Powerdown mode on the 186 processors causes the clock input to the CPU and peripherals to be disabled. To enter Powerdown mode, two things must happen. First, the PWRDN bit in the PWRCON Register must be set. Second, the HLT instruction must be executed. During the HLT instruction, the clock signal to the CPU and integrated peripherals stop (at a logic low level) at the end of the T2 bus state. The CLKOUT signal stops (at a logic high level) at the end of the T3 bus state. To exit Powerdown, an NMI or processor reset must occur.

Idle Mode Functionality - Idle mode on the 186 processors causes the clock input to the CPU to be disabled. To enter Idle mode, two things must happen. First, the PWRDN bit in the PWRCON Register must be set. Second, the HLT instruction must be executed. During the HLT instruction, the clock signal to the CPU stop (at a logic low level) at the end of the T2 bus state. Any unmasked interrupt or NMI will return the processor to Active mode.

AD15:0 During HLT Execution - When executing the HLT instruction after enabling the Powerdown or Idle mode, the 80C18xEB will float its address/data pins AD15:0. The 80C186EA/XL/EC, on the other hand will drive AD15:0 to a logic zero. Users who have a need to drive AD15:0 to a logic zero on the 80C18xEB can use 50 KΩ pulldown resistors.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

3. NMI Entering Powerdown Mode on 80C18x EA/EB/EC

PROBLEM: If an NMI can be received during execution of the HLT instruction when entering Powerdown mode, certain considerations must be made.

IMPLICATION: If an NMI occurs during execution of the HLT instruction when entering Powerdown mode, the processor may to enter Powerdown or may not service the NMI. To avoid this, the NMI pulse width must be extended to allow recognition.

WORKAROUND:

NMI Functionality - NMI is the highest priority interrupt. It cannot be masked by software. To be recognized, NMI must be active for a minimum of one CLKOUT period and meet

required setup and hold times (for recognition at a specific clock edge). If these requirements are met, NMI servicing begins at the next valid instruction boundary.

Powerdown Mode Functionality - Powerdown mode on the 186 processors causes the clock input to the CPU and peripherals to be disabled. To enter Powerdown mode, two things must happen. First, the PWRDN bit in the PWRCON Register must be set. Second, the HLT instruction must be executed. During the HLT instruction, the clock signal to the CPU and integrated peripherals stop (at a logic low level) at the end of the T2 bus state. The CLKOUT signal stops (at a logic high level) at the end of the T3 bus state. To exit Powerdown, an NMI or processor reset must occur.

NMI During HLT Execution - If an NMI occurs before the HLT instruction executes, everything functions properly. The NMI is recognized at the instruction boundary preceding the HLT instruction, the NMI is serviced and the processor then enters powerdown mode.

The problem occurs when an NMI occurs during execution of the HLT instruction. NMI is only serviced at valid instruction boundaries. The HLT instruction, when entering Powerdown, does not really have a boundary, it extends until Powerdown is exited. If NMI occurs between the beginning the T1 bus state and the end of the T2 state, but does not extend into T3, it will not be recognized, and the processor will enter Powerdown mode. The processor does not recognize the NMI request during the HLT instruction until the internal clock has stopped (at the end of T2).

For the NMI to be recognized during the execution of the HLT instruction, the pulse must extend into T3. At this point, the processor has entered Powerdown and synchronized the NMI pulse. The NMI will be processed, but the processor will never enter Powerdown. Essentially, because NMI is active, the processor exits Powerdown as soon as it enters.

In a typical system design using Powerdown mode, NMI can only occur after Powerdown is entered and the clock is stopped. The simplest solution to the problem is to not assert NMI unless the processor has entered Powerdown Mode.

If the system requires periodic NMI pulses, then the NMI pulse width must be long enough to ensure that it will extend into the T3 state of the HLT instruction. A NMI pulse width of three CLKOUT periods guarantees this.

The figures below show NMI occurring at different times during execution of the HLT instruction. Two cases are shown. Figure 7 shows cases where NMI is not recognized. Figure 8 shows cases where NMI is recognized. Both cases assume setup and hold time requirements are met for the NMI input.

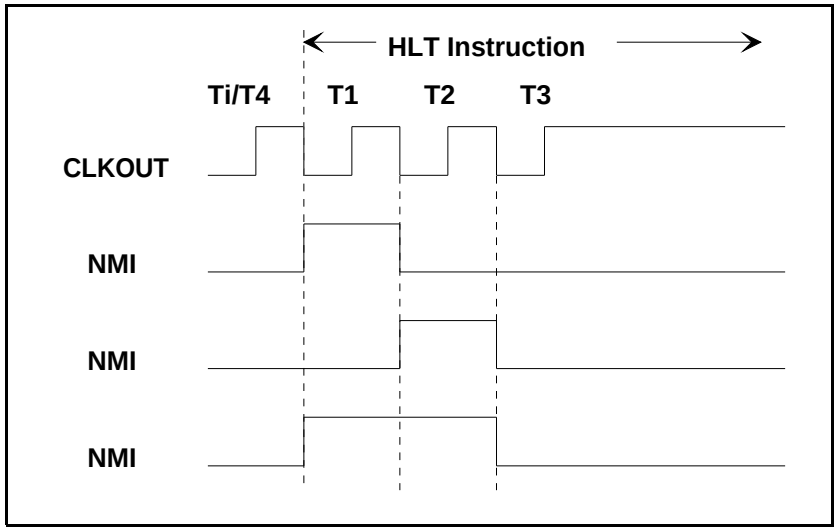

Figure 7. NMI Ignored During HLT Entering Powerdown

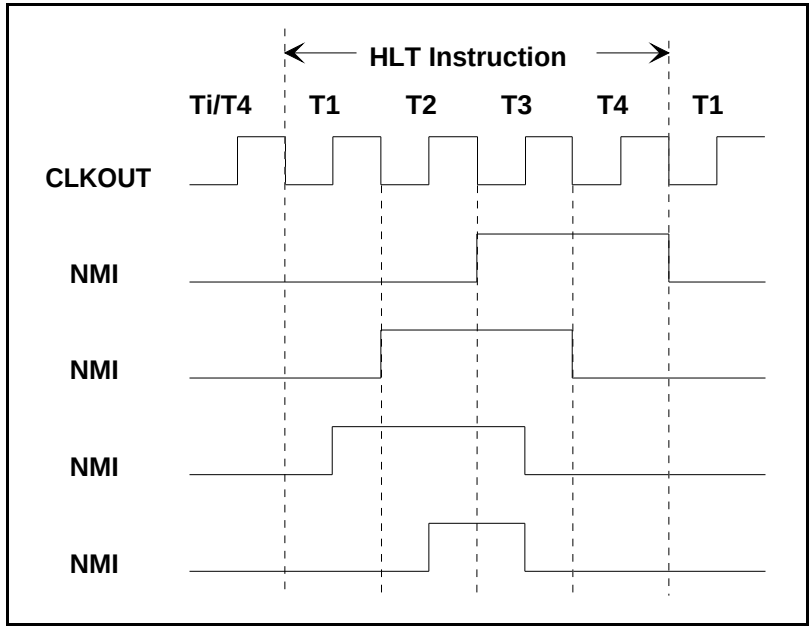

Figure 8. NMI recognized during HLT entering Powerdown

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

4. ONCE Mode

PROBLEM: The condition of driving the A19/ONCE# pin low is not latched on the rising edge of RESIN#, which means that A19/ONCE# must be forced low at all times to remain in ONCE Mode after RESIN# rises.

IMPLICATION: Driving A19/ONCE# low while RESIN# is low enables ONCE Mode. As long as A19/ONCE# remains low the 80C18xEB will remain n ONCE# mode. A19/ONCE# is weakly pulled high while RESIN# is low to prevent accidental entrance in ONCE# mode. When RESIN# is returned high, the 80C18xEB will remain is a reset state, but A19/ONCE# must remain low to continue to enable ONCE Mode. Returning A19/ONCE# to a high level after RESIN# returns high will re-enable all output drivers, however, the 80C18xEB will remain in a reset state. RESIN# must again be driven low to exit the 80C18xEB from the reset state.

WORKAROUND: This is no workaround for this anomaly. ONCE Mode can only be entered and remain active as long as A19/ONCE# is driven low.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

5. RESIN# Hysterisis

PROBLEM: RESIN# has been measured to only have less than 150 mV of Hysterisis depending on the frequency of operation (the higher the frequency, the lower the Hysterisis).

IMPLICATION: The input is very sensitive to noise, especially when using an RC type reset circuit. Noise on the RESIN# pin has been shown to cause the device to lock up while the input makes its transition through the 2.5 V (approx.) volt range.

WORKAROUND: Drive RESIN# with a Schmitt-Triggered device for noise decoupling and to provide a fast transition through the input switching point.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

6. SINT1

PROBLEM: SINT1 will only go active for clock period if a receive or transmit interrupt is pending for serial channel 1.

IMPLICATION: If the interrupt is to be connected to any of the 80C18xEB interrupt lines (INT0-INT4), then SINT must be latched externally using to keep the interrupt active until the CPU can respond.

WORKAROUND: The SINT line can be latched using an external SR-type latch or D-type latch. The user must then clear the latch using software.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

7. INTA# Bus Cycles

PROBLEM: During interrupt acknowledge (INTA) bus cycles, the bus controller may or may not respond to READY. INTA bus cycles are used to support an external slave interrupt controller (such as the 82C59A) when the interrupt controller is programmed for CASCADE Mode.

IMPLICATION: READY is ignored if the previous bus cycle (prior to the first INTA cycle) activated one of the chip-selects whose RDY bit was programmed to 0 (ignore external ready). Ignoring READY means that the INTA cycle will execute with no wait-states. If the previous bus cycle either activated a chip-select in which the RDY bit was programmed to

1 (use external ready), or no chip-selects were activated, then READY can be used to extend an INTA bus cycle.

WORKAROUND: There is no direct workaround for this anomaly. However, the 82C59A-2 device will support zero wait-state operation of INTA cycles up to 16 MHz operation. If the slave interrupt device requires wait-states for INTA cycles, then the chip-selects must all be programmed to use READY (RDY bit set to 1).

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

8. Clock Unit

PROBLEM: CLKOUT will transition on the rising edge of CLKIN instead of the falling edge of CLKIN as mentioned in the datasheet.

IMPLICATION: The fact that CLKOUT hangs on the rising edge of CLKIN does not effect any A.C. timing specifications or any timing waveforms other than T_{cd}.

WORKAROUND: If the system uses a buffered version of CLKIN and depends on the relationship between the transition of CLKIN and CLKOUT, then CLKIN must be inverted to the 80C18xEB.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9. Ipd not fully operational

PROBLEM: Surplus current (Ipd) draw may occur when first entering POWERDOWN Mode.

IMPLICATION: Ipd is correctly tested, but the duration of time it takes to finally reach a passable value can be up to 200 milliseconds. If it takes longer than 200 milliseconds to reach 100 µA, the device failed.

WORKAROUND: NONE. Ipd is correctly tested, but the duration of time it takes to finally reach a passable value can be up to 200 milliseconds. If it takes longer than 200 milliseconds to reach 100 µA, the device failed.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

1. 80C186EB/80C188EB Processor User's Manual

ISSUE: Please make the following corrections to the *80C186EB/80C188EB Microprocessor User's Manual*. These changes will be included in a future revision of the manual.

Page	Change
2-40, Figure 2-25. Interrupt Vector Table	Change Memory Addresses "30, 32, 34, 36, 38, 3A, 3C, 3E, 40, 42, 44, 46, 48, 4A, 4C, 4E, 50, 52" to "38, 3A, 3C, 3E, 40, 42, 44, 46, 48, 4A, 4C, 4E, 50, 52, 54, 56, 58, 5A" respectively.
5-1, section 5.1	Change paragraph to read: "The clock generation circuit (Figure 5-1) includes a crystal oscillator, a divide-by-two counter, power-down, idle, and reset circuitry. See "Power Management" on page 5-10 for a discussion of power management options."
8-3, Table 8-1 Default Interrupt Priorities	Interrupt priorities for INT4:0 should be included in the table. The default priority levels are as follows: INT4 2 INT0 3 INT1 4 INT2 5 INT3 6
8-17, Figure 8-8. Interrupt Mask Register	The reset state for INT3:0 should be Fh, INT4 should be 1h, SER should be 1h, TMR should be 1h
9-5, Figure 9-3.	The stem below Conditional statement "Counter = Compare 'A' ?" should be a "YES" and the stem to the right should be a "NO."