S5U1C33L05D1

USER MANUAL

Rev. 2.0

04/04/08

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1 Overview

The S5U1C33L05D1 board demonstrates the S1C33L05, a 32-bit Seiko Epson microcomputer whit a built-in STN LCD controller.

The circuit board includes 16MB of FLASH memory, 4MB of SRAM, 32MB of NAND Flash memory, 32MB SDRAM and three connectors for interfacing with the S5U1C33L05D1LCD board, S5U1C33L05D1PWM or S5U1C33L05D1DAC board, and the ICD33 debugger. It also provides an external interface for additional I/O.

The S5U1C33L05D1 board is thus also the core of a development environment for developing applications for the S1C33L05.

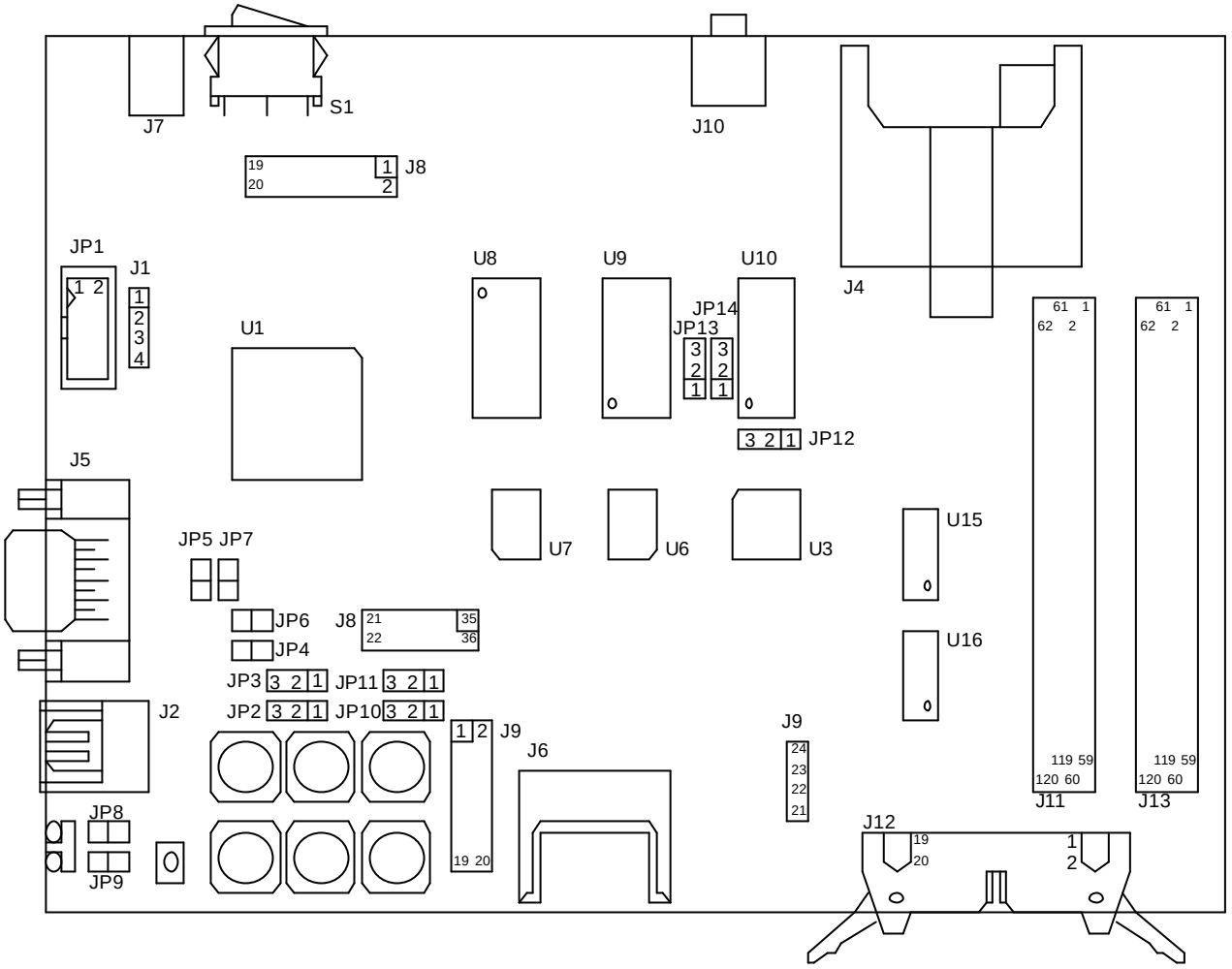


Figure 1. The Layout of S5U1C33L05D1

2 Package

The S5U1C33L05D1 package contains the following items.

(1) S5U1C33L05D1 board 1
(2) S5U1C33L05D1LCD board (LCD display board) 1
(3) S5U1C33L05D1PWM board (PWM audio outputboard) 1
(4) S5U1C33L05D1DAC board (Optional) 1
(5) S5U1C33L05D1KEY board 1
(6) AC adapter (5V DC output), with cable 1
(7) USB cable 1
(8) S5U1C33L05D1 user’s manual (this document) 1

3 Block Diagram

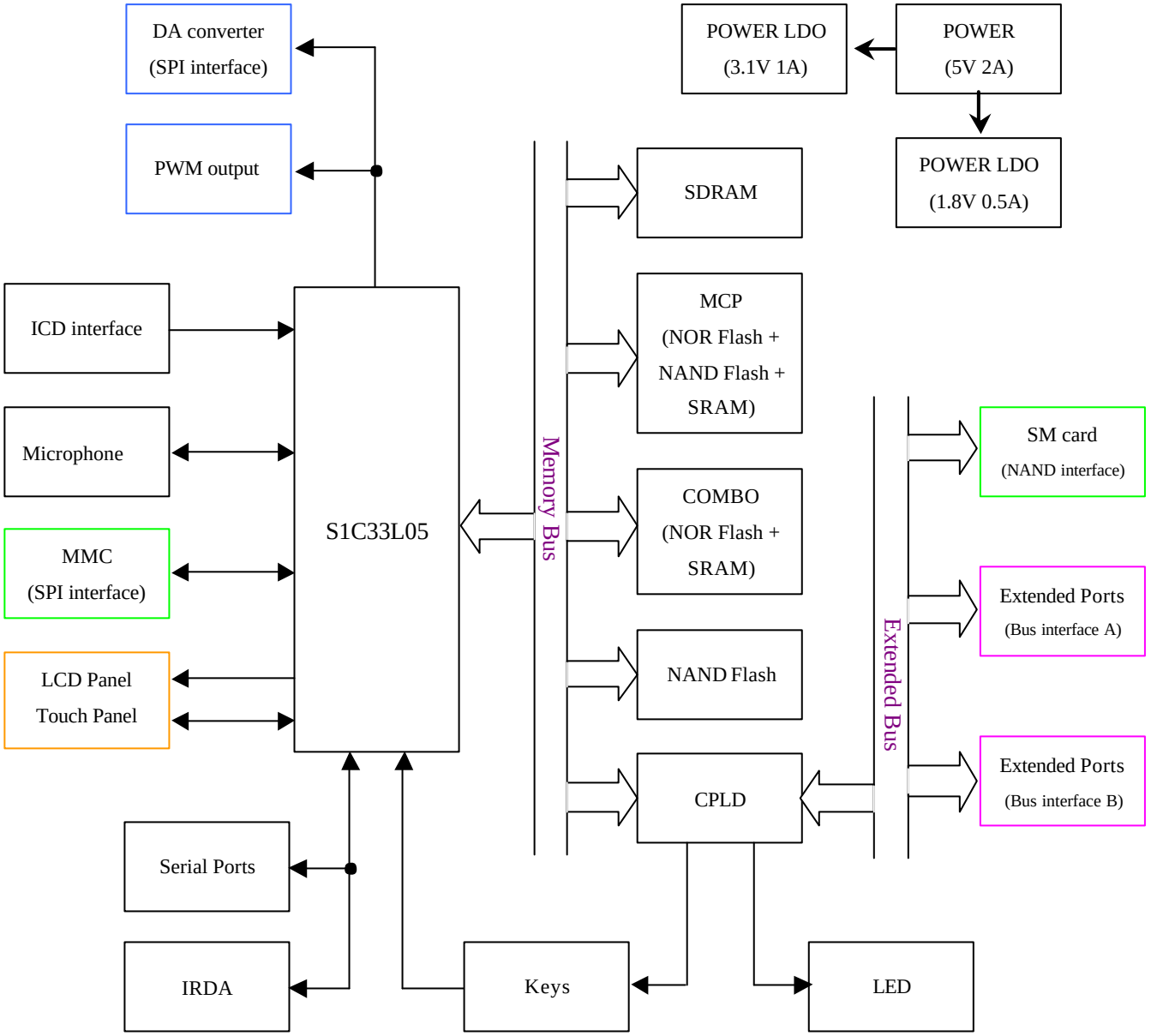


Figure 2. The Block Diagram of S5U1C33L05D1

4 Power Supply

Connecting a 5-volt power supply to the DC IN connector (J7) lights the POWER LED and starts the board. Because S5U1C33L05D1 is for world-wide, a power adaptor (Input: AC 100-240V, output: DC 5V/2A) is selected.

The board derives its internal 3.1-volt and 1.8-volt power supplies from this single 5-volt power supply. The S1C33L05 in this board operates at 3.1V for I/O and 1.8V for the core, while others parts such as memory operates at 3.1V.

The reason why 3.1V is selected is described as follows:

Notes:

1. The maximum power supply of the memory devices (KBB05B400M) is just 3.1V.
2. When using USB function of S1C33L05, the I/O voltage of S1C33L05 must higher than 3.0V.

5 Clock and Boot Settings

The S5U1C33L05D1 uses 48MHz ceramic (special designed for USB) from Murata, as the OSC3 clock. The 32.768KHz crystal is also used for OSC1 clock.

The default setting of JP3 (1-2) turn off the S1C33L05 internal PLL. When setting JP3 to 2-3, the internal PLL is on.

The S1C33L05 working frequency is depending on the OSC3 clock, setting of PLL and S1C33L05 internal register. For details, please refer to S1C33L05 user's manual. The following table shows the recommended clock setting.

	OSC3 divider	PLL setting	CPU frequency	Bus frequency
Default	1/2	X1	24MHz	24MHz
Demo Use	1/2	X2	48MHz	24MHz

Table 1. Recommendation of Clock Setting

The default setting of JP2 (2-3) enables S1C33L05 booting from the external Nor Flash – that is, address 0xC00000 in the Flash memory. When setting the JP2 to 1-2, it enables booting from external 16-bit NAND Flash memory.

6 Memory Map

The jumpers JP10 and JP11 control the address mapping of the 16MB NOR Flash memory and the 8MB SRAM to areas 9+10 and area 17+18. See following setting to see the memory map. Do not use any combination other than those appearing below.

Area	Address	JP10: 1-2 Short JP11: 1-2 Short	JP10: 2-3 Short JP11: 2-3 Short
Area 17+18	0x0FFF_FFFF 0x0800_0000	NOR FLASH	SRAM
Area 15+16	0x07FF_FFFF 0x0400_0000	NAND FLASH	NAND FLASH
Area 13+14	0x03FF_FFFF 0x0200_0000	SDRAM	SDRAM
Area 11+12	0x01FF_FFFF 0x0100_0000	NOR FLASH	NOR FLASH
Area 9+10	0x00FF_FFFF 0x0080_0000	SRAM	NOR FLASH
Area 7+8	0x007F_FFFF 0x0050_0000	Reserved	Reserved
	0x004F_FFFF 0x004C_0000	External Area 2	External Area 2
	0x004B_FFFF 0x004A_0000	External Area 1	External Area 1
	0x0049_FFFF 0x0048_0000	External Area 0	External Area 0
	0x0047_FFFF 0x0040_0000	Extended I/O	Extended I/O

Table 2. Memory Map of S5U1C33L05D1

Note: Because this board supports large memory space, the CEFUNC must be set to “1x”.

7 I/O Port Assignments

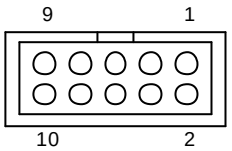
Pin Name	Used By	Function	Pin Name	Used By	Function
P10	ICD	DST0	P31	MMC/SD	SDO
P11		DST1	P32		SPICLK
P12		DST2	P33		SDI
P13		DPCO	P02		MMC #CE
P14		DCLK	K50	Keys	Key Input0
#LCAS	SDRAM	#SDCAS	K51		Key Input1
#HCAS		#SDRAS	K52		Key Input2
P21		#SDWE	K53		Key Input3
P20		SDCKE	P03		Key Input4
BCLK		SDCLK	K60	Microphone Input	ADC inputs0
#CE7		#SDCE	TM0	Extend Audio Output Ports	
P61		SDA10	TM1		
P62		LDQM	TM4		
P63		UDQM	TM5		
PC0	LCD Interface	FPFRAME	P31		
PC1		FPLINE	P32		
PC2		FPSHIFT	#CE8	Sequential ROM	#SQCE
PC3		DRDY	PD0		#SQRD
PB0		FPDAT0	PD1		SQLALE
PB1		FPDAT1	PD2		SQUALE
PB2		FPDAT2	P01	Serial IO & IRDA	FSOUT0
PB3		FPDAT3	P00		FSIN0
PB4		FPDAT4	P05		SOUT1
PB5		FPDAT5	P04		SIN1
PB6		FPDAT6	PD7	IRDA	POWER control
PB7		FPDAT7	P34	NAND Flash & Smart Media Card	#SMWE
P15		POWER control	P35		#SMRE
P16		DOFF control	P24		CLE
K62	Touch Panel Interface	ADC input2	P25		ALE
K63		ADC input3	P40		#WP
K64		Touch Panel interrupt	PD5		RY/#BY
P41		PNP control	#CE5	NAND Flash	#CE of NAND Flash
P42		PNP control	#CE8	Smart Media Card	#CE of Smart Media Card
P06		NPN control	PD3		SM card voltage detector
P07		NPN control	PD4		SM card insert detector
#CE6	CPLD	#CE of extended logic	PD6		SM card protect detector

Table 3. Pin assignment of S1C33L05

8 Connectors

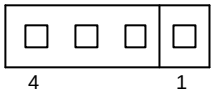
- JP1 and J1 is for connecting the ICD33 debugging tool.
- J8 is for connecting the S5U1C33L05D1LCD board.
- J9 is for connecting the S5U1C33L05D1PWM or S5U1C33L05D1DAC board.
- J12 is for connecting the S5U1C33L05D1KEY board.
- J11 and J13 is for connecting the extended circuits.

8.1.1 JP1 Connector



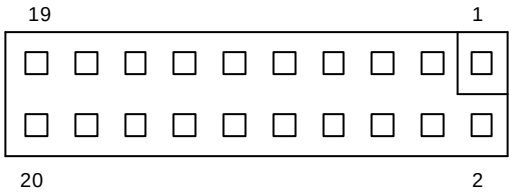
No.	Pin Name	No.	Pin Name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPC0

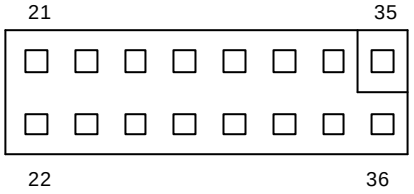
8.1.2 J1 Connector



No.	Pin Name
1	DCLK
2	GND
3	DSIO
4	DST2

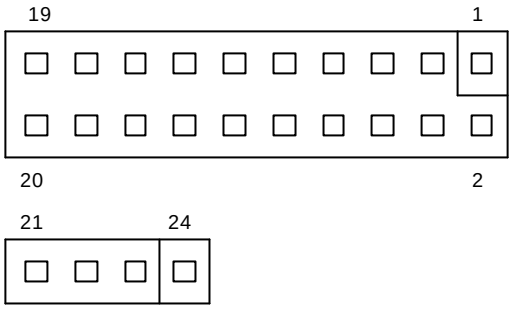
8.1.3 J8 Connector





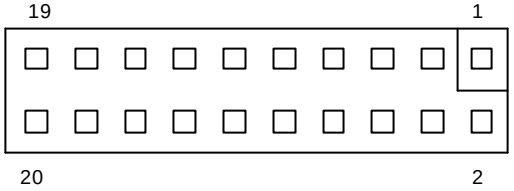
No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	FPDAT7	10	GND	19	GND	28	K64
2	FPDAT6	11	DRDY	20	GND	29	GND
3	FPDAT5	12	FPSHIFT	21	P16	30	GND
4	FPDAT4	13	FPLINE	22	P15	31	P07
5	FPDAT3	14	FPFRAME	23	GND	32	P06
6	FPDAT2	15	GND	24	+3.1V	33	GND
7	FPDAT1	16	GND	25	GND	34	GND
8	FPDAT0	17	K62	26	+5V	35	P41
9	GND	18	K63	27	GND	36	P42

8.1.4 J9 Connector



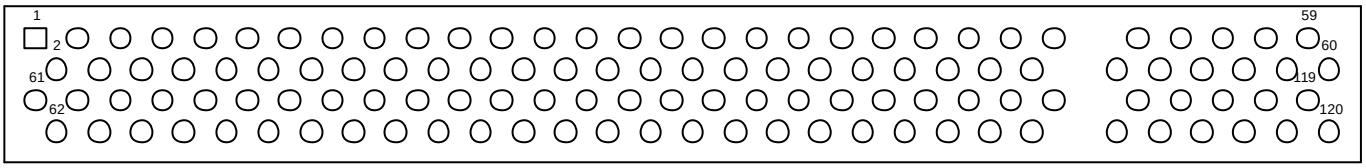
No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	Q13	7	TM4	13	NC	19	SPICLK
2	GND	8	TM5	14	NC	20	SDO
3	GND	9	GND	15	NC	21	GND
4	GND	10	GND	16	GND	22	+3.1V
5	TM1	11	NC	17	GND	23	+5V
6	TM0	12	NC	18	GND	24	GND

8.1.5 J12 Connector



No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	KEYO12	6	KEYO7	11	KEYO2	16	K50
2	KEYO11	7	KEYO6	12	KEYO1	17	K51
3	KEYO10	8	KEYO5	13	KEYO0	18	K52
4	KEYO9	9	KEYO4	14	GND	19	K53
5	KEYO8	10	KEYO3	15	GND	20	P03

8.1.6 J11 and J13 Connector



No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	+3.1V	31	Reserved	61	+3.1V	91	GND
2	NC	32	Reserved	62	EXT_D0	92	EXT_A3
3	NC	33	Reserved	63	EXT_D8	93	GND
4	NC	34	Reserved	64	GND	94	EXT_A4
5	NC	35	NC	65	EXT_D1	95	GND
6	NC	36	NC	66	EXT_D9	96	EXT_A5
7	NC	37	NC	67	GND	97	EXT_A6
8	NC	38	#WAIT	68	EXT_D2	98	EXT_A7
9	NC	39	NC	69	EXT_D10	99	EXT_A8
10	NC	40	NC	70	GND	100	EXT_A9
11	NC	41	NC	71	EXT_D3	101	EXT_A10
12	NC	42	NC	72	EXT_D11	102	EXT_A11
13	NC	43	NC	73	GND	103	EXT_A12
14	NC	44	NC	74	EXT_D4	104	EXT_A13
15	NC	45	#NMI	75	EXT_D12	105	EXT_A14
16	NC	46	NC	76	GND	106	EXT_A15
17	NC	47	GND	77	EXT_D5	107	EXT_A16
18	NC	48	#EXT_WR	78	EXT_D13	108	EXT_A17
19	NC	49	NC	79	GND	109	EXT_A18
20	NC	50	EXT_CS0	80	EXT_D6	110	EXT_A19
21	NC	51	NC	81	EXT_D14	111	EXT_A20
22	NC	52	NC	82	GND	112	EXT_A21
23	NC	53	NC	83	EXT_D7	113	EXT_A22
24	NC	54	EXT_CS1	84	EXT_D15	114	GND
25	NC	55	GND	85	GND	115	#EXT_RD
26	NC	56	EXT_CS2	86	#EXT_BSL	116	NC
27	NC	57	GND	87	GND	117	NC
28	NC	58	NC	88	EXT_A1	118	#RESET
29	NC	59	NC	89	GND	119	#EXT_BSH
30	Reserved	60	+5V	90	EXT_A2	120	+5V

9 Jumpers (Refer to Figure 1. The Layout of S5U1C33L05D1)

- JP2

Booting selector	
1-2 Short	Booting from on board NAND Flash
2-3 Short	Booting from area 10 (NOR FLASH/SRAM)

- JP3

Internal PLL use or not	
1-2 Short	PLL OFF
2-3 Short	PLL ON

- JP4, JP5, JP6, JP7, JP8, JP9

Function	JP4	JP5	JP6	JP7	JP8	JP9
Serial port is SIO0, no IrDA port	Short	Open	Short	Open	Open	Open
Serial port is SIO1, no IrDA port	Open	Short	Open	Short	Open	Open
IrDA port is SIO 0, no serial port	Open	Open	Open	Open	Short	Short
IrDA port is SIO 0, Serial port is SIO1	Open	Short	Open	Short	Short	Short

Note: Other settings are forbidden.

- JP10, JP11 (Using KBB05B400M or KBB06A300M)

Function	JP10	JP11
Area 9+10 as NOR Flash, Area 17+18 as SRAM	2-3 Short	2-3 Short
Area 9+10 as SRAM, Area 17+18 as NOR Flash	1-2 Short	1-2 Short

Notes: Other settings are forbidden.

- JP12

Sequential ROM Setting	
1-2 Short	Sequential ROM not use
2-3 Short	Sequential ROM located into area 14 ***1, 2**

Notes:

1. SDRAM must be less than 16MB and located into area 13.
2. Smart media card can not be used.

- JP13, JP14

Function	JP13	JP14
Using NAND Flash in MCP	2-3 Short	2-3 Short
Using external single device of NAND Flash	1-2 Short	1-2 Short

10 Module Description

10.1 MEMORY

10.1.1 External Memory (NOR Flash and SRAM)

The external memory here means external NOR Flash memory and external SRAM, do not include the external NAND Flash memory (External NAND Flash memory will be described in another section).

The SAMSUNG MCP device is used in S5U1C33L05D1 board. It is KBB05B400M. The following table shows the configuration.

CHIP	NOR FLASH	SRAM
KBB05B400M	16MB	8MB

Table 4. S5U1C33L05D1 Memory Configuration

In default setting, NOR Flash memory is located into area 9+10 while SRAM is located into area 17+18. But changing the JP10 and JP11 can exchange the address of NOR Flash memory and SRAM. Because of lay out problem, when using different chips, the meaning of JP10 and JP11 is different. The following table shows the setting of JP10 and JP11.

Area	Address	JP10: 1-2 Short JP11: 1-2 Short	JP10: 2-3 Short JP11: 2-3 Short
Area 17+18	0x0FFF_FFFF 0x0800_0000	NOR FLASH	SRAM
Area 9+10	0x00FF_FFFF 0x0080_0000	SRAM	NOR FLASH

Table 5. Using KBB05B400M

10.1.2 SDRAM

In S5U1C33L05D1, a 32MB SDRAM is used, which is located into area 13+14. The following figure shows the connection of SDRAM.

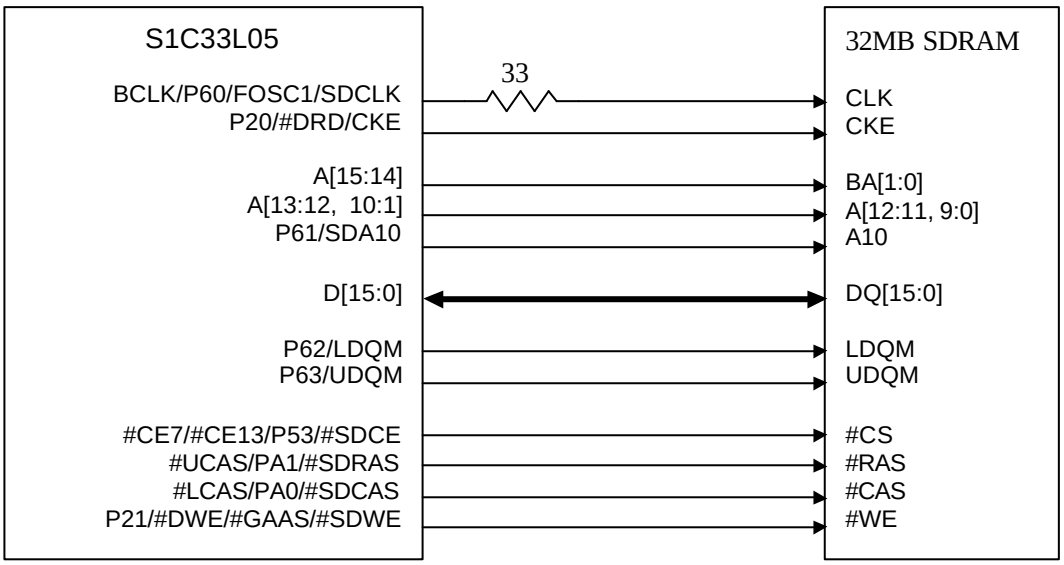


Figure 3. The Connection of SDRAM

Note:
In SDRAM clock line, a 33ohm resistor is placed in serial to keep signal integrity.

10.1.3 NAND FLASH MEMORY

Two kinds of NAND Flash memory are supported in S5U1C33L05D1. They are KBB05B400M, and K9F1G16U0M. Each one has different size. The following table shows the configuration.

CHIP	SIZE
KBB05B400M	32MB
K9F1G16U0M	128MB

Table 6. Size of NAND Flash in S5U1C33L05D1

In S5U1C33L05D1, JP13 and JP14 are used to select different NAND Flash. See following table for JP13 and JP14 setting.

Chip	JP13: 1-2 Short JP14: 1-2 Short	JP13: 2-3 Short JP14: 2-3 Short
KBB05B400M	Not used	Used
K9F1G16U0M	Used	Not used

Table 7. NAND Flash Configuration

The connection between the S1C33L05 and NAND Flash of SAMSUNG MCP is shown as follows:

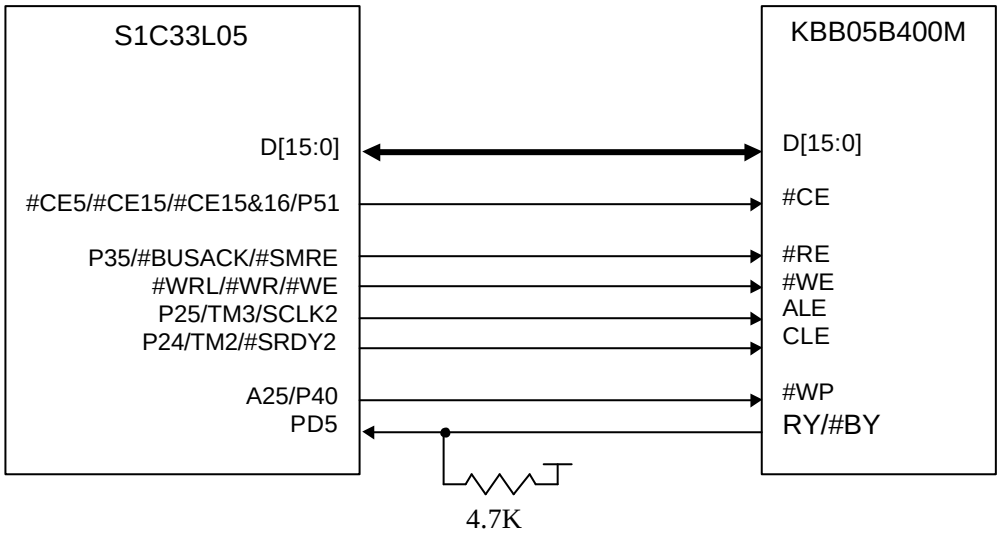


Figure 4. The Connection between S1C33L05 and SAMSUNG MCP

When using KBB06A300M or KBB06A400M, the chip select signal can not be used as GPIO. Otherwise, when CPU access the NAND Flash, a writing operation to the external SRAM may cause the NAND Flash reading error (Because the NAND Flash use the system write signal instead of #SMWE).

The following diagram shows the the connection between the S1C33L05 and NAND Flash(K9F1G16U0M):

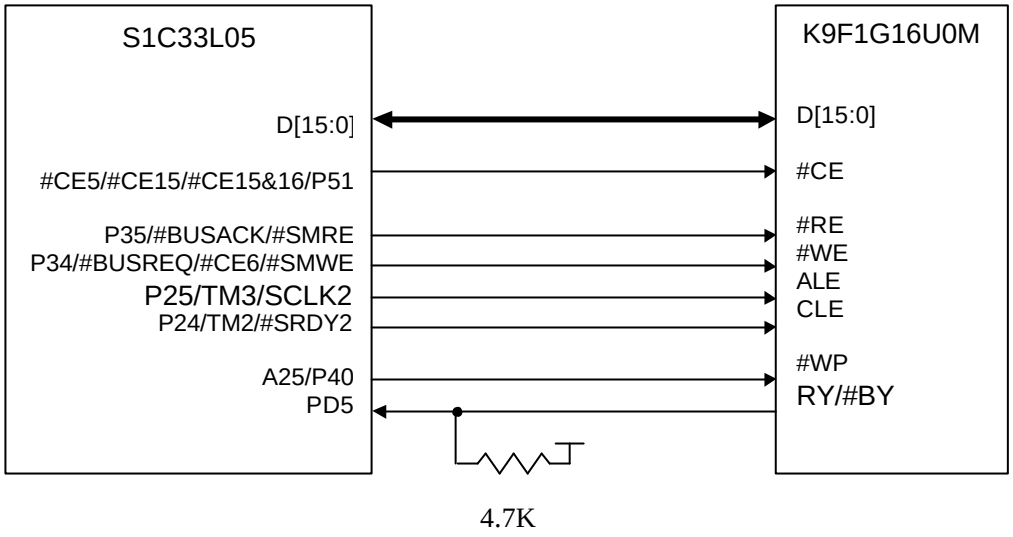


Figure 5. The Connection between S1C33L05 and K9F1G16U0M

When using K9F1G16U0M, the chip select signal can be used as GPIO, because the write signal using the NAND Flash write signal (#SMWE).

The S5U1C33L05D1 also supports smart media card, the connection is shown as follows:

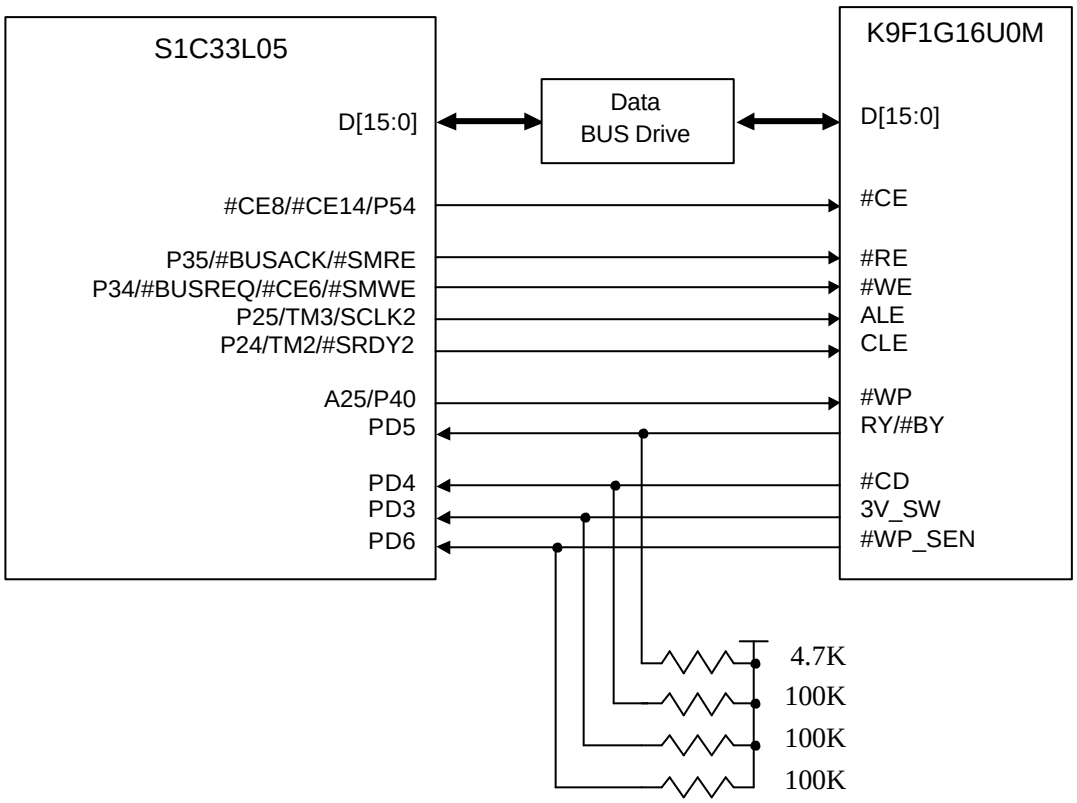


Figure 6. The Connection between S1C33L05 and Smart Media Card

Because the smart media is the external card, a data bus driver is used to isolate the system data bus. The smart media card has some additional signals to indicate the card information to the S1C33L05. The following table shows the additional signal:

Signal	"0"	"1"
#CD	Card inserted	No card inserted
3V_SW	3V card	Not 3V card
#WP_SEN	Write protect	Write not protect

Table 8. Addition signal of smart media card

The smart media card and the NAND Flash can be used simultaneously. Because the address of the smart media is also mapped in area 15+16. When access the smart media card, to avoid conflicting with the NAND Flash on the board, the following steps must be followed:

1. Set the P51 output register high (D[1] / 0x300022 = 1'b1).
2. Set the P51 I/O register as output (D[1] / 0x300023 = 1'b1).
3. Switch to P51 function (D[3:2] / 0x30004A = 2'b01).
4. Access the smart media card.
5. Switch to #CE15 function (D[3:2] / 0x30004A = 2'b00).

10.2 EXTEND OUTPUT PORTS

In S5U1C33L05D1, the I/O ports of the S1C33L05 is not enough, some output ports are extended via the CPLD (XC9572XL). Totally16 output ports are extended through CPLD. 13 output ports are used for the key matrix, 2 output ports are for LED control while 1 output port for audio circuit control.

The following diagram shows how to extend the output ports in CPLD:

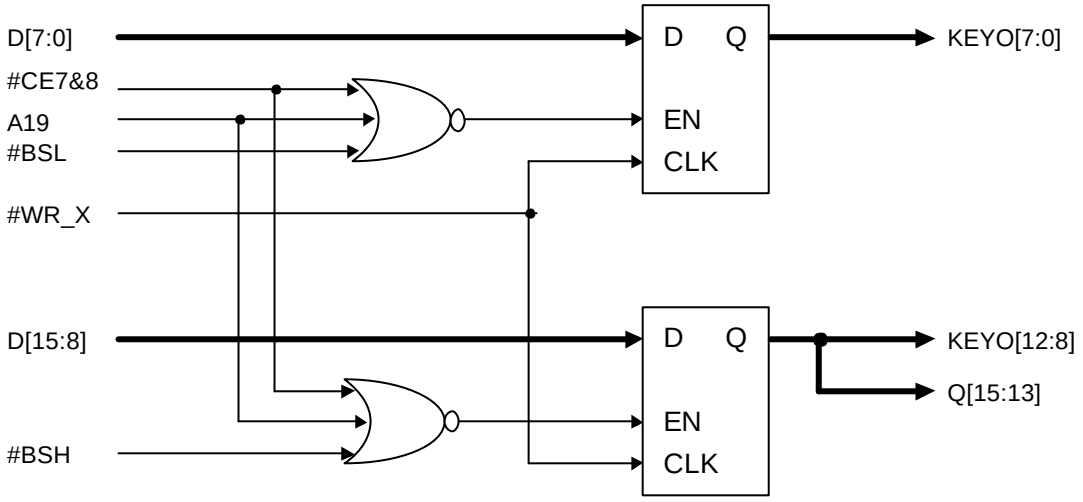


Figure 7. Extended Output Ports Implementation

The following table shows the register of the extended output ports. In order to simplify the circuit of the extended output ports, reading the register of the extended output ports is not supported.

Register name	Address	Bit	Names	Function	Setting				Init.	R/W	Remark
Extended Ports data register	040_0000	DF	Q15	Q15 output data	1	High	0	Low	0	W	Read "0"
		DE	Q14	Q14 output data					0	W	
		DD	Q13	Q13 output data					0	W	
		DC	KEYO12	KEYO12 output data					0	W	
		DB	KEYO11	KEYO11 output data					0	W	
		DA	KEYO10	KEYO10 output data					0	W	
		D9	KEYO9	KEYO9 output data					0	W	
		D8	KEYO8	KEYO8 output data					0	W	
		D7	KEYO7	KEYO7 output data					0	W	
		D6	KEYO6	KEYO6 output data					0	W	
		D5	KEYO5	KEYO5 output data					0	W	
		D4	KEYO4	KEYO4 output data					0	W	
		D3	KEYO3	KEYO3 output data					0	W	
		D2	KEYO2	KEYO2 output data					0	W	
		D1	KEYO1	KEYO1 output data					0	W	
		D0	KEYO0	KEYO0 output data					0	W	

In S5U1C33L05D1, Q15 is used to drive red LED, Q14 is used to drive green LED. Q13 is used in audio circuit (PWM output module). KEYO[12:0] is used in key matrix.

10.3 EXTENDED I/F

In S5U1C33L05D1, an extended interface is provided for adding additional circuits. In this extended interface, all the bus, such as data bus, address bus and control bus are isolated with the internal system bus. The following diagram shows the architecture of the extended interface.

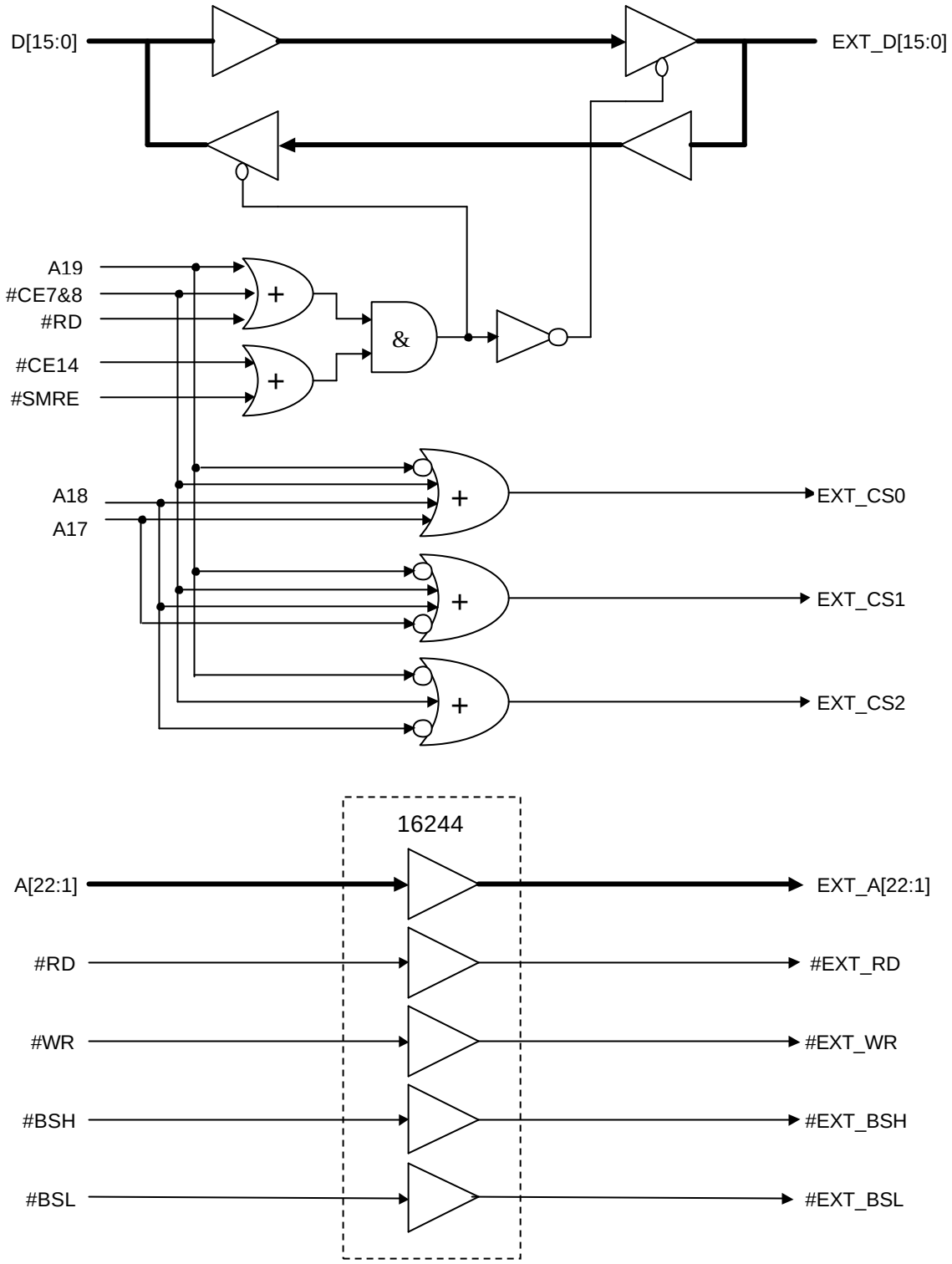


Figure 8. The Diagram of Extended Ports Implementation

The data bus driver and the chip select decoder is implemented in CPLD, while control bus

driver is implemented via the bus driver (74LVTH16244). The address of the extended chip select signal is shown as follows:

Area	Address	JP10: 1-2 Short JP11: 1-2 Short	JP10: 2-3 Short JP11: 2-3 Short
Area 17+18	0x0FFF_FFFF 0x0800_0000	NOR FLASH	SRAM
Area 15+16	0x07FF_FFFF 0x0400_0000	NAND FLASH	NAND FLASH
Area 13+14	0x03FF_FFFF 0x0200_0000	SDRAM	SDRAM
Area 11+12	0x01FF_FFFF 0x0100_0000	NOR FLASH	NOR FLASH
Area 9+10	0x00FF_FFFF 0x0080_0000	SRAM	NOR FLASH
Area 7+8	0x007F_FFFF 0x0050_0000	Reserved	Reserved
	0x004F_FFFF 0x004C_0000	External Area 2	External Area 2
	0x004B_FFFF 0x004A_0000	External Area 1	External Area 1
	0x0049_FFFF 0x0048_0000	External Area 0	External Area 0
	0x0047_FFFF 0x0040_0000	Extended I/O	Extended I/O

Table 9. The Address of the Extended Area

10.4 KEY

Totally 65 keys are supported in S5U1C33L05D1. These 65 keys are implemented via a 13x5 matrix. In these keys, 6 of them has two parts. One part is on the main board, the other part is on the key board. That means, in the S5U1C33L05D1 main board, there are 6 keys in the main board, which has the same function as the keys in the key board. The key matrix is shown as follows:

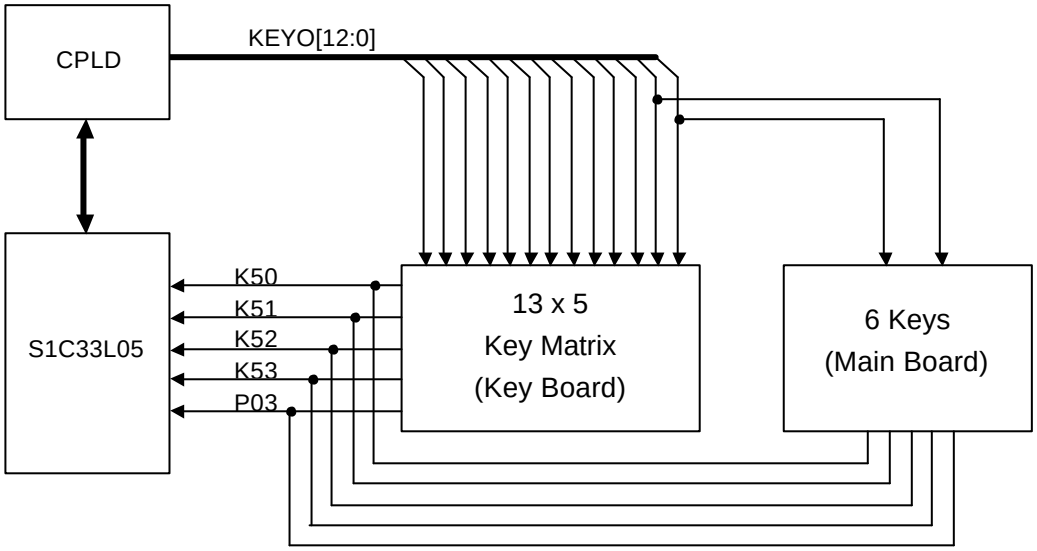


Figure 9. Key Matrix Connection

Note that the register of the 13 output signals from CPLD is write only. Software can not detect the state of the output signals via reading the data register.

10.5 SOUND INPUT

Please refer to EPSON S1C33 Family APPLICATION NOTES.

10.6 SOUND OUTPUT

Please refer to EPSON S1C33 Family APPLICATION NOTES.