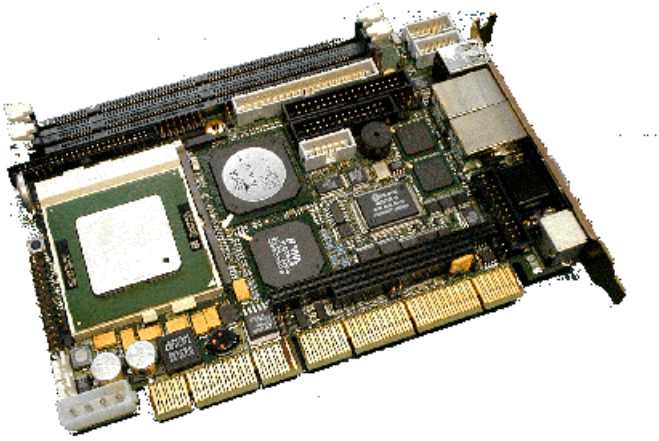
PISA®-PIII-TwisterT

All-In-One Socket370
CPU Card

User's Manual
Version 0.3



10 / 06 / 2003

MSC Vertriebs GmbH
Design Center Neufahrn

Copyright Notice

☝ Important Information

This product is not an end user product. It was developed and manufactured for further processing by trained personnel.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Always observe proper polarities

☝ Caution!

Danger of explosion if the battery is incorrectly replaced. When battery replacement is necessary use only the exact same battery or a battery recommended by the manufacturer.

Pay attention to the local area regulations regarding the proper disposal of used batteries.

Trademarks :

PISA is a registered trademark of JUMP*tec* Industrielle Computertechnik AG
JUMP*tec* is the registered trademark of JUMP*tec* Industrielle Computertechnik AG

1 General Information

1.1 Introduction

The PISA-PIII-TwisterT is an all-in-one single board computer card for the PISA bus (PISA = PCI + ISA), designed for Intel's new generation Pentium™ III and Celeron™ Tualatin CPUs, as well as VIA's C3 CPUs in Socket370 package.

The board uses the VIA ProSavage PN133T chipset (VT8696 TwisterT Northbridge and VT86286B Southbridge) runing at 100 MHz or 133 MHz front side bus.

With an LCD/CRT SXVGA controller, up to two 100MBit Ethernet controllers, an EIDE controller, a floppy controller, as well as sound-, LPT-, keyboard and mouse interfaces, four serial communication ports and four USB ports, the PISA-PIII-TwisterT packs all the functions of an industrial computer onto a single card. This makes it an ideal solution for embedded applications.

Two 168-pin standard DIMM socket are giving you the flexibility to configure your system up to 1 GByte of 3.3V SDRAM (PC100 and PC133) .

The integrated S3 ProSavage4 AGP 4x 2D/3D/Video accelerator with 128-bit graphic engine uses 8, 16 or 32 MByte of system memory. The PISA-PIII-TwisterT board includes one 36-bit DSTN/TFT flat panel and one 2-channel 110 MHz LVDS interface by actually supporting display types with resolutions up to 1400 x 1050 pixels.

Up to two Intel 82551ER PCI 10/100BaseTx Ethernet controllers can be equipped which give access to high speed networks through standard RJ45 connectors in the front panel of the board.

The PISA-PIII-TwisterT includes a high speed, local bus EIDE controller. This controller supports (through ATA PIO) mode3, mode4 and Ultra DMA-33/66/100 hard disks, enabling data transfer rates up to 100 MByte/sec. Up to two devices, including large hard disks, CD-ROM drives, tape backup drives, or other IDE devices may be connected to the 40pin 2,54mm primary IDE header. Optionally the secondary EIDE port can be accessed by mounting a CompactFlash connector onto the solder side of the board.

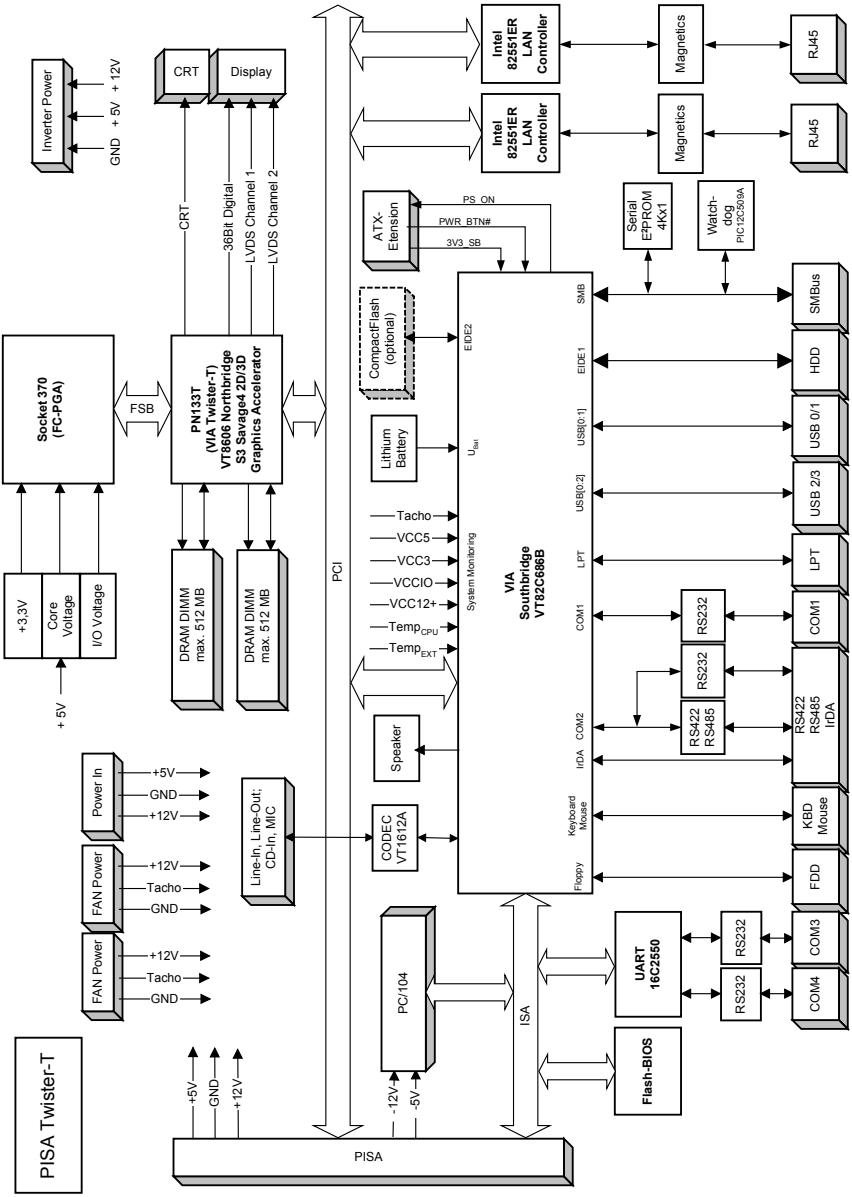
Onboard features also include four high-speed RS-232 serial ports (one configurable as RS422/485), one IrDA, one bi-directional SPP/EPP/ECP parallel port, one floppy drive controller and four USB 1.1 ports.

128kbit/sec stereo applications are supported by a SoundBlasterPro/Direct Sound AC97 Digital Audio controller.

An onboard 5.25" power connector give the possibility to use the PISA-PIII-TwisterT as a standalone system (without a backplane). The implemented PC/104 interface allows you to install additional functions using standard PC/104 modules.

Please visit our web site **http://www.msc.de** (->products ->downloads ->PISA)
where you can find drivers, firmware updates and documentation.

1.2 Block Diagram



1.3 Specifications

Core:

CPU :

- *Socket 370 Intel Pentium III with 512KB L2-Cache, up to 1.26 GHz, 133MHz FSB*
- *Socket 370 Intel Celeron with 256KB L2-Cache, up to 1.4 GHz, 100MHz FSB*
- *VIA C3 Ezra up to 933 MHz, 100/133 MHz FSB*
- *VIA C3 Ezra-T up to 1 GHz, 133 MHz FSB*
- *VIA C3 Nehemiah up to 1.2 GHz, 133 MHz FSB*

ChipSet:

VIA ProSavage PN133T
VT8696 TwisterT North Bridge
VT82686B South Bridge

On-chip Caches:

- *Intel Celeron, 32 KB L1 cache, 256KB L2 cache*
- *Intel Pentium, III 32 KB L1 cache, 512KB L2 cache*
- *VIA C3 CPUs, 128KB L1 cache, 64 KB L2 victim cache*

Memory:

- *2 Standard 168-Pin DIMM sockets*
- *max. 1GByte, PC100 or PC133, independent of FSB speed*

ISA-Bus Interface:

- *VT86286B South Bridge*
- *Standard PISA connector*
- *Standard PC/104 connector*

PCI-Bus Interface:

- *VT8696 TwisterT North Bridge*
- *Standard PISA connector*

Video:

- *S3 ProSavage4 AGP4x SXVGA Controller (integrated into North Bridge)*
- *8/16/32 MB fame buffer (shared with system memory)*
- *CRT-Interface, 15 pin VGA connector integrated into front panel*
- *Flat Panel Interface (36-bit TTL and 2 channel 110 MHz LVDS)*
- *Panel type selectable via BIOS setup*
- *Connector for backlight inverter power supply*

Realtime Clock:

- *VT82686B South Bridge*

- *Lithium battery*

Ethernet:

- *Intel 82551ER Ethernet Controller 10/100 MBit*
- *Second Intel 82551ER Ethernet Controller 10/100 MBit optional*
- *RJ45 standard connectors integrated into front panel*

Floppy Disk:

- *2 drives supported*
- *AT / PS2 compatible floppy disk interface*

Serial:

- *1 x RS232 (COM1)*
- *1 x RS232/RS422/RS485/IrDA, configurable via BIOS setup (COM2)*
- *2 x RS232 (COM3, COM4)*

Parallel:

- *1x parallel Port (PS/2-compatible /ECP/EPP, configurable via BIOS setup)*

USB:

- *2 x USB 1.1 integrated into front panel*
- *2 x USB 1.1 on 2 x 5 pin header*

Keyboard, Mouse:

- *MFII-Keyboard Interface*
- *PS/2-Mouse Interface*

BIOS:

- *512 KByte Flash ROM 29F004 (TSOP32) with integrated 64KB boot block*
- *PhoenixBIOS 4.0 Release 6.1*

Flashdisk:

- *optional : CompactFlash connector on solder side*

Watchdog:

- *PIC12C509 PIC Controller*
- *Programmable delay from 1 to 255 seconds or minutes*
- *Programmable timeout from 1 to 255 seconds or minutes, action : HW-RESET*
- *Re-triggerable via ISA I/O-port*

Sound:

- *SoundBlasterPro Hardware and DirectSound Ready AC'97 Digital Audio Controller*
- *VT1612A AC'97 2.2 VSR Codec*
- *Line-out, Line-in, CD-in, MIC-in*

System Monitoring:

- *2 fans (CPU, system)*
- *3 temperatures (CPU, board, external (2pin pin header))*
- *5 voltages (CPU core voltage, +2.5V, +3.3V, + 5V, +12V)*

Power Supply:

+5V	*±5%*	
+12V	*±5%*	*required for additional PC/104 and fans*
-12V	*±5%*	*only required for additional PC/104 cards*

Supply Current** (Windows 2000 +CPUBURN.EXE)**:

+5V	*6.6 A*	*Intel Celeron 1.2 GHz / 1.4 GHz, 100 FBS*
	6.9 A	*Intel Pentium III 1.26 GHz, 133 MHz FSB*
	5.0 A	*VIA C3 EZRA 800 MHz, 133 MHz FSB*
	5.2 A	*VIA C3 EZRA-T 1.0 GHz, 133 MHz FSB*
	5.5 A	*VIA C3 NEHEMIAH 1.0 GHz / 1.2 GHz, 133 MHz FSB*
+12V	-	*depends on PC/104 card and / or fans*
-12V	-	*depends on PC/104 card*

Environment:

Temperature	operating	0 .. + 60°C
	non operating	-25 .. + 85°C
Humidity (rel.)	operating	0 - 95 %
	non operating	5 - 95 %

Dimensions:

185 x 125 mm

Connectors Overview

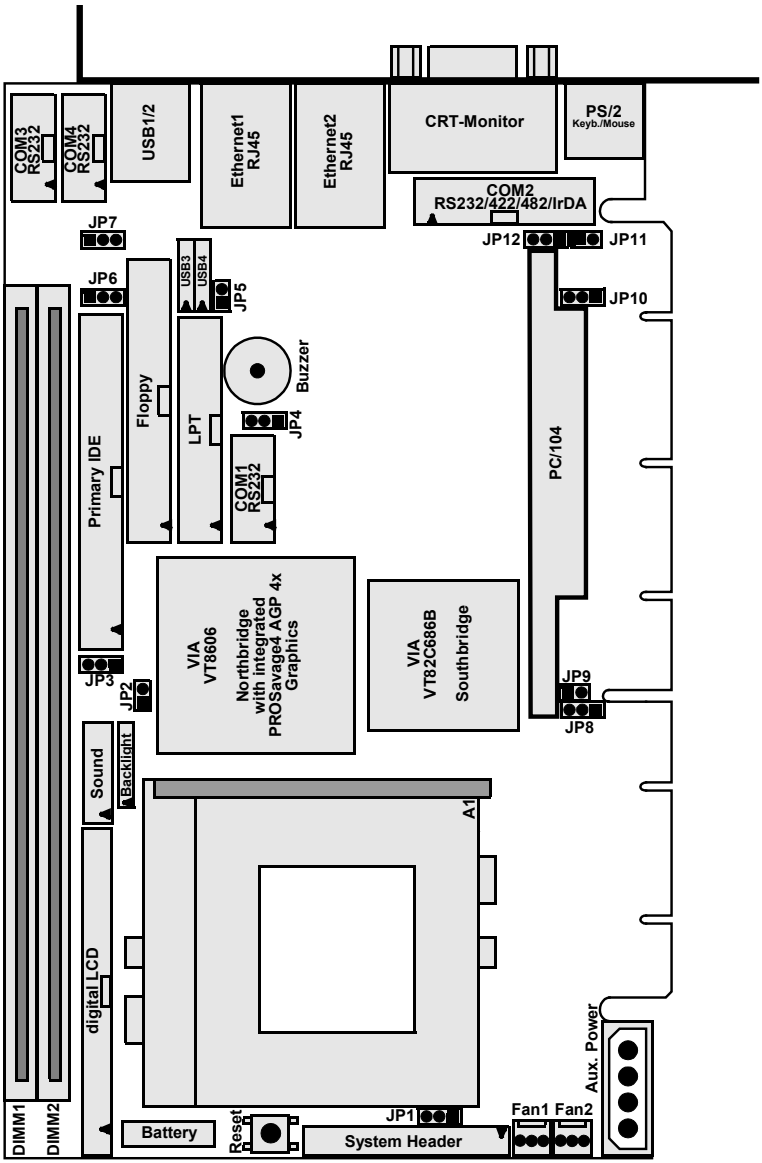
Interface	Connector Type
CPU	staggered 370-pins, ZIF-socket
PCI-Bus	PISA standard edge connector
PC/104 (ISA-Bus)	Standard 64+40-pins connector (female)
Memory	2 x DIMM socket, 168-pins
EIDE: Primary Secondary	IDC header, 40-pins, 2 rows, 2.54mm, CampactFlash socket, 50-pins (optional)
Floppy	IDC header, 34-pins, 2 rows, 2.54 mm
Parallel Port	IDC header, 26-pins, 2 rows, 2.54 mm
COM1	IDC header, 10-pins, 2 rows, 2.54 mm
COM2	IDC header, 20-pins, 2 rows, 2.54 mm
COM3	IDC header, 10-pins, 2 rows, 2.54 mm
COM4	IDC header, 10-pins, 2 rows, 2.54 mm
CRT Interface (15pol. HDSUB)	HDSUB, 15-pins
LCD Panel (digital)	IDC header, 50-pins, 2 rows, 2mm
LCD Panel (LVDS)	FFC connector, 40-pins, 1 row (bottom), 0.5 mm Type HIROSE FH12S-40S-0.5SH
LCD Inverter Power	pin header 6-pins, 1 row, 2.54 mm
LAN 1, 2	RJ-45 (CAT5)
USB 1, 2	Dual USB connector, type A
USB 3, 4	2 x pin header, 5-pins, 1 row, 2.54 mm
Sound	pin header, 14-pins, 2 rows, 2.54 mm
Fan 1, 2	2x pin header, 3-pins, 1 row, 2.54 mm
AUX Power	5¼" power connector
Keyboard / Mouse (external)	PS/2, 6-pins
System Connector: pin header, 30-pins,2 rows, 2.54 mm	
Keyboard / Mouse (intern)	pin header, 7-pins, 1 row, 2.54 mm
Reset	pin header, 2-pins, 1 row, 2.54 mm
Power LED	pin header, 5-pins, 1 row, 2.54 mm
IDE LED	pin header, 2-pins, 1 row, 2.54 mm
Speaker	pin header, 4-pins, 1 row, 2.54 mm
SMBus	pin header, 4-pins, 1 row, 2.54 mm
Temperature sensor	pin header, 2-pins, 1 row, 2.54 mm
ATX extension	pin header, 4-pins, 2 rows, 2.54 mm

Jumpers

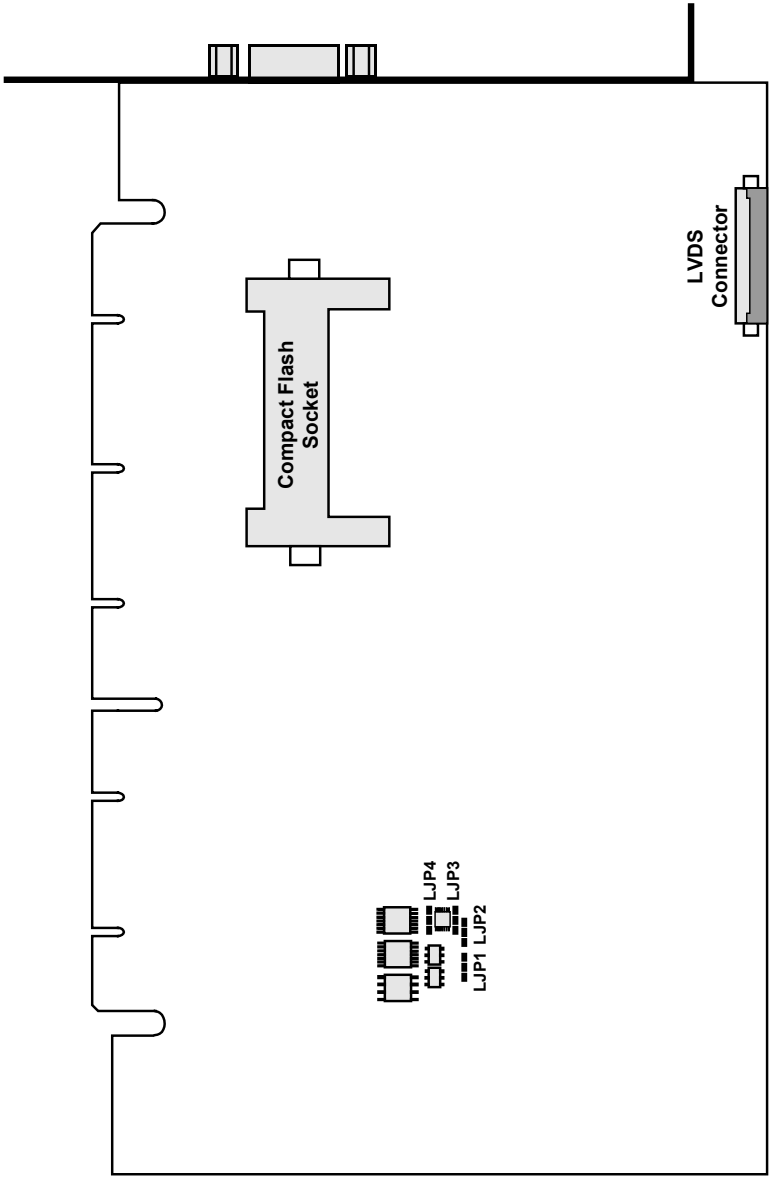
Name	Pins	Description
JP1	3	Processor AGTL voltage level
JP2	2	VT8606 internal AGTL termination resistors enable / disable
JP3	3	Processor pin X4 functionality
JP4	3	Processor FSB frequency selection
JP5	2	Onboard buzzer enable / disable
JP6	3	LCD power supply level
JP7	3	LCD power mode
JP8	3	Clear CMOS
JP9	2	BIOS crises recovery
JP10	3	RS485 receive/transmit control
JP11	2	RS422/RS485 line termination enable / disable
JP12	3	PCI I/O voltage level
LJP1	3	FAN1 voltage level (solder jumper)
LJP2	3	FAN1 voltage level (solder jumper)
LJP[3..4]	3	For internal use, must be always open

1.4 Board Layout

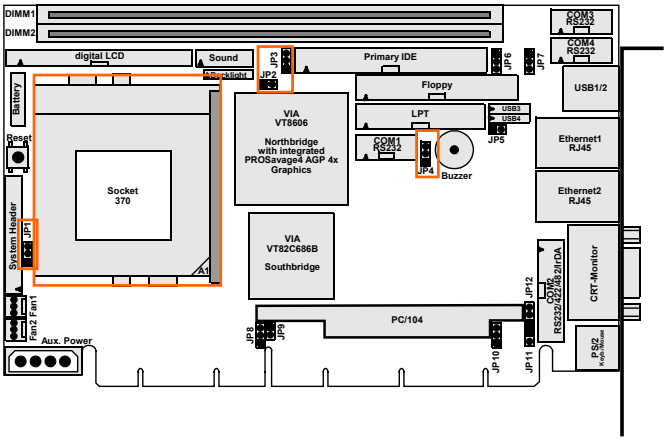
1.4.1 Top Side



1.4.2 Bottom Side



2 Installation



2.1 CPU

The PISA-PIII-TwisterT supports Socket 370 Intel Pentium III and Celeron (both Tualatin Cores only) as well as VIA C3 CPUs.
It is based on the VIA *ProSavage PN133T* chipset VT8606 (TwisterT) northbridge and VT82686B southbridge operating at 100 MHz or 133 MHz front side bus.
The system performance depends on the CPU you choose.

The following table shows the supported CPU types and their recommended jumper settings:

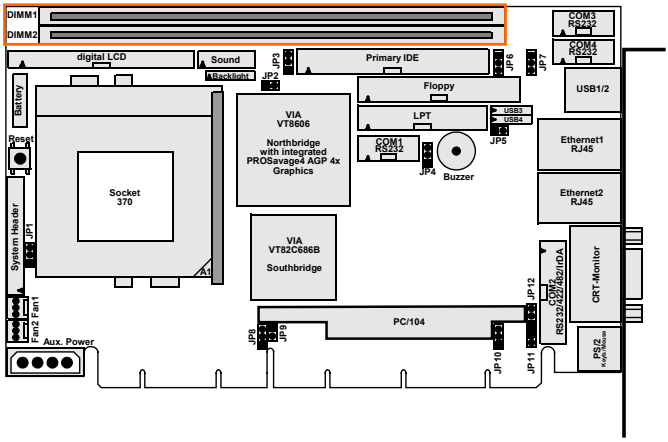
CPU / internal frequency / L2-cache / core voltage	JP1	JP2	JP3	JP4
INTEL Celeron / 1000 / 256 / 100 /1.5	2 – 3	closed	2 – 3	1 – 2
INTEL Celeron / 1100 / 256 / 100 /1.5	2 – 3	closed	2 – 3	1 – 2
INTEL Celeron / 1200 / 256 / 100 /1.5	2 – 3	closed	2 – 3	1 – 2
INTEL Celeron / 1400 / 256 / 100 /1.5	2 – 3	closed	2 – 3	1 – 2
INTEL Pentium III / 1133 / 512 / 133 /1.45	2 – 3	closed	2 – 3	2 – 3
INTEL Pentium III / 1200 / 512 / 133 /1.45	2 – 3	closed	2 – 3	2 – 3
INTEL Pentium III / 1266 / 512 / 133 /1.45	2 – 3	closed	2 – 3	2 – 3
VIA C3 Ezra / 800 / 64 / 133 / 1.35	1 – 2	open	1 – 2	2 – 3
VIA C3 Ezra / 1000 / 64 / 133 / 1.35	1 – 2	open	1 – 2	2 – 3
VIA C3 Ezra-T / 1000 / 64 / 100 / 1.45	2 – 3	closed	2 – 3	1 – 2
VIA C3 Nehemiah / 1000 / 64 / 133 / 1.40	2 – 3	closed	2 – 3	2 – 3
VIA C3 Nehemiah / 1000 / 64 / 133 / 1.45	2 – 3	closed	2 – 3	2 – 3

Note:

- Intel CPUs have 32 Kbyte L1-caches
- VIA C3 CPUs have 128 Kbyte L1-caches.

☝ **Do not run any CPU without an adequate fan and heatsink!**

2.2 SDRAM



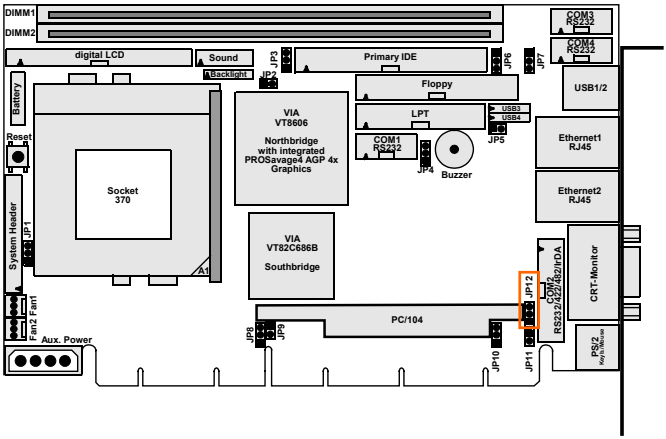
The PISA-PIII-TwisterT board has two DIMM sockets for standard 3,3V SDRAM DIMM modules. The advanced memory controller supports 256 Mbit DRAM technology thus supporting up to 512 Mbyte per bank or 1 Gbyte in one DIMM socket.

The following table shows the SDRAM organizations which are supported:

Organization	Capacity	Module	max. Capacity (2 DIMMs)
4M x 64	32 MByte	single or double sided	64 MByte
8M x 64	64 MByte	single or double sided	128 MByte
16M x 64	128 MByte	single or double sided	256 MByte
32M x 64	256 MByte	single or double sided	512 MByte
64M x 64	512 MByte	single or double sided	1 GByte
128M x 64	1 GByte	double sided	2 GByte

Notes:

- The DRAM controller supports PC133 and PC100 memory modules. The memory timing is installed automatically by the BIOS according to the SPD information read from the serial E^2PROM on the module. SDRAM clock speed is independent of the selected speed of the CPUs front side bus. If PC133 and PC100 memory modules are mixed on the board, the timing parameters of the slower module will be installed.
- PC66 memory modules are not supported.

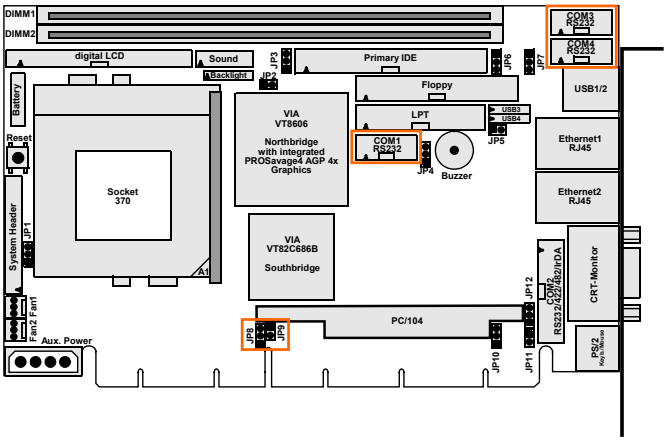


2.3 PCI I/O Voltage

Jumper JP12 selects the PCI-I/O voltage for the PISA board.

JP12	Function
open	Factory default setting. The PISA board is installed in a backplane which connects the VCCIO pin of the PISA slot to the VCCIO pins of the PCI slots.
1 –2	The PISA board is installed in a backplane with 5V PCI slots and the VCCIO pin of the PISA slot is not connected to the VCCIO pin of any PCI slot.
2 - 3	The PISA board is installed in a backplane with 3.3V PCI slots and the VCCIO pin of the PISA slot is not connected to the VCCIO pin of any PCI slot. Or the PISA board is used without a backplane.

Take care about correct setting of jumper JP12 if the PISA-PIII-TwisterT board is installed in a backplane. Wrong settings may damage the board and the backplane.



2.4 Clear CMOS Data and BIOS Flash Recovery Jumper

JP8	Clear CMOS Data
1 – 2	Normal operation
2 - 3	Clear CMOS data
open	No operation

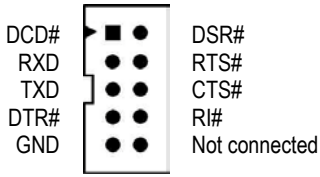
JP9	BIOS Flash Recovery
open	Normal operation
closed	Flash programming

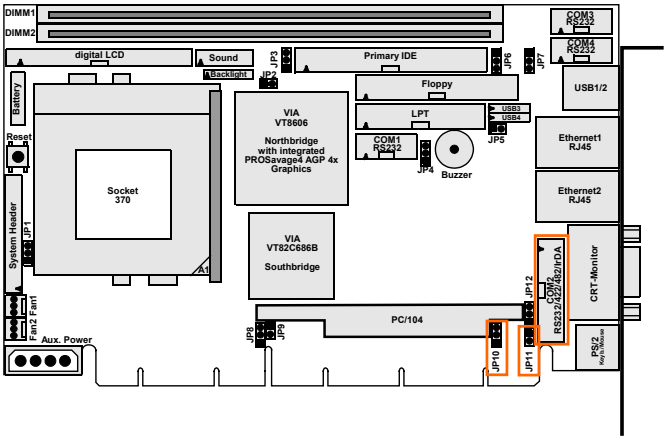
Note:

- For BIOS flash recovery operation JP9 has to be closed before power-up and the crises recovery disk has to be installed in floppy drive A>.

- *To clear the contents of the CMOS (setup configuration) the following procedure has to be done :*
  1. Switch off power.
  2. Install jumper at position 2 – 3 for a few seconds.
  3. Install jumper again at position 1 – 2.

2.5 COM1, COM3 and COM4 (RS232)





2.6 COM2 (RS232/422/485, IrDA)

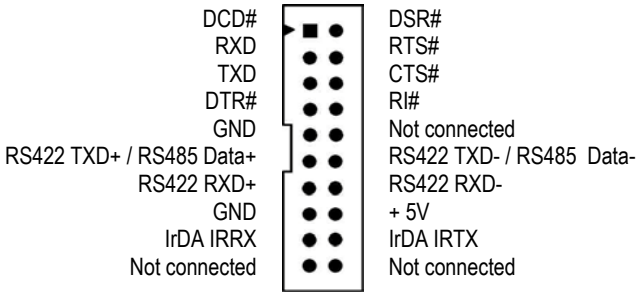
COM2 can be used in RS232, RS422 or RS485 mode. The basic configuration is done via SETUP.

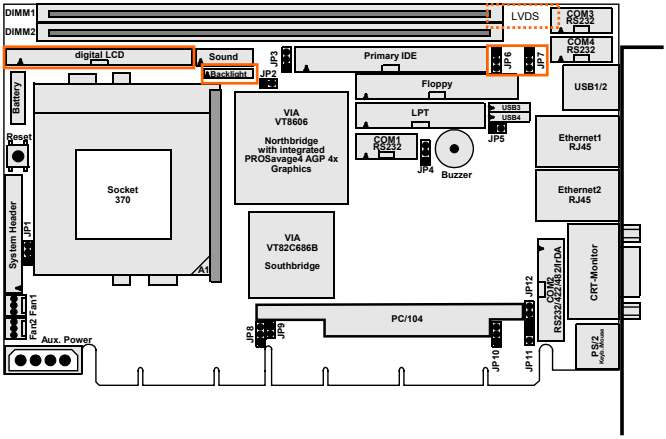
If RS485 mode is selected the signal DTR controls the transmitter, the polarity is determined by JP10.
In RS422 or RS485 mode a 100Ω differential termination resistor may be enabled by JP11.

JP10	Function
1 – 2	DTR low = transmit, DTR high = receive
2 – 3	DTR high = transmit, DTR low = receive
open	No function; do not leave open.

JP11	Function
open	Termination resistor disabled
closed	Termination resistor enabled

Connector COM2





2.7 LCD Interfaces

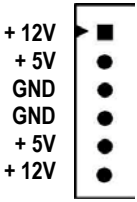
The LCD panel type (technology, resolution) can be selected via SETUP.
JP6 selects the voltage level for panel power supply on both the 50-pin IDC header for digital flat panels and on the 40-pin FFC connector for LVDS panels.
You have to set this jumper according to the type of LCD panel you want to use.
JP7 selects if the display power on the connectors should be permanently on, or switched on an off by the panel power sequencing signal ENVDD.

Jumpers

JP6	LCD Power Level
1 – 2	+ 3.3 Volt
2 – 3	+ 5 Volt
open	Open circuit

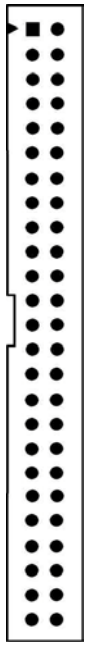
JP7	LCD Power Mode
1 – 2	always on
2 – 3	switched with ENVDD
open	No operation, don't use

Backlight Power (header, 6 pins, 2.54 mm)



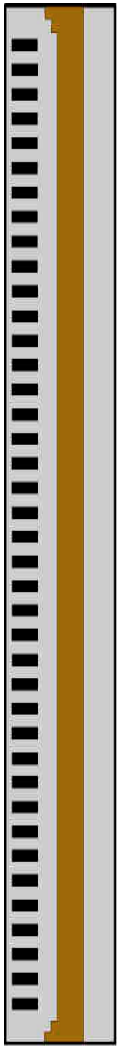
2.7.1 LCD Connectors

Digital (IDC header, 50 pins, 2.0 mm)



+12V	1	2	+12V
GND	3	4	GND
+5V / +3V	5	6	+5V / +3V
ENVEE	7	8	GND
P0	9	10	P1
P2	11	12	P3
P4	13	14	P5
P6	15	16	P7
P8	17	18	P9
P10	19	20	P11
P12	21	22	P13
P14	23	24	P15
P16	25	26	P17
P18	27	28	P19
P20	29	30	P21
P22	31	32	P23
P24	33	34	P25
SHFTCLK	35	36	FLM (VSYNC)
M (DE)	37	38	LP (HSYNC)
GND	39	40	ENBLIGHT
P26	41	42	P27
P28	43	44	P29
P30	45	46	P31
P32	47	48	P33
P34	49	50	P35

LVDS (FCC connector, 40 pins, 0.5 mm)

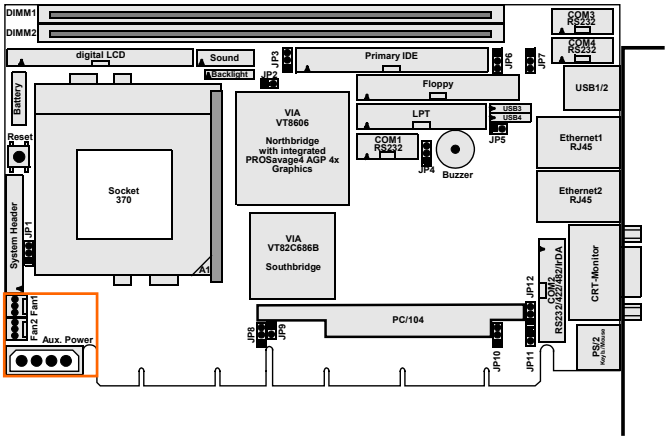


N.C.	1
CH1_RED+	2
CH1_RED -	3
ENVEE	4
CH1_GRN+	5
CH1_GRN -	6
N.C.	7
CH1_BLUE+	8
CH1_BLUE -	9
GND	10
CH1_CLK+	11
CH1_CLK -	12
GND	13
N.C.	14
N.C.	15
PDC_DATA	16
CH2_RED+	17
CH2_RED -	18
PDC_CLK	19
CH2_GRN+	20
CH2_GRN -	21
DETECT#	22
CH2_BLUE+	23
CH2_BLUE -	24
GND	25
CH2_CLK+	26
CH2_CLK -	27
GND	28
N.C.	29
N.C.	30
+5V / +3V	31
+5V / +3V	32
+5V / +3V	33
+5V / +3V	34
ENBLIGHT#	35
GND	36
GND	37
+12V	38
+12V	39
+12V	40

Note: The FCC connector for LVDS uses bottom contacts. Turn flat foil cable contact side top down for insertion.

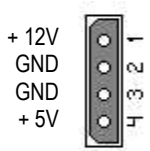
2.7.2 Digital Display Data Mapping

Signal	Pin#	DSTN16	DSTN24	TFT18	TFT24	TFT2x18
P0	9	—	LB3	—	B0	R00
P1	10	—	LB2	—	B1	R10
P2	11	LB1	LB1	B0	B2	R01
P3	12	LB0	LB0	B1	B3	R11
P4	13	—	UB3	B2	B4	R02
P5	14	—	UB2	B3	B5	R12
P6	15	UB1	UB1	B4	B6	R03
P7	16	UB0	UB0	B5	B7	R13
P8	17	—	LG3	—	G0	R14
P9	18	LG2	LG2	—	G1	R14
P10	19	LG1	LG1	G0	G2	R05
P11	20	LG0	LG0	G1	G3	R15
P12	21	—	UG3	G2	G4	G00
P13	22	UG2	UG2	G3	G5	G10
P14	23	UG1	UG1	G4	G6	G01
P15	24	UG0	UG0	G5	G7	G11
P16	25	—	LR3	—	R0	G02
P17	26	LR2	LR2	—	R1	G12
P18	27	LR1	LR1	R0	R2	G03
P19	28	LR0	LR0	R1	R3	G13
P20	29		UR3	R2	R4	G04
P21	30	UR2	UR2	R3	R5	G14
P22	31	UR1	UR1	R4	R6	G05
P23	32	UR0	UR0	R5	R7	G15
P24	33	—	—	—	—	B00
P25	34	—	—	—	—	B10
P26	41	—	—	—	—	B01
P27	42	—	—	—	—	B11
P28	43	—	—	—	—	B02
P29	44	—	—	—	—	B12
P30	45	—	—	—	—	B03
P31	46	—	—	—	—	B13
P32	47	—	—	—	—	B04
P33	48	—	—	—	—	B14
P34	49	—	—	—	—	B05
P35	50	—	—	—	—	B15



2.8 AUX Power Connector

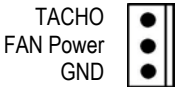
The PISA-PIII-TwisterT board has a 4-pin power connector like standard hard disks have. This connector may be used to power the board if it is used as a stand-alone system without additional ISA- or PCI-cards on a backplane.



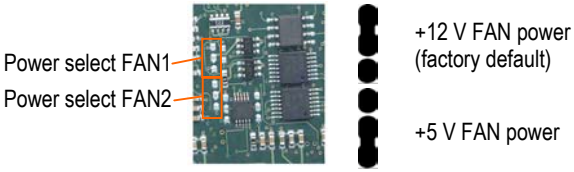
Note: Square marked pin on solder side is pin # 4 (+5V) , **not** pin #1 (+12V).

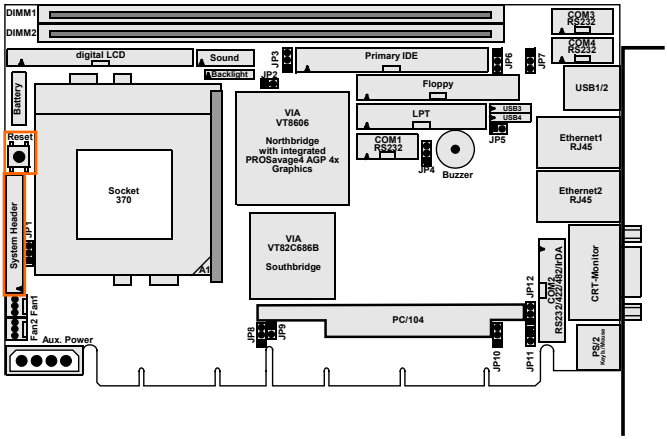
2.9 Fan Connectors

Two Fans may be connected to the board.



Fan power can be selected by solder jumpers LJP1 and LJP2 on the solder side of the PISA-PIII-TwisterT board.

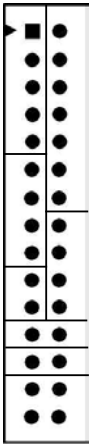




2.10 Onboard Reset Switch

The PISA-PIII-TwisterT board has an onboard switch to reset the system.

2.11 System Header

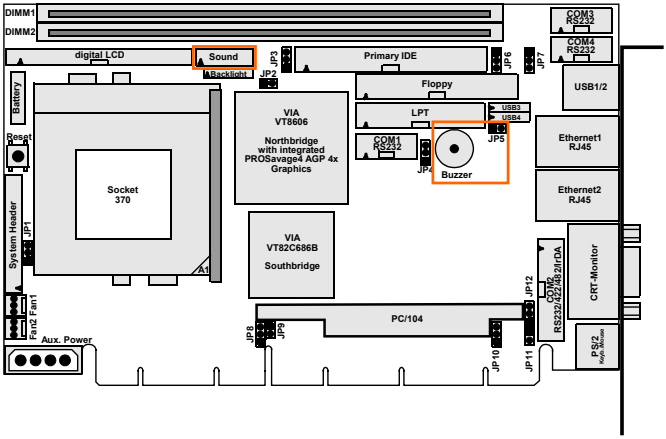


PWR_LED +	1	2	KEYB_CLK
n.c.	3	4	KEYB_DAT
PWR_LED -	5	6	n.c.
n.c.	7	8	GND
GND	9	10	+ 5V
+ 5 V	11	12	MOUSE_CLK
I^2C CLK	13	14	MOUSE_DAT
I^2C DAT	15	16	+ 5V
GND	17	18	n.c.
HD_LED +	19	20	n.c.
HD_LED -	21	22	SPEAKER
EXT_RESET	23	24	GND EXT_RESET
EXT_TEMP(2)	25	26	GND EXT_TEMP
+ 5V_SB (ATX) (2)	27	28	PWRBTN# (ATX) (2)
GND	29	30	PS_ON (ATX) (2)

Notes:

(1) For temperature sensing connect a 10k NTC to EXT_TEMP and GND EXT_TEMP Reference: SEMITEC JT-Thermistor Type 103JT-025, B=3435K.

(2) In order to use ATX extension of the PISA-PIII-TwisterT board connect the appropriate signals of an ATX power supply to these pins.

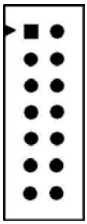


2.12 Onboard Buzzer

The onboard buzzer can be enabled by jumper JP5.

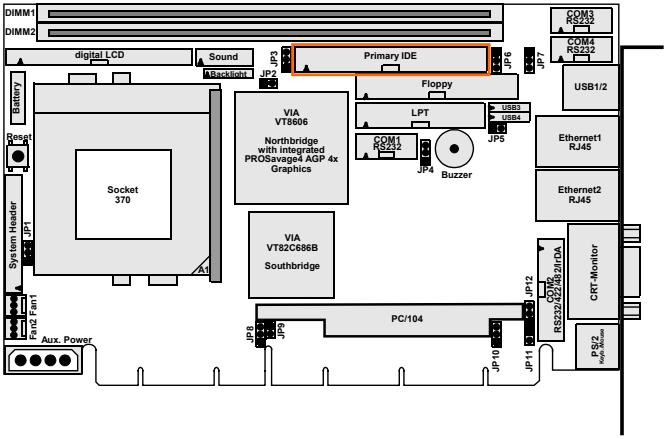
JP5	Buzzer
closed	enabled
open	dsiabled

2.13 Onboard Sound



LINE IN LEFT	1	2	CD IN LEFT
AGND	3	4	CD GND
AGND	5	6	CD GND
LINE IN RIGHT	7	8	CD IN RIGHT
MIC IN	9	10	SOUND LEFT
AGND	11	12	AGND
MIC VCC	13	14	SOUND RIGHT

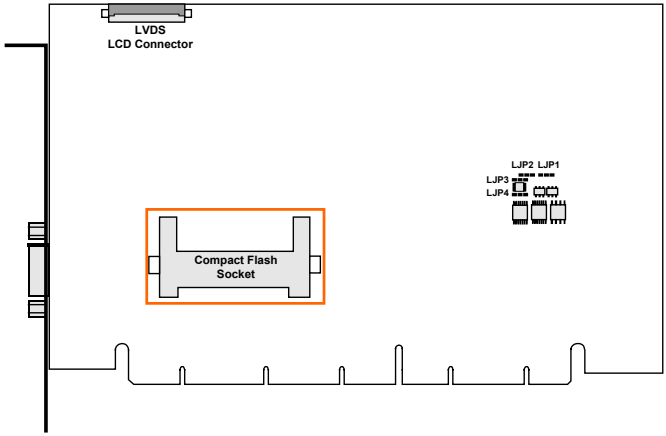
SOUND LEFT and SOUND RIGHT have no additional amplifiers.
Do only connect active speakers to these outputs.



2.14 EIDE

2.14.1 Primary Channel

RESET#	1	2	GND	
DATA7	3	4	DATA	
DATA6	5	6	DATA9	
DATA5	7	8	DATA10	
DATA4	9	10	DATA11	
DATA3	11	12	DATA12	
DATA2	13	14	DATA13	
DATA1	15	16	DATA14	
DATA0	17	18	DATA15	
GND	19	20	KEY	(missing pin)
DRQ0	21	22	GND	
IOW#	23	24	GND	
IOR#	25	26	GND	
IORDY	27	28	CSEL#	
DAK0#	29	30	GND	
IRQ14	31	32	n.c.	
ADR1	33	34	CBLID#	
ADR0	35	36	ADR2	
CS0#	37	38	CS1#	
ACTIV#	39	40	GND	



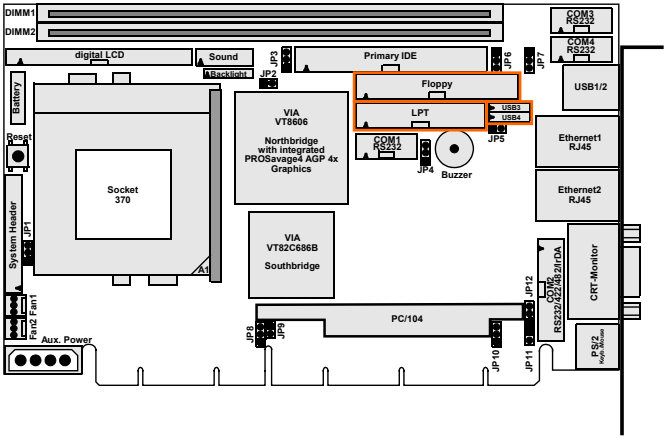
2.14.2 Secondary Channel (optionally), CompactFlash

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	11	GND	21	DATA0	31	DATA15	41	RESET#
2	DATA3	12	GND	22	DATA1	32	CS3#	42	IORDY
3	DATA4	13	+ 5 V	23	DATA2	33	GND	43	n.c.
4	DATA5	14	GND	24	n.c.	34	IOR#	44	+ 5 V
5	DATA6	15	GND	25	n.c.	35	IOW#	45	ACTIVE#
6	DATA7	16	GND	26	n.c.	36	n.c.	46	n.c.
7	CS1#	17	GND	27	DATA11	37	IRQ15	47	DATA8
8	GND	18	A2	28	DATA12	38	+ 5 V	48	DATA9
9	GND	19	A1	29	DATA13	39	Pulldown	49	DATA10
10	GND	20	A0	30	DATA14	40	n.c.	50	GND

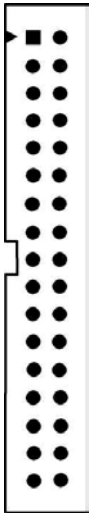
Optionally a CompactFlash socket can be mounted onto the solder side of the PISA-PIII-TwisterT board.

Note:

- CompactFlash cards are IDE compatible and therefore no special Flash driver or a Flash file system is needed. Capacities for CompactFlash range from 8 Mbyte to 2 Gbyte. The CompactFlash socket is routed to the IDE secondary channel.

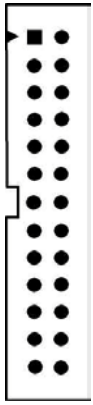


2.15 Floppy Disk



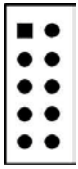
GND	1	2	DENSEL#
GND	3	4	n.c.
GND	5	6	n.c.
GND	7	8	INDEX#
GND	9	10	MTR0#
GND	11	12	DRVSEL1#
GND	13	14	DRVSEL0#
GND	15	16	MTR1#
GND	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WDATA#
GND	23	24	WGATE#
GND	25	26	TRK0#
GND	27	28	WPROT#
GND	29	30	RDATA#
GND	31	32	HEADSEL
GND	33	34	DSKCHG#

2.16 Parallel Port

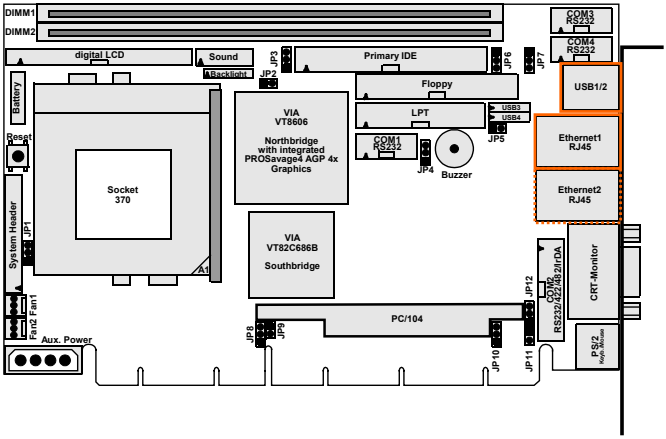


STB#	1	2	AFD#
D0	3	4	ERR#
D1	5	6	INIT#
D2	7	8	SLIN#
D3	9	10	GND
D4	11	12	GND
D5	13	14	GND
D6	15	16	GND
D7	17	18	GND
ACK#	19	20	GND
BUSY#	21	22	GND
PE	23	24	GND
SLCT#	25	26	GND

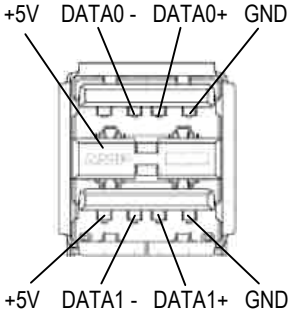
2.17 Internal USB



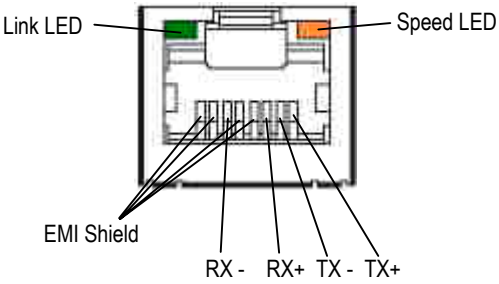
+5V	1	2	+5V
DATA2 -	3	4	DATA3 -
DATA2+	5	6	DATA3+
GND	7	8	GND
SHIELD	9	10	SHIELD



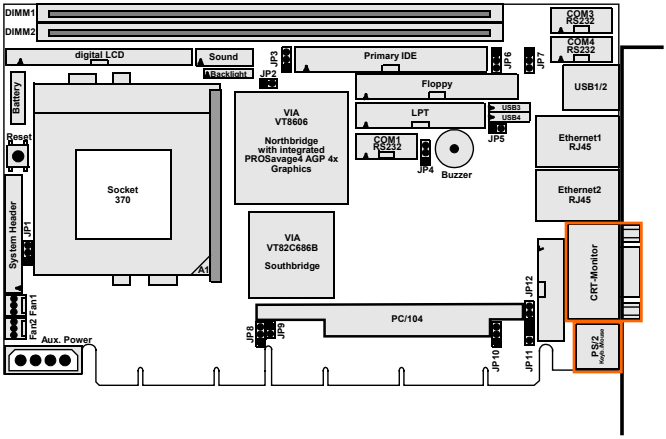
2.18 External USB



2.19 RJ45 (Ethernet)

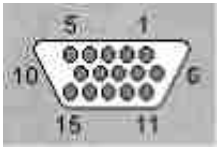


The second Ethernet controller is available as an option.



2.20 CRT

RED	1	9	DDC VCC
GREEN	2	10	GND SYNC
BLUE	3	11	reserved
reserved	4	12	DDC SDA
GND	5	13	HSYNC
GND RED	6	14	VSYNC
GND GREEN	7	15	DDC CLK
GND BLUE	8		



2.21 Keyboard / Mouse Mini-DIN Connector

M_CLK	6 5	KB_CLK
+ 5V	4 3	GND
MDATA	2 1	KB_CLK

Note:

- **A standard PS/2-keybord may be connected directly.**
- **In order to use a mouse or both keyboard and mouse an Y-adapter is needed.**

2.22 PISA Edge-Connector

Pin	ISA Bus Top Layer	ISA Bus Bottom Layer	PCI Bus Top Layer	PCI Bus Bottom Layer
1	IOCHCK#	GND	GND	GND
2	SD7	RESETDRV	GND	GND
3	SD6	+5V	INTB#	INTA#
4	SD5	IRQ9	INTD#	INTC#
5	SD4	-5V	+5V	+5V
6	SD3	DRQ2		
7	SD2	-12V	+5V	V I/O
8	SD1	0WS#	PCIRST#	PCICLK2
9	SD0	+12V	GNT0#	GND
10	IOCHRDY	GND	REQ0#	GNT1#
11	AEN	SMEMW#	GND	GND
12	SA19	SMEMR#	PCICLK1	REQ1#
13	SA18	IOWC#	GND	AD31
14	SA17	IORC#	AD30	AD29
15	SA16	DACK3#	REQ2#	PCICLK3
16	SA15	DRQ3		
17	SA14	DACK1#	GNT2#	PCICLK4
18	SA13	DRQ1	AD28	AD27
19	SA12	REFSH#	AD26	AD25
20	SA11	SYSCLK	AD24	CBE3#
21	SA10	IRQ7	AD22	AD23
22	SA9	IRQ6	AD20	AD21
23	SA8	IRQ5	AD18	AD19
24	SA7	IRQ4	PWRGDIN	REQ3#
25	SA6	IRQ3		
26	SA5	DACK2#	GND	GNT3#
27	SA4	TC	AD16	AD17
28	SA3	BALE	FRAME#	IRDY#
29	SA2	+5V	CBE2#	DEVSEL#
30	SA1	OSC	TRDY#	LOCK#
31	SA0	GND	STOP#	PERR#
32				
33			GND	SERR#
34				AD15
35	SBHE#	MEMCS16#	CBE1#	AD14
36	LA23	IOCS16#	PAR	AD12
37	LA22	IRQ10	GND	GND
38	LA21	IRQ11		
39	LA20	IRQ12	GND	M66EN
40	LA19	IRQ15	AD13	AD10
41	LA18	IRQ14	AD11	AD8
42	LA17	DACK0#	AD9	AD7
43	MEMR#	DRQ0	CBE0#	AD5
44	MEMW#	DACK5#	AD6	AD3
45	SD8	DRQ5	AD4	AD1
46	SD9	DACK6#	AD2	AD0
47	SD10	DRQ6		
48	SD11	DACK7#	+5V	V I/O
49	SD12	DRQ7	+5V	+5V
50	SD13	+5V	GND	GND
51	SD14	MASTER#	GND	GND
52	SD15	GND		

2.23 PC/104 Conncetor

Pin	A	B	C	D
0	—	—	GND	GND
1	IOCHCK#	GND	SBHE#	MEMS16#
2	SD7	RESET	LA23	IOCS16#
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	MEMR#	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	0WS	LA17	DACK0#
9	SD0	+12V	MRDC#	DRQ0
10	IOCHRDY	GND	MWTC#	DACK5#
11	AEN	SMEMW#	SD8	DRQ5
12	SA19	SMEMR#	SD9	DACK6#
13	SA18	/IOWC#	SD10	DRQ6
14	SA17	IORC#	SD11	DACK7#
15	SA16	DACK3#	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 V
17	SA14	DACK1#	SD14	MASTER#
18	SA13	DRQ1	SD15	GND
19	SA12	REFSH#	KEY	GND
20	SA11	SYSCLK	—	—
21	SA10	IRQ7	—	—
22	SA9	IRQ6	—	—
23	SA8	IRQ5	—	—
24	SA7	IRQ4	—	—
25	SA6	IRQ3	—	—
26	SA5	DACK2#	—	—
27	SA4	TC	—	—
28	SA3	BALE	—	—
29	SA2	+5V	—	—
30	SA1	OSC	—	—
31	SA0	MEMW#	—	—
32	GND	GND	—	—

2.24 Watchdog

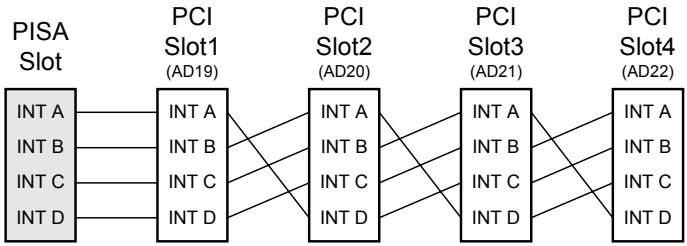
The watchdog can be enabled via SETUP and the user can define if the counter should start during system boot or later by an application software.
It has a programmable delay timer which expires once before the watchdog timer begins counting. After the programmable timeout counter has expired a system reset will be generated.

If enabled in SETUP, application software can access the watchdog register via the I/O address defined in SETUP using IN- and OUT instructions.

ISA Bus	Name	Description
Bit 0	RUN (Read/Write)	1 = timeout counter is running. Setting this bit resets TIMEOUT (bit2) and initializes all counters.
Bit 1	TRIGGER (Read/Write)	must be toggled within the specified time interval to reload the timeout counter.
Bit 2	TIMEOUT (Read only)	0 = no timeout occurred. Default after power-up or after bit0 is set. 1 = timeout has occurred, system was reset. After a timeout the watchdog is stopped until bit0 is set.

2.25 PCI Interrupt Routing

The PISA-PIII-TwisterT board was designed due to **PISA specification Rev. 1.7** released in 1997 by Jumptec® Industrial Computer AG.
For propper BIOS support the following PCI interrupt routing on external backplanes is recommended. This routing mechanism may different from backplanes that were designed in far eastern countries.



Backplane	PISA INT A	PISA INT B	PISA INTC	PISA INTD
Slot 1 (AD19)	INT A	INT B	INT C	INT D
Slot 2 (AD20)	INT D	INT A	INT B	INT C
Slot 3 (AD21)	INT C	INT D	INT A	INT B
Slot 4 (AD22)	INT B	INT C	INT D	INT A

2.26 Interrupts, DMA channels, Upper memory

IRQ	Function	Available	Note
0	Timer 0	No	-
1	Keyboard	No	-
2	Slave 8259	No	-
3	COM2	No	1
4	COM1	No	1
5	SoundBlaster Emulation	No	1
6	Floppy Disk Controller	No	1
7	LPT1	No	1
8	Real Time Clock	No	-
9	-	Yes	-
10	COM3	No	1
11	COM4	No	1
12	PS/2 Mouse	No	1
13	Floating Point Unit	No	-
14	Primary IDE	No	1
15	Secondary IDE	No	1

(1) If the device is disabled in SETUP, the interrupt is available.

PCI Interrupt	Function	Comment
INT A	VGA	chipset internal device
INT B	-	-
INT C	Sound / Ethernet 1	chipset internal / onboard devices
INT D	USB / Ethernet 2	chipset internal / optional onboard devices

PCI Interrupts may be shared with other peripherals.

DMA	Used for	Available	Comment
0	---	Yes	
1	(ECP, if enabled)	(No)	alternate, available if disabled
2	Floppy Disk Controller	No	
3	(ECP, if enabled)	(No)	default, available if disabled
4	Cascade	No	
5..7	-	Yes	

Upper Memory	Used for	Available	Comment
C0000h...CDFFFh	VGA BIOS	No	56 kByte VGA BIOS
CE000h...DBFFFh	-	Yes	ISA bus or shadow RAM
DC000h...DFFFFh	USB legacy	No	ISA bus or shadow RAM if disabled
E0000h...FFFFFh	System BIOS	No	exact start address is displayed on summary screen