Application Note

AN2451/D
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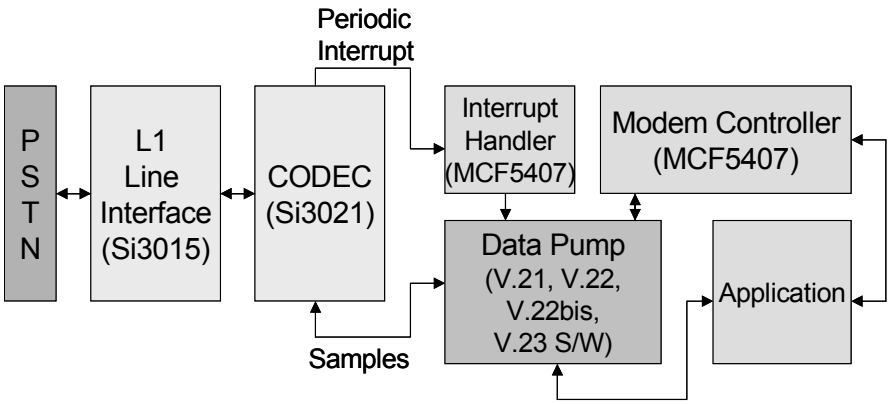
Interfacing a Low Data Rate Soft Modem to the MCF5407 Microprocessor

The traditional modem has been a box or an add-on card with a phone connection on one end and a serial port on the other. It contains a telephone line interface, CODEC, DSP (data pump) and control processor. The DSP converts transmitted data from the PC into signals on the phone line and converts digitised line samples back into demodulated bits (e.g. V.22bis and V.90). The control processor implements AT command interpretation (V.250) and end-to-end data processes such as error control (V.42) and data compression (V.42bis).



The Si3044 DAA chip-set (Si3015 & Si3021) performs the function of an AFE and Line Interface connected to the telephone network.
The MCF5407 ColdFire processor performs interrupt handling and modem control.
The data pump is the software module ported to this device replacing the need for a DSP.
The Application is the background processing whilst a call is in progress.

Figure 1. Block Diagram of a Soft Modem

Soft modems implement DSP functions (data pump) into the serial driver. Typically these drivers depend on an extended instruction set in the CPU. Therefore in this design the data pump is a software module ported to the MCF5407 ColdFire microprocessor (See Figure 1 above).

1 The Attractions of Soft Modems

Cost – CPU's continue to increase in performance. Soft modems are an opportunity to use that CPU performance to save hardware costs.

Flexibility – The fundamental algorithms of the modem are in the driver, which can be modified as easily as any other software module. If a bug is found, it is possible to create a fix and download it to end users through their modems. This is also applicable to modulation scheme upgrades.

1.1 Speed

Higher speed modems require more connect time to deal with extra factors such as timing, adaptive equalisation, echo cancellation and line probing. The higher the speed of the modem the more complex the connection process becomes. If a customer requires a fast connection to browse the Internet this is not a problem. However, if a customer is designing an embedded application where the amount of data in a typical transaction seldom contains more than a few hundred bytes of data then the “less is more” approach should be taken.

If the data content is small (less than 1500bytes) a connection can be established with a lower speed modem and the transaction completed before a higher speed modem would even complete negotiating the connection.

Therefore for the MCF5407 soft modem design targeted at the embedded market place, the V.22bis ITU recommendation has been selected as the highest data rate to be supported. Thus, the MCF5407 soft modem will run at a maximum data rate of 2400bps.

1.2 Target Applications

Many applications in set-top boxes and consumer electronics need to make occasional phone calls to exchange information with a central server. This information is required to exchange billing, financial, or authentication information between a central information system (IS) server and end-consumer equipment. Modems are used because they are still the lowest cost connectivity option.

1.3 Recommendations

All references to V.22bis, V.90, and V.42 etc. are recommendations by the International Telecommunications Union (part of the ITU-T specification list). All “V” listings refer to data communication over the telephone network. Although these recommendations are not law, most telecommunications companies adhere to them in order to move toward a fully compatible global network. The MCF5407 soft modem reference design adheres to these recommendations.

For more information on these standards refer to:
http://www.itu.int/rec/recommendation.asp?type=products&lang=e&parent=T-REC-V

This applications note details the hardware design of a soft modem daughter card that can be interfaced to the M5407C3 evaluation board in order to implement a soft modem design.

2 Design Overview

The object of this section is to outline the principles of the MCF5407 soft modem reference design, to give an overview of the MCF5407 ColdFire microprocessor and the Silicon laboratories Si3044 Data Access Arrangement (DAA) chipset and to explain the reasons for choosing them for this design. For additional and more detailed information on the MCF5407, please refer to the MCF5407 web page: www.freescale.com. For more information on the Si3044 DAA please refer to the user’s manual that can be found at: http://www.silabs.com/products/silldaa.asp.

The MCF5407 will interface to the silicon Laboratories Si3044 DAA chipset via the UART1 interface. A basic block diagram of the hardware is shown in Figure 2. The embedded modem is a S/W module available for download free of charge from the MCF5407 web page. The Si3044 DAA chipset provides the physical interface to the telephone network (PSTN or POTS). The design also includes a loudspeaker to monitor call progress.

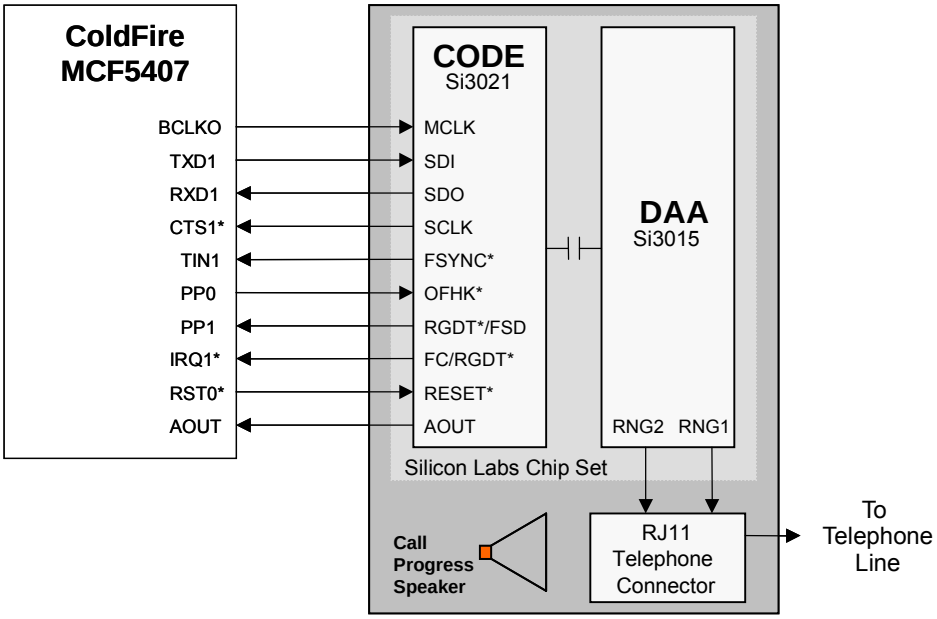


Figure 2. Block Diagram of Soft Modem Reference Design

2.1 MCF5407 ColdFire Microprocessor

The MCF5407 is a 32-bit embedded processor based on the V4 ColdFire core. Designed for embedded control applications, the MCF5407 is the highest performing ColdFire processor available to date.

Serial communications channels are provided by an I^2C interface module and two programmable full duplex UARTs, one of which provides synchronous communications for soft modem applications. Four channels of DMA allow for fast data transfer using a programmable burst mode independent of processor execution. The two 16-bit general-purpose multimode timers provide separate input and output signals. For system protection, the processor includes a programmable 16-bit software watchdog timer. In addition, common system functions such as chip selects, MAC and hardware divide unit, interrupt control, bus arbitration, an IEEE 1149.1 JTAG interface and the real-time BDM interface standard on all ColdFire devices are included.

The decision to use the MCF5407 ColdFire processor was based on the peripheral set, system cost and performance.

The MCF5407 features two independent Universal Asynchronous/Synchronous Receiver/Transmitters. UART1 can be configured in UART mode but also provides synchronous operation and a CODEC interface for soft modem support. UART1 can be configured in one of three modes:

- An 8-bit CODEC interface
- A 16-bit CODEC interface
- An audio CODEC ’97 digital interface controller

For the purpose of this design the MCF5407 will be configured for the 16-bit CODEC as a glue-less interface to the Si3044 DAA chipset.

Soft modem applications tend to be cost critical necessitating the reduction in hardware costs by integrating as much of the modem functionality on one chip. The MCF5407 soft modem is implemented in a competitively priced two-chip solution. The soft modem module is free and since it utilises the V.21, V.22, v.22bis and V.23 data pump standards is not subject to licensing fees.

The MCF5407 is currently available in two speed grades 162MHz and 220MHz. The soft modem utilises the extra performance offered by the MCF5407 whilst leaving plenty of CPU performance to perform other functions.

2.2 Si3044 DAA Chipset

The Si3044 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone requirements. Available in two 16-pin small outline packages (Si3021 CODEC and Si3015 DAA), it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2-4-wire hybrid.

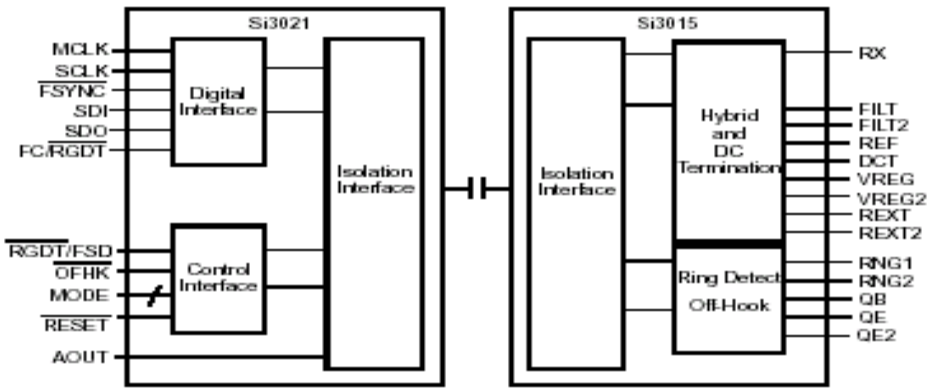


Figure 3. Functional Block Diagram of the Si3044 DAA Chipset

The Si3044 supports data rates up to and including V.90/56Kbps but is not primarily targeted at the PC market.

There are a number of modem chipsets available on the market, adhering to different specifications, with variable amounts of integration and supporting different regions of the world with regards to interfacing to the telephone network.

There are a number of hardware and software blocks required to create a soft modem design, a data pump (can be hardware or software, in the case of this reference design it will be software), a CODEC, a DAA to connect to the telephone network and a serial interface (PCI, serial I/F, SPI, AC-link) to connect to the controller.

As the data pump for this design is implemented in software, the hardware required is a CODEC, DAA and serial interface to the UART on the MCF5407.

Several chipsets were considered from Zilog, Rockwell (now Connexant), TDK and Silicon Laboratories. The SI3044 chipset from Silicon Laboratories meets all the above requirements – CODEC, DAA and UART interface.

Each modem chipset has to be configured to the regional telephone network specification that the modem is designed for. The Si3044 DAA chipset is a global chipset that can be modified by specifying specific parameters to work in every region of the world.

Details on how to configure the DAA chipset for the intended country of use can be found in the software section of this applications note.

3 Hardware Design

The MCF5407 soft modem reference design is developed around the M5407C3 evaluation board using a daughter card for the DAA circuitry. The daughter card connects to the evaluation board using expansion connectors already provided.

The M5407C3 board provides the RS232 interface, BDM interface, 32MB SDRAM and 2MB Flash ROM for system development. For additional detailed information on the evaluation board, including full schematics, refer to the M5407C3 user's manual on the MCF5407 web page.

Figure 2 outlined the hardware design of the soft modem daughter card. The main features and key issues (interface, reset, clocking, power supply and more) are explained in the remainder of this section. Full schematics and schematic summary can be downloaded from the ColdFire website.

3.1 UART1 Interface

The MCF5407 UART module provides a glue-less interface to the Si3044 DAA chipsets serial port (SDO and SDI).

3.1.1 MCF5407 UART1 Interface

UART1 on the MCF5407 provides synchronous operation and a CODEC interface for soft modem support.

On initialisation or reset the UART1 modem settings are set in register MODCTL.

UART1 for this design is configured in modem mode with a 16-bit CODEC interface. The Tx and Rx FIFO's can hold 16 2-Byte samples when in this mode. Tx and Rx FIFO thresholds are set in registers TXLVL and RXLVL respectively on initialisation or reset.

The CODEC(Si3021) of the Si3044 DAA chipset provides a data conversion interface for high-speed modem designs.

UART1 interfaces to the Si3021 via a serial port consisting of Tx and Rx serial data (RxD1 and TxD1) and serial bit clock (/CTS1) and frame inputs (TIN1) from the CODEC.

The serial bit clock is always an input to UART1 in modem mode (on /CTS1). For a 16-bit CODEC the frame sync is also an input to UART1 (on TIN1).

3.1.1.1 MCF5407 UART1 Timing: Transmission

Figure 4 shows example timing for UART1-CODEC interfaces. Note: the UART can be configured to transmit or receive data LSB or MSB first in MODCTL[DTS1], for this design data is transmitted and received MSB first in order to be compatible with the Si3044 DAA chipset.

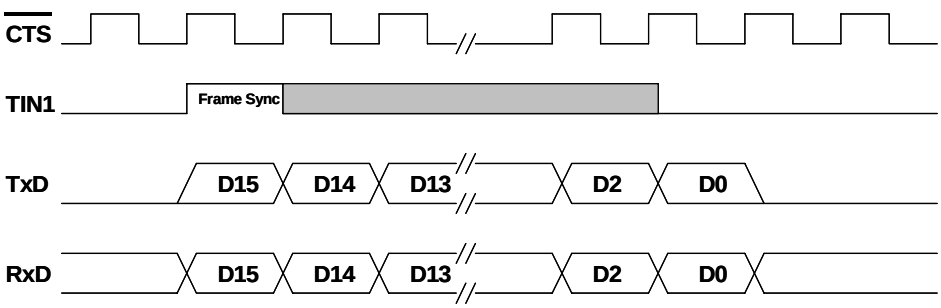


Figure 4. 16-Bit CODEC Interface Timing (MSB first)

When interfaced to a 16-bit CODEC, UART1 starts to send a sample during the 1-bit clock cycle after the rising edge of frame sync. The width of the frame sync pulse makes no difference. After a 16-bit sample is sent, zeros are sent until the next frame sync.

3.1.1.1.1 Reception

Figure 4 shows example timing for the receiver in modem mode.

UART1 starts to receive a sample at the rising edge of frame sync. The width of the frame sync pulse makes no difference.

After the 16-Bit sample is received, the receiver shift register shuts off until the next frame sync occurs.

3.1.1.2 Si3021 CODEC Interface

Si3021 pin descriptions:

- MCLK is the master clock, supplied by BCLKO on the MCF5407 (could also be supplied by the CLKIN signal on the MCF5407) see Clocking section for more details
- $\overline{\text{FSYNC}}$ sends the data framing signal to the TIN pin on the 5407 indicating the start of a communication data frame
- SCLK controls the serial data being received and latches the data being sent. Used as the clock input to UART1 on the MCF5407
- SDO serial port data out (RxD input to the MCF5407)
- SDI serial port data in (TxD output from the MCF5407)
- FC/$\overline{\text{RGDT}}$ an optional signal to instruct the Si3021 that control data is being requested in a secondary frame (connected to -IRQ1 on the MCF5407)
- $\overline{\text{RESET}}$ explained in reset section
- AOUT explained in Call Progress Speaker
- C1A connects to Si3015
- M1=0 and M0=1 selects mode of operation (set to master mode, /FSYNC pulse starts data frame)
- $\overline{\text{RGDT}}$/FSD used to inform the MCF5407 of an incoming call
- $\overline{\text{OFHK}}$ informs the Si3021 that you want to dial out

3.1.1.3 Call Progress Speaker

In order to monitor call progress a small speaker has been included in the daughter card. The Si3044 supports an analog output (AOUT) for driving the call progress speaker. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals.

The recommended application circuit using the LM386 low-power amplifier on the Si3044 data sheet was implemented on the daughter card. R1 and R2 form a voltage divider that provides a gain of –24.4dB in order to prevent the LM386 from being overdriven.

3.1.2 Clocking and Timing

The Si3021 controls the timing of UART1 on the MCF5407 via the SCLK pin. SCLK is generated by the MCLK signal that in turn is driven from the BCLKO pin on the MCF5407. BCLKO is driven at 50MHz on the M5407C3 evaluation board.

The Si3021 contains an on-chip clock generator (See Figure 5) using the single MCLK input frequency (50MHz). The Si3021 can generate all the desired standard modem sample rates from this input.

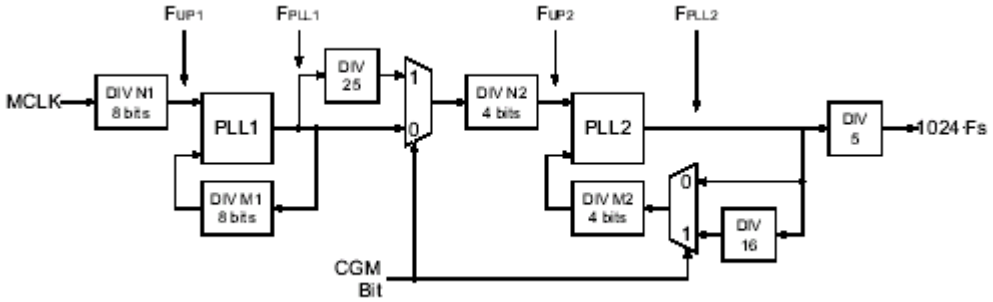


Figure 5. Clock Generation Subsystem of the Si3044 DAA Chipset

The clock generator is programmed according to the Si3044 data sheet, p33 “Setting Generic Sample Rates”. Each of the PLL dividers requires to be set according to the system CLK, In this case 50MHz and the required sampling frequency Fs (9600Hz).

The following equation us used to calculate the values of N1 and M1 (PLL1 dividers), N2 and M2 (PLL2 dividers).

M1*M2/N1*N2=ratio*((5*1024*Fs)/MCLK)

Where ratio = 25/16 for CGM = 1.

For this design the values of N1 and M1 (PLL1 dividers), N2 and M2 (PLL2 dividers) were chosen as:

N1 = 200
N2 = 5
M1 = 128
M2=12.

3.2 Reset/Initialisation

The reset output signal from the MCF5407 processor (/RST0) is used to drive the reset of the Si3044 DAA chipset. At the reset signal all control registers are reset to a predefined initialised state.

The RESET pulse width must be a minimum of 250ns.

The RESET condition guarantees the line-side chip Si3015 is powered down with no possibility of loading the line.

After reset the Si3044 is ready for ring detection and off-hook.

3.3 Power

The M5407C3 board that the soft modem daughter card is interfaced to supplies both 3.3V and 5V.

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