S5U13781R00C100
Reference Board User Manual

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NOTICE

Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13781R00C100 reference board.

The reference board is designed as an evaluation platform for the S1D13781 Display Controller. The S5U13781R00C100 reference board has host controller connector, LCD panel connector, clock generator, SPI flash memory (16Mbit), power regulation circuit for S1D13781 core and DC/DC converter for LED back light.

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2 Features

The S5U13781R00C100 reference board includes the following features:

- QFP 100pin S1D13781F00A100 Display Controller
- 2.54mm pitch vias for host bus interface header
- 2.54mm pitch vias for LCD panel header
- Connection area with 2.54mm pitch vias for header and FPC (0.5mm pitch 55 electrode) connector to connect LCD panel.
- On-board 24MHz crystal
- On-board voltage booster for LED back light (38V 60mA Maximum output at 5V input)
- On-board voltage regulator with 1.5V output from 3.3V/5.5V input for COREVDD and PLLVDD for the S1D13781
- On-board 16Mbit SPI NOR FLASH standard memory

3 Board Settings

3.1 CNF[2:0] Configuration

The S1D13781 has three configuration inputs, CNF[2:0], which are used to configure the S1D13781 host interface type as described in Table 3-1, *Signal Allocation for Host Interface*.

The S5U13781R00C100 reference board defaults to the SPI interface (the default setting for CNF[2:0] = 111).

Table 3-1 Signal Allocation for Host Interface

S1D13781 Pin name	Direct 16bit Mode 1	Direct 16bit Mode 2	Indirect 16bit Mode 1	Indirect 16bit Mode 2	Direct 8bit	Indirect 8bit	SPI
CNF[2:0]	000	001	010	011	100	101	111
CS#	CS#	CS#	CS#	CS#	CS#	CS#	SCS#
WR#	WR#	RDU#	WR#	RDU#	WR#	WR#	SCK
RD#	RD#	RDL#	RD#	RDL#	RD#	RD#	H
UB#	UB#	WRU#	UB#	WRU#	H	H	H
LB#	LB#	WRL#	LB#	WRL#	H	H	H
AB0	TE	TE	TE	TE	AB0	TE	TE
AB1	AB1	AB1	P/C#	P/C#	AB1	P/C#	Low
AB[18:2]	AB[18:2]	AB[18:2]	Low	Low	AB[18:2]	Low	Low
DB0	DB0	DB0	DB0	DB0	DB0	DB0	SI
DB1	DB1	DB1	DB1	DB1	DB1	DB1	SO
DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	L
DB8	DB8	DB8	DB8	DB8	TE	L	L
DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	L	L	L

Notes:

"H" means direct connection to IOVDD

"L" means direct connection to GND

"Low" means internal pull-down for address bus active

TE is determined by REG[22h] Display Settings Register bits 6-5

3.2 Jumper setting

The S5U13781R00C100 reference board includes jumpers which control the functions described in Table 3-2, *Jumper settings*. For jumper locations on the reference board, see Figure 3-1, *Jumper Pin Locations*.

Table 3-2 Jumper Settings

Function	Jumper Settings	Description
Power supply for FLASH memory	J1 1-2 2 3	Supply VDDIO to U2(FLASH-VCC) External power supply to U2（FLASH-VCC） GND
CNF/RESET setting	J2 1-2 3-4 5-6 7-8	CNF0 Short: CNF0=0, Open: CNF0=1 CNF1 Short: CNF1=0, Open: CNF1=1 CNF2 Short: CNF2=0, Open: CNF2=1 RESET Short: RESET=0, Open: RESET=1
Setting for back light LED regulator	J3 1-2 3-4 5-6 7-8	Short: Enables regulator Short: Regulator output current +20mA Regulator output current +20mA Regulator output current +20mA
Power supply for VDDIO / VDDDCDC	J4 3 4	External power supply to VDDIO External power supply to VDDDCDC
On board OSC setting	J6 1-2	Short: Disable on board OSC
On board OSC input	J7 1	External clock input in case of OSC disable

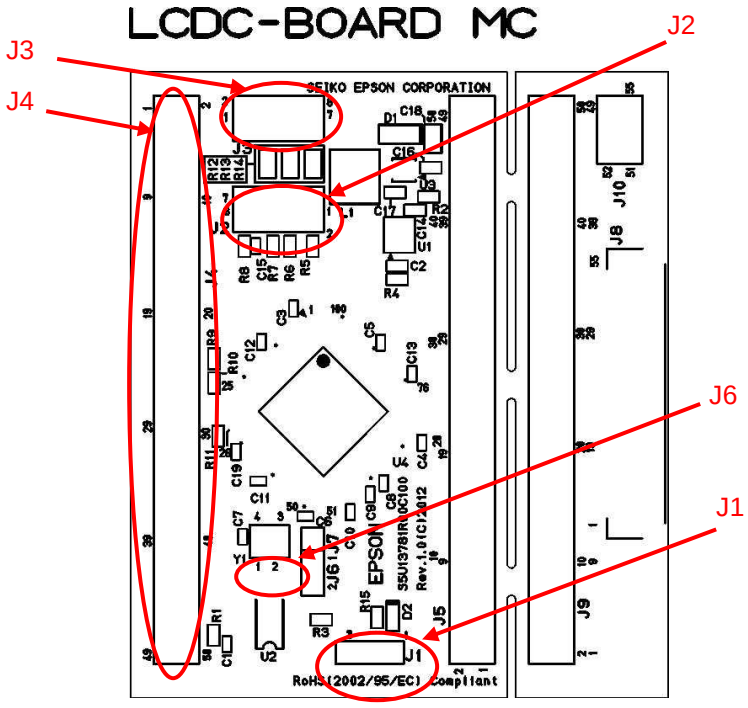

Figure 3-1 Jumper Pin Locations

3.3 Power Supply

The S5U13781R00C100 reference board is designed to supply VDDCORE (1.5V) and LED back light power (LED+/LED-) from the 2.7V to 5.5V input of J4-4 (VDD DCDC).

The voltage output of 2.7V to 3.3V from J4-3 (VDDIO) is used for the U4 (S1D13781 Display Controller) power supply, D2 (LED indicator) and Y1(SG-310SCF 24MHz OSC).

The power for U2 (M25P-16-VMN6P SPI flash memory) is supplied via J1-2 (FLASH-VCC).

3.3.1 VDDCORE

VDDCORE (1.5V) is generated from U1 (BU15TD3WG Voltage regulator) and is used to supply power to COREVDD and PLLVDD of U4 (S1D13781 Display Controller).

3.3.2 LED Back Light LED+/LED- Power Supply

The LED back light power supply (Maximum voltage between LED+ and LED- is 38V) is generated by U3 (TPS61161A voltage booster).

The output current is set by J3 as described in Table 3-2, *Jumper Settings*. Connecting one of J3 3-4, J3 5-6 or J3 7-8 allows 20mA, connecting any two of them allows 40mA and connecting all of them allows 60mA output, maximum.

Table 3-3 Power Supply for S5U13781R00C100

Power Supply	Usage	Voltage Range
VDDIO	Input IOVDD for U4 (S1D13781 Display Controller) Power supply for Y1 （SG-310SCF 24MHz OSC） Power supply for D2(SML-E12M8WT86 LED)	2.7V ～ 3.6V
VDDDCDC	Input Power supply for U1 (BU15TD3WG 1.5V LDO regulator） Power supply for U3(TPS61161A voltage booster)	2.7V ～ 5.5V
FLASH-VCC	Input Power supply for U2(M25P16-VMN6P SP Ⅰ flash memory	2.7V ～ 3.6V
VDDCORE	Output COREVDD and PLLVDD for U4 (S1D13781 LCD controller)	1.5V (Fixed)
LED+ / LED-	Output LED back light power supply	VDDDCDC ～ 38V

Note: Do not short the power supply pins to any other pins.

4 Connectors

The S5U13781R00C100 reference board has via for host interface and panel interface connectors (J4, J5, J8, J9 and J10).

To locate of these connectors on the reference board, see Figure 4-1, *Reference Board Connector Locations*.

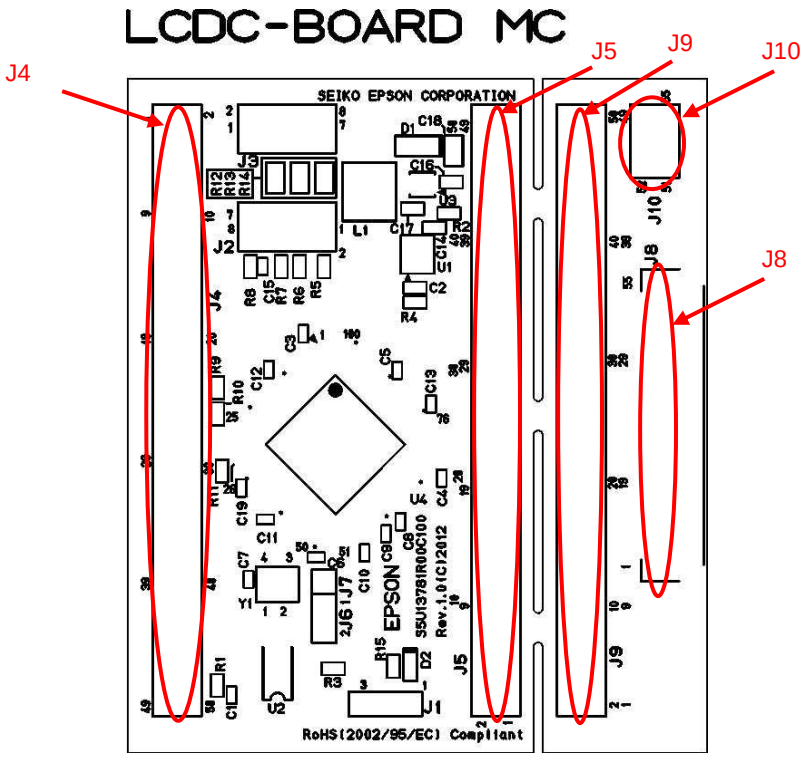

Figure 4-1 Reference Board Connector Locations

4.1 J4 Host Interface Connector

The host interface pins of S1D13781 are connected to J4 of the S5U13781R00C100 reference board. See Figure 7-1, *S5U13781R00C100 Schematic Diagram (1 of 2)*, and Figure 7-2, *S5U13781R00C100 Schematic Diagram (2 of 2)*, for detailed pin allocation.

4.2 J5 Panel Interface Connector

The panel interface pins of the S1D13781 are connected to J5 of the S5U13781R00C100 reference board. See Figure 7-1, *S5U13781R00C100 Schematic Diagram (1 of 2)*, and Figure 7-2, *S5U13781R00C100 Schematic Diagram (2 of 2)*, for detailed pin allocation.

4.3 J8 ～ J9 Connectors for Panel Connection

J8 through J10 on the S5U13781R00C100 reference board are standard connectors used to implement suitable connection for various LCD panels.

J8 is a 0.5mm pitch FPC connector (FH28-55S, bottom electrode type). See Figure 7-1, *S5U13781R00C100 Schematic Diagram (1 of 2)*, and Figure 7-2, *S5U13781R00C100 Schematic Diagram (2 of 2)*, for detailed pin allocation.

5 Others

5.1 Quartz-Crystal Resonator for CLKI

S5U13781R00C100 reference board includes Y1 (SG-310SCF 24MHz oscillator) for the CLKI input of the S1D13781.

The output of the oscillator is disabled by connecting J6 1-2 and enabled by disconnecting.

5.2 SPI flash memory

The S5U13781R00C100 reference board includes SPI NOR FLASH standard memory of 16Mbit capacity. It can be used as external image data storage for the S1D13781.

6 Parts list

Table 6-1 S5U13781R00C100 Bill of Materials

No.	Qty	Reference	PKG	Size	Pin	Part	Description	Manufacturer
1	1	U4	TQFP	14.0x14.0x1.7	100	S1D13781	LCD Controller	EPSON
2	1	Y1	3225	3.2x2.5x1.2	4	SG-310SCF	OSC 24MHz	EPSON
3	1	U3	QFN2 x 2	2.1x2.1x0.8	6	TPS61161ADRVT	LED Driver	TI
4	1	U1	SSOP5	3.1x3.0x1.25	5	BU15TD3WG	Regulator LDO	ROHM
5	1	L1	5050	5.0x5.0x2.0	2	VLCF5020T-220MR75-1	Inductor 22uH	TDK
6	1	D1	3516	3.5x1.6.1.0	2	CRS04	SBD	TOSHIBA
7	1	D2	1608	1.6x0.8x0.36	2	SML-E12M8WT86	LED	ROHM
8	1	U2	SO8N 6x5	5.0x6.2x1.75	8	M25P16-VMN6P-ND	SPI NOR-FLASH 16Mb	Micron
9	1	J8	Bottom electrode	32.0x6.5x2.55	55	FH28-55S-0.5SH(05)	FPC Connector 55P	HIROSE
10	1	C18	2125	2.0x1.25x1.25	2	GRM21BB31H105KA12L	Capacitor 1.0uF 50V/JB	MURATA
11	1	C17	1608	1.6x0.8x0.8	2	GRM188B31E105KA75D	Capacitor 1.0uF 25V/JB	MURATA
12	2	C2,C14	1608	1.6x0.8x0.8	2	GRM188B31E474KA75D	Capacitor 0.47uF 25V/JB	MURATA
13	1	C16	1608	1.6x0.8x0.8	2	GRM188B31E224KA87D	Capacitor 0.22uF 25V/JB	MURATA
14	14	C1,C3,C4,C5, C6,C7,C8,C9, C10,C11,C12, C13,C15,C19	1005	1.0x0.5x0.5	2	GRM155B31C104KA87D	Capacitor 0.1uF 16V/JB	MURATA
15	7	R5,R6,R7,R8, R9,R10,R11	1608	1.6x0.8x0.45	2	RK73H1JTTD4702F	Resistor 47K ohm	KOA
16	1	R15	1608	1.6x0.8x0.45	2	RK73H1JTTD3300F	Resistor 330 ohm	KOA
17	3	R12,R13,R14	2125	2.0x1.25x0.5	2	RK73H2ATTD10R0F	Resistor 10 ohm 1%	KOA
18	4	R1,R2,R3,R4	1608	1.6x0.8x0.45	2	RK73Z1JTTD000	Resistor 0 ohm	KOA

7 Schematic Diagram

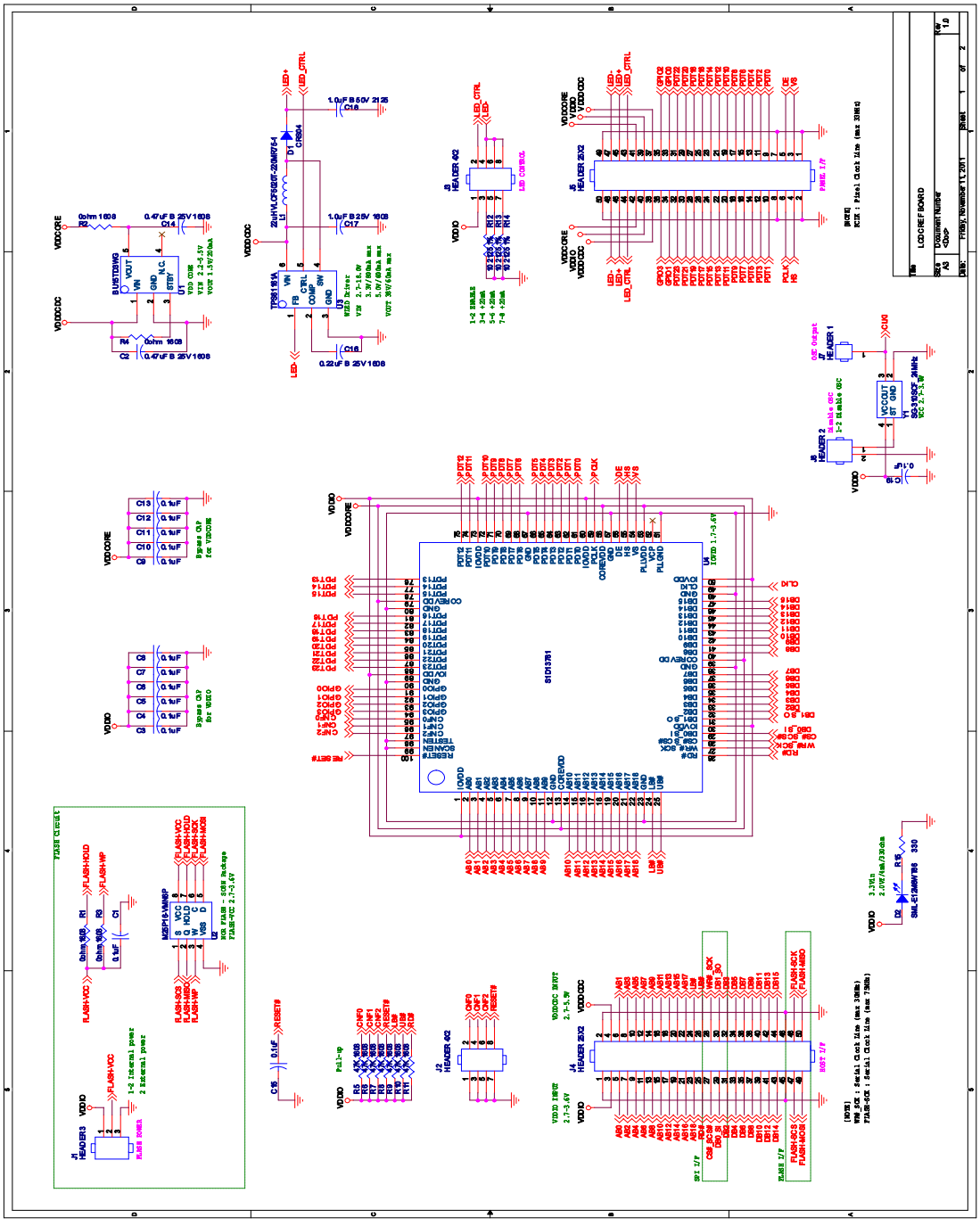

Figure 7-1 S5U13781R00C100 Schematic Diagram (1 of 2)

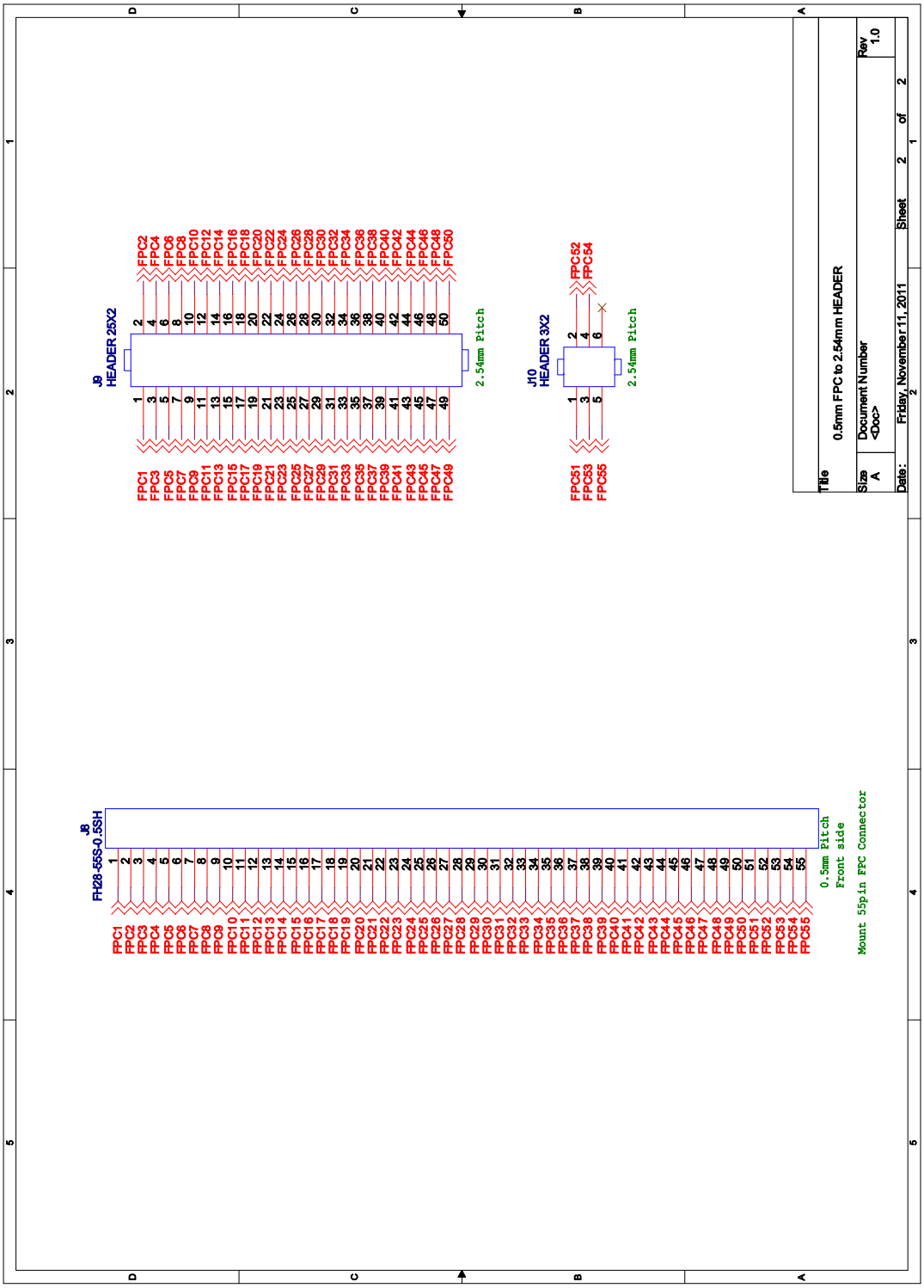

Figure 7-2 S5U13781R00C100 Schematic Diagram (2 of 2)

8 Board Layout and Dimensions

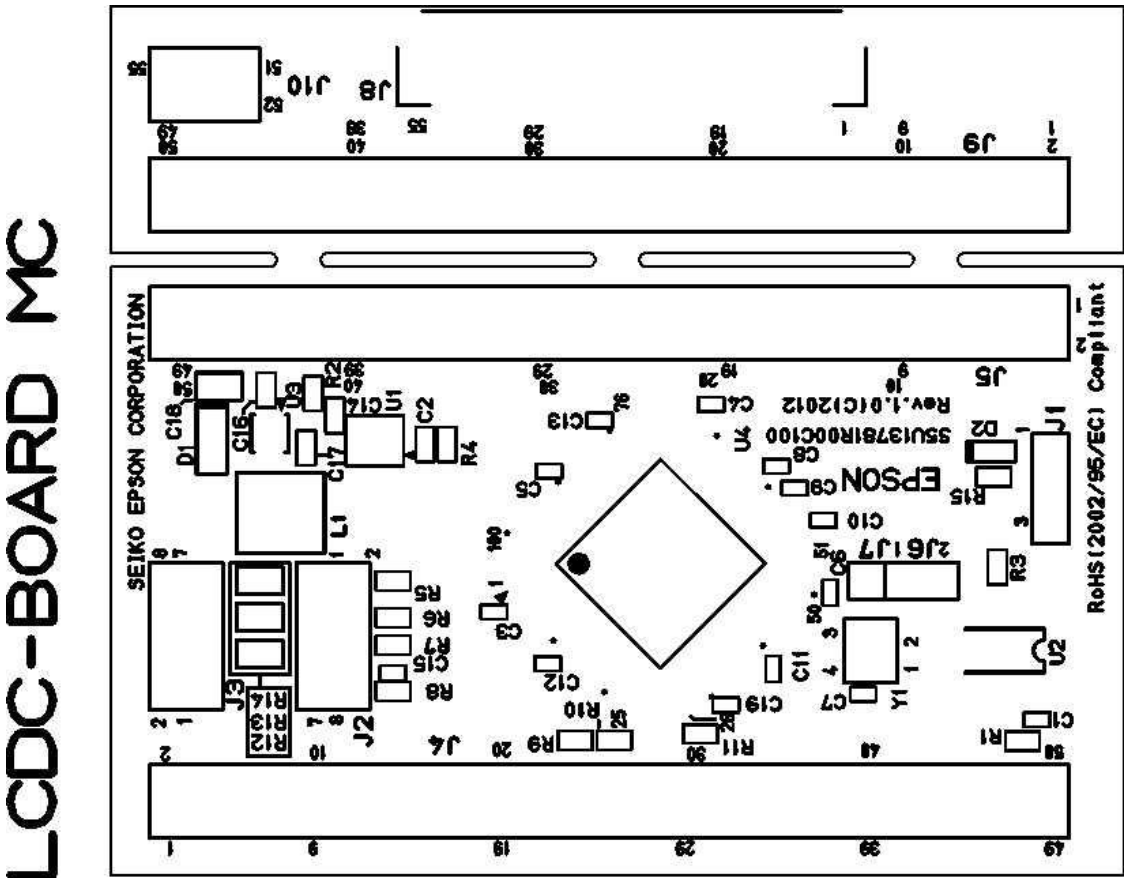

Figure 8-1 S5U13781R00C100 Board Layout Silk Screen

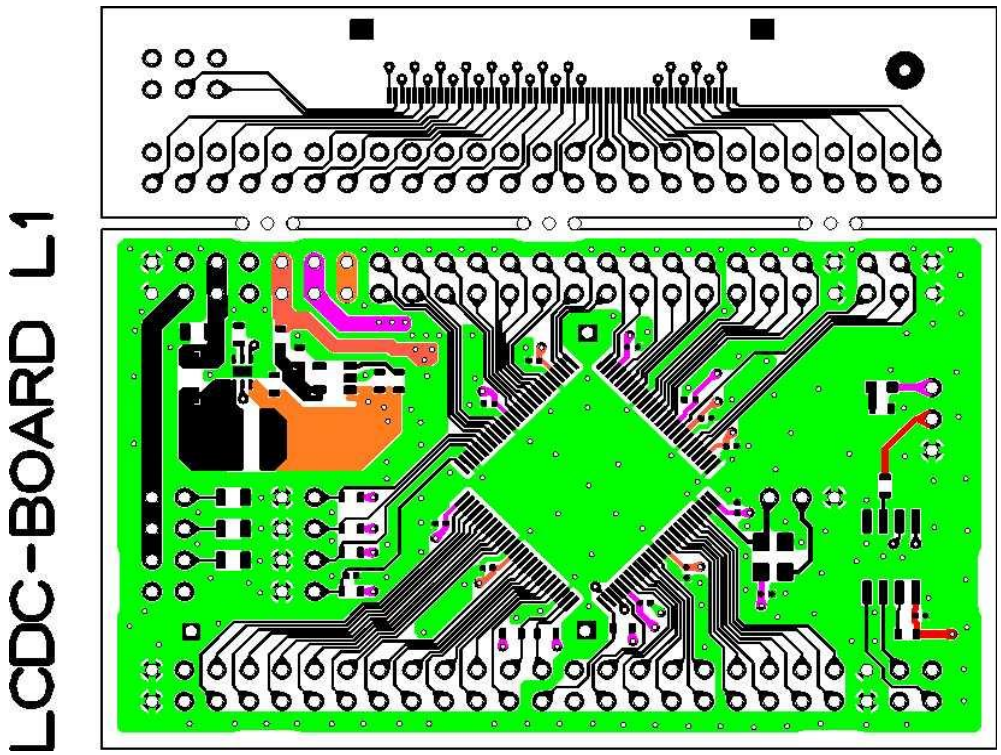

Figure 8-2 S5U13781R00C100 Board Layout Top View

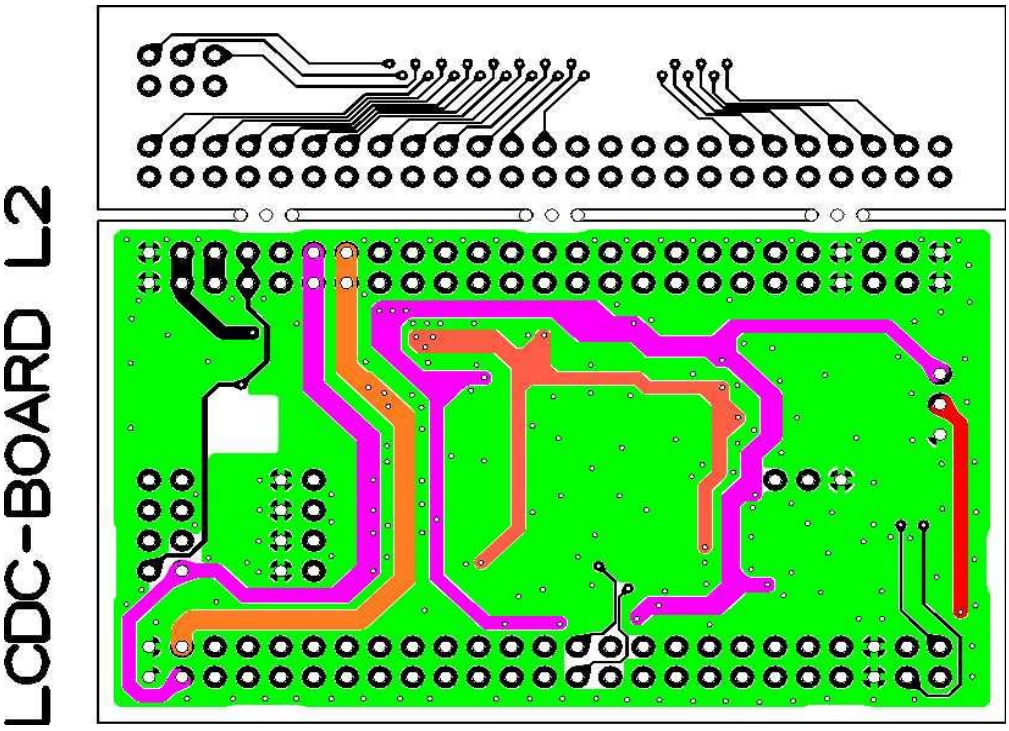

Figure 8-3 S5U13781R00C100 Board Layout Bottom View

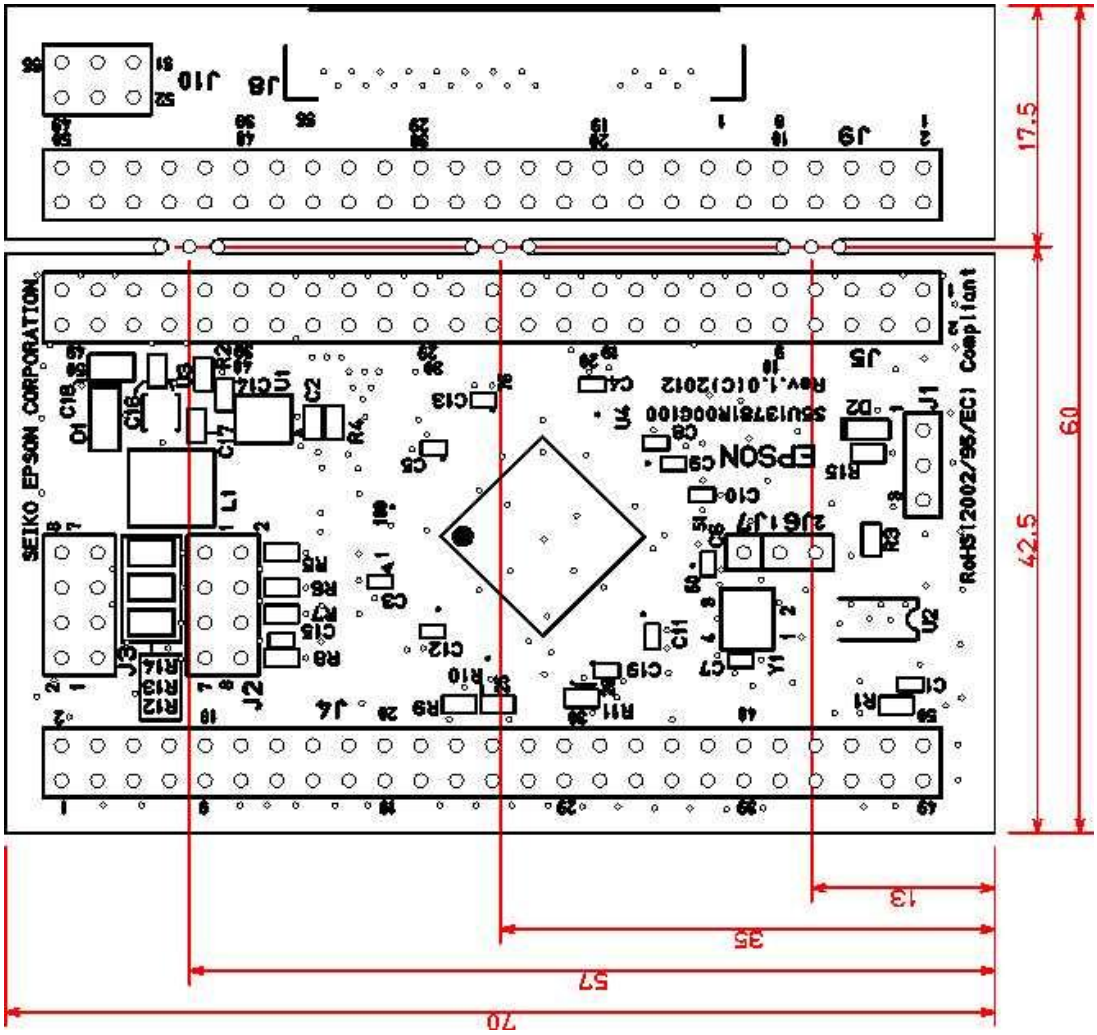

Figure 8-4 S5U13781R00C100 Board Dimensions (units: mm)

9 References

Epson Research and Development, Inc., S1D13781 Hardware Functional Specification, document number X94A-A-001-xx.

10 Change Record

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