DASP-52048

48 Channel DI/O and 1 Timer/Counter Card

User's Manual

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ESD Precautions

Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.

Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.

Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

Trademarks Acknowledgments

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C h a p t e r 1
Introduction

The DASP-52048 is a PCI-bus, 48 TTL digital I/O and one timer/counter card. The DASP-52048 has a higher output current driving capability, allowing it to drive relay or LED elements. The DASP-52048 consists of six 8-bit bi-directional ports and two input lines for interrupt function, with each port allowing users to configure it as inputs or outputs.

Board Identification- Serial Number on EEPROM

The DASP stores the serial number of each DASP in the EEPROM before shipping. The PCI scan utility can scan all the DASP and show users the serial number of each DASP, helping the user to easily identify and access each card during hardware configuration and software programming.

1.1 Features

- **48 digital I/O lines**
- **Higher driving capability than 8255**
- **Output read back status**
- **One 16-bit programmable event counter**
- **One 32-bit programmable timer**
- **Software programmable interrupt handling**
- **Software programmable clock source**
- **Windows® 98/NT/2000/XP and Labview 6.0/7.0 driver**
- **Supported Complete sample program- VB, VC, BCB, Delphi**
- **PCI Scan utility supported**

1.2 Specifications

Digital Inputs

- **Type:** TTL level
- **Input voltage:**
  - High level 2.0V to 5.2V
  - Low level -0.5V to 0.8V
- **Load current:** -0.45mA to +70(A)

Digital Outputs

- **Type:** TTL level
- **Sink Current:** 0.4V@+64mA (Logic level 0)
- **Source current:** 2.4@-15mA (Logic level 1)

Timer/Counter

- **Frequency:** 0 ~ 10 MHz
- **Operation mode:**
  - One 16-bit event counter
  - One 32-bit programmable timer

Interrupt

- **Number:** 2 interrupt source
- **Operation mode:** software programmable

General Environment

- **I/O connector:** 68-pin SCSI-II pin type female
- **Power consumption:** +5V @ 900mA (max.)
- **Operating temperature:** 0 ~ 60°C
- **Storage temperature:** -20 ~ 70°C
- **Humility:** 0 ~ 90% non-condensing
- **Dimensions:** 185mm x 122 mm

1.3 Accessories

To make the DASP-52048 functionality complete, we carry a versatility of accessories for different user's requirements in the following items:

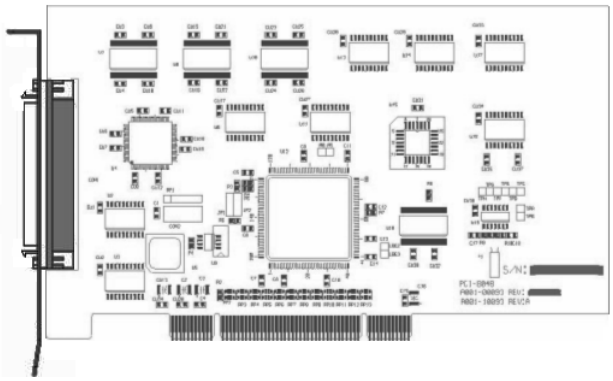
- **Wiring Cable**
  - **CB-89268-2:**
    68-pin SCSI-II pin type male with 2m length
  - **CB-89268-5:**
    68-pin SCSI-II pin type male with 5m length
  - **CB-89468-2:**
    68-Pin SCSI-II (CENTRNIC) to 3-20 Flat 2M Cable
  - **CB-89468-5:**
    68-Pin SCSI-II (CENTRNIC) to 3-20 Flat 5M Cable
- **Terminal Block**
  - **TB-88268:**
    68-pin SCSI-II terminal block with DIN-rail mounting
  - **TB-88320:**
    20-Pin Header Box Male Wiring Terminal Board for DIN-Rail Mounting

The terminal block is directly connected to I/O connector CON1 of the DASP-52048.

- **Daughter Board**
  - **DB-87822:** 16-Channel Isolated D/I Board
  - **DB-87825:** 16-Channel Relay Output Board

Chapter 2
Hardware Installation

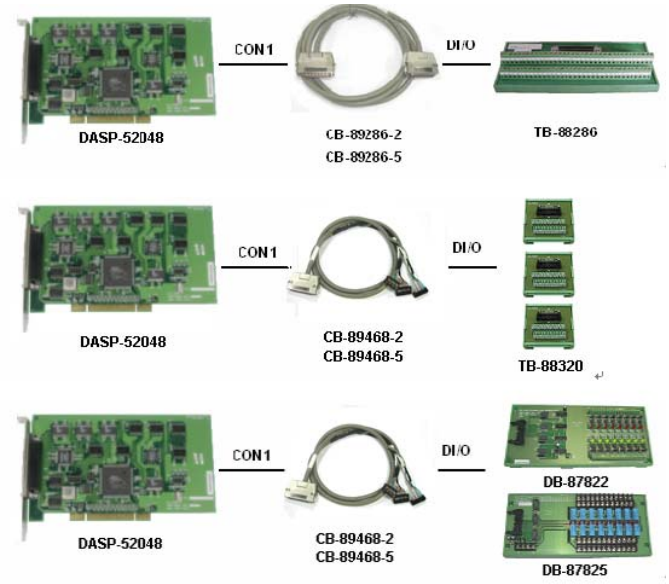
2.1 Board Layout



Board layout for DASP-52048

2.2 Signal Connections

2.2.1 Signal Connection Descriptions

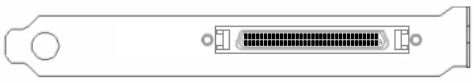


Signal Connections for DASP-52048

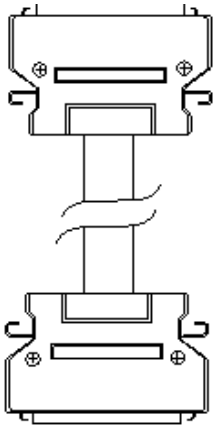
- **CON1:**
  The I/O connector CON1 on the DASP-52048 is a 68-pin SCSI-II pin type connector for digital input/output signals. CON1 enables you to connect to accessories, such as the terminal block TB-88268, with the shielded 68-pin SCSI-II pin type cable CB-89268-2 or CB-89268-5. Another type of accessories, include terminal box with 20-pin header box male connector (TB-88320) and daughter board provides relay out (DB-87825) or photo isolation input (DB-87822) are also provided for signal wiring. A 68-pin SCSI-II (CENTRNIC) to 3-20 flat cable is used associated with these accessories.

2.2.2 Digital Input/Output Connector CON1

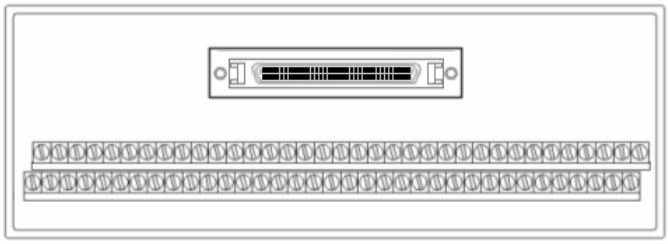
DIO signal connections for DASP-52048 with TB-88268



CON1

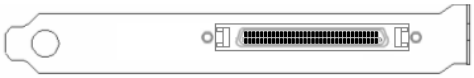


CB-89268

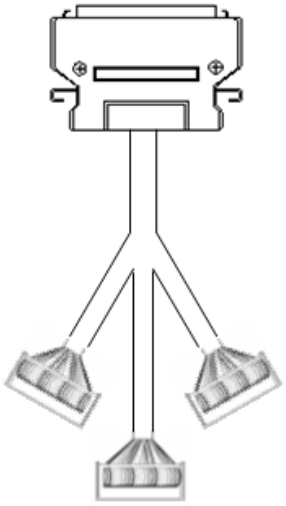


TB-88268

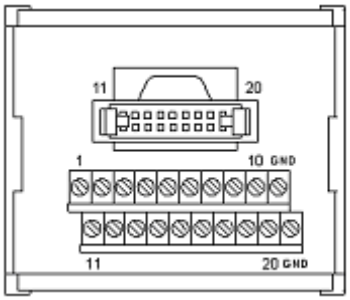
DIO signal connections for DASP-52048 with TB-88320



CON1

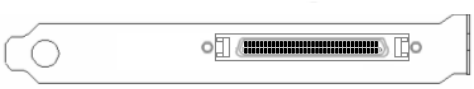


CB-89268

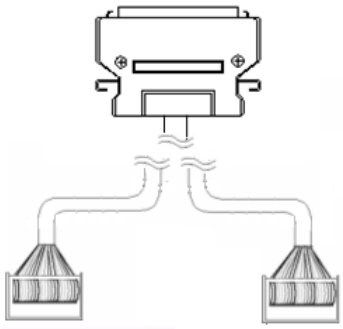


TB-88320

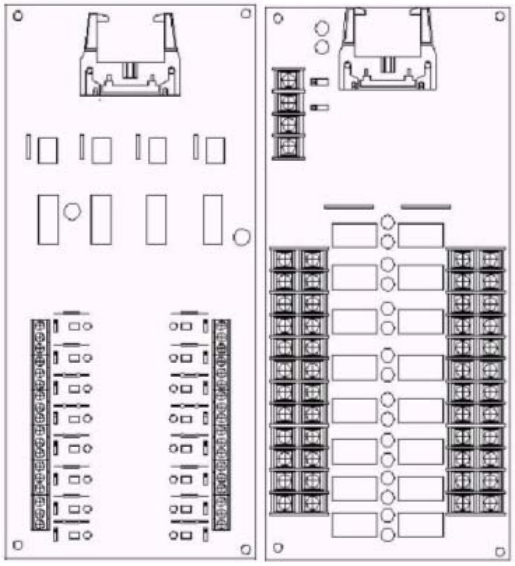
DIO signal connections for DASP-52048 with DB-87822 and DB-87825



CON1



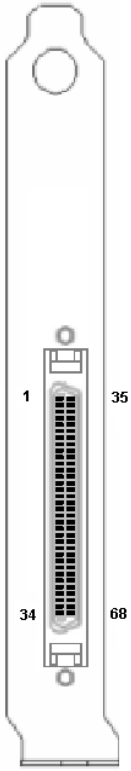
CB-89268



DB-87822 DB-87825

The pin assignment of CON1 of DASP-52048 is listed as follows.

Pin	Description	Pin	Description
1	Ch0 PA D0	35	Ch0 PB D0
2	Ch0 PA D1	36	Ch0 PB D1
3	Ch0 PA D2	37	Ch0 PB D2
4	Ch0 PA D3	38	Ch0 PB D3
5	Ch0 PA D4	39	Ch0 PB D4
6	Ch0 PA D5	40	Ch0 PB D5
7	Ch0 PA D6	41	Ch0 PB D6
8	Ch0 PA D7	42	Ch0 PB D7
9	GND	43	GND
10	+5V	44	+5V
11	Ch0 PC D0	45	Ch1 PC D0
12	Ch0 PC D1	46	Ch1 PC D1
13	Ch0 PC D2	47	Ch1 PC D2
14	Ch0 PC D3	48	Ch1 PC D3
15	Ch0 PC D4	49	Ch1 PC D4
16	Ch0 PC D5	50	Ch1 PC D5
17	Ch0 PC D6	51	Ch1 PC D6
18	Ch0 PC D7	52	Ch1 PC D7
19	GND	53	GND
20	+5V	54	+5V
21	Ch1 PA D0	55	Ch1 PB D0
22	Ch1 PA D1	56	Ch1 PB D1
23	Ch1 PA D2	57	Ch1 PB D2
24	Ch1 PA D3	58	Ch1 PB D3
25	Ch1 PA D4	59	Ch1 PB D4
26	Ch1 PA D5	60	Ch1 PB D5
27	Ch1 PA D6	61	Ch1 PB D6
28	Ch1 PA D7	62	Ch1 PB D7
29	GND	63	GND
30	+5V	64	+5V
31	OSC 4M Hz	65	PCB_CLK
32	82c54 Out0	66	82c54 Out2
33	GND	67	GND
34	+5V	68	+12V

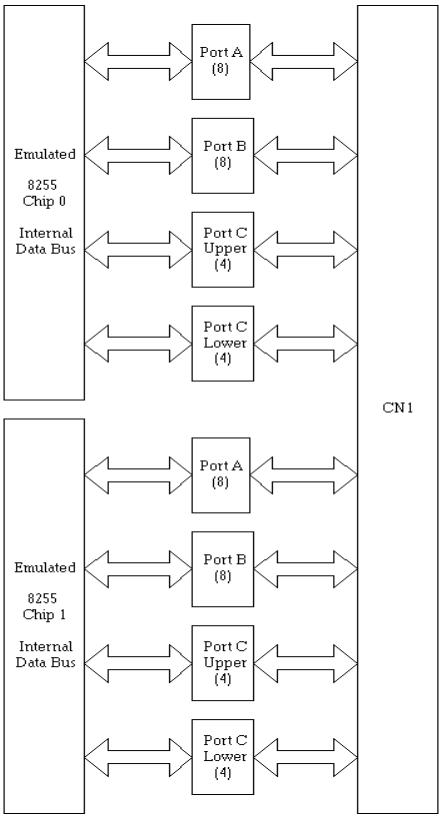


2.3 DI/DO Circuits and Wiring

The TTL digital input and digital output wiring diagrams and functional block diagrams of DASP-52048 are depicted as following figure. The port A and port B of each channel can be configured as input or output ports. The upper nibble or lower nibble of port C can be configured as input or output separately.

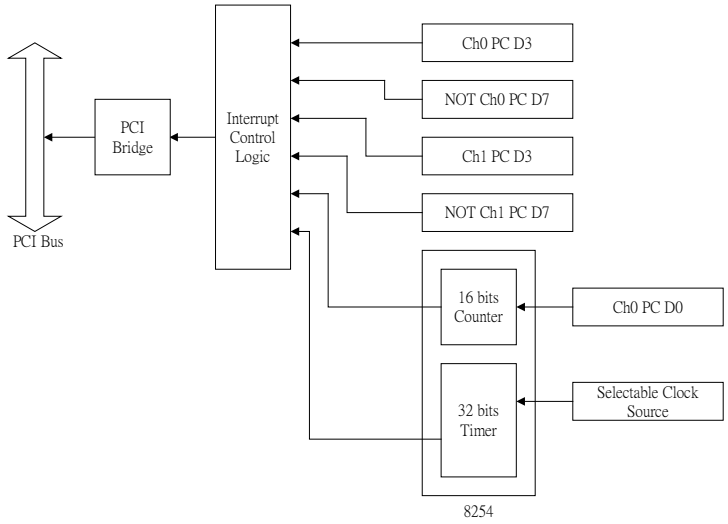
2.3.1 Emulate 8255 I/O Port

The DASP-52048 emulates 2 channels 8255 in mode 0(basic input/output) and has a increased output current of 15mA (source) or 64mA (sink), allowing it to drive LED, relay, etc.



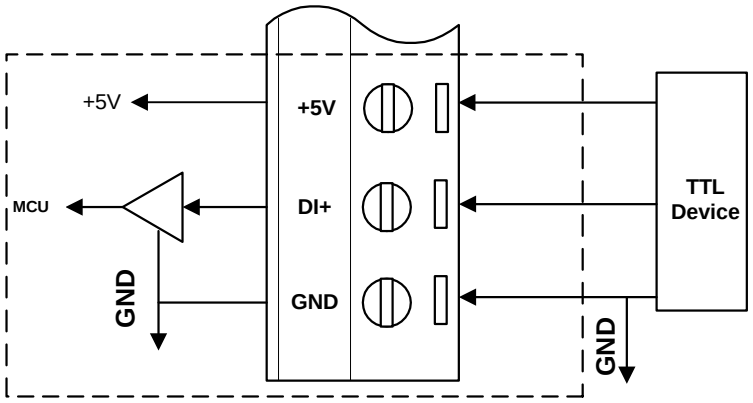
2.3.2 Interrupt Function

The DASP-52048 provides 6 interrupt modes and 4 timer interrupt clock sources. The interrupt function block diagram is given below.



2.3.3 Digital Input Port Circuits and Wiring

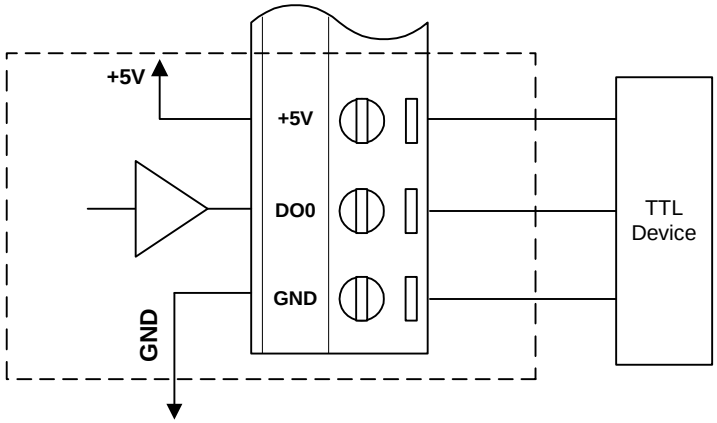
There are up to 48 digital input channels on DASP-52048 board. The following figure demonstrates the circuit configuration of digital input port. The basic layout and wiring is presented as below.



Block Diagram of Internal Circuits and Wiring of TTL Digital Input for DASP-52048

2.3.4 Digital Output Port Circuits and Wiring

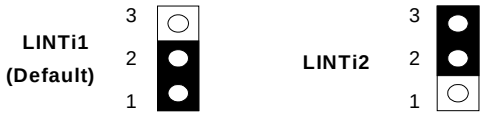
There are up to 48 digital output channels on DASP-52048 board. The following figure demonstrates the circuit configuration. The basic layout is presented as below.



Block Diagram of Internal Circuits and Wiring of TTL Digital Output for DASP-52048

2.3.5 Jumper Settings

JP2 PCI Bus Interrupt Setting



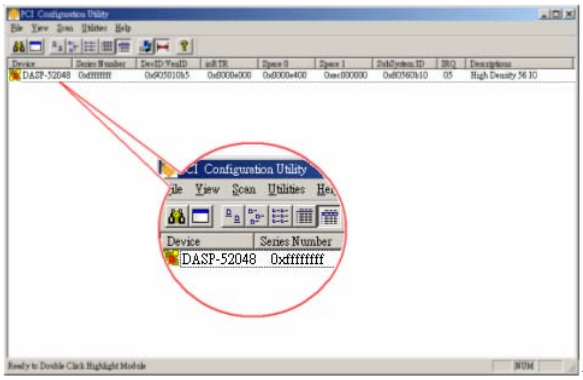
PCI Interrupt (JP2)

2.4 Quick Setup and Test

To install a new DASP-52048 into an IBM PC compatible computer, at first, power-off the PC and open its chassis, then plug the DASP-52048 into a PCI slot of mother-board of the PC. The DASP-52048 is a plug and play device for MS Windows, and the OS will detect your DASP-52048 after you power on the PC. The detail of driver and software installation is described in software manual of DASP-52048.

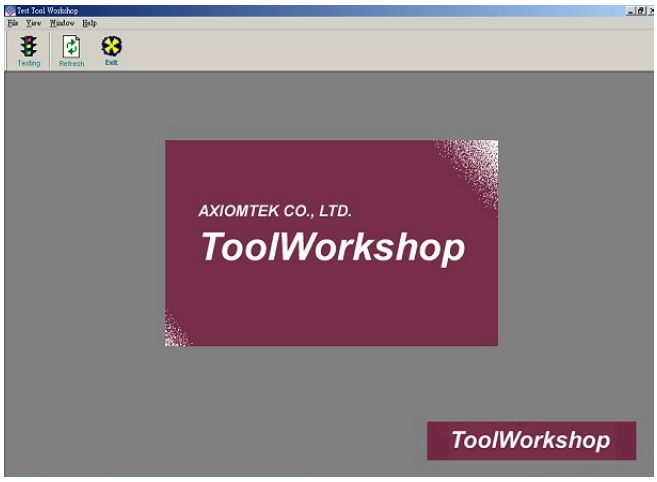
After the hardware and software installation, user can emulate and test DASP-52048 step by step as follows.

- To perform a complete test of DASP-52048, we can route the output channels to the input channels of DASP-52048 directly for read-back, for instance, configure chip 0 port A as output channels and configure chip 0 port B as input channels. And then, by following the DASP-52048 test branch of the *ToolWorkShop* which will fully test all the digital I/O channels of the DASP-52048 as descried in the following paragraphs.
- Launch the '*PCI Configuration Utility*' of DASP-52000 series to ensure that the resource of DASP-52048 is properly dispatched by the OS. Press the *scan* button in the toolbar of the '*PCI Configuration Utility*' to find the installed DASP-52048, and then check the resource list as following figure.

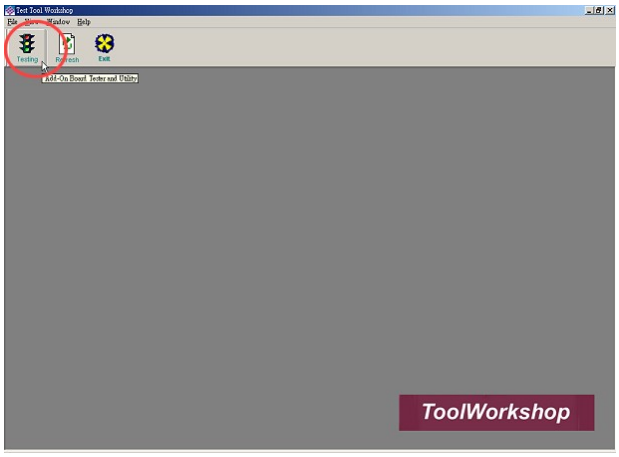


Scan DASP-52048 with PCI Configuration Utility and Check the Dispatched Resource

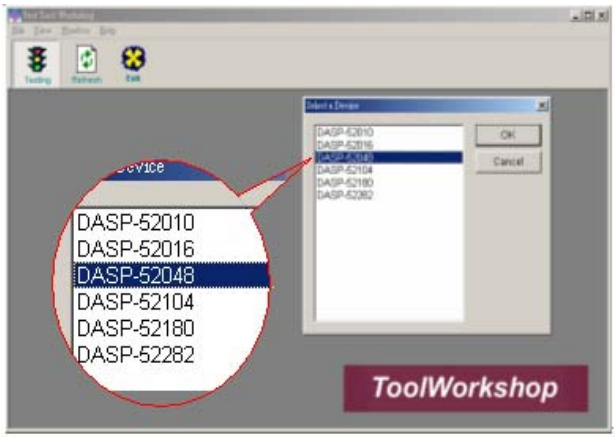
- Exit the '*PCI Configuration Utility*' and launch the '*ToolWorkShop*' for DASP-52048. As shown following figure. Select DASP-52048 as the test target as shown as follows.

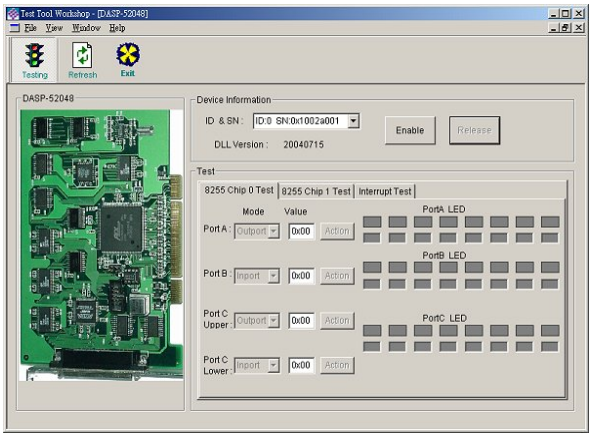


Launch ToolWorkShop



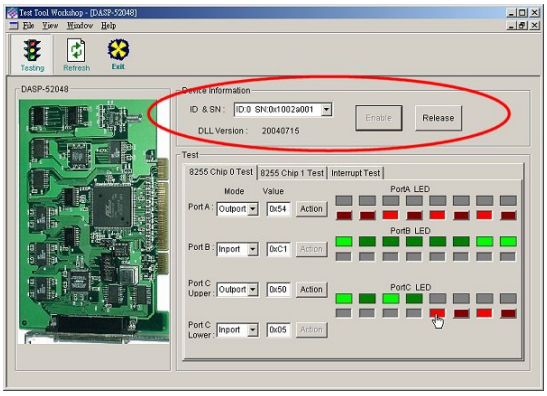
Select Board Test





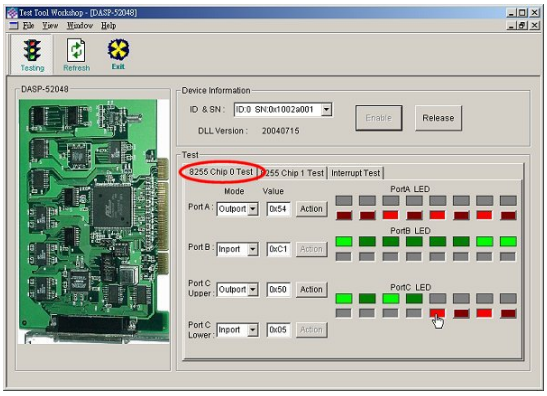
Select Test Target: DASP52048

- Perform DIO test of DASP-52048 as shown in following figure. At first, check the device information and press ***'Enable'*** button to load DASP-52048 library shown as follows.



Check Device Information and Press 'Setup' Button to Load DASP-52048 Library

- At first, configure selected ports as digital input and digital output respectively, for instance, configure port A of chip 0 as input and configure port B of chip 0 as output. Then, writes 0x0ffffff to turn on all the digital output channels of chip 0 port A, and then press the ***'Action'*** button related to it to send the digital output port value to DASP-52048. Then, verify the digital input value presented in the DI/O test panel of '*TOOLWORKSHOP*' for DASP-52048.



Perform Digital Input/Output Test by Set the DO Port Value and Read Back the DI Port Value of DASP-52048

- Before exiting '*ToolWorkShop*', press ***'Release'*** button to release DASP-52048 library.

C h a p t e r 3
Register Structure and Format

3.1 Overview

The DASP-52048 occupies 24 consecutive I/O addresses. The address of each register is defined as the board's base address plus an offset. The I/O registers and their corresponding functions are listed in the followings.

Address	Read	Write
Base + 0	8255 ch0 port A	8255 ch0 port A
Base + 1	8255 ch0 port B	8255 ch0 port B
Base + 2	8255 ch0 port C	8255 ch0 port C
Base + 3	Reserved	8255 ch0 control word
Base + 4	8255 ch1 port A	8255 ch1 port A
Base + 5	8255 ch1 port B	8255 ch1 port B
Base + 6	8255 ch1 port B	8255 ch1 port B
Base + 7	Reserved	8255 ch1 control word
Base + 8	Reserved	Software interrupt trigger
Base + 9	Reserved	Clear interrupt
Base + 10	Reserved	Select CLK and INT source
Base + 11	Read Device label	Reserved
Base + 12	82c54 Counter 0	82c54 Counter 0
Base + 13	82c54 Counter 1	82c54 Counter 1
Base + 14	82c54 Counter 2	82c54 Counter 2
Base + 15	Reserved	82c54 control word

3.1.1 Read/Write 8255 Chip0 Input/Output Port A, B and C (Base Address + Offset 0x00-02)

D7	D6	D5	D4	D3	D2	D1	D0
8 bit Input/Output Data							

3.1.2 Write 8255 Chip 0 Control Word (Base Address + Offset 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	CA	CCU	0	CB	CCL

- **CA**
  Port A input/output control, 1: Input, 2: Output
- **CCU**
  Port C upper 4 bits input/output control,
  1: Input, 2: Output
- **CB**
  Port B input/output control,1: Input, 2: Output
- **CCL**
  Port C lower 4 bits input/output control,
  1: Input, 2: Output

3.1.3 Read/Write 8255 Chip1 Input/Output Port A, B and C (Base Address + Offset 0x04-06)

D7	D6	D5	D4	D3	D2	D1	D0
8 bit Input/Output Data							

Please refer to base address + 0 – 2

3.1.4 Write 8255 Chip 1 Control Word (Base Address + Offset 0x07)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	CA	CCU	0	CB	CCL

Please refer to base address + 3

3.1.5 Write Soft Interrupt Trigger (Base Address + Offset 0x08)

D7	D6	D5	D4	D3	D2	D1	D0
Writ any value to trigger interrupt							

3.1.6 Write Clear Interrupt (Base Address + Offset 0x09)

D7	D6	D5	D4	D3	D2	D1	D0
Write any value to clear interrupt							

3.1.7 Write Clock and Interrupt Source Selection (Base Address + Offset 0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	CS1	CS0	TE	IntrS2	IntrS1	IntrS0

- **TE**
  Trigger edge selection
  0: Falling edge trigger, 1: Rising edge trigger
- **Interrupt Source Selection:**

IntrS2	IntrS1	IntrS0	Mode	Interrupt Function
0	0	0	0	8255 Chip0 D0
0	0	1	1	Timer Trigger
0	1	0	2	Chip0 D3
0	1	1	3	NOT Chip0 D7
1	0	0	4	Chip1 D3
1	0	1	5	NOT Chip1 D7
1	1	0	6	Soft Trigger
1	1	1	7	Disable Interrupt

- **Clock Source Selection:**

CS1	CS0	Function
0	0	32.768KHz (RTC)
0	1	0.5MHz
1	0	1MHz
1	1	2MHz

3.1.8 Read Device Label (Base Address + Offset 0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
Device Label: 0x0F							

3.1.9 Read/Write 82c54 Counter 0 – 2 (Base Address + Offset 0x0C-0E)

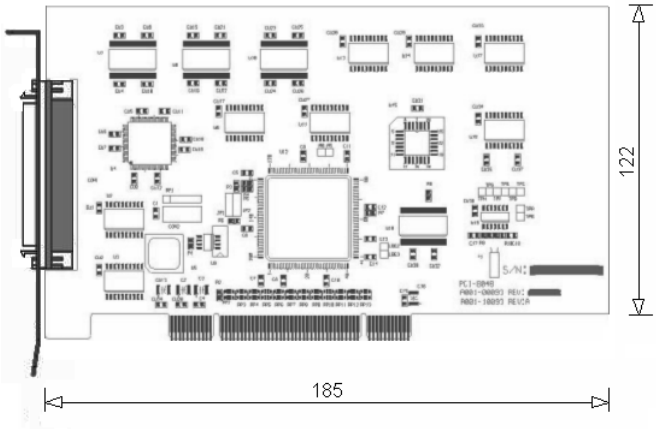
D7	D6	D5	D4	D3	D2	D1	D0
8 bit counter value							

3.1.10 Write 82c54 Counter Control Word (Base Address + Offset 0x0F)

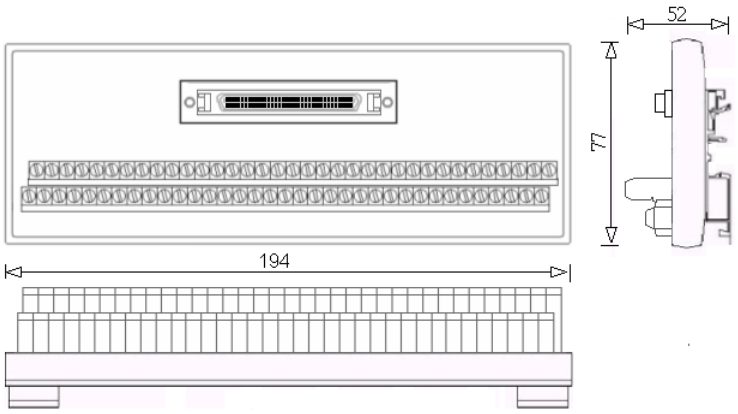
D7	D6	D5	D4	D3	D2	D1	D0
8 bit 82c54 control word							

Appendix A
Dimension of DASP-52048 and Accessories

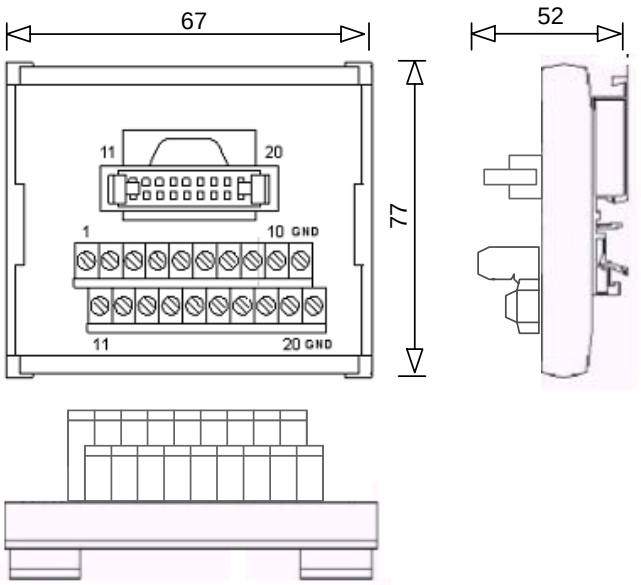
- **DASP-52048**



- **TB-88268**



- **TB-88320**



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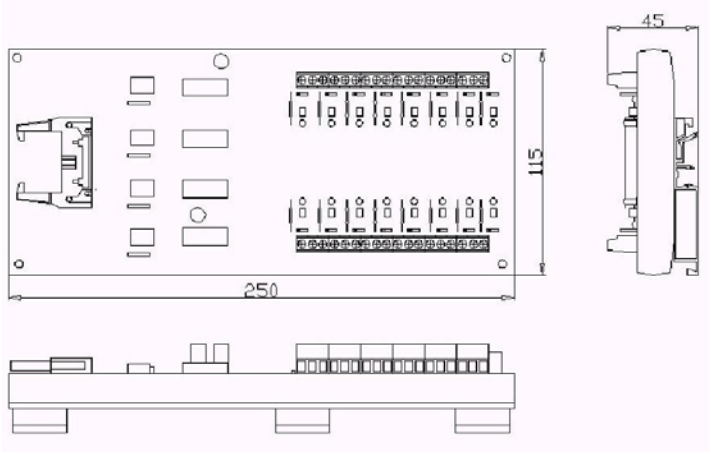

- **DB-87825**