Sauna Technical Note #9-01

Converting $R_{junction\text{-}to\text{-}ambient}$ To $R_{junction\text{-}to\text{-}case}$ For Quad Flat Pack IC Packages

Introduction

The Quad Flat Pack (QFP) package is a widely-used IC package for surface mount circuit boards (see Figure 1). Frequently, these QFP semiconductors dissipate one or more watts. At these wattage levels, it becomes necessary to perform a careful thermal analysis to insure that junction temperatures are not excessive.

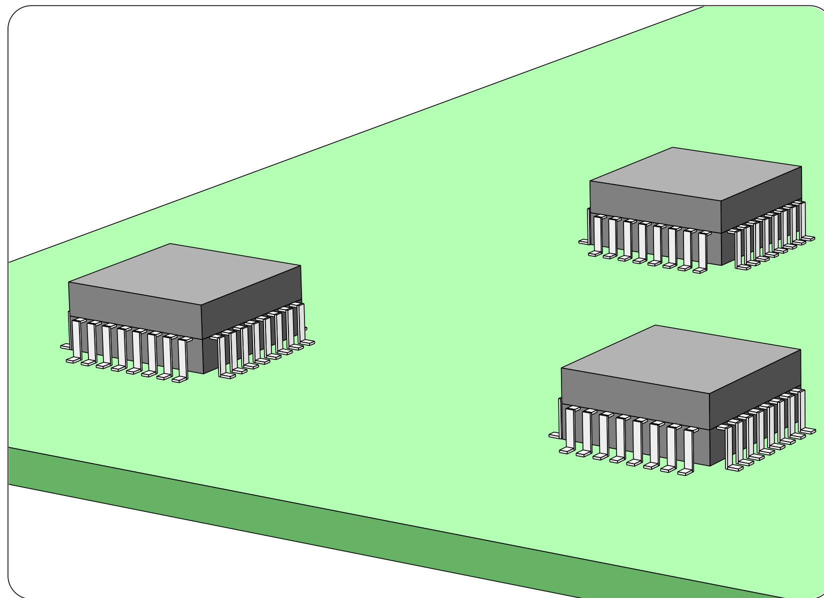

Figure 1: Quad flat pack IC's on circuit board

The most commonly used thermal rating for QFP IC's is the junction-to-ambient thermal resistance, or $\mathbf{R}_{j\text{-}a}$ (also referred to as $\Theta_{j\text{-}a}$). However, since the heat dissipation of a QFP IC is strongly linked to the copper characteristics of the circuit board, $\mathbf{R}_{j\text{-}a}$ is not very meaningful unless the engineer knows the copper properties of the circuit board used to obtain $\mathbf{R}_{j\text{-}a}$. So it is vitally important that the engineer obtain the characteristics of the manufacturer's test board. Once the test board characteristics are available, it becomes possible to reverse-engineer the $\mathbf{R}_{j\text{-}a}$ number to obtain a junction-to-case thermal resistance. The junction-to-case thermal resistance ($\mathbf{R}_{j\text{-}c}$, also referred to as $\Theta_{j\text{-}c}$) can then be used with Sauna.

This technical note explains the JEDEC and SEMI standards for test boards. If the IC manufacturer has rated the IC according to these standards, you will have sufficient information to reverse-engineer the $\mathbf{R}_{j\text{-}a}$ number and obtain a $\mathbf{R}_{j\text{-}c}$. This technical note includes a step-by-step example problem.

JEDEC and SEMI standards

In the past, $\mathbf{R}_{j\text{-}a}$ numbers provided by manufacturers were not particularly reliable because there was a great deal of variation in test circuit boards and methods. However, over the last few years there has been a strong standardization effort made by the JEDEC JC-15.1 committee, resulting in JEDEC Standards 51-3 (Low Effective Thermal Conductivity Test Board For Leaded Surface Mount Packages) and JEDEC Standard 51-7 (High Effective Thermal Conductivity Test Board For Leaded Surface Mount Packages). Many manufactures now test in accordance with these standards. These standards can be downloaded at no charge from *www.jedec.org*.

Besides the JEDEC standards, there is also a standard from the SEMI organization: SEMI G42-0996 (Specification For Thermal Test Board Standardization For Measuring Junction-To-Ambient Thermal Resistance Of Semiconductor Packages). This standard can be downloaded from *www.semi.org* for a $50 fee. The SEMI standard specifies both a single layer and four layer board. Also, the SEMI standard describe test boards for other package styles, such as DIP's and PGA's. In fact, this is one of the major flaws of the standard. It simply covers too much material and lacks detail.

The JEDEC and SEMI standards are similar but not identical. You will need to know which standard was used to generate $\mathbf{R}_{j\text{-}a}$ for a particular component. Thermal Solutions believes that the JEDEC standards are superior because there is a more complete specification of the test board. Also, the JEDEC spec seems to be gaining in popularity and the standard can be downloaded at no cost. For this reason, this technical note is based on the JEDEC standards. However, you should be aware that the SEMI standard is still used by a number of manufacturers.

Heat transfer in a QFP semiconductor

Before going any further, it's a good idea to review heat flow inside a Quad Flat Pack IC. Figure 2 shows a cross-section of a typical QFP (no thermal enhancements):

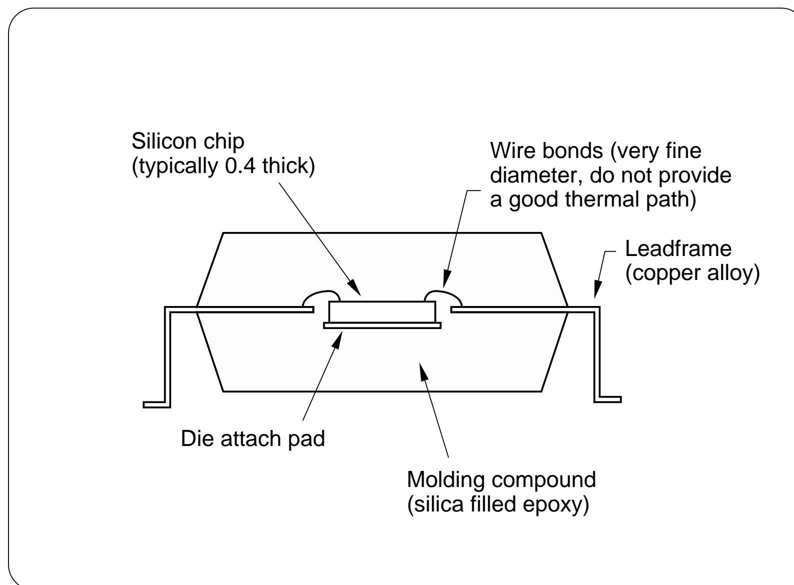

Figure 2: Cross-section of quad flat pack (not thermally enhanced)

Heat is generated in the silicon chip. There are basically three paths for the heat: (1) upwards through the molding compound and out to the environment, (2) downward through the molding compound and air gap to reach the circuit board and (3) through the copper leadframe to reach the circuit board. The first two paths are of limited value because of the low thermal conductivity of the molding compound. (Molding compound has better thermal conductivity than standard epoxy, but it's still a relatively poor thermal conductor.) Also, heat which flows up from the chip will be limited by the small amount of dissipating surface area available on the top of the package.

This leaves the third heat flow path: the copper leadframe. (The term leadframe refers to the ensemble of leads which flare out from the silicon chip, initially these leads are all formed from a single piece of metal.) Most heat will leave the package through the leads for two reasons. First, the leads have high thermal conductivity. Second, the leads are soldered to copper traces on the circuit board which provides additional dissipating surface area. This is the key item to remember: **most of the heat leaves the QFP package through the leads**.

While the copper leadframe has high thermal conductivity, there is an important barrier in this heat flow path. Because the wire bonds are of very small diameter, there is an appreciable thermal resistance between the silicon and the edge of the leadframe. Because the bond wires are so small, heat is forced to conduct through a section of molding compound.

Since there is an appreciable thermal barrier between the chip and leadframe, some packages are enhanced to reduce this resistance. As a typical example, consider the QFP package shown in Figure 3. In this case a copper "heat spreader" has been added below the silicon chip. In this package, the primary chip-to-leadframe heat flow path is through heat spreader. It is still necessary to conduct heat through the molding compound but the conduction cross-sectional area is greater. (Heat can cross that gap between the heat spreader and leadframe over a relatively wide area.) It's important to remember that a heat spreader functions by reducing the chip-to-leadframe thermal resistance. With or without a heat spreader, most of the heat still leaves a QFP package through the leads.

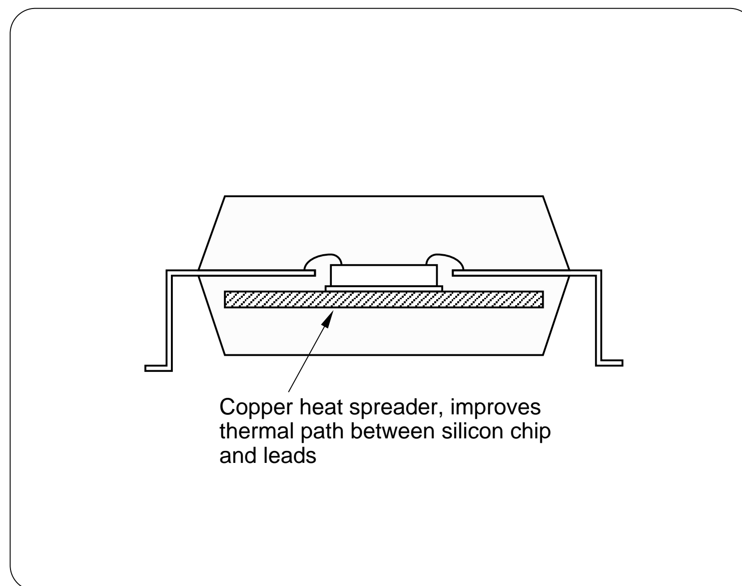

Figure 3: Cross-section of thermally enhanced Quad Flat Pack

Besides the heat spreader approach shown in Figure 3, there is another class of thermally enhanced QFP. This type of enhanced package is known as the "thermal lead" package. In this package, the die attach pad (see Figure 2) is integral with several of the leads in the leadframe (typically ground leads). So certain leads on the package have a very low junction-to-lead thermal resistance while the remaining leads have a normal (high) thermal resistance. The thermal lead package is most commonly seen in DIP style packages, rather than QFP's. Most TO-220 packages are thermal lead packages because one of the leads is part of the same piece of copper plate as the mounting flange. This technical note does not cover the modeling of QFP's with thermal leads. If you need help with this subject, please contact Technical Support.

This concludes the brief discussion of heat transfer in QFP packages. For more information, you may wish to download this document:

www.amkor.com/assembly_and_test/Services/Package_Characterization/thermal/files/elcool.pdf

This article was written by Bruce Guenin of Amkor and gives further details on the subject, with a number of informative illustrations.

The JEDEC test boards

Before going further, you should go to *www.jedec.org/DOWNLOAD/default_stds.htm* and download JESD51-3 (single layer test board) and JESD51-7 (four layer test board). You should also download JESD51-2 (natural convection test procedure) and JESD51-6 (forced convection test procedure).

Spend some time reading these standards. This technical note gives an overview of the standards but it's no substitute for reading the standards themselves.

Figure 4 on the next page shows an example of the test board for a QFP with a body size of 7 mm x 7 mm. The component under test is mounted at the center of a 76.2 x 76.2 square on the end of the board opposite from the edge connector.

For the 51-3 board, the board is single sided with 2 ounce copper.

For the 51-7 board, a four layer board is used. The two internal planes are solid and the back side traces are left undefined. The component and back side plating is 2 ounce copper. The internal planes are 1 ounce copper.

For large QFP's, body size ≥ 27 mm x 27 mm, the test board becomes larger. The board width becomes 101.6 while retaining the same height of 114.3. The component is mounted at the center of a 101.6 x 101.6 square, opposite from the edge connector.

The component side traces flare out uniformly to reach a square which is 50 mm larger than the body dimension. Since the test board in Figure 4 is based on a 32 lead QFP with a 7 mm body dimension, the leads flare out to reach a 57 mm square. Outside of the 57 mm square, the traces are left undefined. If desired, a company can route traces down to the edge connector, but the traces must stay clear of the flareout area. It is also legal to connect jumper wires between the vias and the edge connector area.

Note the copper coverage on the board. Immediately adjacent to the component, the copper coverage is usually around 50%. For the 7 mm component shown in Figure 4, the lead pitch is 0.8 mm and the trace width is 0.25. This is a copper coverage of 0.25/0.8 = 31%. However, most QFP's have much higher lead counts and will have copper coverage close to 50%.

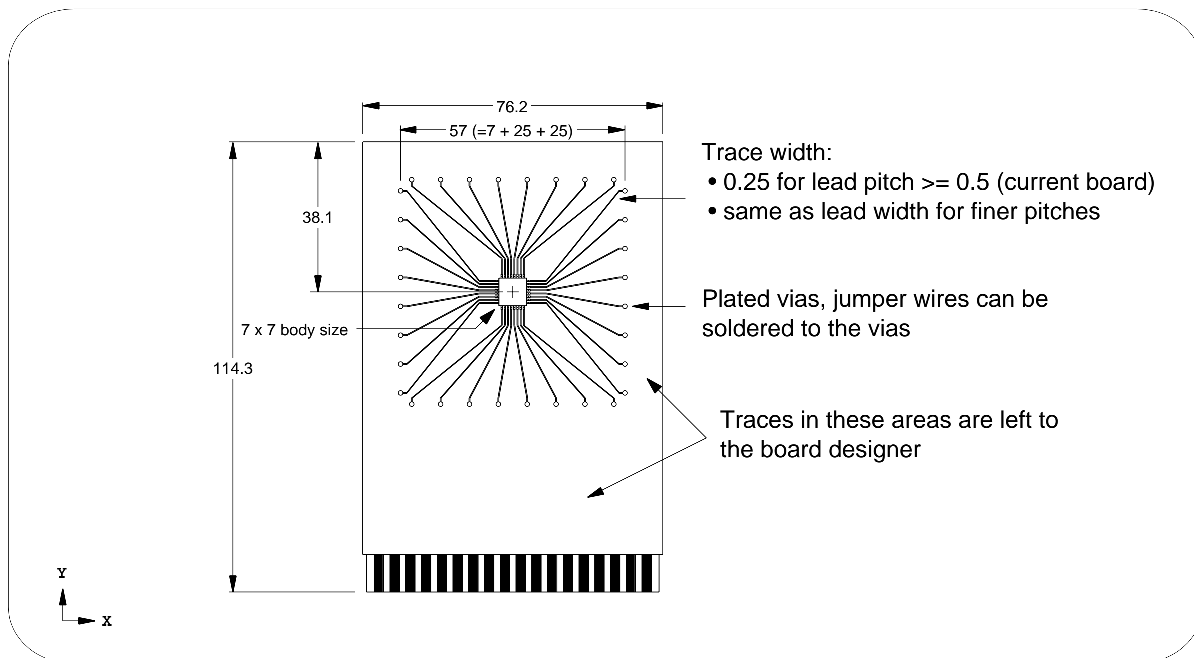

Figure 4: Component side traces for QFP with 7 mm body dimension, 0.8 mm lead pitch

At the edge of the flareout square, the copper coverage is (8 x 0.25) / 57 = 3.5%. Once again, most QFP's have higher lead counts and will have increased copper density at the edge of the flareout area. The average copper coverage for the flareout square can be approximated by taking the average of the maximum coverage (next to component) and minimum coverage (edge of flareout). For the board shown in Figure 4, the average copper coverage is (31 + 3.5)/2 = 17.25%.

When you read the standard, be sure to note that the test board is not 100% defined. In particular, be sure to look at Figure 6 in the 51-7 standard. This trace pattern allows for testing components of different size and lead count on the same test board. However, for smaller components the leads do not flare out in the same way as a pattern designed for just that chip size. However, the standard states that this type of test board is legal. Another area of ambiguity is the thickness of the laminate layers in the 51-7 standard. The A dimension in Figure 1 of the standard is specified to be $0.25 \leq A \leq 0.50$. It is strange indeed that this dimension was not specified exactly. But still, all things considered, these standards are a great improvement over the past situation.

Reverse-engineering to obtain junction-to-case resistance

Now it's time to convert all this information into something usable for Sauna. This technical note give the procedure for modeling the QFP as a footprint heat source. An even better approach is to model the QFP as a stackup, but that is left to *Technical Note #10 - An Equivalent Stackup Model Of A Quad Flat Pack IC*.

Here's an overview of the procedure to follow (an example problem is given later):

1. Create a model of the JEDEC test board. If you have data for both the single layer and four layer board, it is preferable to model the four layer board because this board is less

dependent on the details of the component side traces, which can vary from manufacturer to manufacturer. You do not need to model the entire board, only the 76.2 x 76.2 square which contains the QFP and flareout. For QFP's with a body size which is 27 mm or larger, you should model the 101.6 mm x 101.6 mm square containing the QFP and flareout.

As specified by the 51-2 standard, the circuit board should be horizontal.

2. Place a special footprint heat source at the appropriate location. Initially, the $\mathbf{R}_{j\text{-}c}$ should be 0.01°C/W. **The footprint area is defined by the limits of the leads (tip-to-tip dimension), not the body.**

3. Add float resistors.

4. Calculate temperatures for natural cooling @25°C.

5. You should obtain a junction temperature which is less than the value obtained using the manufacturer's $\mathbf{R}_{j\text{-}a}$. Your junction temperature is less because you assumed an $\mathbf{R}_{j\text{-}c}$ of 0.01°C/W, which is obviously too small.

Calculate the $\mathbf{R}_{j\text{-}c}$ which will produce the correct junction temperature.

6. Edit the $\mathbf{R}_{j\text{-}c}$ of the footprint heat source to use the new value. (For the Sauna model, the case temperature represents the average QFP lead temperature.)

7. Calculate temperatures to verify that the correct junction temperature is obtained.

8. If possible, calculate temperature for forced convection to verify that the correct temperatures will be obtained.

When these steps are completed, you can use the footprint heat source with your Sauna model.

Sample problem - preparations

For the sample problem, you will model a 144 lead QFP with a 20 mm x 20 mm body size. The overall (tip-to-tip) dimension is 22 mm x 22 mm, which includes the lead foot.

The $\mathbf{R}_{junction\text{-}to\text{-}ambient}$ data for a low profile QFP is as follows:

	Still Air $\mathbf{R}_{j\text{-}a}$ (°C/W)	**200 fpm** $\mathbf{R}_{j\text{-}a}$ (°C/W)	**500 fpm** $\mathbf{R}_{j\text{-}a}$ (°C/W)
Single layer JEDEC board	38.0	31.2	28.1
Four layer JEDEC board	31.7	26.9	24.9

The $\mathbf{R}_{j\text{-}a}$ data was obtained from the Amkor Technology website:

www.amkor.com/assembly_and_test/products/quad/lqfp/Data_Seet/lqfp.pdf

Amkor Technology is a manufacturer of semiconductor packages. There's quite a bit of useful information on their website.

As mentioned above, you will not model the entire circuit board. Instead, you will simply model the 76.2 x 76.2 portion which contains the QFP and lead flareout. Since the flareout is included to provide uniform test results from test board to test board, it is presumed that the board temperature will be close to the ambient temperature at the edge of the flareout region. Also, the standards really don't define the traces outside the flareout. It's rather difficult to model something which isn't defined. So it is recommended that only the flareout portion of the board is modeled.

You need to obtain the copper coverage. This part has a lead pitch of 0.5 mm, so the trace width is 0.25 mm. Next to the QFP, the copper coverage is 0.25/0.50 = 50%. The flareout square is 20 + 50 = 70 mm x 70 mm. Since there are 36 leads on a side, the copper density is 36 (0.25)/70 = 12.86%. The average copper coverage = (.5 + .1286)/2 = 31.4%.

Now you are ready to model the test board.

Modeling the single layer board

You will start with the single layer board:

1. Create a horizontal circuit board:

Model → Assembly → Circuit Brd → "One layer" → Horizontal → "76.2,76.2" → .062"/1.6mm → (0,0,0) → G10 Epx/Gls → One → Two Oz → Prompt → "31.4"

2. Switch to a top orthogonal view.

3. The required footprint size is 484 mm^2 (22 mm x 22 mm). To obtain exactly this footprint size, you need to slice to create an assembly which is exactly 484 mm^2. Perform a 2 Point slice:

Edit → Plate/Board → Subdivide → 2 Pt Slice → No Priority → Coords/Trap → "27.1,0,-27.1" → Coords Trap → "49.1,0,-49.1" → All In Wind → USE

4. Now you are ready to place the footprint source which represents the QFP. You should use the wattage which was used when generating $\mathbf{R}_{j\text{-}a}$. For the current example, the Amkor data specifies that $\mathbf{R}_{j\text{-}a}$ is based on $\mathbf{q}$ = 1 watt. Initially you will be using $\mathbf{R}_{junction\text{-}to\text{-}case}$ = 0.01°C/W and $\mathbf{R}_{case\text{-}to\text{-}sink}$ = 0.01°C/W. (Later on you will increase $\mathbf{R}_{j\text{-}c}$ to match the numbers on the data sheet.)

Model → Heat Input → Footprint → "1" → ".01" → "QFP-144" → Special → "484" → <Enter> → Enter Rth → ".01" → One → trap left edge of center assembly → Digitize → digitize at the center of the board

The heat source should be created at the center of the board. There should be 4 case-to-sink resistors between the heat source and the board.

If you were modeling a smaller QFP, there wouldn't be 4 case-to-sink resistors. In this case, you should re-mesh to obtain 4 case-to-sink resistors.

5. Switch to a front orthogonal view.

6. Add float resistors on both sides of the board (be sure to use the "Enter Later" dissipation mode):

Model → Amb + Float → Isoltd->Fix → "Room Amb" → Enter Later → Both Sides → All In Wind → USE

7. Turn off fixed nodes.

8. Calculate temperature for natural cooling at a 25°C ambient. You should obtain T_j = 48.95°C.

9. The manufacturer specifies an $\mathbf{R}_{j\text{-}a}$ of 38.0°C/W for natural cooling. So you should have obtained T_j = 25 + (1) 38.0 = 63.0°C, which is 14.05°C higher than the value obtained with your model. So you need to increase your $\mathbf{R}_{j\text{-}c}$ from 0.01°C/W to 14.06°C/W. Make this change:

Edit → Heat Input → Footprint → Junct/Case → trap the heat source → "14.06"

10. Recalculate temperatures for natural cooling @25C. Now you should obtain T_j = 63.00°C, which matches the T_j calculated using the manufacturer's $\mathbf{R}_{j\text{-}a}$.

11. Save the model as QFP144_1_lyr.smf

File → Save As → "QFP144_1_lyr.smf" → click on Save button (hit <Enter> for HPUX version)

12. Now let's try calculating temperature with 200 fpm forced convection:

Analyze → Calc Temps → Steady → Forced Air → Feet/Minute → 200 → "25"

You should obtain T_j = 55.59°C. With the $\mathbf{R}_{j\text{-}a}$ from Amkor, you would obtain 56.2°C, so there is good agreement.

13. Finally, calculate temperatures with 500 fpm:

Steady → Forced Air → Feet/Minute → 500 → "25"

You should obtain T_j = 52.99°C, in close agreement with Amkor's number of 53.1°C.

As you have just seen, it's really quite easy to simulate the QFP on the single layer test board. Next, you will simulate the QFP on the four layer board. If everything works properly, there will be good agreement in the $\mathbf{R}_{\text{junction-to-case}}$ obtained for the single layer and four layer test boards.

Four layer test board - preparations

Modeling the single layer test board was easy. It's a bit more difficult to create the four layer board. **As a prerequisite, you should have worked through *Intermediate Exercise 3: More On Layer By Layer Board Models*.**

If you look at Figure 1 in Standard 51-7, you will see that the laminate thicknesses are not rigidly defined. As mentioned earlier, this is really an unnecessary flaw in the standard. The

"A dimension", which is the thickness of the outer laminate (prepreg) layers, is given as ranging from 0.25 mm to 0.50 mm.

Thermal Solutions recommends that you use an "A dimension" of 0.010" = 0.254 mm. This is a very common laminate thickness and is likely to be chosen by many manufacturers. Also, this "A dimension" is reasonably close to the value specified by the SEMI G42-0996 standard (0.2 mm). This is convenient because there will undoubtedly be some manufacturers that conclude that a SEMI G42-0996 board is "close enough" to be considered a JEDEC board (see discussion below). So you will be using the laminate thicknesses shown in Figure 5. Since the outer layers are 0.010, the middle laminate layer will be 0.031" (0.787 mm).

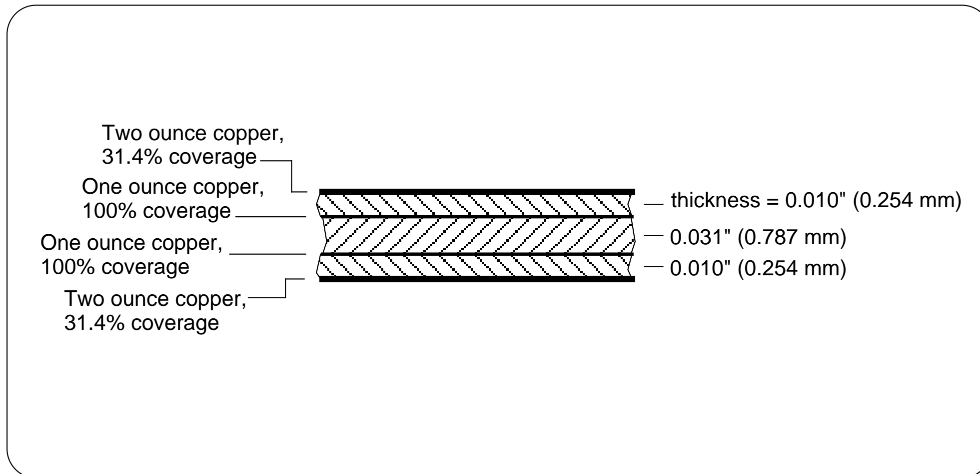

Figure 5: Thicknesses for four layer test board

Modeling the four layer test board

Now you are ready to create the four layer board. (Note that you will be following the checklist on page 3-28 of the Sauna User Manual.) Do the following:

1. Delete the existing model (it was saved earlier).

2. Use **Visibility → Turn On → All** to make all elements visible.

3. If necessary, switch to a front orthogonal view.

4. For a four layer board, you will create four board assemblies which are 0.0155" (.3937 mm) thick. (You may wish to refer to the checklist on page 3-28 of the Sauna user manual.) Create the first layer:

Model → Assembly → Circuit Brd → "Layer>1" → Horizontal → "76.2,76.2" → .016"/0.4mm → (0,0,0) → G10Epx/Gls → One → One oz. → 100%

This board assembly has the proper properties for the inner layers (1 oz copper, 100% coverage).

5. Zoom in on the left corner of the board.

6. Use "Copy" to create three additional board assemblies:

Move/Copy → Copy → Three → Trap 1 Assy → trap board → Trap Dy → trap lower edge of board → trap upper edge of board

7. Now you need to change the copper coverage for the top and bottom layer. The top layer coverage was calculated as 31.4%. You don't know what the bottom layer coverage is, so just assume that it is the same as the top layer.

Edit the copper coverage with:

Edit → Plate/Board → Board Props → Copper → Coverage → Prompt → "31.4" → Entire Brd → place top and bottom boards in group → USE

8. Change the copper weight for the top and bottom layer:

Copper → Weight → Two oz. → place top and bottom boards in group → USE

9. Change the edge area assignment to "100% Component" for the top two layers:

Edit → Plate/Board → Area Params → Edge Area → 100% Comp → place top two layers in group → USE

10. Change the edge area assignment to "100% Secondary" for the bottom two layers.

100% Secdry → place bottom two layers in group → USE

11. Now you need to obtain the layer-to-layer resistance. The thicknesses are as shown in Figure 5. As specified in the standard, there are no vias in the flareout area. Since the via density is zero, you do not need to specify via diameter, plating thickness, etc. when calculating the resistance. You can obtain the unit area resistance with:

<F8 Toolbox> → Cond Rth → Rect Volume → "1,1,.254" → Non-Metal → Circuit Brd → G10Epx/Gls → Screen

You should obtain $\mathbf{R}_{unit}$ = 863.95°C-mm^2/W. This is the interface resistance you will use to join "Layer>1" (bottom layer) to "Layer>2" and to join "Layer>3" to "Layer>4" (top layer).

12. You also need $\mathbf{R}_{unit}$ for the middle laminate layer. Clear the Info report from the screen, then enter:

Rect Volume → "1,1,.787" → Non-Metal → Circuit Brd → G10Epx/Gls → Screen

You should obtain $\mathbf{R}_{unit}$ = 2676.87°C-mm^2/W, which you will use to join "Layer>2" to "Layer>3".

13. Clear the Info report from the screen, then join the layers together:

Model → Join → Stack → Enter Unit → "864" → Grp 2 Assy → place Layer>1 and Layer>2 in group → USE

Stack → Enter Unit → "864" → Grp 2 Assy → place Layer>3 and Layer>4 in group → USE

Stack → Enter Unit → "2677" → Grp 2 Assy → place Layer>2 and Layer>3 in group → USE

14. In a moment, you will save this test board. You will be able to reuse this model the next time you need to obtain a $\mathbf{R}_{\text{junction-to-case}}$ for a QFP.

Before saving, use **<F7 Info> → Trap** to verify that the joins, copper weight, etc. have been modeled correctly.

15. Save the model as "JEDEC51-7.smf":

File → Save As → "JEDEC51-7" → click on Save button (hit <Enter> if using HPUX version)

16. Now that you have created the four layer board, the next few steps are the same as when simulating the single layer board.

Switch to a top orthogonal view.

17. As you did above, slice to obtain an assembly which is exactly 484 mm^2:

Edit → Plate/Board → Subdivide → 2 Pt Slice → X=Con First → Coords/Trap → "27.1,0,-27.1" → Coords Trap → "49.1,0,-49.1" → All In Wind → USE

With the single layer board you used the "No Priority" option. But this time you used "X=Con First". This was done to reduce the number of assemblies so that Sauna Standard users can perform the necessary slicing without exceeding the assembly limit of 25. (In general, models are more accurate if you use "No Priority", but the differences are usually minor.)

18. Now you will place a footprint source on the center assembly of the top layer. In a top, orthogonal view, it's easy to trap the correct assembly because of the 3D trapping priority. As before, you will initially use $\mathbf{R}_{\text{junction-to-case}}$ = 0.01°C/W and $\mathbf{R}_{\text{case-to-sink}}$ = 0.01°C/W:

Model → Heat Input → Footprint → "1" → ".01" → "QFP-144" → Special → "484" → <Enter> → Enter Rth → ".01" → One → trap left edge of center assembly → Digitize → digitize at the center of the board

The heat source should be created at the center of the board with 4 case-to-sink resistors between the heat source and the board. (For smaller footprints, it would be necessary to re-mesh all assemblies to obtain the desired 4 case-to-sink resistors.)

19. Use **<F7 Info> → Heat Input** to verify that the heat source is on the top layer (SA-Layer>4).

20. Switch to a front orthogonal view.

21. Add float resistors on both sides of the board (be sure to use the "Enter Later" dissipation mode):

Model → Amb + Float → Isoltd->Fix → "Room Amb" → Enter Later → Both Sides → All In Wind → USE

22. Verify that there are two fixed nodes above the board and two fixed nodes below the board. To see this , zoom in around the fixed nodes.

23. Turn off fixed nodes.

24. Resize the window with **<F4 Zoom Out>**

25. Calculate temperature for natural cooling at a 25°C ambient. You should obtain T_j = 39.37°C.

26. Amkor specifies a $\mathbf{R}_{j\text{-}a}$ of 31.7°C/W for natural cooling on the four layer board, which translates into an expected T_j of 56.7°C. This is 17.33°C higher than the initial T_j. So you need to increase your $\mathbf{R}_{j\text{-}c}$ from 0.01°C/W to 17.34°C/W. Make this change:

Edit → Heat Input → Footprint → Junct/Case → trap the heat source → "17.34"

Note that the $\mathbf{R}_{j\text{-}c}$ for the four layer test board is 17.34°C/W, while the $\mathbf{R}_{j\text{-}c}$ obtained earlier for the single layer board was 14.06°C/W. The two $\mathbf{R}_{j\text{-}c}$ values are reasonably close. As explained later, it is recommended that you use the $\mathbf{R}_{j\text{-}a}$ associated with the four layer board.

27. Recalculate temperature for natural cooling at 25°C. Now you should obtain the target T_j of 56.70°C.

28. Once again, calculate temperatures for 200 fpm:

Analyze → Calc Temps → Steady → Forced Air → Feet/Minute → 200 → "25"

You should obtain T_j = 51.65°C. With the $\mathbf{R}_{j\text{-}a}$ from Amkor, you would obtain 51.9°C, so there is good agreement.

29. Finally calculate temperatures with 500 fpm:

Steady → Forced Air → Feet/Minute → 500 → "25"

You should obtain T_j = 50.27°C, in close agreement with Amkor's number of 49.9°C.

This completes the analysis of the four layer board. Since you already saved the board model (JEDEC51-7.smf), you can delete the current model.

As you have just seen, it is not particularly difficult to reverse-engineer the $\mathbf{R}_{j\text{-}a}$ for the four layer board. The hardest part was defining the board, but you only have to do that one time. You can use reuse JEDEC51-7.smf whenever analyzing QFP packages. However, you will probably need to change the component side copper coverage to match the component being modeled.

Comparing results for the single layer and four layer board

The above analysis produced $\mathbf{R}_{jc\text{-}1\ layer}$ = 14.06°C/W and $\mathbf{R}_{jc\text{-}4\ layer}$ = 17.34°C/W. At first glance, this seems to be very good agreement. However, the actual discrepancy between the two values is around 20%. Fortunately, this will only translate into a few degress change in junction temperature.

In general, **the four layer result should be considered more accurate.** With the four layer board, the board conductivity is dominated by the internal planes. The results are not overly sensitive to the copper coverage on the component side. The single layer board conductivity is more sensitive to the details of the component side traces, and these traces are not rigidly defined by

the standard. Consequently, you shouldn't average the one layer board and four layer board results. Instead, just use the four layer $\mathbf{R}_{j\text{-}c}$.

If you are in a hurry and don't want to simulate both the single layer and four layer board, just simulate the four layer board. You won't always have a choice, sometimes data is only provided for one of the boards.

Differences between JEDEC board and SEMI board

Here's a list of the differences between the JEDEC board and the SEMI board:

1. The JEDEC board is larger for QFP body sizes ≥ 27 mm x 27 mm.

2. The component side trace width for the JEDEC board is 0.25 mm for lead pitches of 0.5 mm or greater. For finer pitches, the trace width is equal to the lead width. On the SEMI board, the trace width varies from 0.15 mm trace width for a 0.3 mm lead pitch, up to a trace width of 0.35 mm for a 0.65 mm lead pitch.

3. The plating weight for the component (flareout) side is 2 oz. for the JEDEC board and 1 oz. for the SEMI board. For the four layer JEDEC board, backside weight is 2 oz. Internal planes for both boards are 1 ounce copper.

   As described to Thermal Solutions by a JEDEC committee member, the 2 oz. plating was chosen so that the initial plating will be 1 ounce, which will then build up to 2 oz. when the via holes are plated. Interestingly enough, this person's opinion was that many SEMI boards actually had 2 oz. plating thickness for this very same reason, meaning that these boards are not compliant.

4. The four layer board described in the SEMI standard has different laminate (prepreg) thicknesses.

5. The position of the component is different for the two standards.

6. The internal planes of the SEMI four layer board cover the entire board, excluding the edge connector area. For the JEDEC board, the internal planes are restricted to a 76.2 x 76.2 square or 101.6 x 101.6 mm square, depending on package size (the internal planes are specified as slightly smaller, 74.2 x 74.2 or 99.6 x 99.6).

So, as you can see, the test boards are similar but not identical. The most significant difference is that the JEDEC board is larger for body size greater than 27 x 27. For the single layer board, the copper weight difference is significant provided that the SEMI board is truly compliant (see #3 above). Also, note that the internal planes cover nearly all of the SEMI four layer board, not just a 76.2 x 76.2 square.

As an engineer, you will want to find out which test board was used to generate $\mathbf{R}_{j\text{-}a}$. If you are unable to find out, it is recommended that you assume that the JEDEC four layer board was used. Then apply a safety factor.

An improved QFP model - the equivalent stackup

In the above example, you modeled the QFP as a footprint heat source. To obtain a more accurate model, you can also represent the QFP as a stackup. This is described in *Technical Note #10 - An Equivalent Stackup Model Of A Quad Flat Pack IC*. The equivalent stackup is not difficult to create and you don't need to know exact die size, die bond method or other internal parameters. All the required information can be obtained from a standard data sheet.

The equivalent stackup model has these advantages:

- mass of the QFP is defined
- QFP contributes additional surface area (unlike a footprint heat source)
- more accurate description of the heat flow path through the leads
- includes a heat flow path out through the top of the component
- provides a way to model surface mount parts which have leads on only two sides
- in shade mode, component stackup is visible

The big disadvantage of the equivalent stackup model is that a number of assemblies are created, causing problems for Sauna Standard users. **Sauna Standard users must represent QFP packages with footprint heat sources**.

This concludes this technical note. If there are questions, please contact Technical Support. ◆

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