# ProceV™


Preliminary Data Book

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# 1.0 Scope

The purpose of this data book is to provide architectural, hardware and installation information for the ***ProceV***™ system.

This data book is organized in the following chapters:

**Introduction** – Board description and purpose.

**Key Features** – Main features and performance.

**Standard Models** – Standard product models available.

**Architecture** – Board architecture, components**,** busses and clocks**.**

**DMA Controller** – DMA operation and performance.

**Connectors** – Board connectors' description and pin-out.

**Memories** – Memory structure.

**LEDs** – LEDs functions.

**Technical Specifications** - Electrical, mechanical and other technical specifications.

**Installation** – Requirements and installation instructions.

**GIDEL Accessories** – GiDEL management software and IPs.

**Appendix** – Additional information.

**References** – List of referenced documents.

**Glossary –** Term definitions and acronyms.

**Revision History –** Board and document revision history.

# 2.0 Introduction

The ***ProceV***™ system provides a high-capacity, high-speed FPGA-based platform along with 16+GB of memory with ~20GB/s sustain access rate. The combination of high-speed direct communication to the FPGA via PCIe gen 3, CXP, SFP+, RJ45 and General Purpose physical layer interface makes the ProceV ideal for HPC(High Performance Computing) and high performance low-latency networking applications.

The ***ProceV*** architecture, based on Altera's Stratix *V* FPGA technology, is capable of running at typical system speeds of 150-450 MHz.

The ***ProceV*** is 8-lane PCI Express hosted offering both high performance and flexible architecture, based on massive memory and diverse add-on daughterboards for large application needs. In addition to two SODIMM sockets, 1.6Gb/s each, providing up to 16 GB of ECC DDR3 memory, the ProceV provides an option for 2×144 Mb or 2×36 Mb on-board DDRII$^{+}$ SRAM memory. This vast memory conjoined with PCIe connection permits strong co-processing between a PC with standard OS and the FPGA accelerator.

The ***ProceV*** system, supported by GiDEL's ***ProcDeveloper's Kit***™ management software and soft IPs, offers an incredible improvement in time-to-market.

In addition, the ***ProceV*** is enhanced by GiDEL's line of ***PSDB*** daughterboards enabling interfacing with external I/O lines and video applications, including SDI, DVI and Camera Link standards.

ProceV supports new simple SerDes-based fast connections between boards and accessories of up to 169 Gb/s full duplex.

The ***ProceV*** system is suitable for the following applications:

- ✓ High-speed low latency networking and network analysis
- ✓ Trading
- ✓ Life science Applications
- ✓ ASIC and SoC Prototyping
- ✓ DSP (Digital Signal Processing) and HPRC (High Performance Reconfigurable Computing)
- ✓ Surveillance, Machine Vision and Imaging
- ✓ High performance acquisition systems

The ***ProceV*** all-inclusive system, composed of on-board controllers and automatic code generation application software, eliminates the need to:

- ✓ Write a PCI Express driver.
- ✓ Write an application driver layer.
- ✓ Define board constraints.
- ✓ Design memory controller.
- ✓ Write environment FPGA code.

With the ***ProceV*** system and supporting development tools designers can focus on their proprietary value-added design instead of spending valuable time recreating standard design components. GiDEL's soft IPs and automatic HDL code generation enable high speed and easy-to-use parallel access to large memories. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them. For information on other design entry tools, please contact GiDEL.

# 3.0 Key Features

- Support Altera Stratix V GX (A3, A7, AB) and GS (D5, D8) FPGAs.
- Gen-3 8-lane PCI Express host interface and stand alone option.
- Four level memory structure (**16+ GB**).
  - ✓ Up to 2640 M20K (20K-bit) SRAM blocks (50 Mb) - 8,000 GB/s typical throughput
  - ✓ Up to 17,960 Enhanced MLAB (640-bit) SRAM blocks (8 Mb)
  - ✓ 2 × DDR3 ECC SODIMMs Banks with up to a total of 16 GB at a sustain throughput of 19.2 GB/s
  - ✓ Optional 2 × 144Mb or 2 × 36Mb DDRII$^{+}$ SRAM memories (up to 450Mhz)
- Typical system frequency of 150 - 450MHz.
- Up to 32 DMA channels.
- Up to 3,926 of 18x18 bit multipliers implemented in Stratix V devices.
- Optional: 1 CXP connector cage suitable for 100 Gigabit Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 Gigabit Ethernet, or single Infiniband 12×QDR link
- Optional: 2 SFP+ cage suitable for 10 Gigabit Ethernet and Optical Transport Network
- Optional: RJ45 port suitable for 1000MBase-T and 100MBase-TX
- 2 High-Speed Inter-Board connectors (up to 12×14.1 Gb/s) for board to board and Proc High-Speed (PHS) daughterboards connectivity
- PHS daughterboards enabling additional protocol and connectivity options such as CoaXPress, QSFP and SAS/SATA.
- 12 general purpose LVTTL External IOs
- Support for a single PSDB type 1 daughter board used for a GiDEL's off-the-shelf or user add-on Interface including logic Analyzer mictors, Camera Link, SDI, DVI and other interfaces.
- Immediate and simple high bandwidth use of the on-board memories with the innovative GIDEL ***ProcMultiPort***™ configurable IP (a part of GIDEL Proc Developer's Kit). Each memory can be used for parallel data streaming, and for debug data capture.
- Flexible clocking System.
- Temperature monitoring.
- Supported by GiDEL's Proc Developer's Kit management software.
- Drivers for Windows and Linux 64-bit Operating Systems.

## 3.1. ProceV Performance

The ***ProceV*** system provides high performance capabilities. Table 1 details the ***ProceV's*** throughput and memory capacity. Note that the performance is dependent on Proc board model.

***Table 1: ProceV Memory Throughput***

| Memory Structure | Capacity | Typical Data Rate Per Single Data Bit | Throughput* |
|---|---|---|---|
| Embedded in FPGA | Up to 2640 x M20K Blocks | 300 MHz | 8,000 GB/s |
| Optional On-Board Memory | 2 x 144Mb or 2 x 36Mb SRAM (36-bit) | 800 Mb/s | 6.4 GB/s |
| SODIMM Modules | 2 x 8GB DDR3 | 1600 Mb/s | 19.2 GB/s |

* Refer to the Appendix for throughput calculations (paragraph 13.1)

For further information regarding the embedded memory blocks, refer to the ***Altera Stratix V Handbook***.

# 4.0 Standard Models

This chapter details the standard models product available.

The model names have the following structure: ***Proceaa-bcdeefg*****,** where:

**aa**: Type of Stratix V devices:
GX Device: **A3**, **A7**, **AB**
GS Device: **D8**

**b**: Speed grade:
**A** = -1 speed grade, **B** = -2 speed grade, **C** = -3 speed grade

**c:** CXP Option:
**X**=CXP, **Blank**= without CXP

**d:** SFP+ option:
**S**=with SFP+ A and B, **Blank**=without SFP+

**ee:** 1Gbit Ethernet PHY Option:
**1G** =with PHY, **Blank** without PHY

**f:** SRAM Option:
**M** = 2×36 Mb 450 Mhz DDRII+ SRAMs,
**Blank**= without SRAM, other combinations are available for a quantity if 10 or more boards

**g:** External Clock Option:
**CK**= External clock, **Blank**= without external clock

The following table is a list of the available ***ProceV*** models:

***Table 2: GiDEL ProceV Standard Models***

| Ordering Code** (Basic Models) | Stratix V Device | Speed Grade | DDR III SODIMM Sockets | LEs* | M20K Blocks | 18×18 Multipliers |
|---|---|---|---|---|---|---|
| ***ProceV*****A3-C** | 5S**GX**A3 | -3 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-CX** | 5S**GX**A3 | -3 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-CS** | 5S**GX**A3 | -3 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-CXS** | 5S**GX**A3 | -3 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-B** | 5S**GX**A3 | -2 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-BX** | 5S**GX**A3 | -2 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-BS** | 5S**GX**A3 | -2 | 2 | 340 K | 957 | 512 |
| ***ProceV*****A3-BXS** | 5S**GX**A3 | -2 | 2 | 340 K | 957 | 512 |

(***Table 2*** – continued from previous page)

| Ordering Code** (Basic Models) | Stratix V Device | Speed Grade | DDR III SODIMM Sockets | LEs* | M20K Blocks | 18×18 Multipliers |
|---|---|---|---|---|---|---|
| ***ProceV*A7-BXS** | 5S**GX**A7 | -2 | 2 | 622 K | 2,560 | 512 |
| ***ProceV*AB-BXSM** | 5S**GX**AB | -2 | 2 | 952K | 2,640 | 704 |
| ***ProceV*D8-BXSM** | 5S**GS**D8 | -2 | 2 | 695 K | 2,567 | 3,926 |

* LE=Logic Element. For further information on the Stratix V LEs, refer to ***Stratix V Device Handbook*** (Altera Corporation).

**For other ProceV models, contact GiDEL.

**NOTE**: Default transceivers are K2=12.5 Gb/s; for transceivers K1=14.1 Gb/s, please contact GiDEL.

# 5.0 Architecture

This chapter details the ***ProceV*** architecture and components.

## 5.1. ProceV Block Diagram

The ***ProceV*** system Block Diagram is shown in Figure 1.

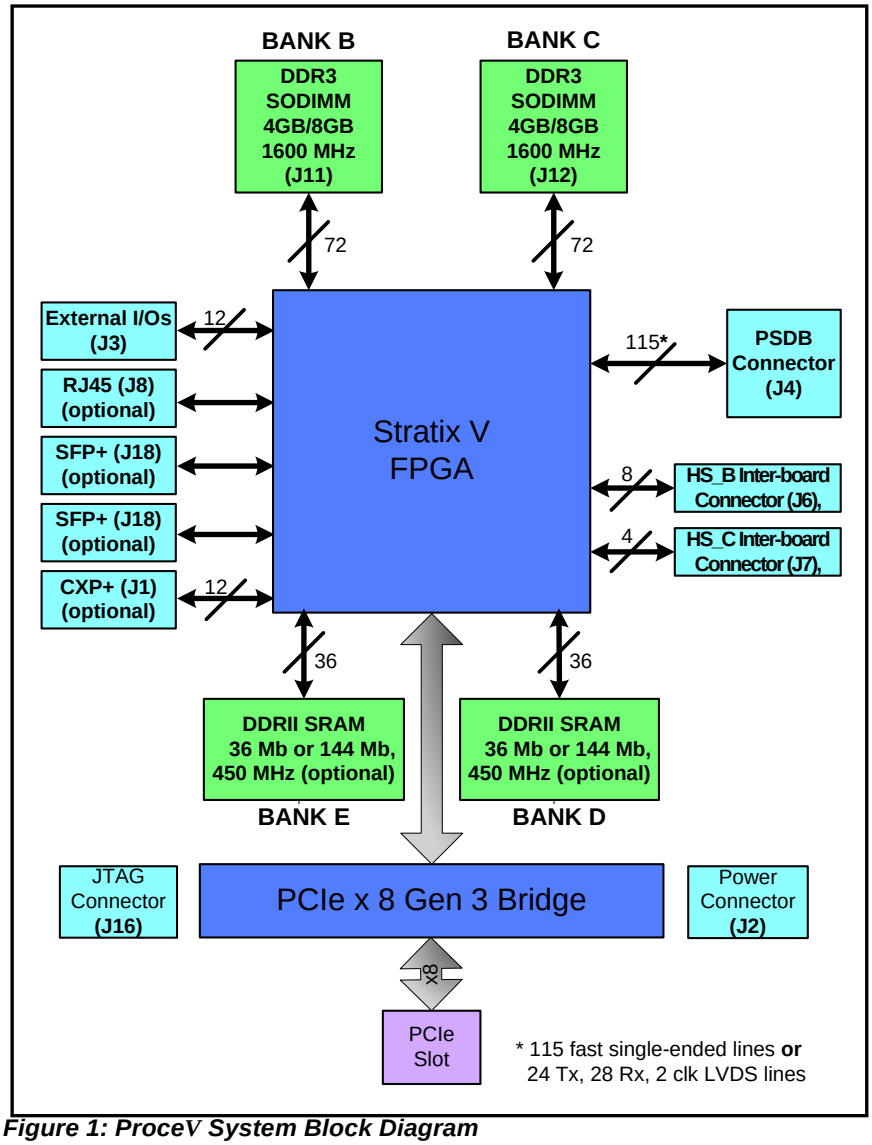


***Figure 1: ProceV System Block Diagram***

The ***ProceV*** system includes the following components:

- One ALTERA Stratix V GX or GS FPGA in 1517 package.
- 8 lane PCI Express Gen 3 interface.
- Optional: 2 x 144 Mb or 2×36 Mb DDRII$^{+}$ SRAM@450MHz on-board memories (optional).
- 2 x 8 GB DDR3 SODIMM sockets.
- Optional: 1 CXP connector cage suitable for 100 Gigabit Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 Gigabit Ethernet, or single Infiniband 12×QDR link (up to 12×14.1 Gb/s - supports splitter cable 1 to 12).
- Optional: 2 x SFP+ cage suitable for Fiber Channel, Gigabit Ethernet and Optical Transport Network (up to 14.1 Gb/s/SFP+)
- Optional: RJ45 port suitable for 1000MBase-T and 100MBase-TX
- 2× High-Speed connectors (up to 12×14.1 Gb/s) for inter-board and proprietary daughterboards connectivity
- 12 general purpose LVTTL External IOs
- External clock input via an SMA connector
- 1 PSDB Type 1 *(Proc* Daughterboard) connector with 115 I/Os or 24 LVDS TX, 28 LVDS RX and 2 LVDS clock inputs channels
- JTAG connection for the STRATIX V FPGA.
- Stand-alone capability

## 5.2. ProceV Signal Buses

The ***ProceV*** connectivity is automatically generated by the ***ProcWizard***™ software (included in ***Proc Developer's Kit)***. The ***ProcWizard*** generates the top-level design and entity/module interconnectivity in Verilog, VHDL or AHDL format, including all the ***ProceV*** buses as is described in the following sections. The buses are assigned names accordingly. However, the generated names may change if a PSDB daughterboard is added to the ***ProceV*** board. In such a case, buses that are connected to that PSDB will be named according to the corresponding buses on the PSDB.

The single-ended buses on ***ProceV*** boards are designed to provide maximum connectivity flexibility. However, user must take care to **avoid bus contention.** Always use one source at a time for a single signal.

To improve EMC characteristics, it is recommended to drive all unused connectivity pins to 0 (from one source).

The PSDB connector (J4) can operate in two unique modes: single-ended mode and differential (LVDS) mode. The following sections detailed the connectivity buses of each of the noted modes.

### 5.2.1. PSDB Connector (J4) Buses- Single-Ended Mode

The PSDB connector (J4) in single-ended mode includes the L[84:0], L_IN[7:0], L_IO[19:0] and clk_out[1:0] buses as follows:

**PSDB IN buses (l_in)**

**l_in**, for backward compatibility, is used as dedicated 8-bit input (from PSDB to the STRATIX *V* FPGA). If needed L_IN signals may also operate as outputs.

**Note:** The L_IN bus connects the FPGA to the PSDB connector **J4** as shown in Figure 1.

**PSDB I/O buses (l_io)**

**l_io** is a 20-bit bidirectional I/O bus connecting the STRATIX *V* FPGA device to its PSDB.

**PSDB I/O buses (I)**

**I** is an 85 bit bidirectional I/O bus connecting the STRATIX *V* FPGA device to its PSDB.

The **I[35]** and **I[38]** lines are connected to optional global clock input pins of the Stratix *V* device. They may be used as bus clock signals or clock inputs.

For information on **J4** pin-out, refer to section 7.2.

### *5.2.2. PSDB Connector (J4) Buses- LVDS mode*

The PSDB connector (J4) in LVDS mode includes 24 differential transmit lines (**tx[23:0]**), 28 differential receive lines (**rx[27:0]),** and 2 differential receive reference clocks (**clk_rx[1:0]**) as detailed in ***section 7.2.***

### 5.2.3. Internal Bus

***GiDEL ProcWizard*** generates an Avalon bus and a simple logic bus that delivers direct access to internal memory-mapped I/Os and a simple interface to the internal memories. The simple bus generated by the ***ProcWizard*** is called the **Internal bus**.

For further information, please refer to the ***Proc Internal Bus Data Book.***

### 5.2.4. General purpose I/O Bus

The ***ProceV*** provides 12 bidirectional buffered LVTTL general purpose IO lines via the **J3** connector. The **J3** connectivity is divided into two IO data groups: **IO[7..0]** and **IO[11..8].** The **j3_ext_io_dir0** and **j3_ext_io_dir1** signals define the data transmission direction for **IO[7..0]** and **IO[11..8]**, respectively; direction is relative to the STRATIX *V* FPGA. When **j3_ext_io_dir[1:0]** is driven high, the data is outputted from the FPGA, and when the pin is driven low, the data is inputted to the FPGA. On power-up, all 12 I/O lines are automatically configured as inputs. Some of the I/Os are connected to pull-up and pull-down resistors ensuring a stable default high or low at power up.

These signals may be connected via optocoupler, differential buffer, or other type of buffers on a dedicated interface board.

## 5.3. ProceV Clocking System

***GiDEL ProceV*** boards have a flexible clocking system.

The clocks in ***ProceV*** boards are routed as shown in the following diagram:

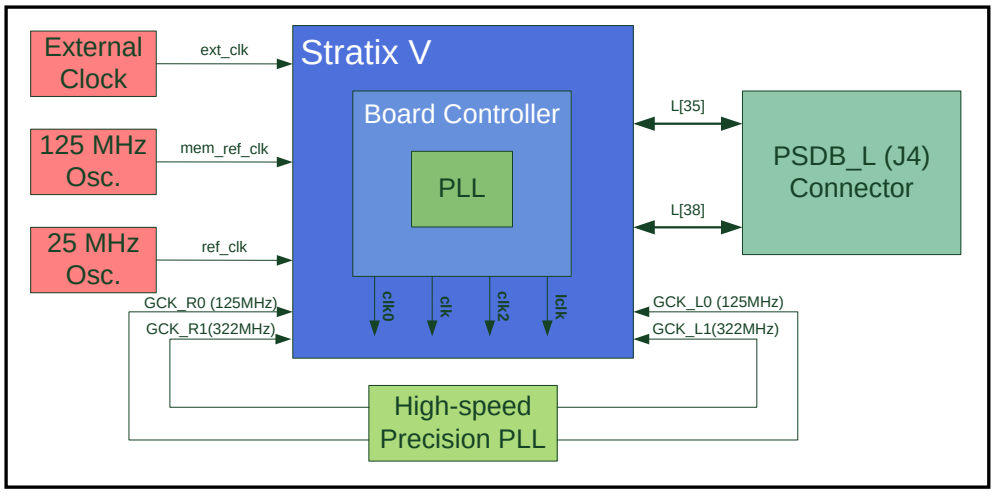


***Figure 2: ProceV Clock System***

### 5.3.1. ProceV Global Clocks

**ref_clk** is a 25Mhz oscillator input that is used to generate internal clocks.

The **clk0**, **clk** and **clk2** frequencies can be set via the *ProcWizard* development software.

#### clk0

The **clk0** is used for backward design compatibility. It is the main system clock that drives the Stratix *V* FPGA. Within the FPGA device, individual clocks for internal logic can be derived from this clock.

#### clk

**clk** is used as main logic clock and it is equal to *clk0* × *2* or *clk0* × *3*.

#### lclk

**lclk** is the **Local bus** clock that drives the Stratix *V* FPGA local bus related logic. **lclk** frequency is up to 250 MHz.

#### clk2

**clk2** is an auxiliary clock that may be used as a slow emulation clock. Clk2's frequency is derived from clk0 divided by an even number.

#### Memory reference clocks

**mem_ref_clk** is a 125 Mhz clock used as SODIMM **Bank B** and **Bank C** reference clocks.

The **mem_ref_clk** is fixed at 125 Mhz for all GiDEL boards enabling code migration and a fixed frequency source.

### 5.3.2. ProceV Individual Clocks

#### External clock inputs

**ext_clk** is an external clock received from the SMA connector (**J17**).

In single-ended mode, J4 PSDB_L has two external dedicated clock inputs **I[35]** and **I[38]** mode and in LVDS mode two differential receive locks **clk_rx [1:0].**

**J4** PSDB_L is a PSDB type 1 connector with 2 backward compatible output clocks clk_out[1:0]. On the ProceV clk_out[1:0] may also be used as regular I/Os.

### 5.3.3. ProceV High-Speed Reference clocks

The high-speed reference clocks are generated from an external high-precision PLL and are in particularly intended for driving the Stratix V transceivers. There are four high-speed reference clocks, two connected to the left side and two to the right side of the Stratix V device as follows:

| Reference Clock | Frequency | Description |
|---|---|---|
| Gck_R0 | 125 MHz | Connecting to the devices right side |
| Gck_R1 | 322.265 MHz | Connecting to the devices right side |
| Gck_L0 | 125 MHz | Connecting to the devices left side |
| Gck_L1 | 322.265 MHz | Connecting to the devices left side |

# 6.0 DMA Controller

***The ProceV*** board has 32 DMA channels. The DMA channels enable the board to have master control over the PCIe, while keeping simple internal logic and random access as slave only. The DMA is controlled by a driver and enables easy and effective usage of memory and system resources.

User's hardware design may control the data flow on DMA channels. For this purpose the customer should use the **user_dreq** bus. Each bit within the bus corresponds to a specific DMA channel; for example, **user_dreq[3]** corresponds to DMA channel 3.

After the software has initialized a DMA channel, the DMA controller starts transferring data. Data continues to be transferred as long as the **user_dreq** signal remains low for that channel. When the **user_dreq** signal rises, the DMA controller holds the transfer. This may take up to 10 local clocks. Data transfer resumes upon asserting **user_dreq** signal low.

| | |
|---|---|
|  | 1. It is not mandatory to control **user_dreq** signals. If **user_dreq** signals are not connected, once the DMA channel has been initialized by the software, it will operate continuously until all data has been transferred.<br>2. The DMA controller may stop and resume the DMA transfer based on the PCIe bus, internal bus and system activities. |

## 6.1. DMA Performance

The DMA performance depends on:

- ✓ Block size
- ✓ Active PCI Express payload
- ✓ Host mother board and chipset

Table 3 and Table 4 detail the Benchmark system and the DMA performance, respectively.

***Table 3: DMA Performance Benchmark System***

| Components | Specifications |
|---|---|
| **Processor** | **TBD** |
| **Motherboard** | **TBD** |
| **Chipset** | **TBD** |
| **Active PCI Express lanes** | **TBD** |
| **PCI Express payload (Bytes)** | **TBD** |
| **DMA block size (Mega Bytes)** | **TBD** |

***Table 4: DMA Performance***

| Test | | Results |
|---|---|---|
| **Board to PC speed** | | **TBD** |
| **PC to board speed** | | **TBD** |

# 7.0 Connectors

The following chapter details the ***ProceV*** connectors' functionality and pin-out.

## 7.1. Board Connectors Overview

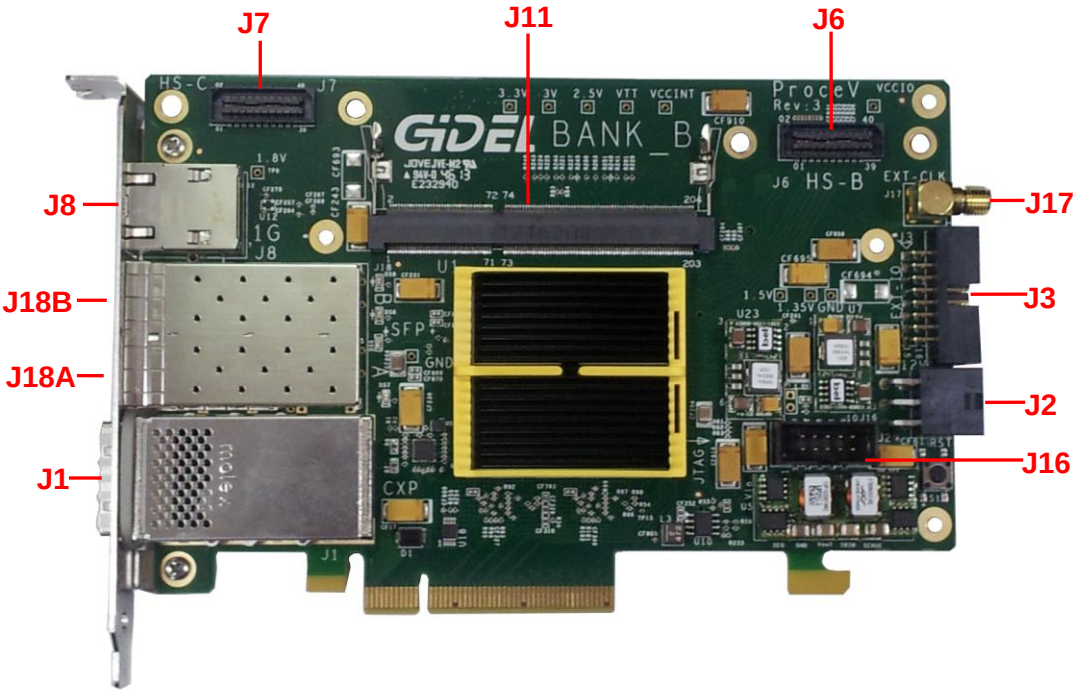


***Figure 3: Components Side (CS) Connectors***

| Connector | Function |
|---|---|
| J1 | CXP (optional) |
| J2 | 12V external source |
| J3 | External I/O |
| J6 | High-speed inter-board connector B |
| J7 | High-speed inter-board connector C |
| J8 | RJ45 1000MBase-T and 100MBase-TX (optional) |
| J11 | DDR3 SODIMM (Bank B) |
| J16 | JTAG |
| J17 | SMA for external clock (optional) |
| J18(A and B) | 2 × SFP+ (optional) |

***Table 5: Component Side Connector Description***

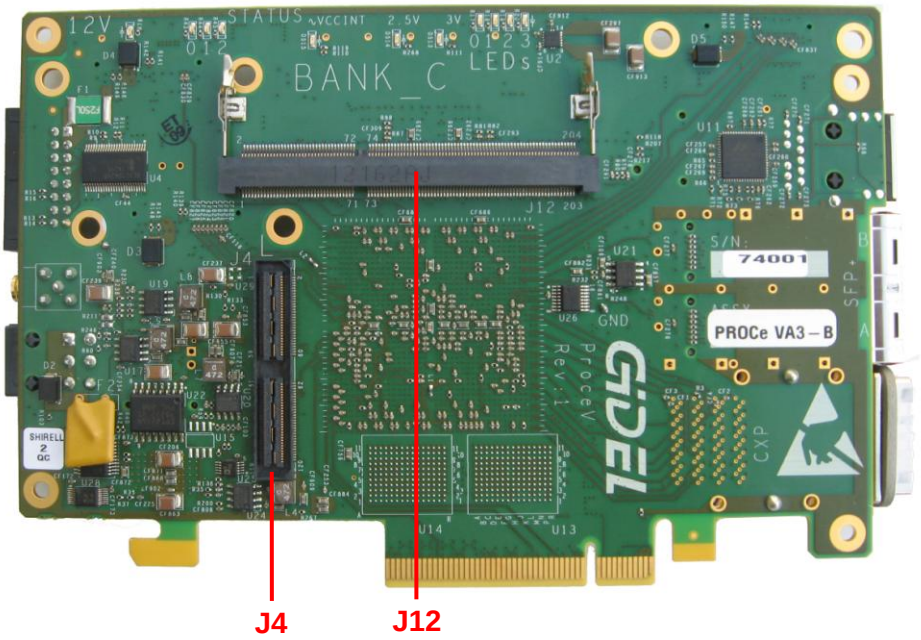


*Figure 4: Print Side (PS) Connectors*

*Table 6: Print Side Connector Description*

| Connector | Function |
|---|---|
| J12 | DDR3 SODIMM (Bank C) |
| J4 | Daughterboard (PSDB)<br>To connect via the PC's panel, you must use PSDB_6C cable kit. |

## 7.2. CXP Connector (J1)

The ProceV board has a single CXP connector cage enabling up to 12 full duplex transceivers at 600 Mb/s -12.5/14.1 Gb/s suitable for 100 Gigabit Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 Gigabit Ethernet, 12×10Gigabit Ethernet or a single 120Gb/s Infiniband 12×QDR link.

The CXP connector interfaces with the FPGA via the following top-level signals:

| FPGA Top-Level Signal | Equivalent CXP Protocol Name | FPGA I/O Direction | Description |
|---|---|---|---|
| cxp_rx[11:0] | Rx[11:0]p/n | Differential Input | FPGA SerDes data inputs |
| cxp_tx[11:0] | Tx[11:0]p/n | Differential Output | FPGA SerDes data outputs – this signals are coupled with their differential pair cxp_txn[0..11] |
| cxp_prsnt_l | PRSNT_L | Input | **1**: CXP module is absent<br>**0**: CXP module is plugged. |
| cxp_int_reset | INT_L/RESET_L | Open Collector I/O | Open collector bi-directional signal.<br>Reset signal when driven "0" by the host.<br>Interrupt signal when driven "0" by the module. |
| cxp_sda | SDA | Open Collector I/O | $I^2C$ data |
| cxp_scl | SCL | Open Collector Output | $I^2C$ clock |

***Table 7: CXP Top-Level Signals***

## 7.3. SFP+ Connectors (J18)

The ProceV has dual SFP+ cage suitable also for 2 × 10 Gigabit Ethernet cupper and Optical Transport Network.

| Connector A Top-Level Signals | Connector B Top-Level Signals | Equivalent SFP+ Protocol Name | FPGA I/O Direction | Description |
|---|---|---|---|---|
| sfp_tx_fault_a | sfp_tx_fault_b | TX_FAULT | Input | Module Transmitter Fault. |
| sfp_tx_disable_a | sfp_tx_disable_b | TX_DISABLE | Output | Transmitter Disable |
| sfp_sda_a | sfp_sda_b | SDA | Open collector I/O | $I^2C$ Data |
| sfp_scl_a | sfp_scl_b | SCL | Open collector I/O | $I^2C$ Clock |
| sfp_mod_abs_a | sfp_mod_abs_b | MOD_ABS | Input | 1: Module Absent, 0: Module assembled |
| sfp_rs[1]:0_a | sfp_rs[1]:0_b | RS[1]:0 | Output | Rate Select |
| sfp_rx_los_a | sfp_rx_los_b | RX_LOS | Open Drain Input | Receiver Loss of Signal Indication |
| sfp_rd_a | sfp_rd_b | RD- /RD+ | Differential Input | Receiver Data Input. |
| sfp_td_a | sfp_td_b | TD- /TD+ | Differential Output | Transceiver Data Output. |
| sfp_link_ledn_a | **sfp_link_ledn_b** | - | Output | LED; 0: Illuminate |
| sfp_trafic_ledn_a | sfp_trafic_ledn_b | - | Output | LED; 0: Illuminate |

***Table 8: SFP+ Top-Level Signals***

## 7.4. High Speed Inter-Board Connectors (J6,7)

The ProceV has two HS (High-Speed) inter-board connectors for board to board and daughterboards connectivity. These connectors are designated HS-B and HS-C, respectively. The HS connectors have Rx and Tx differential pairs that are connected to a Stratix V 600 Mb/s - 12.5/14.1 Gb/s transceivers. The Rx pair are designated ***hs_rxp[X]*** and ***hs_rxn[X]***, and the Tx pair are designated ***hs_txp[X]*** and ***hs_rxn[X]***. The Rx and Tx pairs together provide a full duplex lane with a throughput of up to 14.1 Gb/s. Connector HS-B has up to 8 full duplex lanes and connector HS-C has up to 4 full duplex lanes. Each of the transmit lines is connected to a 100 nF serial capacitor.

The following tables list the HS connectors' pin-out:

***Table 9: HS-B Connector (J6) Pin-out***

| Pin | External Signal Description | Pin | External Signal Description |
|---|---|---|---|
| 1 | hs_rxp0 | 2 | hs_txp0 |
| 3 | hs_rxn0 | 4 | hs_txn0 |
| 5 | hs_rxp1 | 6 | hs_txp1 |
| 7 | hs_rxn1 | 8 | hs_txn1 |
| 9 | hs_rxp2 | 10 | hs_txp2 |
| 11 | hs_rxn2 | 12 | hs_txn2 |
| 13 | hs_rxp3 | 14 | hs_txp3 |
| 15 | hs_rxn3 | 16 | hs_txn3 |
| 17 | hs_rxp4 | 18 | hs_txp4 |
| 19 | hs_rxn4 | 20 | hs_txn4 |
| 21 | hs_rxp5 | 22 | hs_txp5 |
| 23 | hs_rxn5 | 24 | hs_txn5 |
| 25 | hs_rxp6 | 26 | hs_txp6 |
| 27 | hs_rxn6 | 28 | hs_txn6 |
| 29 | hs_rxp7 | 30 | hs_txp7 |
| 31 | hs_rxn7 | 32 | hs_txn7 |
| 33 | 12v | 34 | 12v |
| 35 | hs_sdi | 36 | hs_sdo |
| 37 | hs_present | 38 | GND |
| 39 | hs_sci | 40 | hs_sco |

*Table 10: HS-C Connector (J7) Pin-out*

| Pin | External Signal Description | Pin | External Signal Description |
|---|---|---|---|
| 1 | hs_rxp0 | 2 | hs_txp0 |
| 3 | hs_rxn0 | 4 | hs_txn0 |
| 5 | hs_rxp1 | 6 | hs_txp1 |
| 7 | hs_rxn1 | 8 | hs_txn1 |
| 9 | hs_rxp2 | 10 | hs_txp2 |
| 11 | hs_rxn2 | 12 | hs_txn2 |
| 13 | hs_rxp3 | 14 | hs_txp3 |
| 15 | hs_rxn3 | 16 | hs_txn3 |
| 17 | hs_refckp | 18 | GND |
| 19 | hs_refckn | 20 | GND |
| 21 | Reserved | 22 | Reserved |
| 23 | Reserved | 24 | Reserved |
| 25 | Reserved | 26 | Reserved |
| 27 | Reserved | 28 | Reserved |
| 29 | Reserved | 30 | Reserved |
| 31 | Reserved | 32 | Reserved |
| 33 | 12v | 34 | 12v |
| 35 | hs_sdi | 36 | hs_sdo |
| 37 | hs_present | 38 | GND |
| 39 | hs_sci | 40 | hs_sco |

To interconnect between two HS connectors you must use the following **SAMTEC** cable or an equivalent cable: HQDP-020-[**XX.XX**]-TBR-TTL-2-B, where **XX.XX** specifies the length in inches.

This cable crosses left-side pins with right-side pins (e.g., pin1 with pin2).

**Note:** The 12V supplies up to 0.5A per connector.

*Table 11: HS Connectors' Top-Level Signals*

| HS-B Signals (J6) | HS-C Signals (J7) | HS Connector Name | FPGA I/O Direction | Description |
|---|---|---|---|---|
| hs_rx_b [7:0] | hs_rx_c [3:0] | hs_rxp/n | Input | 8 / 4 Differential receivers* |
| hs_tx_b [7:0] | hs_tx_c [3:0] | hs_txp/n | Output | 8 / 4 Differential transmitters* |
| | hs_refck_c | hs_refck/n | Input | Differential reference clock |
| hs_prsnt_b | hs_prsnt_c | hs_present | Input | **1**: the connector is not used<br>**0**: Other board / daughterboard is connected. |
| hs_sco | | hs_sci | Output | This is a 2-wire single-ended daisy chain connecting:<br>FPGA → HS_B → HS_C → FPGA** |
| hs_sdo | | hs_sdi | Output | |
| hs_sci | | hs_sco | Input | |
| hs_sdi | | hs_sdo | Input | |

* All receive and transmit lines are directly connected to the Stratix V transceiver with a throughput rate of 600 Mb/s - 12.5/14.1 Gb/s.

** If one of the HS_B/C is not connected, the connection will be by-passed on the board. The daisy chain protocol may be user-defined or TBD.

## 7.5. PSDB Connector (J4)

***The ProceV*** board supports a single PSDB (type 1) daughterboards. The PSDBs enable I/O connectivity to the FPGA in such standards as Camera Link, SDI, HDMI, etc. All the PSDBs are automatically identified by the ***ProcWizard***.

For further information on PSDB type 1, refer to ***PSDB1 Reference Guide***.

The PSDB connector, **J4**, is located on the Print side of the ProceV board as shown in Figure 4. **J4** is 120-pin multi-purpose connector that can also be used in LVDS mode.

Table 12 and Table 13 provide pin-out information for the **J4** PSDB connector. The PSDB connector is a multi-purpose connectors that can function in single-ended or LVDS mode as detailed in Table 12 and Table 13, respectively.

| | |
|---|---|
|  | All the signals marked as **Reserved**, are reserved for GiDEL use. These pins must be left unconnected on the user's PSDB. |

| | |
|---|---|
|  | When a GiDEL PSDB is connected to the ProceV, the generated FPGA top-level bus names that appear in the tables below **will be changed** to match the relevant PSDB functionality. |

*Table 12: PSDB_L(J4) connector pin-out*

| Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal |
|---|---|---|---|---|---|---|---|
| 1 | L0 | 34 | L_IO5 | 67 | GND** | 100 | L60 |
| 2 | CLK_OUT1 | 35 | L24 | 68 | L_IN5 | 101 | L61 |
| 3 | L1 | 36 | L74 | 69 | L38 | 102 | L_IO17 |
| 4 | DB0 | 37 | L25 | 70 | L_IN4 | 103 | L62 |
| 5 | L2 | 38 | L_IO6 | 71 | Reserved* | 104 | L63 |
| 6 | L_IN1 | 39 | L26 | 72 | L39 | 105 | L64 |
| 7 | L4 | 40 | L75 | 73 | L40 | 106 | L_IO18 |
| 8 | L3 | 41 | L27 | 74 | L_IO10 | 107 | L65 |
| 9 | L5 | 42 | L_IO7 | 75 | L41 | 108 | L66 |
| 10 | L_IN0 | 43 | L28 | 76 | L42 | 109 | L67 |
| 11 | L7 | 44 | L76 | 77 | L43 | 110 | L_IO19 |
| 12 | L6 | 45 | L29 | 78 | L_IO11 | 111 | L68 |
| 13 | L8 | 46 | L_IO8 | 79 | L44 | 112 | L69 |
| 14 | L_IO0 | 47 | L30 | 80 | L45 | 113 | L70 |
| 15 | L10 | 48 | L77 | 81 | L46 | 114 | L_IN6 |
| 16 | L9 | 49 | L31 | 82 | L_IO12 | 115 | L71 |
| 17 | L11 | 50 | L78 | 83 | L47 | 116 | L_IN7 |
| 18 | L_IO1 | 51 | L32 | 84 | L48 | 117 | L72 |
| 19 | L13 | 52 | L79 | 85 | L49 | 118 | 12V (0.3A) |
| 20 | L12 | 53 | L33 | 86 | L_IO13 | 119 | L73 |
| 21 | L14 | 54 | L80 | 87 | L50 | 120 | CLK_OUT0 |
| 22 | L_IO2 | 55 | L34 | 88 | L51 | 121 | **GND*** ** |
| 23 | L16 | 56 | L_IN2 | 89 | L52 | 122 | **GND*** ** |
| 24 | L15 | 57 | L82 | 90 | L_IO14 | 123 | **GND*** ** |
| 25 | L17 | 58 | L81 | 91 | L53 | 124 | **GND*** ** |
| 26 | L_IO3 | 59 | L83 | 92 | L54 | 125 | **VCC*** ** |
| 27 | L19 | 60 | L_IN3 | 93 | L55 | 126 | **VCC*** ** |
| 28 | L18 | 61 | L35 | 94 | L_IO15 | 127 | **VCC*** ** |
| 29 | L20 | 62 | L84 | 95 | L56 | 128 | **VCC*** ** |
| 30 | L_IO4 | 63 | DB1 | 96 | L57 | | |
| 31 | L22 | 64 | L_IO9 | 97 | L58 | | |
| 32 | L21 | 65 | L36 | 98 | L_IO16 | | |
| 33 | L23 | 66 | L37 | 99 | L59 | | |

* Reserved for GiDEL use; must be disconnected on the user's PSDB.

** GND pins must be connected to GND.

*** These are virtual signals. The PSDB connectors have two power strips in the middle. Signals [121..124] are connected to the top middle strip and signals [125..128] are connected to the bottom one. The top strip must be connected to GND and the bottom strip to the PSDB 3.3V source.

Table 13: PSDB_L (J4) pin-out in LVDS Mode

| Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal |
|---|---|---|---|---|---|---|---|
| 1 | RXp0 | 34 | TXn7 | 67 | GND** | 100 | TXp19 |
| 2 | TXp0 | 35 | RXn8 | 68 | NC**** | 101 | RXn23 |
| 3 | RXn0 | 36 | TXp8 | 69 | CLK_RXp1 | 102 | TXn19 |
| 4 | DB0 | 37 | RXp9 | 70 | NC**** | 103 | RXp24 |
| 5 | RXp1 | 38 | TXn8 | 71 | Reserved* | 104 | TXp20 |
| 6 | TXn0 | 39 | RXn9 | 72 | TXp11 | 105 | RXn24 |
| 7 | RXn1 | 40 | TXp9 | 73 | CLK_RXn1 | 106 | TXn20 |
| 8 | TXp1 | 41 | RXp10 | 74 | TXn11 | 107 | RXp25 |
| 9 | RXp2 | 42 | TXn9 | 75 | RXp17 | 108 | TXp21 |
| 10 | TXn1 | 43 | RXn10 | 76 | TXp13 | 109 | RXn25 |
| 11 | RXn2 | 44 | TXp10 | 77 | RXn17 | 110 | TXn21 |
| 12 | TXp2 | 45 | RXp11 | 78 | TXn13 | 111 | RXp26 |
| 13 | RXp3 | 46 | TXn10 | 79 | RXp18 | 112 | TXp22 |
| 14 | TXn2 | 47 | RXn11 | 80 | TXp14 | 113 | RXn26 |
| 15 | RXn3 | 48 | RXp13 | 81 | RXn18 | 114 | TXn22 |
| 16 | TXp3 | 49 | RXp12 | 82 | TXn14 | 115 | RXp27 |
| 17 | RXp4 | 50 | RXn13 | 83 | RXp19 | 116 | TXp23 |
| 18 | TXn3 | 51 | RXn12 | 84 | TXp15 | 117 | RXn27 |
| 19 | RXn4 | 52 | RXp14 | 85 | RXn19 | 118 | 12V (0.3A) |
| 20 | TXp4 | 53 | RXp15 | 86 | TXn15 | 119 | NC |
| 21 | RXp5 | 54 | RXn14 | 87 | RXp20 | 120 | TXn23 |
| 22 | TXn4 | 55 | RXn15 | 88 | TXp16 | 121 | GND*** |
| 23 | RXn5 | 56 | NC**** | 89 | RXn20 | 122 | GND*** |
| 24 | TXp5 | 57 | RXp16 | 90 | TXn16 | 123 | GND*** |
| 25 | RXp6 | 58 | NC**** | 91 | RXp21 | 124 | GND*** |
| 26 | TXn5 | 59 | RXn16 | 92 | TXp17 | 125 | VCC*** |
| 27 | RXn6 | 60 | NC**** | 93 | RXn21 | 126 | VCC*** |
| 28 | TXp6 | 61 | CLK_ RXp0 | 94 | TXn17 | 127 | VCC*** |
| 29 | RXp7 | 62 | NC**** | 95 | RXp22 | 128 | VCC*** |
| 30 | TXn6 | 63 | DB1 | 96 | TXp18 | | |
| 31 | RXn7 | 64 | TXp12 | 97 | RXn22 | | |
| 32 | TXp7 | 65 | CLK_RXn0 | 98 | TXn18 | | |
| 33 | RXp8 | 66 | TXn12 | 99 | RXp23 | | |

* Reserved for GiDEL use; must be disconnected on the user's PSDB.

** GND pins must be connected to GND.

*** These are virtual signals. The PSDB connectors have two power strips in the middle. Signals [121..124] are connected to the top middle strip and signals [125..128] are connected to the bottom one. The top strip must be connected to GND and the bottom strip to the PSDB 3.3V source.

****Should not be connected in LVDS mode.

## 7.6. External I/O Connector (J3)

The ***ProceV*** provides 12 bidirectional buffered LVTTL general purpose IO lines via the **J3** connector. The **J3** connectivity is divided into two IO data groups: **IO[7..0]** and **IO[11..8].** The **ext_io_dir0** and **ext_io_dir1** signals define the data transmission direction, relative to the STRATIX *V* FPGA. When the **ext_io_dir** pin is driven high, the data is outputted from the FPGA, and when the pin is driven low, the data is inputted to the FPGA. On power-up, all 12 I/O lines are automatically configured as inputs.

The following table describes the **J3** I/O connector pin-out:

| Pin | Signal | Top-Level Signal Name | Default I/O Resistance* | Description |
|---|---|---|---|---|
| **1** | VCC | N/A | N/A | 3.3 volt power |
| **2** | IO0 | j3_ext_io[0] | 10KΩ pull-up | I/O Bus |
| **3** | VCC | N/A | N/A | 3.3 volt power |
| **4** | IO1 | j3_ext_io[1] | 10KΩ pull-up | I/O Bus |
| **5** | GND | N/A | N/A | GND |
| **6** | IO2 | j3_ext_io[2] | N/A | I/O Bus |
| **7** | GND | N/A | N/A | GND |
| **8** | IO3 | j3_ext_io[3] | N/A | I/O Bus |
| **9** | IO4 | j3_ext_io[4] | N/A | I/O Bus |
| **10** | IO5 | j3_ext_io[5] | N/A | I/O Bus |
| **11** | IO6 | j3_ext_io[6] | 10KΩ pull-down | I/O Bus |
| **12** | IO7 | j3_ext_io[7] | 10KΩ pull-down | I/O Bus |
| **13** | IO8 | j3_ext_io[8] | 10KΩ pull-up | I/O Bus |
| **14** | IO9 | j3_ext_io[9] | 10KΩ pull-up | I/O Bus |
| **15** | IO10 | j3_ext_io[10] | 10KΩ pull-down | I/O Bus |
| **16** | IO11 | j3_ext_io[11] | 10KΩ pull-down | I/O Bus |

***Table 14 : J3-General Purpose IO Connector Assignments***

*Default input resistance at power up and when the rbf is not loaded.

The **J3** connector maximum IO working frequencies are as follows:

***Table 15: IO Working Frequency***

| Cable Length | Maximum Frequency |
|---|---|
| 0.5 meter | 40 Mb/s |
| 6.0 meters | 5 Mb/s |

## 7.7. RJ45 Connector (J8)

The ProceV has a single RJ45 port suitable for 1000MBase-T and 100MBase-TX.

The RJ45 is connected to the FPGA via Marvel's 88E1118R Alaska Gigabit Ethernet Transceiver.

| Top-Level Signals | FPGA I/O Direction | Description** |
|---|---|---|
| phy_resetn | Output | Hardware Reset: 0=Reset, 1=Normal |
| phy_mdio | Open collector I/O | Management Data with an on board pull-up Resistor |
| phy_md | Output | Management Clock data Reference for the serial Management Interface |
| phy_rx_clk | Input | RGMII Receive Clock provides a 125Mhz, 25 Mhz or 2.5 Mhz reference clock derived from the received data stream. |
| phy_rx_ctrl | Input | RGMII Receive Control |
| phy_rxd[3:0] | Output | RGMII Receive Data |
| phy_tx_ctrl | Output | RGMII Transmit Control |
| phy_tx_clk | Output | RGMII Transmit Clock provides a 125Mhz, 25 Mhz or 2.5 Mhz reference clock. |
| phy_txd[3:0] | Output | RGMII Transmit Data |

***Table 16: 88E1118R PHY Top-Level Signals***

## 7.8. External Power (12V) Connector (J2)

The External Power connector (J2) is 75W in accordance to the PCI Express REV. 3.0 ver. 0.9 2 x 3 Auxiliary Power Specification.

The J2 connector is specifically used for connecting the ProceV to a 25W slot or when operating in stand-alone mode.

***Table 17: Power Connector Pin Map (cable side)***

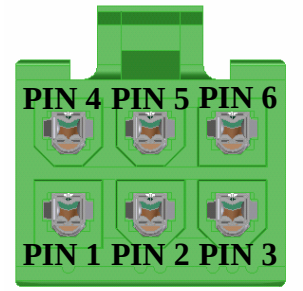


***Table 18: Power Connector (J2) Pin-out***

| Pin | Function |
|---|---|
| 1 | 12V |
| 2 | 12V |
| 3 | 12V |
| 4 | GND |
| 5 | GND (Sense0) |
| 6 | GND |

# 8.0 Memories

The ***ProceV*** system memory has a four-level structure as follows:

Two-level structure of Stratix *V* embedded memories with ultra-high bandwidth:

1. **MLAB** (Memory Logic Array Blocks) 640-bit Memories
2. **M20K Blocks** 52 Mb Memories

Additional two level structure of peripheral on-board memory blocks:

3. **SRAM** (optional) 2 ×144/36 Mb 36-bit wide
4. **DDR3 DRAM SODIMM** 2×8GB 72-bit wide

## 8.1. Two-level structure Stratix *V* embedded memory

The Stratix *V* embedded memory includes two different sizes of embedded memory. Each embedded memory block can be configured (depth x width), via the Quartus software, to be a single-port RAM, dual-port RAM, ROM, or shift register.

For further information on the *Stratix V* embedded memories, refer to ***Stratix V Device Handbook*** (Altera Corporation).

## 8.2. On-board Memory Blocks - DDRII+ SRAM (optional)

The ***GiDEL ProceV*** board has up to two 144 Mb or 36Mb DDRII+ SRAM 36-bits wide devices (**Block D and E**) connected directly to the Stratix *V* device. The SRAM maximum working frequency is up to 450 Mhz.

## 8.3. ECC DDR3 DRAM SODIMM Modules – 72 bit wide

For additional memory, Stratix $V$ device is supported by two DDR3 Modules slots (204-Pin un-buffered SODIMM with ECC). Each DDR3 slot has a maximum capacity of 8GB. The two SODIMM memory modules are designated **Block B** and **Block C,** respectively**.**

The ***GiDEL ProcMultiPort*** controller can be used with the SODIMM modules to enable new design methodologies by replacing large and complicated designs and reducing development time. For further information, refer to the ***ProcMultiPort Data Book***. Altera or any other DRAM controller may also be used.

## 8.4. SODIMM Connectivity

The following table shows the SODIMM memory modules' top-level connectivity.

***Table 19: SODIMM Top-Level Signals***

| Bank B Top-Level Signals | Bank C Top-Level Signals | Equivalent SODIMM Signal Name | I/O Directions | Description |
|---|---|---|---|---|
| addr_b[0-15] | addr_c[0-15] | A(0-15) | Output | Address Outputs |
| dq_b[0-63] | dq_c[0-63] | DQ(0-63) | I/O | Data input/output: bidirectional data bus. |
| cb_b[0-7] | cb_c[0-7] | CB(0-7) | I/O | Check bits: used for system error detection and correction. |
| dqm_b[0-8] | dqm_c[0-8] | DM(0-8) | Output | Data mask (x8 devices only): DM is an Output mask signal for the SODIMM to write data. |
| dqs_b[0-8] | dqs_c[0-8] | DQS(0-8) | I/O | Data strobe: differential data strobes (coupled with differential pairs DQSn(0-8)) |
| dqsn_b[0-8] | dqsn_c[0-8] | DQSn(0-8) | I/O | Data strobe: differential data strobes (coupled with differential pairs DQS(0-8)) |
| ba_b[0-2] | ba_c[0-2] | BA(0-2) | Output | Bank address inputs: define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| ck_b(0-1) | ck_c(0-1) | CK(0-1) | Output | Clock: differential clock inputs. these signals (coupled with differential pairs CKn(0-1)) |
| ckn_b(0-1) | ckn_c(0-1) | CKn(0-1) | Output | Clock: differential clock inputs ( coupled with differential pair CK(0-1)) |
| cas_b | cas_c | CASn | Output | Command Output |
| ras_b | ras_c | RASn | Output | Command Output |
| we_b | we_b | Wen | Output | Command Output |

| | | | | |
|---|---|---|---|---|
| cke_b[0-1] | cke_c[0-1] | CKE(0-1) | Output | Clock enable:Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM |
| cs_b[0-1] | cs_c[0-1] | S(0-1)n | Output | Chip select:Enables (registered LOW) and disables (registered HIGH) the command decoder |
| resetn_b | resetn_c | Resetn | Output (LVCMOS) | Reset:RESETn is an active LOW asychronous Output that is connected to each DRAM and the registering clock driver. |
| odt_b[0-1] | odt_c[0-1] | ODT(0-1) | Output | On-die termination:Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. |
| event_b | event_c | EVENTn | Input (Open Drain) | Temperature event:The EVENTn pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. |
| sda | sda | SDA | I/O | Serial data:Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I2CC bus. |
| scl | scl | SCL | Output | Serial clock for temperature sensor/SPD EEPROM |

## 8.5. SRAM Connectivity

The ProceV has an optional dual DDR II+ synchronous SRAM memory modules referred to as Bank D and Bank E. There are two SRAM device options:

1. SRAM 144 Mb - Cypress CY7C1650KV18.
2. SRAM 36 Mb - Cypress CY7C1250KV18-450BZXC

The following table shows the 144 Mb SRAM memory modules' top-level connectivity.

***Table 20: SRAM Top-Level Signals***

| Bank D (U13) Top-Level Signals | Bank E (U14) Top-Level Signals | FPGA I/O Direction | Description |
|---|---|---|---|
| addr_d[21:1] | addr_e[21:1] | Output | Address **[1]** |
| dq_d[35:0] | dq_e[35:0] | I/O | DQ (Data input / output ) |
| cq_d | cq_e | Differential Input | Synchronous echo clock outputs |
| cqn_d | cqn_e | Differential Input | Synchronous echo clock outputs. this signal is coupled with its differential pair cq_d/e |
| r_wn_d | r_wn_e | Output | When LDn low,<br>**1**: Read operation,<br>**0**: Write operation |
| k_d | k_e | Differential Output | Positive clock Output. |
| kn_d | kn_e | Differential Output | Negative clock Output. This signal is coupled with its differential pair k_ |
| bwsn_d[3:0] | bwsn_e[3:0] | Output | Byte write select (BWS) - Active low. Used to select which byte is written into the device **[2]** |
| ldn_d | ldn_e | Output | Synchronous load |
| qvld_d | qvld_e | Input | Valid Input indicator. The Q Valid indicates valid Input data. QVLD is edge aligned with CQ and CQn. |

**[1]** The Address is in 72-bit wide data (One address per DDR data).

For lower cost SRAM the address lines are reduced.

In some SRAMs A0 may be added to have address at 36 bit resolution.

**[2]** BWS 0 controls D[8:0], BWS 1controls D[17:9], BWS 2 controls D[26:18] and BWS 3 controls D[35:27]

For further information regarding the 144Mb SRAM, refer to the Cypress SRAM CY7C1650KV18 datasheet (doc #: 001-44061).

For further information regarding the 36Mb SRAM, refer to the Cypress SRAM CY7C1250KV18-450BZXC datasheet (doc #: 001-57834).

**Note:** Outputs are Synchronous to K clock. Inputs are Synchronous to CQ echo clock.

# 9.0 LEDs

All of the ***ProceV*** LEDs (accept SFP+ LEDs) are located on the top of the PS (Print Side) of the board.

## 9.1. Power LEDs

The ***ProceV*** board has four power LEDs as follows:

***Table 21: Power LEDs***.

| | LED Name | Function |
|---|---|---|
| 1. | 12V | 12 V - when LED illuminates it indicates there is power. |
| 2. | ~Vccint | 0.9 or 0.85 V – when LED illuminates it indicates a power failure |
| 3. | 2.5V | 2.5 V - when LED illuminates it indicates that there is power. |
| 4. | 3V | 3.0 V - when LED illuminates it indicates that there is power. |

## 9.2. Status LEDs

The ***ProceV*** board has three Status LEDs as follows:

***Table 22: Status LEDs***

| | LED Name | Function |
|---|---|---|
| 1. | Status0 | Temperature indicator:<br>Blinking LED indicates that temperature is approaching to critical level.<br>Constant illuminated LED: indicates overheating. |
| 2. | Status1 | Blinking to indicate that card is operational |
| 3. | Status2 | Indicates that the board has established link with the PCI Express slot |

**Note**: The status LEDs name at the FPGA top level is status_ledn.

## 9.3. General Purpose User LEDs

***ProceV*** boards contain four general purpose user LEDs connected to the Stratix *V* FPGA. The user LEDs name at the top level is ledn[3:0] accordingly. The LEDs are active low (Asserting a logical "0" to a LED signal will illuminate it).

## 9.4. SFP+ LEDs

***ProceV*** boards contain four SFP+ LEDs located in CS (Component Side) close to the SFP+ connector; these LEDs may be used for SFP+ trafix information or as User defined.

# 10.0 Technical Specifications

## 10.1.Electrical and Mechanical Environment

### 10.1.1. Humidity

The ***ProceV*** is operational under the following conditions:

Humidity: 10 - 90% (non-condensing)

### 10.1.2. Temperature

***ProceV*** board is equipped with an on-board temperature controller.

The maximal operating temperature of the on-board STRATIX *V* FPGA is $85^0$C. If an FPGA exceeds this temperature the user logic will be reset. At $70^0$C, an interrupt will be issued indicating that the temperature is approaching critical level.

The ***ProceV*** operating limits depend on the IC type, the computer ambient temperature, and the computer air flow as detailed in the following table:

***Table 23: ProceV Operating Conditions***

| IC Type | Max Power consumption per IC[W] | Max. Computer Ambient Temp(C°) | Min Computer Air Flow [m/sec] |
|---|---|---|---|
| All | TBD | TBD | TBD |

## 10.2.MTBF

The Mean Time Between Failures (MTBF) for the ProceV board is**: 700,000 Hours.**

Note: For Models with a limited VCCINT of up to 16A, the MTBF is**: 900,000 Hours.**

## 10.3. ProceV Mechanical Description

***ProceV*** mechanical dimensions, shown in Figure 5, comply with the PCI Express standard half length form factor.

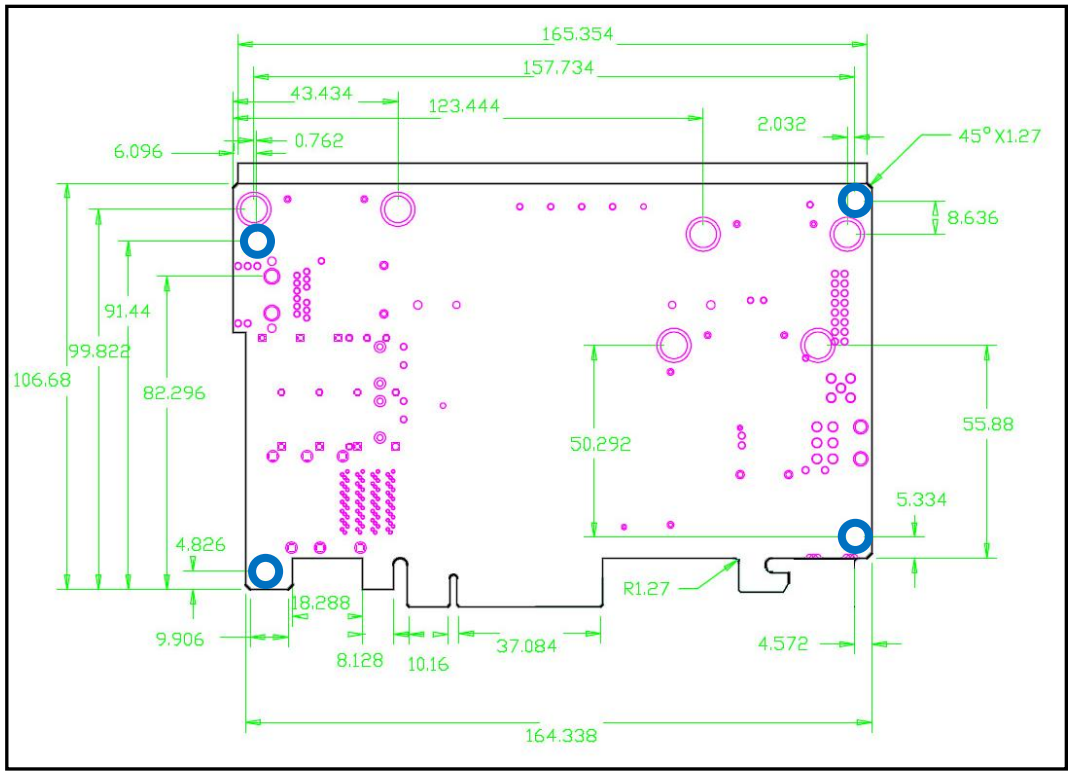


***Figure 5: ProceV Mechanical Dimensions (in mm)***

For ***ProceV*** daughterboard (PSDB) mechanical dimensions please refer to the specific PSDB's Data Book.

**Note**: The blue circles in the figure indicate mounting location for stand-alone.

## 10.4. Power Consumption

***ProceV*** is powered by 12V, supplied either by the PCI Express slot, by an external power supply or both. The maximum allowable current is summarized in the following table:

***Table 24: Maximum current Limits***

| 12V Source | Max Current |
|---|---|
| External & PCIe Slot | 5A |

The following table summarizes the ***ProceV*** internal voltage sources available for user controlled resources:

***Table 25: ProceV Internal Voltage Sources***

| Name | Voltage | Description | Max Allowable Current |
|---|---|---|---|
| VCCINT | 0.9V | Stratix V core voltage | 30A (1, 2) |
| 3.3V | 3.3V | Modules and cable connected peripherals. | 5.4A (3) |
| VCCMEM1 | 1.8V | DDRII+ SRAM power supply | 2.5A (4) |
| VCCMEM2 | 1.35V | DDRIII SODIMM power supply | 5.3A (5) |
| PSDB VCCIO | 2.5V ≥ | PSDB I/O power supply | 3A (6) |

(1) The VCCINT current consumption depends on the FPGA logic usage and on the system frequency. For precise power consumption information, refer to Quartus power analyzer report.

(2) The VCCINT is limited to 16A for the ProceV models of Altera's Startix V GX A3 FPGA with Speed Rates of 3 and 4.

(3) The 3.3V is the total current available for the following modules: SFP+ (A and B), CXP, External_IO (J3), PSDB (J4).

(4) The VCCMEM1 is the current that can be supplied to both SRAMs and the FPGA's 1.8V VCCIO. The current values depend on the SRAM capacity and the frequency rate. For more information on the SRAM, refer to their manufacturer's data sheet.

(5) The VCCMEM2 current Max current supplied to both of the SODIMMs + the FPGA's 1.35V VCCIO. The current values depend on the SODIMM capacity and the sustain rate. For more information on the SODIMM, refer to their manufacturer's data sheet.

(6) The VCCIO supplies power to the PSDB IOs. The power consumption is dependent on I/O frequency and toggle rate. For precise power consumption information, refer to Quartus power analyzer report.

Total power consumption of ***ProceV*** can be calculated according to the following formulas:

$P_{TOTAL}$ = 4.0W + $P_{Modules}$ + 1.1* ($P_{FPGA}$ + $P_{memories}$)

$P_{FPGA}$ = FPGA power dissipation

$P_{Modules}$ = 1.1×Σ (3.3V power modules and external dependencies)

+ Σ (12V power modules and external dependencies)

$P_{memories}$= Sum of SODIMM (1.35V) and SRAM power dissipation

Note: $P_{TOTAL}$ must be <= 54W (or 57 for 5% power supply accuracy)

## 10.5. ProceV Timing Model

### 10.5.1. Groups Skew

*Table 26: Groups Skew*

| module | Name | Maximum Group Skew [ps] |
|---|---|---|
| PCI | PCIe_tx[7:0] | 135 |
| | PCIe_rx[7:0] | 135 |
| CXP | CXP_tx[11:0] | 70 |
| | CXP_rx[11:0] | 70 |
| HS | HS_rx [3:0] B or C | 70 |
| | HS_tx [3:0] B or C | 70 |
| SODIMM | SODIMM bank B or C all DQ groups | 135 |
| | SODIMM bank B or C DQ Group **(1)** | 20 |
| | SODIMM bank B or C Address & Control **(2)** | 45 |
| SRAM | SRAM bank D or E Address & Control **(3)** | 45 |
| | SRAM bank D or E Data & Clock **(4)** | 25 |
| LVDS | PSDB_LVDS_tx_ [27:0] | 100 |
| | PSDB_LVDS_rx_ [27:0] | 100 |

**Notes:**

1. Every group of SODIMM DQ contains 8 lines of DQ, 1 of Diff DQS, 1 of DM.
2. Every group of SODIMM CONTROL contains 2 lines of Diff CK, Addresses, BA, RASn, CASn, ODT, CKE, Sn and WEn.
3. Every group of SRAM Address & Control contains Diff line of K, Addresses, LDn, odt, qvld and R/Wn.
4. Every group of SRAM Data & Clock contains Diff line of CQ, BWSn and DQ.

.

### 10.5.2. Clock Accuracy

***Table 27: Clock Accuracy***

| Name | Description | Maximal Deviation |
|---|---|---|
| $Osc_{ppm}$ | Oscillator accuracy | 10 ppm |

### 10.5.3. System I/O Frequency

***Table 28: System I/O Frequency***

| Bus | Maximum Frequency |
|---|---|
| **PSDB:Single-Ended ( L_IN, L_IO,L_IO,L )** | 300 Mb/s |
| **PSDB: LVDS** | 1.25 Gb/s |
| **Memory** bank B and C (SODIMM) | 1600 Mb/s (800 DDR) |
| **Memory** bank D and E(SRAM) | 900 Mb/s (450 DDR) |

* Frequencies are PSDB design dependent.

# 11.0 Installation

## 11.1. Requirements

To compile HDL designs for ***ProceV*** boards, the following system requirements are necessary:

- ✓ The installed Quartus version must support Stratix *V* devices and their specific packages.
- ✓ The user's computer must be at least a I7 with sufficient memory, normally 6GB.
- ✓ 64 bit OS
- ✓ 8-lane PCIe slot

| | |
|---|---|
|  | ***GiDEL Proc Developer's Kit*** and ALTERA Quartus software may run on the same or different computers. |

## 11.2. Installing the ProceV board

| | |
|---|---|
|  | Inserting/removing the ***ProceV*** board to/from the PCI Express slot when power is ON is **NOT PERMITTED**.<br>Inserting/removing daughterboards to/from ***ProceV*** daughterboard connectors is **NOT PERMITTED** when power is ON. These operations might damage ***ProceV*** board devices or the daughterboard |

## 11.3. Loading Designs in PCI Express Mode

Configuring the Stratix *V* FPGA (.rbf file loading) via the PCI Express bus by one of the following methods:

1. The GiDEL ProcWizard (GiDEL's development software) can be used to automatically load the device(s) at startup. In addition, ProcWizard provides a command that reloads the FPGA in real-time.
2. The user software can load the FPGA via the Application Driver automatically generated by the ProcWizard. The design is automatically loaded upon creation of the Application Driver class object or later on by using the InitIC() API method.

For further information, please refer to the ***ProcWizard User's Manual***

**NOTE:** Please contact GiDEL for availability of the noted automatic FPGA configuration loading and partial reconfiguration via PCIe.

Alternatively you may upload the code via the JTAG connector or store the design in the EPC device.

For users that do not use the Proc Developer’s kit, they may use any other Altera options.

# 12.0 GiDEL Accessories

## 12.1. GiDEL Proc Developer's Kit™

***GiDEL Proc Developer's Kit*** for **ASIC/SoC/IP & System Development** is a set of building blocks designed for fast, high-productivity system development. It is a complete system solution including boards, software tools, IPs and optional daughterboards. The main software tools and IPs are detailed in the following paragraphs.

## 12.2.GiDEL ProcWizard™

***GiDEL ProcWizard*** is an innovative tool providing a convenient developer environment that automatically generates the hardware/software interface for project-level user applications. It has been developed for high system performance. The ***ProcWizard*** automatically interfaces between the SW and the HDL applications running on the ***ProceV*** system. It generates an application driver (a C++ class) for each application/configuration.

The application driver can be generated for Windows environment. The driver is built in two layers: a Lower Layer and an Upper Layer.

The Lower Layer, the Proc class supplied with the ***ProcWizard***, implements basic board functionality such as: FPGA loading, DMA interfaces, interrupt service routines, board clocking system setups and board information acquisition such as the number of FPGAs, their size, the speed grade, etc.

The Upper Layer is automatically generated by ***ProcWizard***. This class inherits from the Proc class and implements all the application-specific functionality. It loads the Stratix *V* devices, sets up the board clocking and initializes all the class members to allow simple access to the board application from the user workspace.

The ***ProcWizard*** can also automatically generate the following:

- HDL code interface module/entity (Verilog, VHDL or AHDL) that communicates with the software driver
- ProcMultiPort (on-board memory controller) instantiations
- Basic PLLs to control external memories
- Top-level design that connects all instantiations with user modules/entities and the on-board local bus and memories
- Device constraints including FPGA pin-out, pin power voltage (VCCIO), Quartus operation recommendations, etc.

The ***ProcWizard*** also enables the user to:

- Test and debug the design in a PC environment
- Access the board with a structural browser and macros/scripts
- Load/save and compare memory files to check data transfers
- Real-time access to the registers/memories defined in the design.
- Documentation generation in HTML or DOC format that describes in detail the generated features

For more information, please refer to the ***ProcWizard User's Manual***.

## 12.3.GiDEL ProcMultiPort™

***ProcMultiPort*** is a GiDEL IP that provides an advanced controller for on-board memories. This controller has up to 16 ports; each port featuring a simple FIFO or random access.

All ports are connected to the same memory domain and can be accessed independently or simultaneously, with individual clock domains and data widths. ***ProcMultiPort*** segmented mode provides the ability to logically enlarge the FPGA memory size.

The innovative ***ProcMultiPort*** concept enables new design methodologies that can replace many large and complicated designs, thus reducing the development effort. For example, it can replace swappable double buffers or implement multiple logical memories in the same physical memory.

For more information, please refer to the ***ProcMultiPort IP User's Guide.***

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## 12.4.GiDEL ProcMegaDelay™

***ProcMegaDelay*** is a GiDEL IP that provides a simple and convenient way to create large delay lines/frame delays. ***ProcMegaDelay*** eliminates the need to use standard delay lines utilizing internal FPGA memories. Instead, it uses the on-board memory, thus enabling generation of very large delay lines.

***ProcMegaDelay*** is typically used for 2D/3D video processing, where very large quantities of data must be stored in memory and extracted later. ***ProcMegaDelay*** makes it possible to compare two (not necessary consecutive) video frames, or to write video stream as it arrives, and read it frame by frame for further processing.

For more information, please refer to the **ProcMegaDelay IP User's Guide**.

## 12.5.GiDEL ProcMegaFIFO™

***ProcMegaFIFO*** is a GiDEL IP that provides a simple and convenient way to transfer data to/from GiDEL ***Proc*** boards. With ***ProcMegaFIFO***, using the on-board memory as a very large FIFO, data may be transferred between the host PC and user's sub-designs, or between sub-designs.

***ProcMegaFIFO*** eliminates the need to take care of synchronization when transferring data between designs. The software no longer needs to respond to the hardware in real-time. Hardware designs may now transfer data in bursts and withdraw it in a continuous stream.

***ProcMegaFIFO*** uses special arbitration techniques when transferring data between the host PC and user's sub-designs. These techniques prevent memory overflows/underuse, thus using the maximum available bandwidth for data transfers.

Request and Acknowledge signals ensure correct data transfers. On the software side, the Proc class methods perform automatic initialization of the FIFO logic and enable easy data transfers by using DMA.

For more information, please refer to the ***ProcMegaFIFO* IP *User's Guide***.

## 12.6. GIDEL PSDB Daughterboards

GiDEL provides a diverse line of off-the-shelf daughterboards, referred to as **PSDBs**, that mount directly onto the ***ProceV*** board. The PSDBs enable to connect to Ethernet and to external I/O lines, and to interface with video applications, including DVI, SDI, and Camera Link standards.

For detailed list of GiDEL's PSDB daughterboards, refer to the ***PSDB Compatiblity Data Sheet.*** Note that the ***ProceV*** supports PSDB type 1 daughterboards only.

# 13.0 Appendix

## 13.1. Throughput Calculations

### 13.1.1. M20K Throughput Calculations

- Largest bit width configuration of the M20K block : **40**
- Width in true dual-port mode: 2x40 bit = 80 bit = **10 Byte**
- Maximum M20K blocks usage in a 5SGXAB device: **2640**
- Typical performance: **300 MHz**

**M20K throughput** = 10 x 2640 x 300 **≈ 7,920 GB/s**

### 13.1.2. Stratix V MLAB Throughput Calculations

- Largest bit width configuration of the MLAB block: **20**
- Width in true dual-port mode: 2x20 bit = 40 bit = **5 Bytes**
- Maximum MLAB blocks in single 5SGXAB device: **17960**
- Typical performance: **300 MHz**

**MLAB throughput** = 5 Bytes×17960×300 MHz**≈ 26,940GB/s**

### 13.1.3. On-board SRAM Memories Throughput Calculations

- Onboard memory performance: **400 MHz (DDR)**
- Bus Width: 36-bit = **4 -Bytes**
- Number of (optional) on-board memory modules: **2**

**On-board Memory throughput** = (400×2)×4×2 **≈ 6.4 GB/s**

### 13.1.4. DDR3 SDRAM SODIMM Throughput Calculations

**SODIMM (Bank B and C)**:

- Bank SODIMM performance: 1600 Mb/s (DDR)
- Bus width: 8-byte
- ProcMultiPort controller DRAM access-rate efficiency: 75%
- Number of Bank B SODIMM modules: 1.

**Throughput per SODIMM = 1600 Mb/s×8×0.75×1 = 9600 MB/s.**

**Total Throughput (Bank B + C) ≈ 9.6 GB/s + 9.6 GB/s = 19.2 GB/s**.

### 13.1.5. Additional Devices Needed

**PSDB connector sockets:**

QTH-060-**XX**-F-D-A (Samtec)

Where, **XX** specifies the connector height as shown in Table 29:

***Table 29: PSDB Connector Heights.***

| XX | Height |
|---|---|
| **– 01** | (5,00) .198 |
| **– 02** | (8,00) .316 |
| **– 03** | (11,00) .434 |
| **– 09** | (14,00) .552 |
| **– 04** | (16,00) .630 |
| **– 05** | (19,00) .748 |
| **– 06** | (22,00) .866 |
| **– 07** | (25,00) .984 |
| **– 08** | (30,00) 1,181 |

The GiDEL default standard PSDB connector size is 0.434” (11.0mm)

# 14.0 References

## 14.1.References

- *Stratix V Device Handbook, Altera Corporation*
- *ProcWizard User's Manual*
- *ProcMultiPort IP User Guide*
- *Proc Internal Bus Data Book*
- *PSDB1 Reference Guide*
- *PCIe Gen 3 Specifications*
- *CXP Specifications*
- *SFP+ Specifications*
- *Marvel's 88E1118R Data Sheet*
- *Micron MT18KSF1G72HZ-1G6 8GB ECC DDR3 SODIMM Data Sheet*
- *Apacer 78.C2GCT.AT00C 8GB ECC DDR3 SODIMM Data Sheet*
- *Micron MT18KSF51272HZ-1G4 4GB ECC DDR3 SODIMM Data Sheet*
- *Apacer 78.B2GCS.AT00C 8GB ECC DDR3 SODIMM Data Sheet*
- *Cypress CY7C1650KV18-450BZC 144Mb DDRII+ SRAM Data Sheet*
- *Cypress CY7C1250KV18-450BZXC 3Mb DDRII+ SRAM Data Sheet*
- *SAMTEC HQDP High-Speed Cable Data Sheet*

# 15.0 Glossary

*Table 30: Table of Acronyms*

| ACRONYMS | DESCRIPTION |
|---|---|
| ASIC | Application Specific Integrated Circuit |
| DDR | Double Data Rate |
| DRAM | Dynamic Random Access Memory |
| FPGA | Field Programmable Gate Array |
| IP | Intellectual Property |
| LVDS | Low Voltage Differential Signaling |
| MTBF | Mean Time Between Failures |
| PCB | Printed Circuit Board |
| PLL | Phased-Locked Loop |
| PSDB | ProceV Daughterboard |
| RTL | Register Transfer Logic |
| SoC | System-on-Chip |
| IC | Integrated Circuit |

# 16.0 Revision History

## 16.1.PCB History

***Table 31: PCB History***

| Revision | Changes |
|---|---|
| Rev. 1 | Initial PCB |
| Rev. 2 | • Changes of HS connector data:<br>○ Removal of HS-A connector<br>○ HS-B pin-out change |

## 16.2.Firmware History

***Table 32: Firmware History***

| Revision | Changes |
|---|---|
| Rev 46 | Initial code |

## 16.3.ProceV Data Book History

***Table 33: Data Book History***

| Date | Changes |
|---|---|
| 10/2012 | Initial document |
| 12/2012 | • Update of ProceV models<br>• Update according to PCB Rev. 2<br>• Update of System Diagram |
| 05/2013 | • Addition of high-speed reference clocks for Stratix V transceivers<br>• Update of board models including an option for 36 Mb DDR$^{+}$ SRAM option |
| 01/2014 | • Update of model numbering<br>• Updated Fig. 3: Components Side Connectors<br>• Updated the HS connector connectivity (Table 9, 10, 11) |