Mimosa22
User Manual

(Preliminary version)

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Document history		
Version	Date	Description
1.0	November 2007	Based on Mimosa16 Version

Mimosa22 chip			
Version	Date	Description	Comments
1.0	Submitted October 07	AMS 035 Opto Version, 576 x 136 pixels	Preliminary version

Mimosa22

Mimosa22

1 Introduction

Mimosa22 is intermediate prototype before the final sensor chip of EUDET JRA1 beam telescope for the ILC vertex detector studies. Its architecture is based on the Mimosa16 which is a fast binary readout Monolithic Active Pixel Sensor (MAPS). Mimosa22 has been designed in AMSC35B4O1 CMOS-Opto 0.35 µm.This CMOS-Opto process has 4 metal layers and 2 poly layers, and uses 14 µm epitaxial wafers. The Process Design Kit V3.70 has been provided by CMP. The design tools are CADENCE DFII 5.1 with DIVA, ASSURA, CALIBRE rules. The chip has been submitted in a Multi Chip Run via CMP the 26 October 2007 in the run # A35C5-4.

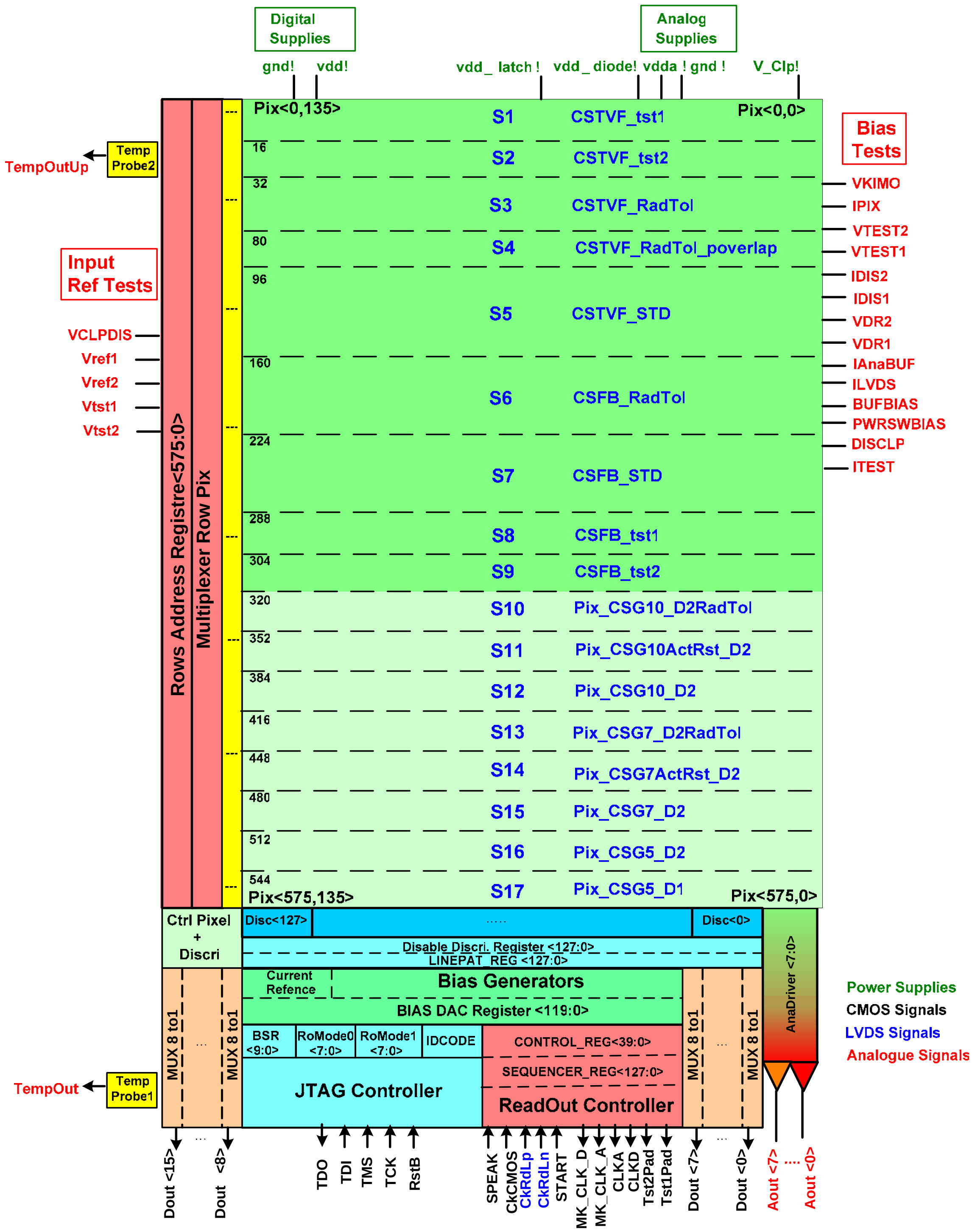
The sensor matrix is composed by 576 x 136 pixels of 18.4 µm pitch which are based on self biased diode and the reset diode architectures. The chip consists of seventeen sub- array of pixels, 128 column-level discriminators for signal sparsification, a fully programmable digital sequencer and output multiplexers for binary outputs.

The operation sequence of Mimosa22 is:

1. Power On Reset or Reset on RstB pad (active at low level)
2. Setup of the chip with programmable registers accessed via an embedded slow control Jtag interface:
   - Load the DACs which bias the analogue blocks
   - If necessary, load the ReadOut Register with a specific configuration. The default setup on power on reset allows a normal readout once the biases have been set.
3. Readout of the chip
   - The chip is driven by a 100 MHz clock. The readout starts when the input “START” token has its rising signal sampled by the internal 100 MHz clock.
   - Few digital markers are available for the control of the readout process
   - Pixels are sequentially read out in a specific order explained later in the document
   - Successive pixel frames are read until the readout clock is stopped.

A frame resynchronisation can be performed at any time by setting up the “START” token again.

Mimosa22



Mimosa22 functional view
Does not correspond to the floorplan neither for the core, neither for the pad ring

Test matrix	Row addresses range	Circuit type	Diode area (μm^2)	V_Clp (V)	Vdd_ diode (V)	Row Number	Name
S1	15-0	High gain CS + Time-variant feedback	4.5x4.5	2.1-2.4	-	16	CSTVF_tst1
S2	31-16	High gain CS +Time-variant feedback	3.8x3.8	2.1-2.4	-	16	CSTVF_tst2
S3	79-32	High gain CS + Time-variant feedback	3.8x3.8	2.1-2.4	-	48	CSTVF_RadTol (1)
S4	95-80	High gain CS + Time-variant feedback	3.8x3.8	2.1-2.4	-	16	CSTVF_RadTol_poverlap (1)
S5	159-96	High gain CS + Time-variant feedback	3.8x3.8	2.1-2.4	-	64	CSTVF_STD
S6	223-160	High gain CS + Self-biased	4.3x3.4	2.1-2.4	-	64	CSFB_RadTol (1)
S7	287-224	High gain CS + Self-biased	4.3x3.4	2.1-2.4	-	64	CSFB_STD
S8	303-288	High gain CS + Self-biased	4.4x4.4	2.1-2.4	-	16	CSFB_tst1
S9	319-304	High gain CS + Self-biased	3.4x3.4	2.1-2.4	-	16	CSFB_tst2
S10	351-320	High gain CS + Reset	3.85x3.95	2.1	0.9	32	Pix_CSG10_D2RadTol
S11	383-352	High gain CS + Time-variant feedback	3.375x4.5	2.1	-	32	Pix_CSG10ActRst_D2
S12	415-384	High gain CS + Reset	3.375x4.5	2.1	0.9	32	Pix_CSG10_D2
S13	447-416	CS + Reset	3.85x3.95	2.1	0.9	32	Pix_CSG7_D2RadTol
S14	479-448	CS + Time-variant feedback	3.375x4.5	2.1	-	32	Pix_CSG7ActRst_D2
S15	511-480	CS + Reset	3.375x4.5	2.1	0.9	32	Pix_CSG7_D2
S16	543-512	CS + Reset	3.375x4.5	2.1	1.05	32	Pix_CSG5_D2
S17	575-544	CS + Reset	3.45x3.625	2.1	1.05	32	Pix_CSG5_D1

Summary of pixel matrix

(1) For the RadTol pixel, the Voltage name RadTolPixGate is set to 0 V by default value or can be adjustable.

2 Control Interface

The control interface of Mimosa22 complies with Boundary Scan, JTAG, IEEE 1149.1 Rev1999 standard. It allows the access to the internal registers of the chip like the bias Register and the different registers control. On Power-On -Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

Mimosa22 has been designed in order to be fully adjustable via the control interface. Nevertheless several voltages level can be set both via the control interface a via a pad.

2.1 JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	5 Bit Code$_{16}$	Selected Register	Notes
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG mandatory instruction
INTEST	03	BSR	JTAG mandatory instruction
CLAMP	04	BYPASS	JTAG mandatory instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
ID_CODE	0E	DEV_ID register	User instruction
BIAS_GEN	0F	BIAS_DAC	User instruction
PATTERN_REG	10	LINEPAT_REG	User instruction
DIS_LATCH	11	DIS_DISCRI	User instruction
SEQ_REG	12	SEQUENCER_REG	User instruction
CTRL_REG	13	CONTROLER_REG	User instruction
NU1	14	(1)	Reserved, Not Used
NU2	15	(1)	Reserved, Not Used
NU3	16	(1)	Reserved, Not Used
NU4	17	(1)	Reserved, Not Used
NU5	18	(1)	Reserved, Not Used
NU6	19	(1)	Reserved, Not Used
NU7	1A	(1)	Reserved, Not Used
NU8	1B	(1)	Reserved, Not Used
NU9	1C	(1)	Reserved, Not Used
RO_MODE1	1D	ReadOut Mode 1	User instruction
RO_MODE0	1E	ReadOut Mode 0	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
DEV_ID	32	R Only	
BYPASS	1	R Only	
BSR	10	R/W	
BIAS_DAC	120	R/W	Previous value shifted out during write
RO_MODE0	8	R/W	Previous value shifted out during write
RO_MODE1	8	R/W	Previous value shifted out during write
CONTROL_REG	40	R/W	Previous value shifted out during write
SEQUENCER_REG	128	R/W	Previous value shifted out during write
DIS_DISCRI	128	R/W	Previous value shifted out during write
LINEPAT_REG	128	R/W	Previous value shifted out during write
NU1,NU2,…,NU9	0	-	Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of Mimosa22 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.2.2 DEV_ID Register

The Device Identification register is implemented. It is 32 bits long and has fixed value hardwired into the chip. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip.
Mimosa22 ID_CODE register value is *0x4D323201*.

Bit #	Bit Name	Purpose	Default value $Code_{16}$		
31-0	ID_CODE	Device Identification register	4D323201	*ASCII*	*HEX*
				'M'	4D
				'2'	32
				'2'	32
				<SOH>	01

2.2.3 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.4 Boundary Scan Register

The Boundary Scan Register, according with the Jtag instructions, tests and set the IO pads. The Mimosa22 BSR is 10 bits long and allows the test of the following input and outputs pads.

Bit #	Corresponding Pad	Type	Signal	Notes
9	SPEAK	Input	SPEAK	Active Readout Marker & Clock
8	CkCMOS	Input	CkCMOS	CMOS Clock
7	START	Input	START	Readout : Input synchronisation
6	LVDS CkRdLn/CkRdLp	Input	ClkLvds	Resulting CMOS signal after LVDS Receiver
5	MK_CLK_D	Ouput	MK_CLK_D	Readout : Digital Marker & Clock
4	MK_CLK_A	Ouput	MK_CLK_A	Readout : Analogue Marker & Clock
3	CLKD	Ouput	CLKD	Readout Digital Clock
2	CLKA	Ouput	CLKA	Readout Analogue Clock
1	Tst2Pad	Ouput	Tst2Pad	Readout Test Pad 2
0	Tst1Pad	Ouput	Tst1Pad	Readout Test Pad 1

2.2.5 BIAS_DAC Register

The BIAS_DAC register is 120 bit wide; it sets simultaneously the 15 DAC registers.
As show bellow these 8-bit DACs set voltage and current bias. After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit. The current values of the DACs are read while the new values are downloaded during the access to the register. An image of the value of each DAC can be measured on its corresponding test pad.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
119-105	DAC14	IKIMO	External circuit monitoring	VKIMO
111-104	DAC13	IPIX	Pixel source follower bias	IPIX
103-96	DAC12	IVTST2	Test Level, emulates a pixel output	VTEST2
95-88	DAC11	IVTST1	IDEM	VTEST1
87-73	DAC10	IDIS2	Discriminator bias 2	IDIS2
79-72	DAC9	IDIS1	Discriminator bias 1	IDIS1
71-64	DAC8	IVDREF2	Discriminator Reference 2	VDREF2
63-56	DAC7	IVDREF1	Discriminator Reference 1	VDREF1
55-48	DAC6	IAnaBUF	Analogue Buffer bias	IAnaBUF
47-40	DAC5	ILVDS	LVDS PAD bias	ILVDS
39-32	DAC4	ID2PWRS	Discriminator bias 2 (mode low consp.)	
31-24	DAC3	ID1PWRS	Discriminator bias 1 (mode low consp.)	
23-16	DAC2	IBufBias	Ref&Tst Buffer bias	BUFBIAS
15-8	DAC1	IPwrSWBias	Discriminator Power Pulse bias	PWRSWBIAS
7-0	DAC0	ICLPDISC	Discriminator Clamping bias	DISCLP

2.2.6 RO_MODE0 Register

The RO_MODE0 registers are 8 bits large; they allow the user to select specific digital mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	En_TstBuf	Enable the internal injection of VTEST	0	External injection of VTEST
6	En_HalfMatrx	Set the row shift register to 320 in place of 576 bits.	0	Normal mode, 576 row shift register selected
5	DisLVDS	Disable LVDS and active clock CMOS.	0	LVDS selected
4	En_LineMarker	Add two rows at the end of matrix for a chip Readout: The LINEPAT_REG register is selected to emulate discriminators outputs. For analogue outputs, the 2 Test Levels, VTEST1 and VTEST2 are selected which emulate a pixel output.	0	Normal mode
3	MODE_SPEAK	Select Marker signal or Readout Clock for digital and analogue data (MK_CLKA and MK_CLKD pads)	0	Marker signal active
2	Pattern_Only	Test Mode: Select LINEPAT_REG to emulate discriminators outputs	0	Normal mode
1	En_ExtStart	Enable external START input synchronisation (1)	0	Normal mode
0	JTAG_Start	Enable Jtag START input synchronisation (2)	0	

(1) The minimum wide of asynchronous external START is 500 ns, and this signal is active at high level.

(2) When En_ExtStart is disabled, it's possible to generate internal START by accessing JTAG_Start bit. JTAG_Start signal is realized by three JTAG access: First step, this bit is set to 0, second step it is set to 1, and at last it is set to 0.

2.2.7 RO_MODE1 Register

The RO_MODE1 registers are 8 bits large; they allow selecting specific analogue mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	NU4	Reserved, Not Used		
6	NU3	Reserved, Not Used		
5	NU2	Reserved, Not Used		
4	DisBufRef	Disable the internal reference	0	Select Internal Buffer
3	NU1	Reserved, Not Used		
2	En_AOP_Disc	Enable the Power pulse Amplifier	0	Normal mode
1	En_Pulse_Discri	Enable the discri power pulse mode	0	Normal mode
0	En_TstDis	Enable the discri. test mode	0	Normal mode

2.2.8 CONTROL_REG Register

The CONTROL_REG registers are 40 bits large; they allow setting parameters of the readout controller.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	
39-36	NU	Reserved, Not Used	0	
35-33	SelPad1	Selection bit of Test1Pad	0	MK_Test_A signal
32-30	SelPad2	Selection bit of Test2Pad	0	MK_Test_D signal
29-20	RowMkLast	Row number of the frame. It depends of readout mode. When the En_HalfMatrx mode is active, the value is 0x013F otherwise 0x023F. When the En_LineMarker mode is active, add two rows at the end of matrix.	023F	Normal mode, the number of row matrix is 576.
19-10	RowMkd	Selection parameter of row for digital marker (MK_Test_D)	0	Digital marker place is first row of matrix during the readout
9-0	RowMka	Selection parameter of row for analogue marker (MK_Test_A)	0	analogue marker place is first row of matrix during the readout

The purpose of this array is to describe the internal signals which can be checked using 2 test pads (Tst1Pad and tst2Pad). The internal signals can be selected with SelPad1 and SelPad2 bits.

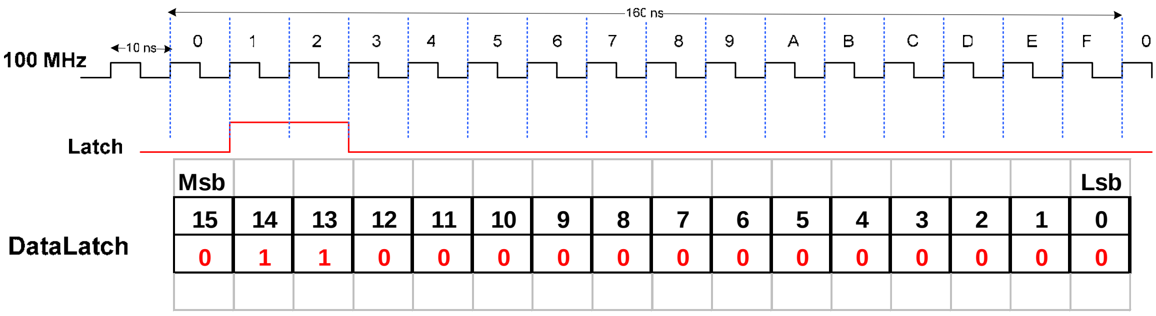
SelPad1	Tst1Pad	Purpose	SelPad2	Tst2Pad	Purpose
0	MK_Test_A	Analogue marker is shifted of 80 ns to MK_A signal. This signal rises up at the beginning read phase and falls down at the end of Calib phase. It depends of RowMka selection parameter.	0	MK_Test_D	Digital marker corresponding to last serialized digital data. It depends of RowMkd selection parameter.
1	Mk_Rd	Analogue marker corresponding to Rd phase of readout pixel. It depends of RowMka selection parameter	1	PwrOns	Same signal as PwOn, but shifted of 16 main clock
2	Mk_Calib	Analogue marker corresponding to Calib phase of readout pixel. It depends of RowMka selection parameter	2	PwOn	Activate power supply for pixel
3	CkDiv32	CkDiv16 signal is devised by 2	3	SlcRowInt	Connect pixel output to common column
4	MK_A	Analogue marker corresponding to readout pixel sequence. It depends of RowMka selection parameter.	4	Clp	Set reference voltage for clamping
5	Clp	Set reference voltage for clamping	5	RstDiode	Set reference voltage for diode
6	Latch	Latch state of the discriminator	6	Rd	Sample before clamping
7	CkDiv16	Main Clock is devised by 16	7	Calib	Sample after clamping

2.2.9 SEQUENCER_REG Register

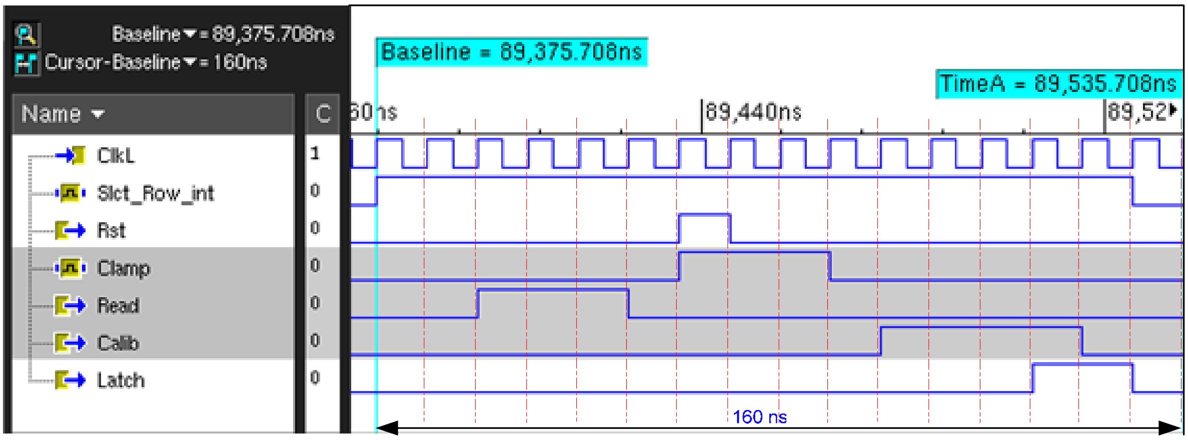
The SEQUENCER_REG registers are 128 bits large; this register contains all parameters to generate readout pixel and discriminator sequence.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	Signal Name
127-112	DataRdPix	Connect pixel output to common column	7FFF	Slct_Row_Int
111-96	DataRst1	Set reference voltage for diode	0040	Rst
95-80	DataClp	Set reference voltage for clamping	01C0	Clamp
79-64	DataCalib	Sample after clamping	3C00	Calib
63-48	DataRdDsc	Sample before clamping	001C	Read
47-32	DataLatch	Latch state of the discriminator	6000 (1)	Latch
31-0	DataPwrOn	Activate power supply for pixel	7FFFFFFF	Pwr_On

(1) Example: Generation of Latch Signal

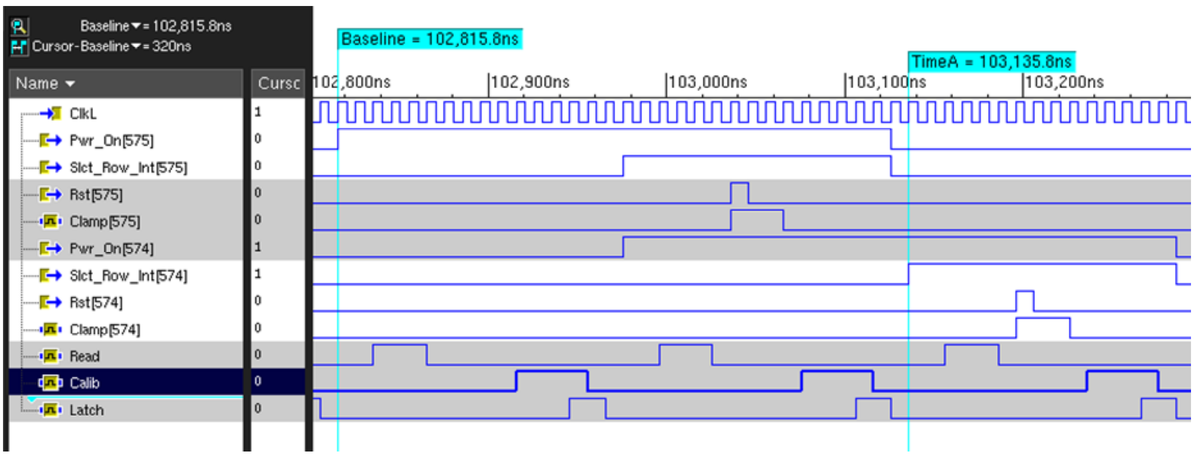


- Related timing with f_{ClkL}=100 MHz (Read, Calib, Latch signals are used by the column readout circuitry).



For Sub arrays S6-S9, S11 and S14, the Rst signal is not used for pixel.

- This is readout sequence of the pixel and discriminator for 2 successive rows of matrix. In the wave form, the indexation of internal signal vectors is reversed compared with the Mimosa22 functional view (for example, the signal Pwr_On[575] corresponds to the row at the top of matrix).



For Sub arrays S10-S17, the Pwr_On signal is not used for pixel.

2.2.10 DIS_DISCRI Register

The DIS_DISCRI register is 128 bits large. The purpose of this register is to disable the discriminator on a specific column if it is noisy, by gating Latch signal and setting the output discriminator at 0.
The default value of the DIS_DISCRI register is 0; it means that all discriminators are activated. Setting a bit to 1 disables the corresponding discriminator. In Mimosa22, the DisableLatch<127> is on the left hand side while DisableLatch<0> is on the right hand side.

127 (Msb)	**0 (Lsb)**
DisableLatch<127>	**DisableLatch<0>**

2.2.11 LINEPAT_REG Register

The LINEPAT_REG register is 128 bits large. The purpose of this register is to emulate discriminators outputs rows in *En_LineMarker* and Pattern_Only modes.

When Pattern_Only is active, during the readout of matrix, the value of LINEPAT_REG is read to emulate discriminators outputs of each matrix row. This mode corresponds to debug mode, it allows verify the digital processing.

In the *En_LineMarker* mode, it adds two rows at the end of matrix for a readout chip and the LINEPAT_REG register is read to emulate the discriminators outputs of these two supplementary rows. This mode allows generating pattern marker in matrix data frame to detect chip readout desynchronization.

Bit #	**Bit Name**	**Purpose**	**Basic configuration value Code$_{16}$**
127-0	LinePatReg	Emulate discriminators rows	AAFFFFFF_AAAAAAAA_55555555_22FFFF11 (1)

(1) Example of pattern used in simulation.

3 Running Mimosa22

The following steps describe how to operate Mimosa22

3.1 After reset

On RstB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_DISC is set to 0, i.e. all columns are selected
- RO_MODE0 is set to 0
- RO_MODE1 is set to 0
- CONTROL_REG is set to 0
- SEQUENCER_REG is set to 0
- LINEPAT_REG is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.
The same for the RO_MODE0, RO_MODE1, CONTROL_REG, SEQUENCER_REG, LINEPAT_REG and DIS_DISC registers if the running conditions differ from defaults.
Finally the readout can be performed either in normal mode or in test mode.

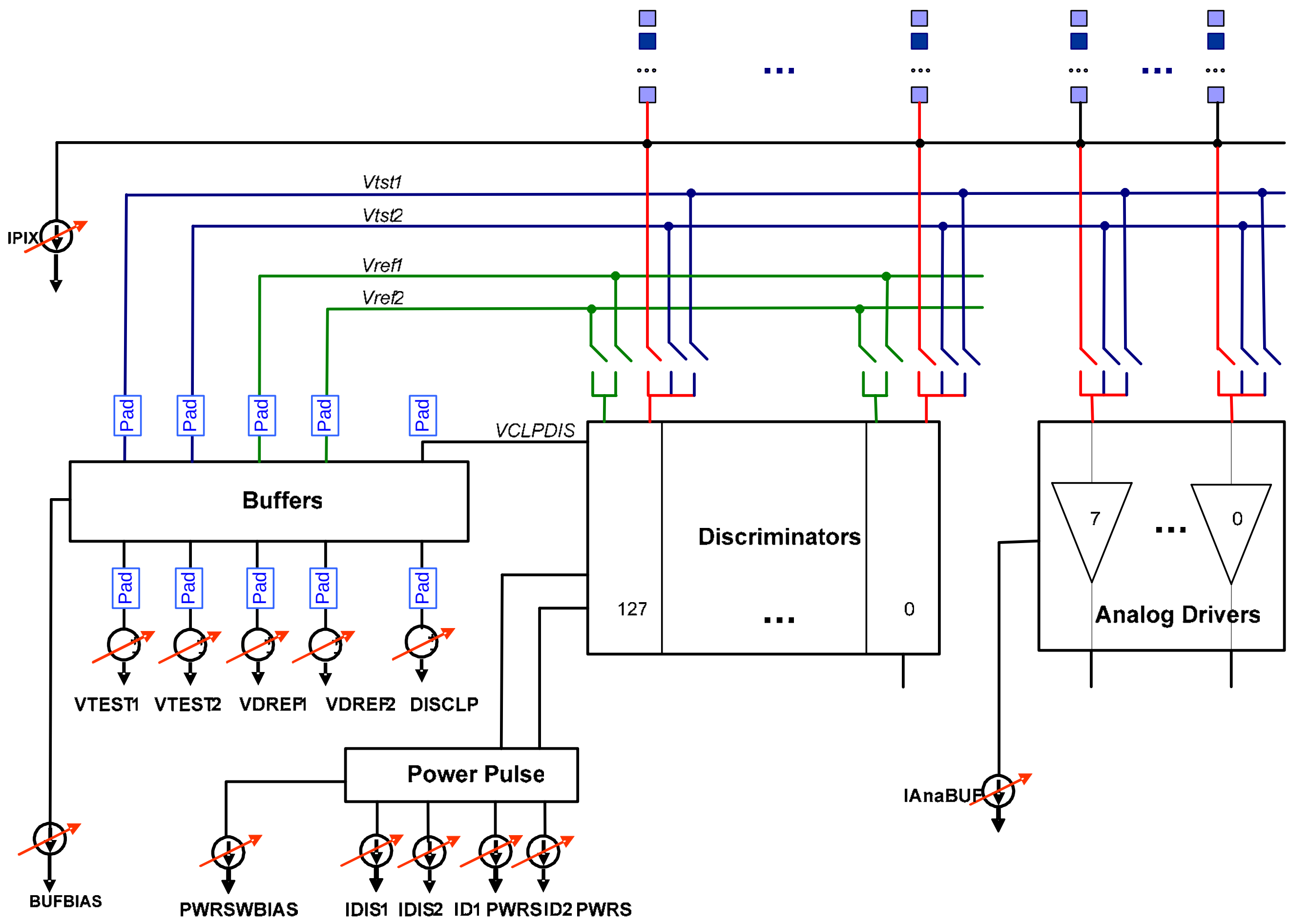
3.2 Biasing Mimosa22

The BIAS_DAC register has to be loaded before operating Mimosa22.
The 15 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output.
The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range	Experimental
	$Code_{16}$ - $Code_{10}$	DacInternal current-µA	Output value			$Code_{16}$ - $Code_{10}$
IKIMO	64-100	100	1 V	10 mV	From 0 up to 2.55 V	
IPIX	32-50	50	50 µA	1 µA	From 0 up to 255 µA	
IVTST2	71-113	113	1.182 V	10 mV	From 1 up to 1.5 V	
IVTST1	8C-140	140	1.183 V	250 µV	From -30 up to 34 mV	
IDIS2	20-32	32	5 µA	156 nA	From 0 up to 255 µA	
IDIS1	20-32	32	10 µA	312 nA	From 0 up to 255 µA	
IVDREF2	71-113	113	1.182 V	10 mV	From 1 up to 1.5 V	
IVDREF1	80-128	128	1.182 V	250 µV	From -30 up to 34 mV (1)	
IAnaBUF	32-50	50	500 µA	10 µA	From 0 up to 255 µA	
ILVDS	20-32	32	7 µA	218 nA	From 0 up to 255 µA	
ID2PWRS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
ID1PWRS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
IBufBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
IPwrSWBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
ICLPDISC	64-100	100	2.1 V	10 mV	From 1.2 up to 3.2 V	

(1) Referenced with respect to IVDREF2. The threshold voltage of the discriminators ΔVth is defined as Vref1-Vref2 (Vref1=Vref2+ΔVth).

Bias synthetic block diagram



3.3 Setting the Readout Configuration Registers

If the desired operating mode does not correspond to the default one, set RO_MODE0, RO_MODE1, CONTROL_REG, SEQUENCER_REG, LINEPAT_REG registers following the §2.2.6, §2.2.7, §2.2.8, §2.2.9, §2.2.11.

3.4 Readout

3.4.1 Signal protocol

After JTAG registers have been loaded, the readout of Mimosa22 can be initialized with following signal protocol:

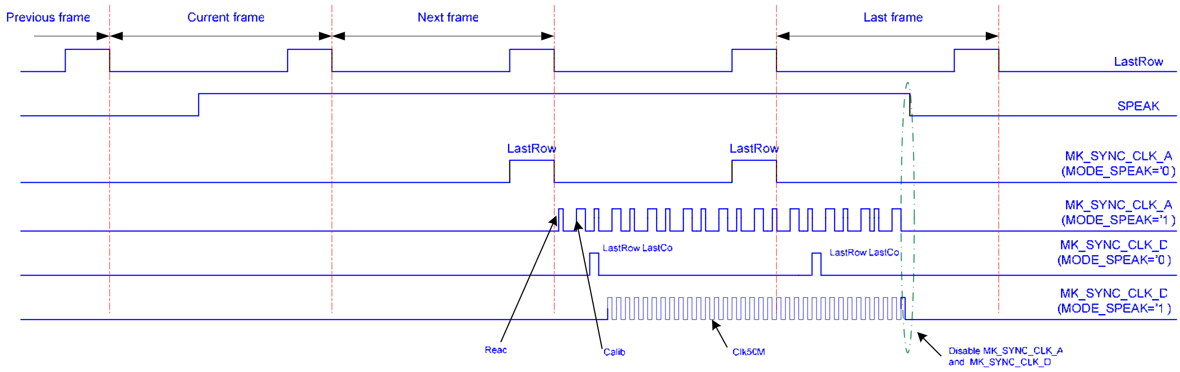
- Start readout clock (CK100M);
- Set SPEAK signal to 0;
- Set START signal to 1 during 500 ns (minimum).The internal reset is created after 15 ns on the rising edge of START. After this reset, Clk50M (input clock with a ½ ratio) and CkDiv16 (input clock with 1/16 ratio) are generated;
- The readout controller starts at the first falling edge of CkDiv16 after START set to 0.

Signal markers allow the readout monitoring and the data outputs (analogue and digital) sampling:

- CLKA and CLKD are running when readout controller starts. CLKA is signal which is generated by logic OR between Read and Calib signals. And CLKD corresponds to Clk50M;
- When SPEAK signal is active, markers of synchronisation for analogue and digital outputs are generated on MK_CLK_A and MK_CLK_D pads.

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read until the readout clock is stopped.
A frame resynchronisation can be performed at any time by setting up the “START” token again.



SPEAK signal allows to generate markers signals which are used by DAQ. When SPEAK signal is set to 1 during the current frame, analogue marker appears on MK_SYNC_CLK_A pad and digital marker appears on MK_SYNC_CLK_D pad during next frame.

In the MODE_SPEAK=’0’ (see Figure 5.a), the MK_SYNC_CLK_A marker corresponds to last row of the frame and the MK_SYNC_CLK_D marker corresponds to last bit frame.

In the MODE_SPEAK=’1’ (see Figure 5.b), MK_SYNC_CLK_A signal corresponds to a sampling clock for analogue outputs data (same as CLKA) which starts at the first row of frame. MK_SYNC_CLK_D signal corresponds to readout clock for digital data (same as CLKD) which starts at the first bit frame.

When SPEAK signal is set to 0, MK_SYNC_CLK_A and MK_SYNC_CLK_D are set to 0.

3.5 Analogue and digital Data Format

Two Types of signal can be generated on analogue outputs:

- Normal pixel signal
- Test signal

In concern to digital outputs, two types of signal can be generated:

- Digitalization pixel signal by discriminator
- Test pattern , read to LINEPAT_REG register

3.5.1 Normal mode data format

The chip has columns parallel process readout. The first 128 columns are connected to discriminators, multiplexed onto 16 outputs. The last 8 columns of 136 are connected to output analogue buffers. Their analogue outputs can be observed directly on the output pads. The digital part includes three blocks. One is JTAG controller interface which allows configure the internal registers used to readout chip. The second circuit generates the patterns necessary for addressing, resetting and double sampling of the signals in pixels in a column parallel way. The rows are selected sequentially using a multiplexer every 16 clock cycles. The last circuit realizes a temporal multiplexing of the binary outputs at a frequency value half that of the main clock frequency.

For Mimosa22, Col.127 is at the left of matrix and Col.0 is at the right. The row at the top of matrix is read out first. 16 multiplexers (8:1) serialize the digital row data onto 16 output pads. The bit which is first selected in the serial 8 bits stream corresponds to the Msb bit (see the table below). Data are serialized on falling edge clock of CLKD.

The Vref1 voltage is applied to the negative discriminator input during the read phase and the Vref2 voltage is applied during the Calib phase. The difference voltage Vref1 – Vref2 set the threshold of the discriminator. Voltages can be adjustable via 2 DACs or can be provided via 2 pads.

Output pad	**Digital output**							
	(Msb)							**(Lsb)**
Dout<15>	Col.127	Col.126	Col.125	Col.124	Col.123	Col.122	Col.121	Col.120
Dout<14>	Col.119	Col.118	Col.117	Col.116	Col.115	Col.114	Col.113	Col.112
Dout<13>	Col.111	Col.110	Col.109	Col.108	Col.107	Col.106	Col.105	Col.104
Dout<12>	Col.103	Col.102	Col.101	Col.100	Col.99	Col.98	Col.97	Col.96
Dout<11>	Col.95	Col.94	Col.93	Col.92	Col.91	Col.90	Col.89	Col.88
Dout<10>	Col.87	Col.86	Col.85	Col.84	Col.83	Col.82	Col.81	Col.80
Dout<9>	Col.79	Col.78	Col.77	Col.76	Col.75	Col.74	Col.73	Col.72
Dout<8>	Col.71	Col.70	Col.69	Col.68	Col.67	Col.66	Col.65	Col.64
Dout<7>	Col.63	Col.62	Col.61	Col.60	Col.59	Col.58	Col.57	Col.56
Dout<6>	Col.55	Col.54	Col.53	Col.52	Col.51	Col.50	Col.49	Col.48
Dout<5>	Col.47	Col.46	Col.45	Col.44	Col.43	Col.42	Col.41	Col.40
Dout<4>	Col.39	Col.38	Col.37	Col.36	Col.35	Col.34	Col.33	Col.32
Dout<3>	Col.31	Col.30	Col.29	Col.28	Col.27	Col.26	Col.25	Col.24
Dout<2>	Col.23	Col.22	Col.21	Col.20	Col.19	Col.18	Col.17	Col.16
Dout<1>	Col.15	Col.14	Col.13	Col.12	Col.11	Col.10	Col.9	Col.8
Dout<0>	Col.7	Col.6	Col.5	Col.4	Col.3	Col.2	Col.1	Col.0

3.5.2 Test mode data format

This test readout mode allows obtain the transfer function of discriminator and calibrate the pixel readout chain.

During the test mode the pixel matrix is not connected to discriminators and output analogue buffers. Instead of this, two test levels Vtst1, Vtst2 are connected to discriminator inputs to emulate pixel signal.

The Vtst1 voltage is applied to the positive discriminator input during the Read phase and the Vtst2 voltage is applied during the Calib phase. Voltages can be adjustable via 2 DACs or can be provided via 2 pads. The difference voltage Vtst1 – Vtst2 corresponds to the pixel output signal.

3.6 Mimosa22 Chronograms

The following chronograms describe typical access to the chip; Reset, JTAG download sequence and then the readout.

3.6.1 Normal Readout

Figure 1 show the beginning of typical data readout mode. After Reset and JTAG setting, one can see the initialisation phase of the readout of the first pixel row.

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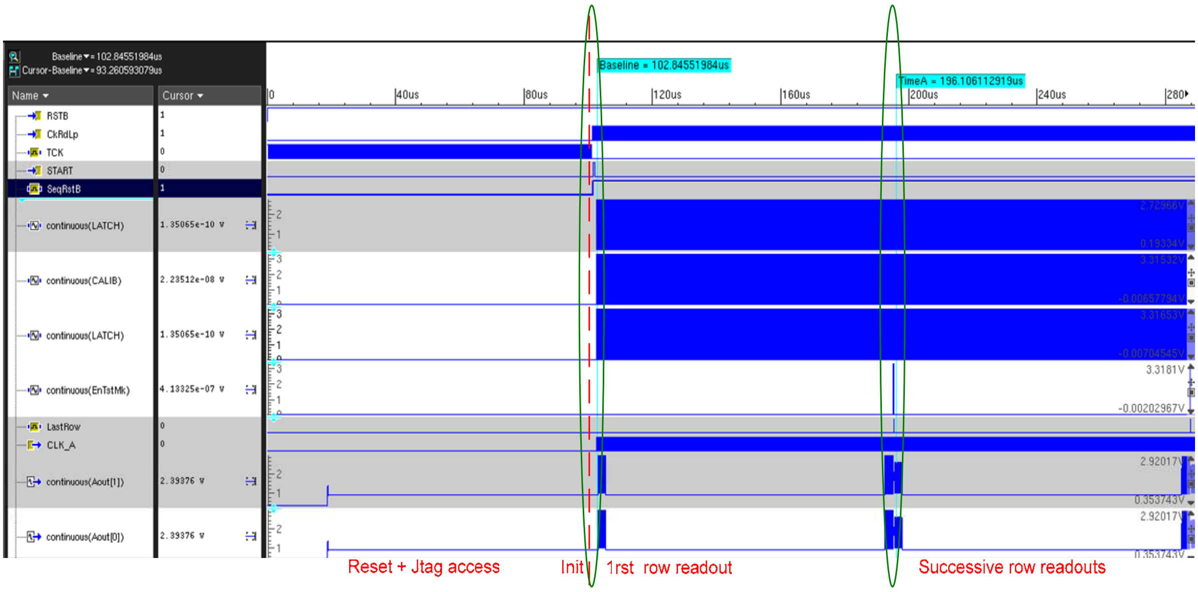


Figure 1

3.6.2 Readout synchronisation

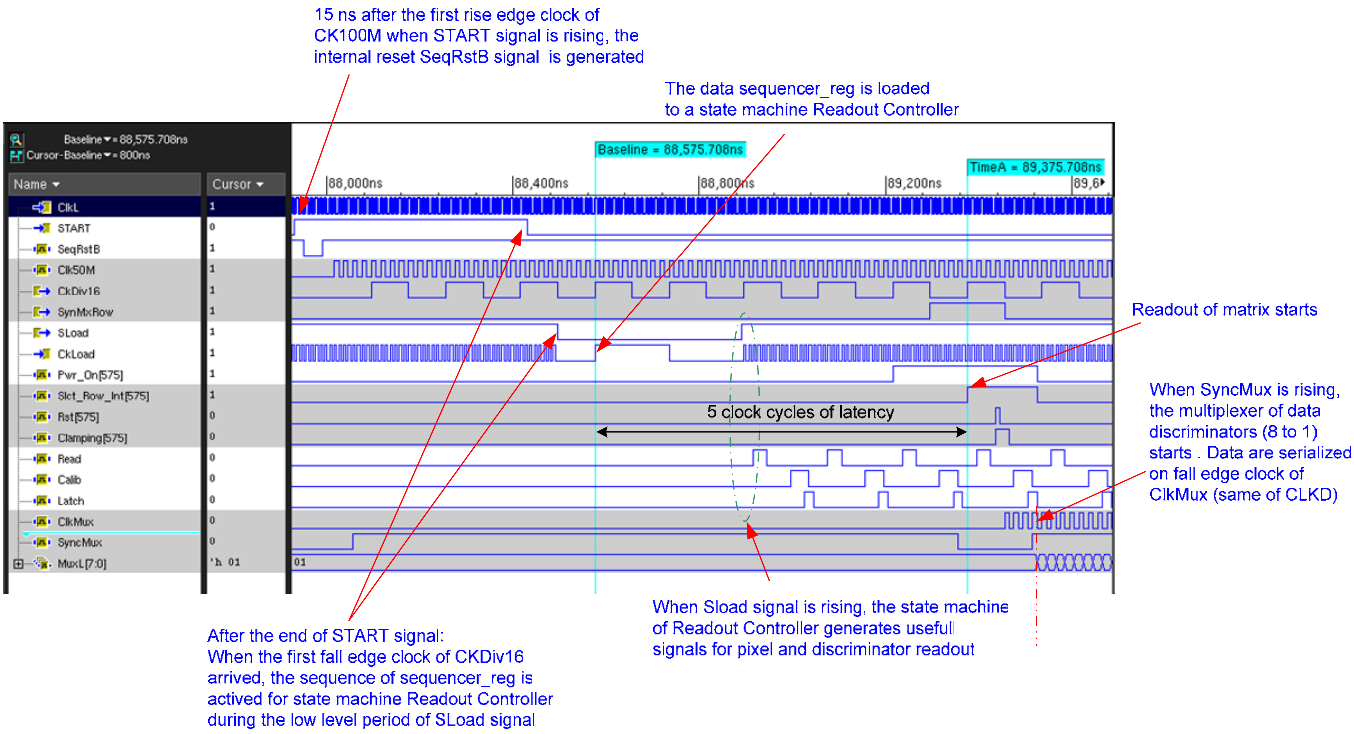


Figure 2

Figure 2 zoom on the readout start. After a latency of 5 CkDiv16 cycles, readout of matrix starts.

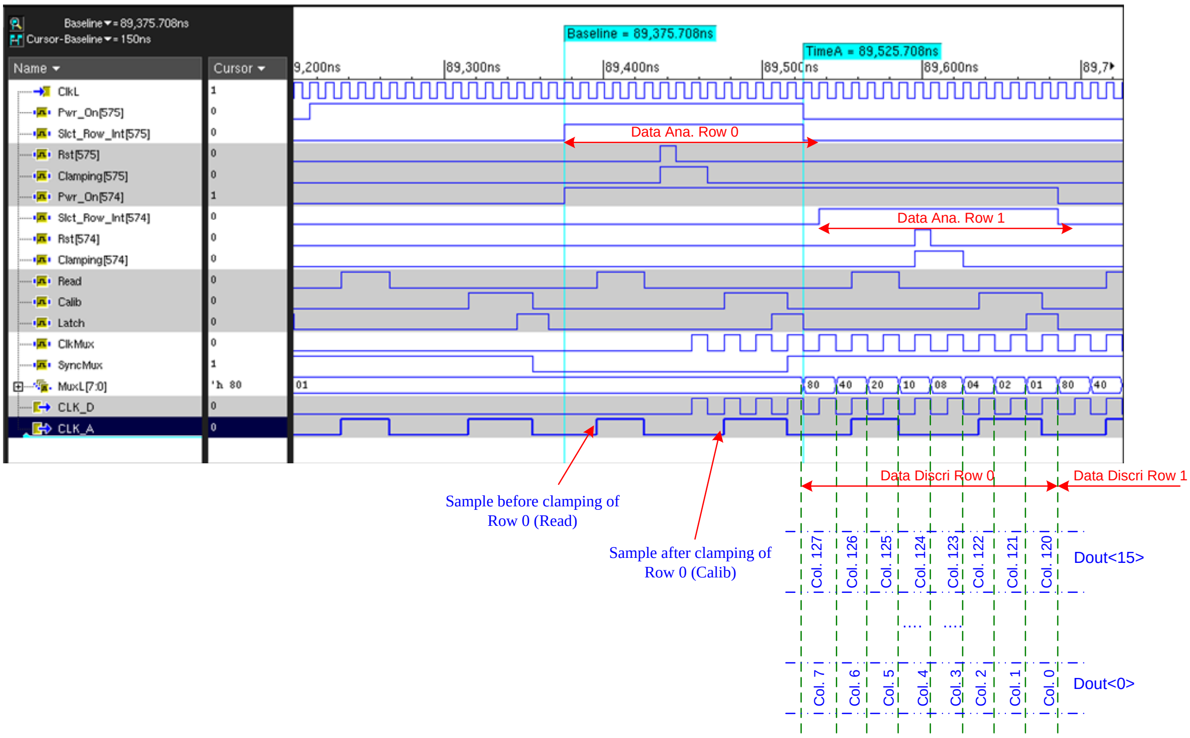


Figure 3

Figure 3 shows the first row of the readout matrix and the beginning of digital data serialization sequence.

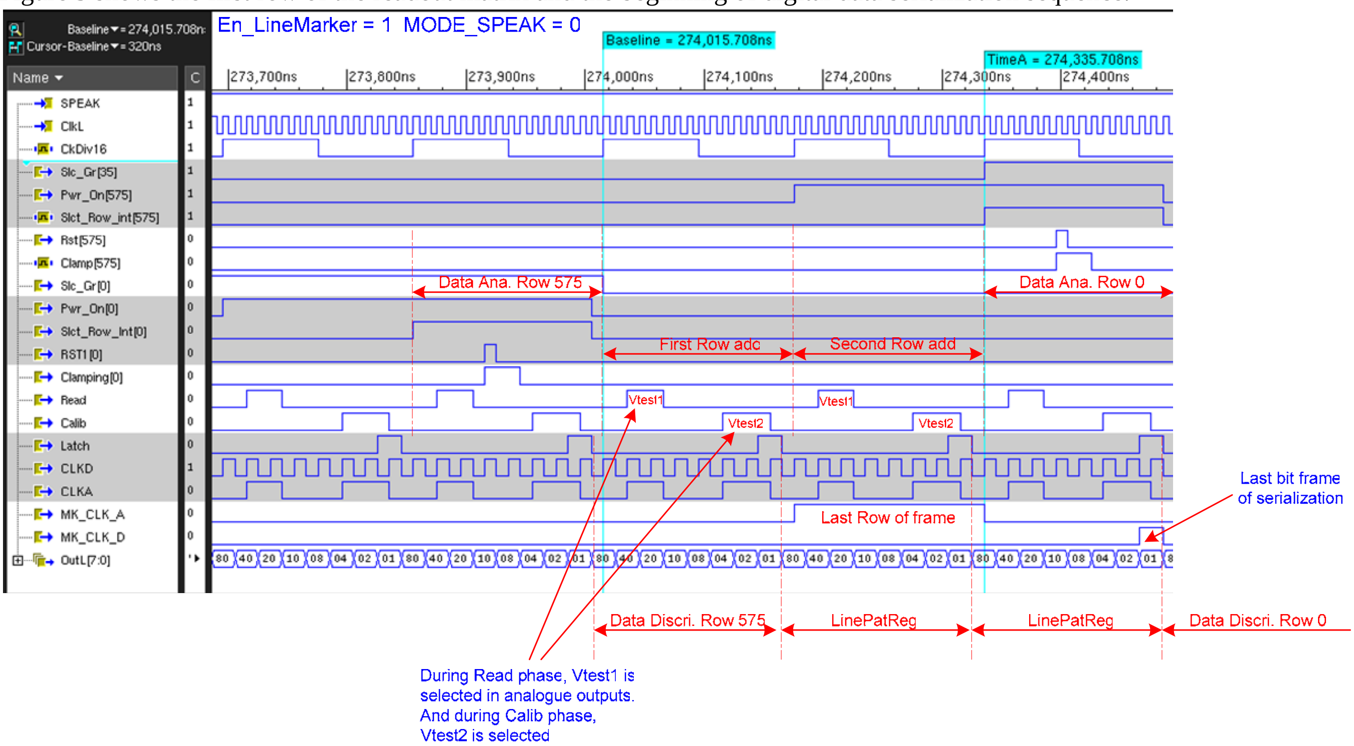
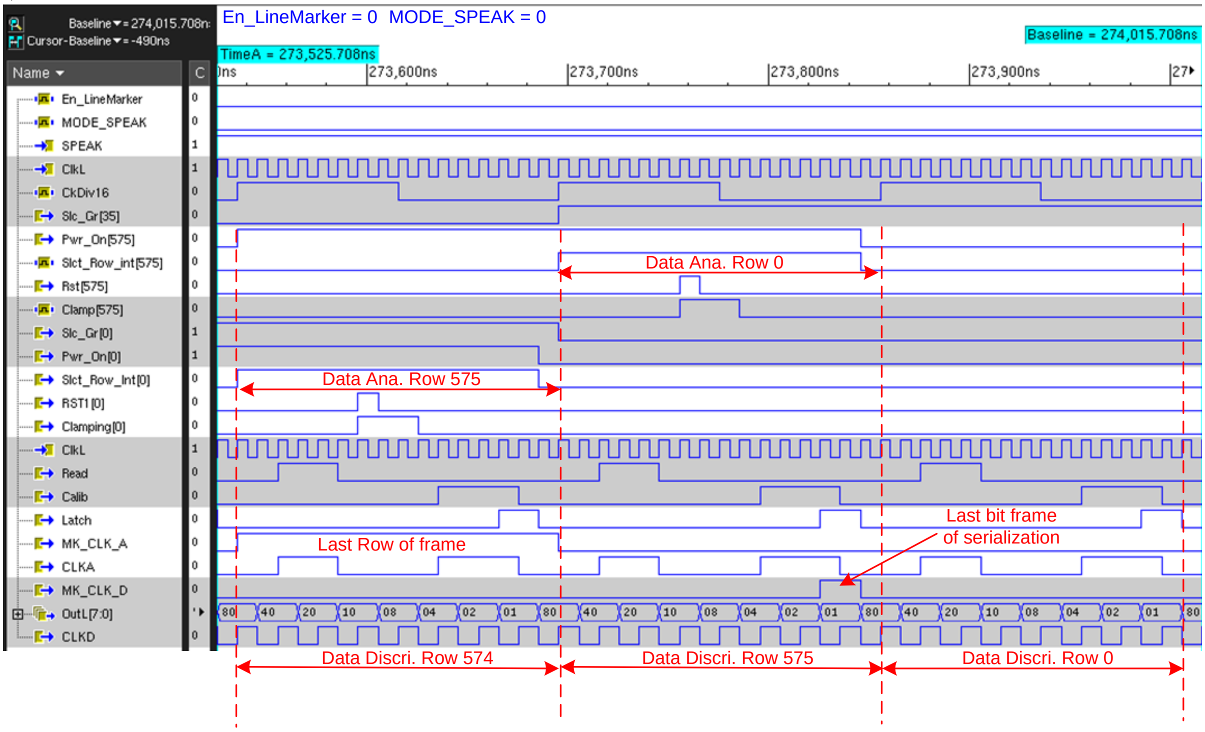


Figure 4

Figure 4 shows the last row readout followed by the first row of the next frame, when En_LineMarker is set to 1 and MODE_SPEAK is set to 0. These options are set via the RO_MODE0 register.

a)



b)

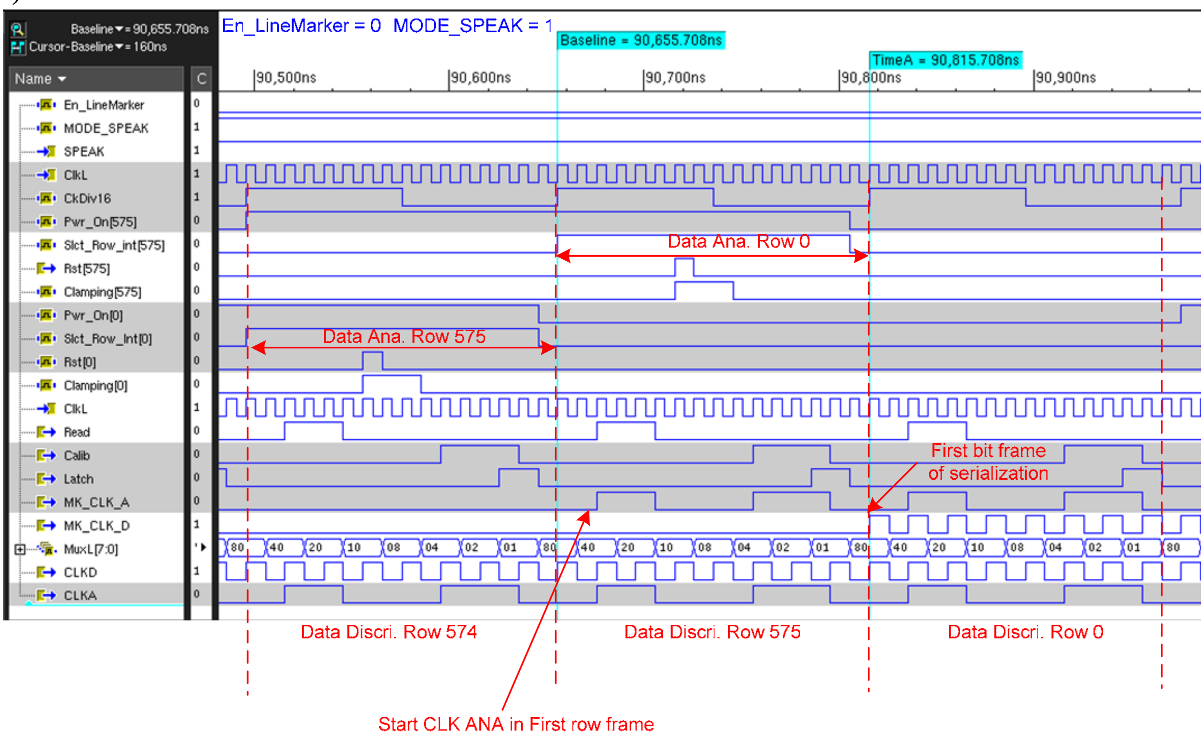


Figure 5

Figure 5 shows the last row readout followed by the first row of the next frame, when En_LineMarker is set to 0. For Figure 5.a MODE_SPEAK is set to 0, and for Figure 5.b MODE_SPEAK is set to 1.

3.6.3 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 µS	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 100 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	START Setup/Hold Time	5 nS	Chip Initialisation, CMOS signal.
	SPEAK Setup/Hold Time	5 nS	Active Readout Marker & Clock
Analogue Driver	Input Dynamic range		
	Rise time		
	Fall time		
	Bandwidth		
	Output Current Range		

4 Pad Ring

The pad ring of Mimosa22 is build with

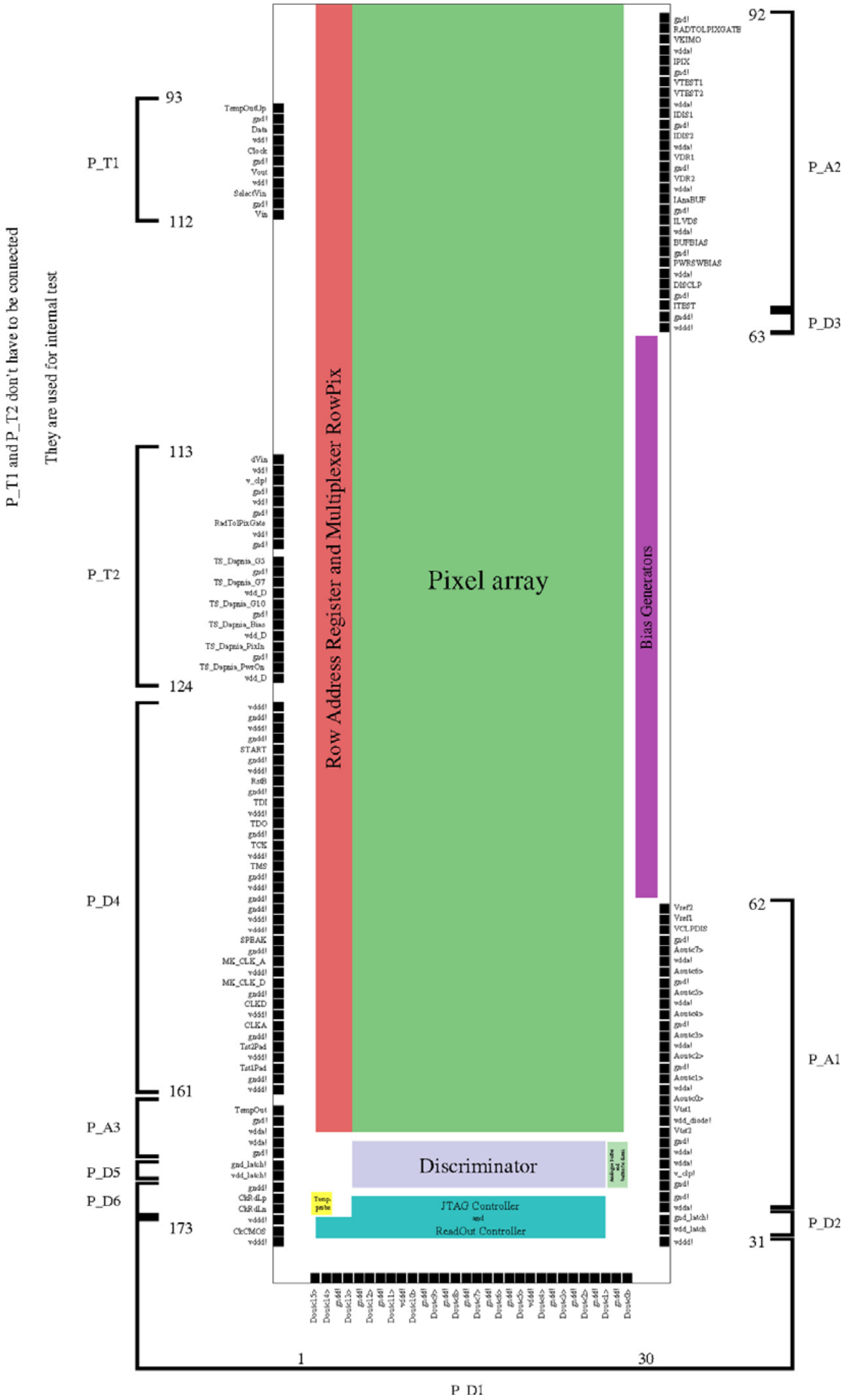
• Pads full custom designed for some of the analogue signals and power supplies
• Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 8 functional independent parts

- CMOS JTAG and Test purpose pads
- LVDS Read Out Drivers
- Digital outputs
- Read Out Analogue Outputs
- Bias Test
- Analogue and Digital Power supplies
- Test structure 1
- Test structure 2

Each part has its own supply pads.

4.1 Mimosa22 Pad Ring and Floor Plan View



4.2 Pad List

The bonding of the power supply pads specified in red colour is mandatory

Pad ring segment 1 – P_D1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
1	Dout<15>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 127-120
2	Dout<14>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 119-112
3	gnd	Output buffer ground	GND3OP	Output buffer ground
4	Dout<13>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 111-104
5	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
6	Dout<12>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 103-96
7	gnd	Output buffer ground	GND3OP	Output buffer ground
8	Dout<11>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 95-88
9	vdd	Output buffer supply	VDD3OP	Output buffer supply
10	Dout<10>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 87-80
11	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
12	Dout<9>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 79-72
13	gnd	Output buffer ground	GND3OP	Output buffer ground
14	Dout<8>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 71-64
15	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
16	Dout<7>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 63-56
17	gnd	Output buffer ground	GND3OP	Output buffer ground
18	Dout<6>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 55-48
19	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
20	Dout<5>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 47-40
21	vdd	Output buffer supply	VDD3OP	Output buffer supply
22	Dout<4>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 39-32
23	gnd	Output buffer ground	GND3OP	Output buffer ground
24	Dout<3>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 31-24
25	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
26	Dout<2>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 23-16-
27	gnd	Output buffer ground	GND3OP	Output buffer ground
28	Dout<1>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 15-8
29	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
30	Dout<0>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 7-0
31	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
173	CkCMOS	Clock buffer, 2 mA	ICCK2P	CMOS clock
174	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core

Pad ring segment 1 – P_D2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
32	vdd_latch	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core only for LATCH
33	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core only for LATCH

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Pad ring segment 1 – P_A1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
34	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
35	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
36	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
37	v_clp		DIRECTPAD	Clamping voltage for pixel array
38	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
39	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
40	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
41	Vtst2		DIRECTPAD	External injection of Vtest2
42	vdd_diode		DIRECTPAD	Detection diode supply (Dapnia Design)
43	Vtst1		DIRECTPAD	External injection of Vtest1
44	Aout<0>		DIRECTPAD	Analogue output
45	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
46	Aout<1>		DIRECTPAD	Analogue output
47	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
48	Aout<2>		DIRECTPAD	Analogue output
49	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
50	Aout<3>		DIRECTPAD	Analogue output
51	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
52	Aout<4>		DIRECTPAD	Analogue output
53	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
54	Aout<5>		DIRECTPAD	Analogue output
55	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
56	Aout<6>		DIRECTPAD	Analogue output
57	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
58	Aout<7>		DIRECTPAD	Analogue output
59	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
60	VCLPDIS		DIRECTPAD	External injection of Discri clamping
61	Vref1		DIRECTPAD	External injection of Discri Ref1
62	Vref2		DIRECTPAD	External injection of Discri Ref2

Pad ring segment 1 – P_D3				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
63	vdd	Core logic and periphery cells ground	AVDD3ALLP	Ground periphery & core only for DAC
64	gnd	Core logic and periphery cells supply	AGND3ALLP	Supplies periphery & core only for DAC

Pad ring segment 1 – P_A2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
65	ITEST	Analog I/O pad, 0 Ω serial	APRIOP	Reference current (1µA)
66	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
67	DISCLP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Output for Discri Clamping
68	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
69	PWRSWBIAS	Analog I/O pad, 0 Ω serial	APRIOP	Discri Power Pulse Voltage Bias
70	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
71	BUFBIAS	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Ref&Tst Buffer voltage bias
72	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
73	ILVDS	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: LVDS PAD voltage bias
74	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
75	IAnaBUF	Analog I/O pad, 0 Ω serial	APRIOP	Analogue Output Buffer bias
76	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
77	VDR2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Reference 2
78	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
79	VDR1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Reference 1
80	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
81	IDIS2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Bias 2
82	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
83	IDIS1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Bias 1
84	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
85	VTEST2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: VTEST2
86	VTEST1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: VTEST1
87	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
88	IPIX	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Pixel Array Bias
89	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
90	VKIMO	Analog I/O pad, 0 Ω serial	APRIOP	A reference voltage from DAC output
91	RADTOLPIXGATE	Analog I/O pad, 0 Ω serial	APRIOP	POLY Gate voltage for Andrei RadTol Pix
92	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core

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Pad ring segment 1 – P_D4				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
125	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
126	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
127	vdd	Output buffer supply	VDD3OP	Output buffer supply
128	gnd	Output buffer ground	GND3OP	Output buffer ground
129	START	CMOS Input Buffer	ICP	Readout: Input synchronisation
130	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
131	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
132	RstB	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Asynchronous Active Low Reset
133	gnd	Output buffer ground	GND3OP	Output buffer ground
134	TDI	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
135	vdd	Output buffer supply	VDD3OP	Output buffer supply
136	TDO	Tri-State Output Buffer, 4 mA	BT4P	JTAG Serial Data Out
137	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
138	TCK	CMOS Clock Input Buffer, 2 mA	ICCK2P	JTAG Clock
139	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
140	TMS	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
141	gnd	Output buffer ground	GND3OP	Output buffer ground
142	vdd	Output buffer supply	VDD3OP	Output buffer supply
143	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
144	gnd	Output buffer ground	GND3OP	Output buffer ground
145	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
146	vdd	Output buffer supply	VDD3OP	Output buffer supply
147	SPEAK	CMOS Input Buffer	ICP	Active Readout Marker & Clock
148	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
149	MK_CLK_A	Tri-State Output Buffer, 2 mA	BT2P	Readout: Analogue Marker & Clock
150	Vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
151	MK_CLK_D	Tri-State Output Buffer, 2 mA	BT2P	Readout: Digital Marker & Clock
152	gnd	Output buffer ground	GND3OP	Output buffer ground
153	CLKD	Tri-State Output Buffer, 2 mA	BT2P	Readout Digital clock
154	vdd	Output buffer supply	VDD3OP	Output buffer supply
155	CLKA	Tri-State Output Buffer, 2 mA	BT2P	Readout Analogue clock
156	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
157	Tst2Pad	Tri-State Output Buffer, 2 mA	BT2P	Readout Test Pad
158	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
159	Tst1Pad	Tri-State Output Buffer, 2 mA	BT2P	Readout Test Pad
160	gnd	Output buffer ground	GND3OP	Output buffer ground
161	vdd	Output buffer supply	VDD3OP	Output buffer supply

Pad ring segment 1 – P_A3				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
162	TempOut	Direct Pad, no protections	DIRECTPAD	Temperature probe output
163	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core
164	vdda	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core
165	vdda	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core
166	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core

Pad ring segment 1 – P_D5				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
167	vdd	Core logic and periphery cells supply	VDD3ALLP	Supplies periphery & core for DAC
168	gnd	Core logic and periphery cells gnd	GND3ALLP	Ground periphery & core for DAC

Pad ring segment 1 – P_D6				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
169	gnd	Core logic and periphery cells ground	GND3ALLP	Ground periphery & core
170	CkRdLp	LVDS In +	Full Custom	Readout Clock Signal
171	CkRdLn	LVDS In -	Full Custom	Readout Clock Signal
172	vdd	Core logic and periphery cells supply	VDD3ALLP	Supplies periphery & core

Pad ring segment P_T1 (Pad 94 to 112) and Pad ring segment P_T2 (Pad 113 to 124) are used only for internal test.