Atlas SCT Off-Detector Laboratory Electronics

OptIF-B User Manual

Maurice Goodrick, University of Cambridge, Cavendish Labs

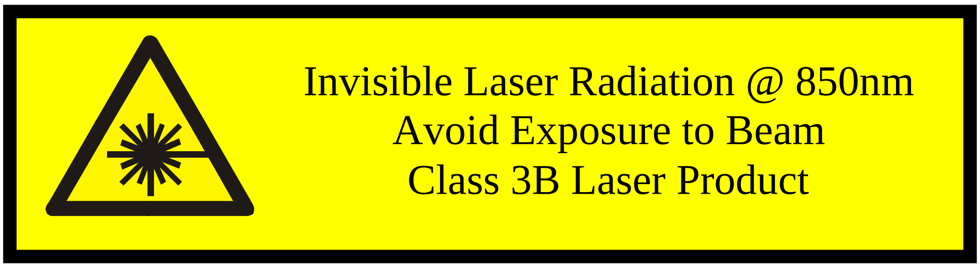
This is a Preliminary Version.

1. Introduction

OptIF-B is an Opto-Electrical Interface for use by the Atlas SCT community primarily during the development phase of the Silicon Detector Modules. It is intended as a companion to the MuSTARD Data Acquisition module, and the SLOG Command and Clock Generation module. In common with these, it is in a standard 6U VME format. OptIF-B is a development of OptIF.

2. Safety

OptIF-B houses an array of 12 VCSEL lasers. These can each emit up to 1mW of average optical output at 850nm wavelength. A safety guard with electrical interlock is provided, and must be used as intended. The user must take relevant action to ensure operation within statutory regulations, which may depend on the country of use.



3. Outline Functionality

Fig 1 shows the Block Diagram and Layout of OptIF-B.

- OptIF-B processes 12 Command streams:
  - Commands and Clocks are accepted from the 50-way front panel connector
  - The 12 Command Streams and one of the Clocks are combined using Bi-Phase-Mark (BPM) encoding
  - The BPM signals are used to drive an array of 12 VCSELs (Lasers) with a connector interface to a 12-fibre ribbon
- OptIF-B also processes 12 streams of Optical Data:
  - accepts Data on a 12-fibre ribbon
  - converts to electrical signals
- There is provision to monitor laser output
- The infra-structure is included to allow control of laser temperature

4. Detailed Functionality

4.1. Clock and Command

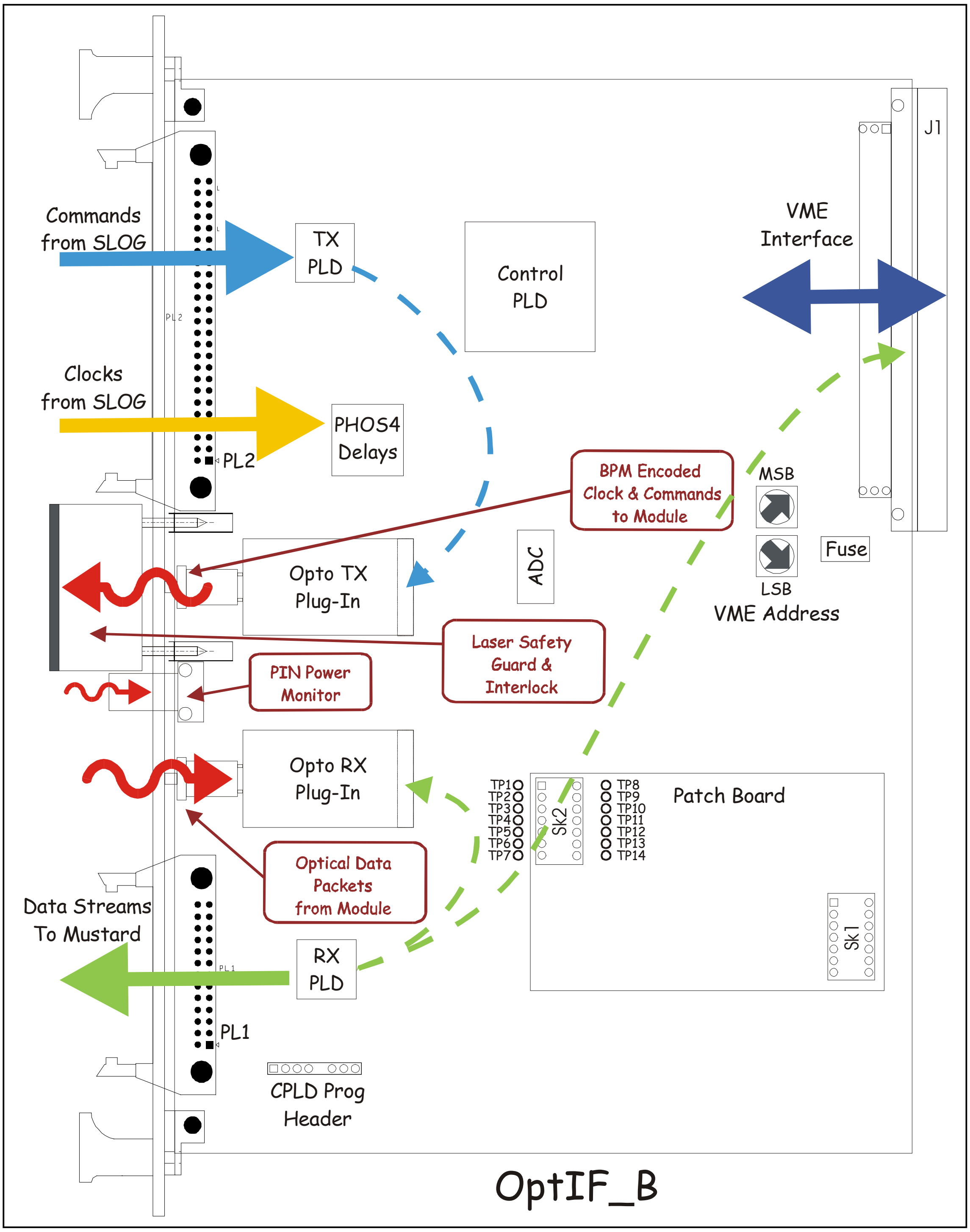
- Clocks and Commands are accepted from the 50-way front panel connector PL2 as differential LVDS signals. These are 100 Ohm terminated on board.
- 4 of the available SLOG clocks are used for various on-board clocking functions, as described below.
- The Command Streams pass through the TX- CPLD, which can perform a variety of operations for lab work: normally the data is passed straight through to the Opto-TX Plug-In. Four TX-MODE control bits can be set to select the action of the TX-CPLD.
- The Opto-TX Plug-In is the same as that used by the Atlas SCT Back-Of-Crate card. It uses a BPM12 chip to combine the Clock and Commands using Bi-Phase-Mark encoding, and to drive the 12-stream VCSEL array with an MT12 fibre connector interface to a 12-way fibre ribbon. On board DACs allow the laser currents to be independently adjusted. Registers in the BPM12 allow control of the BPM signals.

4.2. Data Streams

- Optical data is received via an MT12 fibre ribbon connector by the Opto-RX Plug-In. This is the same as those used by BOC (but see note in the Reference section)
- The Opto-RX has an array of 12 PIN diodes connected to a DRX ASIC. On-board DACs allow the threshold to be adjusted
- The data streams pass through the RX-CPLD: in normal mode this simply passes the asynchronous data on to the 26-way front panel connector PL1 as LVDS signals
- The operation of the RX-CPLD is selected by 4 RXMode control bits
- Pre defined modes are: NORMAL - asynchronous data, 1-to-1 stream mapping, and PIXEL - data on 6 fibres (2-7 of 0-11) is clocked at 40MHz at two different phases to provide 12 40MS/s LVDS data streams.
- There is provision to pass the data outputs of the RX-CPLD to VME. This gives the possibility of doing data "Snap-Shots" and capturing short time sequences (but only with additions to the firmware in the RX-CPLD)
- The TX-CPLD can also be re-programmed via the CPLD Programming Header

4.3. The VME Interface

- The VME Interface is A24D16 Slave
- it responds to Standard Non-Privileged Data Transfers (AM[5:0] = 0x39) and to Standard Supervisory Data Transfers (AM[5:0] = 0x3D)
- the top 8 bits of the VME address (A[23:16]) are tested against the setting of 2 hex switches
- all useful registers and functions are accessed through a window of 256 word addresses, corresponding to A[8:1]
- Address bits A[15:9] are not tested
- Thus, if the switch settings are ML ("MS" and "LS" switches), the module occupies the address space from 0xML0000 to 0xMLfffe. But only even addresses in the range 0xML0000 to 0xML01fe need be used.



- VME transfers are accepted without Bus Error for the entire occupied address space, even if the particular address has no defined function. Data returned from unassigned addresses is undefined.
- Some operations started by VME access take a substantial time to complete. These "slow" operations are: Writing to the Laser Current and Threshold MultiDACs, Writing to the Delay chips, and Converting the Laser Power sample to digital form ready for reading. There is no pipelining of operations, so conflicts may occur if further slow operations are attempted. More information is given in the Reference section of this document.

4.4. Extended Features

- There is a PIN diode in an ST fibre connector housing together with amplifier and ADC converter intended for monitoring average laser power. One or more of the 12 command streams can be coupled back into this using a suitable fibre harness.

- It is foreseen that controlling the temperature of the VCSELs may help with power stability in sensitive applications. Accordingly, the Opt-TX Plug-In can be equipped with a Peltier heat pump and temperature sensor. There is a site for a Patch Board with 14 uncommitted connections plus access to the power rails.
- It is also foreseen that this module could be used for the generation of Module Test Data (both Strip and Pixel), but this will rely on the availability of an Opto-TX without BPM encoding
- The TX-CPLD, the RX-CPLD and the Control CPLD can be re-programmed via the CPLD Programming Header, but this requires detailed understanding of the hardware, as well as access to the appropriate Lattice CAD and JTAG Download software.
- The data outputs of the RX-CPLD are accessible from the VME data bus under the control of the Control CPLD: this gives the possibility of readily adding features found useful in BOC testing (using the BOC-RIG module):
  - Doing a data snap shot
  - And, with additions to the RX-CPLD, being able to record a short sequence of data that can subsequently be read-out over VME

5. Reference Section

5.1. Front Panel Connectors PL1 and PL2

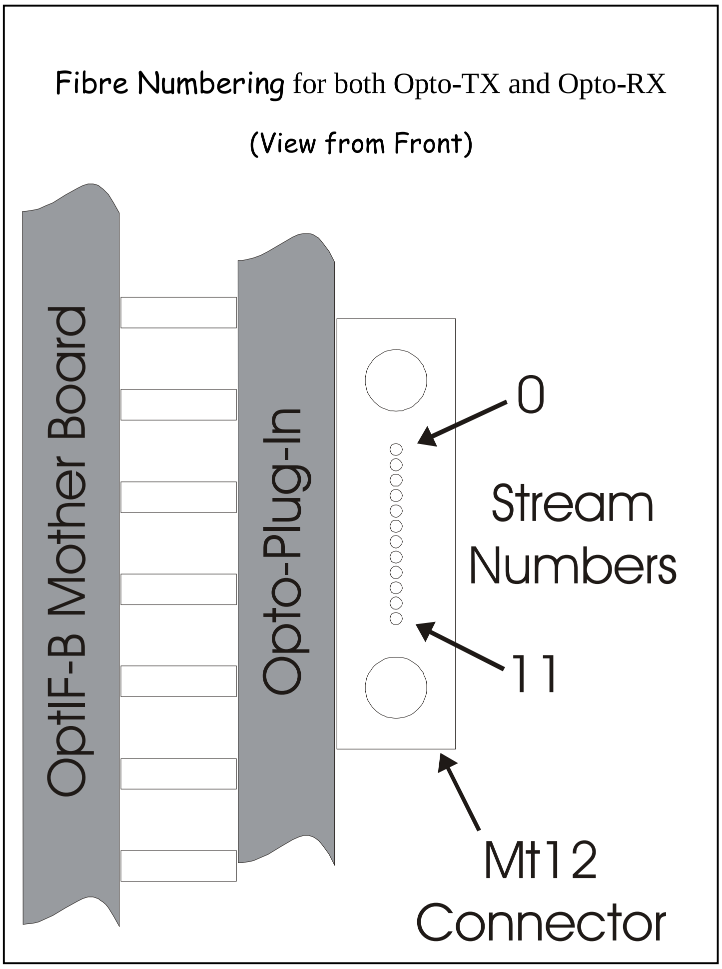
Gnd	26	25	Gnd
D11-			D11+
D10-			D10+
D9-	20	19	D9+
D8-			D8+
D7-			D7+
D6-			D6+
D5-			D5+
D4-	10	9	D4+
D3-			D3+
D2-			D2+
D1-			D1+
D0-	2	1	D0+

PL1: MuSTARD Connections

Gnd	50	49	Gnd
D11-			D11+
D10-			D10+
D9-			D9+
D8-			D8+
D7-	40	39	D7+
D6-			D6+
D5-			D5+
D4-			D4+
D3-			D3+
D2-	30	29	D2+
D1-			D1+
D0-			D0+
NC			NC
NC			NC
NC	20	19	NC
NC			NC
NC			NC
NC			NC
NC			NC
NC	10	9	NC
CK3-			CK3+
CK2-			CK2+
CK1-			CK1+
CK0-	2	1	CK0+

PL2: SLOG Connections

5.2. MT12 Fibre Connectors



Fibre Numbering for both Opto-TX and Opto-RX

(View from Front)

5.3. Address Maps

- The **TOP-LEVEL** Address Map gives an overview, and the detail is given by:
- **Detailed** Address Map, and
- **BPM12** Address Map

TOP-LEVEL Address Map

OptIF_B VME Address Map (add Base Address)

VME Offset Byte	VME Offset Word	Function
0F8	7C	
0F0	78	
0E8	74	
0E0	70	
0D8	6C	
0D0	68	
0C8	64	
0C0	60	
0B8	5C	
0B0	58	
0A8	54	
0A0	50	
098	4C	
090	48	RX_DACs - Thresholds
088	44	
080	40	
078	3C	
070	38	
068	34	
060	30	
058	2C	
050	28	
048	24	
040	20	
038	1C	
030	18	
028	14	
022	11	
018	0C	Clock Phases
010	08	OptIF-B Registers
008	04	
000	00	OptIF-B Info

VME Offset Byte	VME Offset Word	Function
1F8	FC	
1F0	F8	
1E8	F4	
1E0	F0	
1D8	EC	
1D0	E8	
1C8	E4	
1C0	E0	
1B8	DC	
1B0	D8	
1A8	D4	
1A0	D0	
198	CC	
190	C8	TX_DACs - Laser Currents
188	C4	
180	C0	
178	BC	
170	B8	
168	B4	BPM12
160	B0	
158	AC	
150	A8	
148	A4	
140	A0	
138	9C	
130	98	
128	94	
120	90	
118	8C	
110	88	
108	84	
100	80	

Accessing Byte Addresses 0200 to FFFF is Not Defined
(Address Bits A[15:9] are ignored)

Detailed Address Map

VME Offset Byte	VME Offset Word	Hard-ware	Bits Used	Access	Description	Acts On
1FE	FF	^	^		^	^
^	^	^		Unused		^
198	CC	^	^		^	^
196	CB	TX_DAC_HI	bit[7:0]	Write	BPM12 Current Controls: 0-255 for approx. 0-18mA	Current for Laser 11
194	CA		bit[7:0]	Write		Current for Laser 10
192	C9		bit[7:0]	Write		Current for Laser 9
190	C8		bit[7:0]	Write		Current for Laser 8
18E	C7		bit[7:0]	Write		Current for Laser 7
18C	C6		bit[7:0]	Write		Current for Laser 6
18A	C5	TX_DAC_LO	bit[7:0]	Write		Current for Laser 5
188	C4		bit[7:0]	Write		Current for Laser 4
186	C3		bit[7:0]	Write		Current for Laser 3
184	C2		bit[7:0]	Write		Current for Laser 2
182	C1		bit[7:0]	Write		Current for Laser 1
180	C0		bit[7:0]	Write		Current for Laser 0
^	^	^		Unused		^
16E	B7	BPM 12	See Separate Table for BPM Addressing			
^	^					
102	81					
100	80					
^	^	^		Unused		^
096	4B	RX_DAC_Odd	bit[7:0]	Write	DRX12 Thresholds: 0-255 for 0-255uA	Threshold for Stream 11
094	4A	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 10
092	49	RX_DAC_Odd	bit[7:0]	Write		Threshold for Stream 9
090	48	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 8
08E	47	RX_DAC_Odd	bit[7:0]	Write		Threshold for Stream 7
08C	46	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 6
08A	45	RX_DAC_Odd	bit[7:0]	Write		Threshold for Stream 5
088	44	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 4
086	43	RX_DAC_Odd	bit[7:0]	Write		Threshold for Stream 3
084	42	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 2
082	41	RX_DAC_Odd	bit[7:0]	Write		Threshold for Stream 1
080	40	RX_DAC_Even	bit[7:0]	Write		Threshold for Stream 0
^	^	^		Unused		^
020	10	Clock Phases	bit[4:0]	Write	PHOS4 Delays: 0-24 ns	BPM Clock
01E	0F		bit[4:0]	Write		TX_Clock1
01C	0E		bit[4:0]	Write		TX_Clock0
01A	0D		bit[4:0]	Write		RX_Clock1
018	0C		bit[4:0]	Write		RX_Clock0
016	0B	OptIF-B Registers			Spare	Reserved
014	0A				Spare	Reserved
012	09				Spare	Reserved
010	08		bit[7:0]	Read	Monitor ADC	Laser Power Monitor
00E	07		bit[6,0]	R-W	Control Word	Control/Status in a Word
00C	06		bit[1,0]	R-W	Resets	MDAC_Reset,BPM_Reset
00A	05		bit[3:0]	R-W	TX_Mode	Command Stream Mode
008	04		bit[3:0]	R-W	RX_Mode	Data Stream Mode
006	03	OptIF-B Info	bit[7:0]	Read	Manuf	CB (Hex)
004	02		bit[7:0]	Read	Module Type	45 (Dec)
002	01		bit[7:0]	Read	Module Vers	00-FF
000	00		bit[7:0]	Read	Firmware Vers	00-FF

Notes:

1. The Control/Status Word has no Write action at present. The bits are:

   [x,x,x,x,LaserBlockIn,ADCBusy,MDAC_Busy,ClockPhase_Busy]

BPM12 Address Map

BPM12 Registers (BPM12 Registers are Read-Write)

Byte Address	Word Address	Laser Number	Function	Bits	Reset Value (Hex)
16E	B7	None	Test Circuit Control Word 1 Bit 6 (0x40) Inhibits Internal Clock	?	?
16C	B6				
16A	B5				
168	B4				
166	B3	None	Test Circuit Control Word 0 Bit 5 (0x20) Inhibits RAND & TRIG O/Ps	?	?
164	B2				
162	B1				
160	B0				
15E	AF	11	Fine Delay	6:0	0
15C	AE	11	Coarse Delay	4:0	0
15A	AD	11	Mark-Space	4:0	13 (~50%)
158	AC	11	Stream Inhibit	0:0	0 (=Enabled)
156	AB	10	Fine Delay	6:0	0
154	AA	10	Coarse Delay	4:0	0
^	^	^	^	^	^
^	^	^	^	^	^
12A	95	5	Mark-Space	4:0	13 (~50%)
128	94	5	Stream Inhibit	0:0	0 (=Enabled)
126	93	4	Fine Delay	6:0	0
124	92	4	Coarse Delay	4:0	0
122	91	4	Mark-Space	4:0	13 (~50%)
120	90	4	Stream Inhibit	0:0	0 (=Enabled)
11E	8F	3	Fine Delay	6:0	0
11C	8E	3	Coarse Delay	4:0	0
11A	8D	3	Mark-Space	4:0	13 (~50%)
118	8C	3	Stream Inhibit	0:0	0 (=Enabled)
116	8B	2	Fine Delay	6:0	0
114	8A	2	Coarse Delay	4:0	0
112	89	2	Mark-Space	4:0	13 (~50%)
110	88	2	Stream Inhibit	0:0	0 (=Enabled)
10E	87	1	Fine Delay	6:0	0
10C	86	1	Coarse Delay	4:0	0
10A	85	1	Mark-Space	4:0	13 (~50%)
108	84	1	Stream Inhibit	0:0	0 (=Enabled)
106	83	0	Fine Delay	6:0	0
104	82	0	Coarse Delay	4:0	0
102	81	0	Mark-Space	4:0	13 (~50%)
100	80	0	Stream Inhibit	0:0	0 (=Enabled)

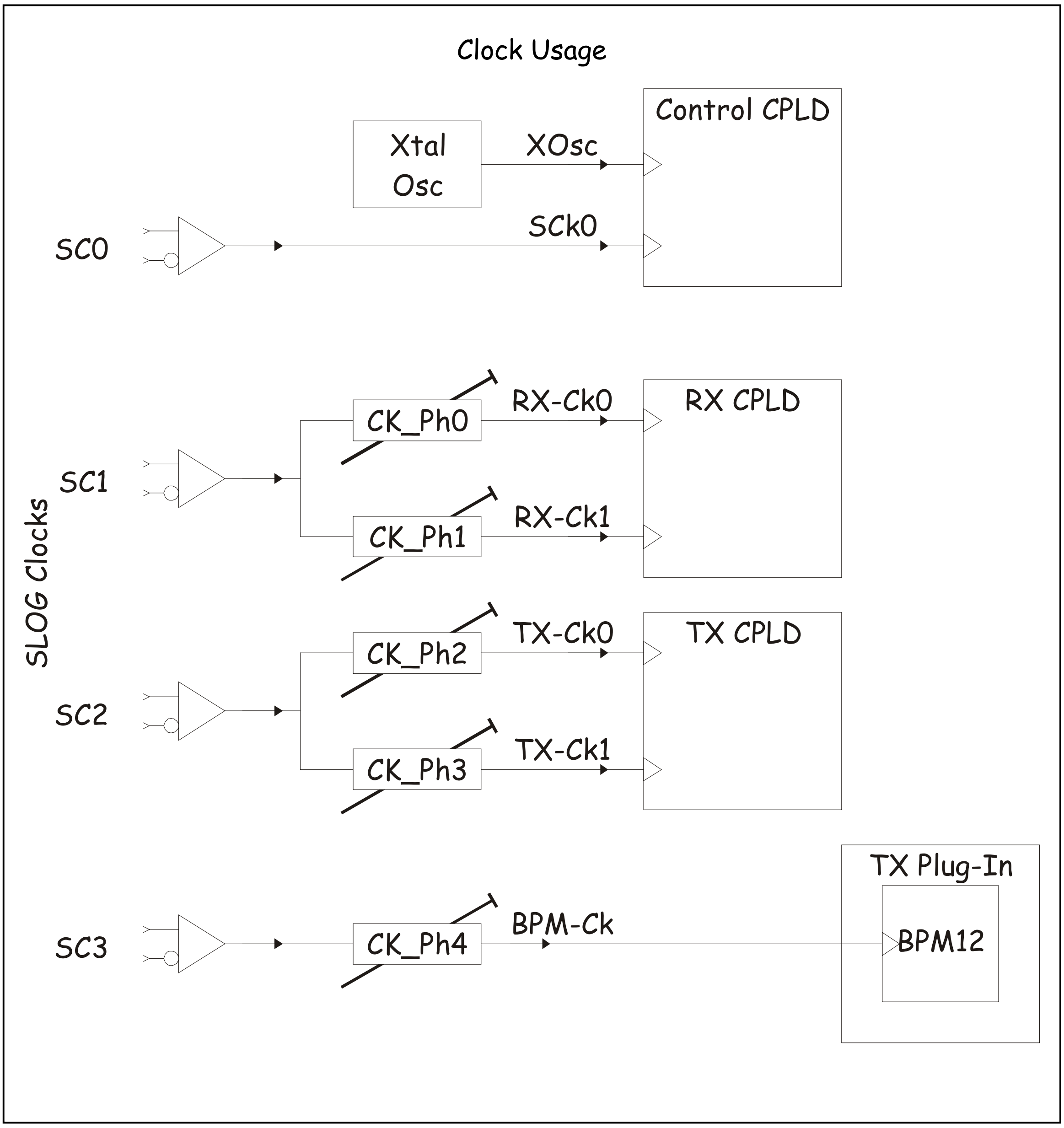
Notes:

1. To ensure the BPM internal test circuits are inactive, write 0x20 to MLx160 and 0x40 to MLx168
2. BPM registers are Read/Write: unused bits are undefined when Read, Don't-Care when Written

5.4. Clocks

The 4 Clock inputs are used as shown below.

See Detailed Address Map for addresses of the Clock Phases. These are Write-Only. Valid settings are 0-24, giving phase adjustment over the full 25ns period in 1ns steps. Settings outside the range 0-24 will not give valid clocks. Note also that the PHOS4 delay chips used need to be reset after power up by issuing a dummy Write command. Writing any delay value to any delay stream will do this, but note that the SLOG clocks should be turned on first.



5.5. Data Thresholds: RX-DACs

- Write-Only - Slow Operation
- Set to 0-255 for Thresholds of 0-255uA (approx. 0-500uW optical power)
- These (and the Laser Currents) are all set to 0 by asserting the MDAC_Reset bit (bit 1) in the OptIF-B Reset register (address MLx00c)

5.6. Laser Currents: TX-DACs

- Write-Only - Slow Operation
- Set to 0-255. This is a non linear control: there is around 1mA of laser current up to a setting of around 95. Thereafter the current increases roughly linearly to around 18mA for a setting of 255. Lasing will not start until the threshold current is reached (around 3mA). The maximum power output per laser (with the currently available Opto-TX Plug-Ins) is 2200uW (1200uW average over any 50ns period).
- These (and the Data Thresholds) are all set to 0 by asserting the MDAC_Reset bit (bit 1) in the OptIF-B Reset register (address MLx00c)

6. Sample Initialisation Procedure

```
// ********************************************************
short init_IFB(short p) // This routine may contain some debris
// ********************************************************
{ short dd,ee,ff,stream,dacv ;
  unsigned short errors;
// Laser DAC settings
  short int lasi[12]= {0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0,0xc0} ;

 printf("OptIF-B Module Info:\n");
 VXIpeek(IFB_CREGS+0x2,2,&ee); // Read Module Type
 VXIpeek(IFB_CREGS+0x1,2,&ff); // Read Module Version
 printf("..Module Type and Version is: %03iv%02X\n", ee & 0xFF, ff & 0xFF) ;
 VXIpeek(IFB_CREGS+0x3,2,&ee); // Read Module Manuf
 printf("..Manufacturer is: %02X\n", ee & 0xFF) ;
 VXIpeek(IFB_CREGS+0x0,2,&ee); // Read Firmware version
 printf("..Firmware version is: %03i\n\n", ee & 0xFF) ;
//
//  first set up PHOS4s to ensure there's a 40MHz clock
//   ... Note SLOG will need clocks enabling first
 VXIpoke(IFB_CLOX+0,2,0) ; // Dummy
 VXIpoke(IFB_CLOX+0,2,0) ; // RX_Clock0
 VXIpoke(IFB_CLOX+1,2,0) ; // RX_Clock1
 VXIpoke(IFB_CLOX+2,2,0) ; // TX_Clock0
 VXIpoke(IFB_CLOX+3,2,0) ; // TX_Clock1
 VXIpoke(IFB_CLOX+4,2,0) ; // BPM_Clock
// Now reset BPM and DACs:
  VXIpoke(IFB_CREGS+6,2,3);
  VXIpoke(IFB_CREGS+6,2,0);
// now rest of CREGS
 VXIpoke(IFB_CREGS+4,2,0); // RXMode
 VXIpoke(IFB_CREGS+5,2,0); // TXMode
//
dacv  = 0x80 ;  // Ball park ... 16-Nov-02
// now set up TXDACS and BPM registers to defaults
  for(stream=0;stream<12;stream++) // set up DACs
  { VXIpoke(IFB_TXDAX+stream,2,lasi[stream]); // laser currents
    VXIpoke(IFB_RXDAX+stream,2,dacv);         // Thresholds
  }
// Common BPM Registers
   VXIpoke(IFB_BPM+0x30,2,0x20); // Inhibit RAND and TRIGGER Outputs
   VXIpoke(IFB_BPM+0x34,2,0x40); // Inhibit Internal Clock
   for(stream=0;stream<12;stream++) // per stream BPM registers
   { VXIpoke(IFB_BPM+0+4*stream,2,0x00); // Stream Inhibit=0 (0 or 1)
     VXIpoke(IFB_BPM+1+4*stream,2,0x12); // Mark-Space   (0-0x1f)
     VXIpoke(IFB_BPM+2+4*stream,2,0x00); // Coarse delay (0-0x1f)
     VXIpoke(IFB_BPM+3+4*stream,2,0x00); // Fine delay   (0-0x7f)
   }
  return(0);
} // ********************************************************
```

7. Additional Info

- Opto-Plug-Ins … connectors: the Opto Plug-Ins available to date use an array of individual pins as the connector to the motherboard (34 for the Opto-RX, 38 for the Opt-TX). Future Plug-Ins will use a 40-pin Samtec connector with 0.8mm spacing. An adapter card will be available to allow the new Plug-Ins to be used on OptIF-B.
- Slow Operations:
    - Laser Current settings .. take about 20us to complete
    - Data Threshold settings.. take about 20us to complete
    - Clock Phase settings .. take about 200us to complete

  The general idea is that starting such operations will not result in the VME transfer being held up. But any subsequent VME Write to OptIF-B will be held up until the slow operation is complete (the VME Acknowledge is withheld). Such a "hang-up" can be avoided by Reading the OptIF-B Status word - Reads are not held up by any slow operations - and looking at the MDAC_Busy and ClockPhase_Busy bits (bits 1 and 0). The following IFB_WPOKE() function does this testing before writing:

```
// ********************************************************
void IFB_WPOKE(unsigned short *addptr, UINT16 a)
// ********************************************************
{      UINT16 count,busy;
    busy = 1;
      for(count = 0;((count<1000) && busy);count++)
      {  VXIpeek(IFB_CREGS+7,2,&busy);
         busy = busy & 0x3;}
      if (count < 1000)
      { VXIpoke(addptr,2,a);
        return;}
      else
      { printf("IFB_WPOKE: timeout\a\n");
        return;}
}
// ********************************************************
```

- Reading the Laser Power Monitor (not yet fully implemented) is also a slow operation involving starting a conversion that takes about 1.5us to produce an answer for reading. The plan is that the first read yields rubbish data, but kicks off a sample and conversion. Bit 2 of the Status word (ADCBusy) goes high until the conversion is complete. The next Read of the Power Monitor gives the reading, and kicks off another conversion.
- Sample Initialisation Procedure for OptIF-B

…ooOoo…