

## Description

The ISL54065EVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54065 IC.

The ISL54065 IC is a single supply Dual Single-Pole Double Throw (SPDT) analog switch with negative swing capability, sub- $\Omega$  ON-resistance and low power dissipation. The ISL54065 is designed for applications that require an analog switch that may see voltages below ground at the switch terminals, such as audio and video. The ISL54065EVAL1Z evaluation board is developed to evaluate the ISL54065 IC, integrating many features for ease of use in examining the performance of the device under various operating conditions. To help understand the operation of the ISL54065 IC and the ISL54065EVAL1Z evaluation board, it is recommended to study the Evaluation Board Schematic on page 5 of this application note, and refer to the datasheet for the ISL54065 IC.

The ISL54065 IC is a dual SPDT analog switch that is capable of swinging down to 6.5V below the positive supply rail. For example, if the supply is at +1.8V, the switch terminal analog operating range is from -4.3V to +1.8V. The ISL54065 also integrates Click and Pop Elimination Circuitry to remove transient noises at the speaker during power ON/OFF of an audio system. The evaluation board contains standard RCA/BNC connectors and a single headphone jack to allow the user to easily interface with the IC to evaluate its functions, features, and performance. The evaluation board has selectable output loads of 20k $\Omega$  and 32 $\Omega$  resistors to simulate an audio amplifier pre-amp or stereo headphones. The board also has DC blocking capacitors at the switch input to remove the DC bias of single supply amplifiers.

This application note will guide the user through the process of configuring and using the evaluation board to evaluate the ISL54065 device.

## Key Features

- Selectable Output Resistive Loads and Input DC Blocking Capacitors
- RCA Audio Input/Output Jacks, Stereo Headphone Output Jack and BNC Connectors
- Convenient Test Points and Connections for Test Equipment
- Click and Pop Elimination Circuitry
- Manual or External Logic Input Control

## Picture of Evaluation Board (Top View)



FIGURE 1. ISL54065EVAL1Z EVALUATION BOARD

## Board Architecture/Layout

### Basic Layout of Evaluation Board

A picture of the evaluation board is located in Figure 1. The ISL54065 IC is soldered onto a 12 Ld wide DIP header board. The DIP header board is mounted to the center of the evaluation board. The evaluation board integrates the necessary connections and components to interface with the ISL54065 for ease of operation.

### Power Supply

The ISL54065 IC requires a supply voltage in the range of +1.8V to +6.5V for proper operation. Banana jacks for  $V_{CC}$  (J1) and GND (J2) are located at the top of the board. The evaluation board contains a 10 $\mu$ F bulk capacitor and a 0.1 $\mu$ F high frequency decoupling capacitor at the supply lines.

### Logic Control

The evaluation board contains two types of logic control to the digital logic inputs of the ISL54065 IC available to the user. The logic pins can be controlled either through manual or external operation. The logic control pins are manually toggled by the SPST switches mounted on the evaluation board (S1-S3). When the switch is in the up position (H) the associated logic pin is pulled to  $V_{CC}$  for logic HIGH. When the switch is in the down position (L) the associated logic pin is pulled to GND for logic LOW. For manual operation, the jumpers JP5-JP8 need to be in the 1-2 position.

Note: When JP6 is in the 1-2 position, the CP pin is automatically logic HIGH.

For external control via a function generator or switched source, set the jumpers JP5-JP8 in the 2-3 position. This

by-passes the SPST switches and routes the logic control to the BNC connectors (J11-J14 located on the right side of the board).

Note: S2 and S3 have a 3.9M $\Omega$  pull-down resistor hard-wired from the INx pin to GND. These resistors do not appear on the ISL54065EVAL1Z Board Schematic on page 5.

### Switch Terminals

The evaluation board contains components to interface with all six terminals of the Dual SPDT switch. The common (COM) terminals of the switch are located in the upper right section of the evaluation board. The Normally Open (NO) and Normally Closed (NC) terminals of the switch are located on the left side of the evaluation board. All switch terminals include both RCA jacks and BNC connectors. The COM terminals also include a headphone jack (HJ1) for connecting a stereo headphone or line level plug.

Refer to Table 1 for a list of the pins on the ISL54065 IC and the associated components on the evaluation board. The evaluation board also includes Test Points for convenient locations to probe specific pins on the IC.

**TABLE 1. BOARD COMPONENT TABLE**

ISL54065 PIN	EVALUATION BOARD CONNECTION	TEST POINT
VCC	J1	TP1
GND	J2	TP2
EN	S1, J11	TP7
CP	J12	TP8
IN1	S2, J13	TP9
IN2	S3, J14	TP10
NO1	J3, J4	TP3
NC1	J5, J6	TP4
COM1	J15, J16, HJ1	TP11
NO2	J9, J10	TP6
NC2	J7, J8	TP5
COM2	J17, J18, HJ1	TP12

Note: The audio inputs (NCx and NOx) have a 200 $\mu$ F series DC blocking capacitance that can be used for AC coupling audio signals that are DC biased in single supply systems. If the audio source is not DC biased or if the audio source already has a DC blocking capacitor, it is recommended to bypass the capacitors (C3-C10) by placing jumpers on JP1-JP4. The capacitance can be reduced to 100 $\mu$ F by depopulating the 0 $\Omega$  resistor on R1-R4.

The audio outputs (COM1 and COM2) have selectable output loads on the evaluation board. Jumpers JP9 and JP10 configure the output load resistance. When the jumpers are in the 1-2 position, the load impedance is 32 $\Omega$ .

When the jumpers are in the 2-3 position, the load impedance is 20k $\Omega$ . If the user decides to have no load impedance on the evaluation board, simply remove the jumpers.

### Power Supply

The DC power supply connected at banana jacks J1 (VCC) and J2 (GND) provides power to the evaluation board. The evaluation board requires a +1.8V to +6.5V DC power supply for proper operation. The power supply should be capable of delivering 100 $\mu$ A of current.

### Logic Control

The state of the ISL54065 device is determined by the Truth Table as defined in the ISL54065 datasheet. When in manual operation mode, the logic being toggled by the SPST switches (S1-S3) will always drive the voltage of the logic pin to V<sub>CC</sub> for a HIGH and GND for a LOW. In external control mode, the voltages being driven by an external source must meet appropriate V<sub>IH</sub> and V<sub>IL</sub> levels as defined in the datasheet.

The control pins are 1.8V logic compatible up to a +3.3V supply, which allows for control via a standard  $\mu$ controller.  
 Logic "0" (LOW) when  $\leq 0.5V$   
 Logic "1" (HIGH) when  $\geq 1.4V$

When operating above +3.3V supply, refer to the datasheet for appropriate logic levels to drive the logic pins. It is always recommended to drive the logic pins to the positive supply rail (V<sub>CC</sub>) and GND to minimize power consumption.

### Logic States

#### INPUT SELECT (INX) PINS

If the INx Pins are logic "HIGH", then the NOx switches are turned ON and the NCx switches are turned OFF. If the INx Pins are logic "LOW", then the NCx switches are turned ON, and the NCx switches are turned OFF.

#### ENABLE (EN) PIN

If the EN Pin is logic "HIGH" the switches are active and their logic state dependent on the INx pins. If the EN Pin is logic "LOW", both COMx terminals are turned OFF from the NCx and NOx switch terminals. The part is disabled and no signals will pass through the switch.

#### CLICK AND POP (CP) PIN

If the CP Pin is logic "HIGH", shunt resistors are activated on the NOx and NCx terminals to ground when the switch is OFF. For example, if INx is logic "HIGH", the NCx switches are turned OFF. There will be a shunt resistance from the NCx to ground. The value of this resistor is dependent on supply voltage, but is typically 140 $\Omega$  with a 3.3V supply.

Driving the CP pin logic "LOW" will deactivate the Click and Pop Elimination Circuitry and there will be no active shunt resistors on the switch terminals when a switch is turned OFF.

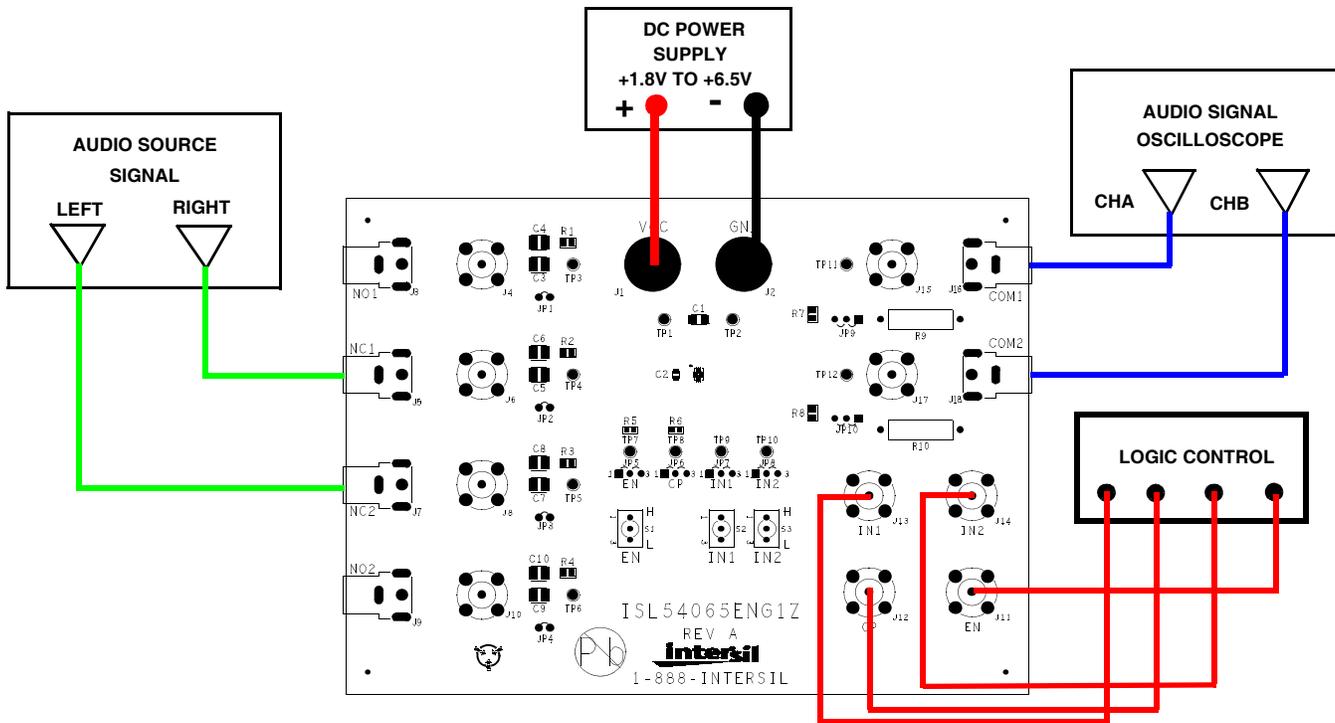


FIGURE 2. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

Note: If the CP is logic “HIGH”, and EN is logic “LOW”, the NCx and the NOx switch terminals will have the Click and Pop Elimination Circuitry active. Under this scenario, both switch terminals will have a shunt resistor to ground.

### CLICK AND POP OPERATION

Single supply audio sources are biased at a DC offset that generates transients during power ON/OFF of the audio source. This DC offset is coupled through a blocking capacitor that is needed to remove the DC bias to the speaker, causing a transient voltage at the load. For example, when the source is OFF and suddenly turned ON with a DC offset, the capacitor will develop a voltage equal to the DC offset. If the ISL54065 does not have the Click and Pop Elimination Circuitry active, a transient discharge will occur in the speaker, generating a Click and Pop noise.

For proper operation of Click and Pop elimination, the switch terminal that is being connected to the speaker should be

connected through the shunt resistor before connecting to the load. This allows any transients generated by the source to be discharged through the shunt resistor first, eliminating any audible click and pop noises. With a typical DC blocking capacitor of 200 $\mu$ F and the shunt resistance having a typical value of 140 $\Omega$ , allowing a 250ms dead time in for discharging a transient will eliminate the click and pop noise.

### Applications

The ISL54065 is designed to be a Dual SPDT switch for multiplexing or switching of signals that require low insertion loss, low power consumption, and negative voltage swing capability. Such applications include Audio/Video equipment, battery or portable devices and medical equipment. In addition, the Click and Pop Elimination Circuitry makes it ideal for portable audio such as MP3 players and cell phones.

### **Using The Board (Refer to Figure 2)**

#### **Lab Equipment**

The equipment, external supplies and signal sources needed to operate the board are listed below:

1. +1.8V to +6.5V DC Power Supply
2. Audio Signal Generator
3. Audio Signal Oscilloscope
4. Logic Control Generator and/or Pulse Generator

#### **Initial Board Setup Procedure**

1. Attach the evaluation board to the DC power supply at J1 (VCC) and J2 (GND). Positive terminal at J1 and negative terminal at J2. The supply should be capable of delivering +1.8V to +6.5V and 100 $\mu$ A of current.
2. Connect the Audio Source Signal to the NOx or NCx BNC inputs. The analog input voltage range can be from V<sub>CC</sub>-6.5V up to VCC.

3. Connect the Audio Signal Oscilloscope to the COMx BNC outputs.
4. Connect the Logic Control generator to the INx logic inputs.
5. Set the EN pin to logic "HIGH" to have the switches active.

#### **NCx Switches Active**

1. Drive the INx pins to logic "LOW".
2. The NCx switches are now connected to the COMx terminals.
3. The NOx switches have shunt resistors on the terminals to ground.

#### **NOx Switches Active**

1. Drive the INx pins to logic "HIGH".
2. The NOx switches are now connected to the COMx terminals.
3. The NCx switches have shunt resistors on the terminals to ground.

# ISL54065EVAL1Z Evaluation Board Schematic

