BusWorks® 900EN Series
10/100 Mbps Industrial Ethernet I/O Modules

Model 900EN-S005 5-Port 10/100M Ethernet Switch

USER'S MANUAL

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Symbols on equipment:

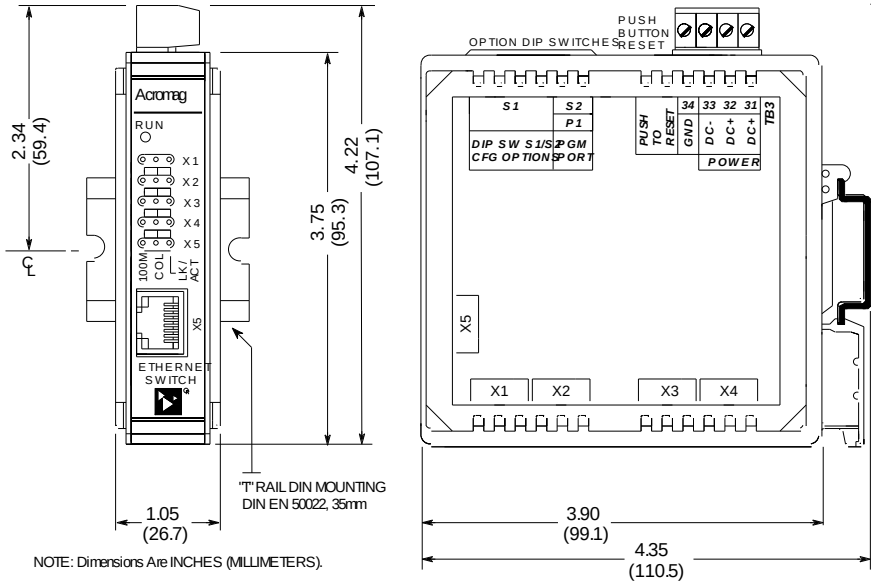
Means "Refer to User's Manual (this manual) for additional information".

IMPORTANT SAFETY CONSIDERATIONS

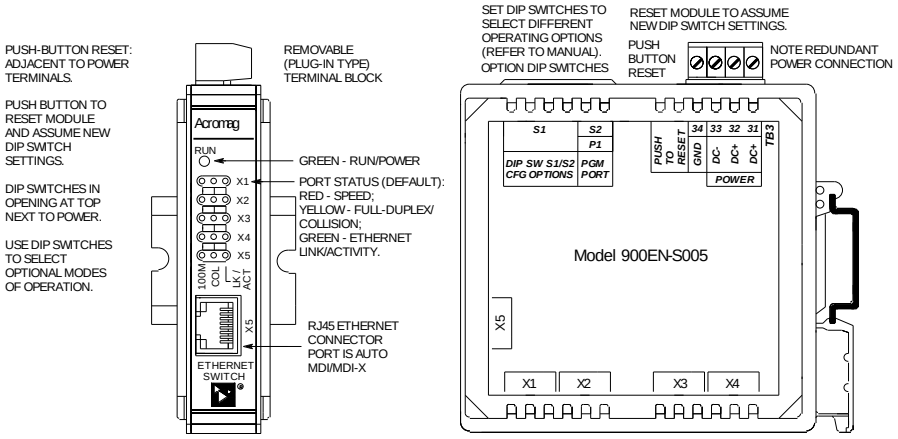
You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

GETTING STARTED

TECHNICAL REFERENCE



MODEL 900EN-S005 ENCLOSURE DIMENSIONS



The port status LED indicators are programmable via DIP switches and have two possible display modes that combine indication of speed, collision, duplex, link, and activity. By default (Mode 0), they indicate the following:

LED 1 (Red)	LED 2 (Yellow)	LED 3 (Green)
Speed (ON=100Mbps, OFF=10Mbps)	Full-Duplex (ON)/ Collision (Blink ON/OFF)	Link (ON) + Activity (Blink ON/OFF)

You may refer to Basic Operation of this manual for information on how to select the optional LED display mode.

Note (COL LED): This LED is used to indicate Collisions or Full-Duplex. If only one ethernet device is connected to a switch port, then a full-duplex connection is formed via auto-negotiation, and no collisions are possible. In this case, the COL LED will be ON to indicate full-duplex, not collision. Collisions may only occur for half-duplex communication with more than one device connected to a switch port.

MOUNTING AND DIMENSIONS

Unit mounts to "T" type DIN rails (35mm, type EN50022).

Units may be mounted side-by-side on 1-inch centers.

WARNING: *IEC Safety Standards may require that this device be mounted within an approved metal enclosure or sub-system, particularly for applications with exposure to voltages greater than or equal to 75VDC or 50VAC.*

CONTROLS & INDICATORS

Green Run LED is ON if power is ON.

Red, Yellow, and Green Port Status Indicators - Refer to the table below for default LED indication.

DIP Switches (S1 & S2) – Used to select optional modes of operation (refer to Basic Operation section).

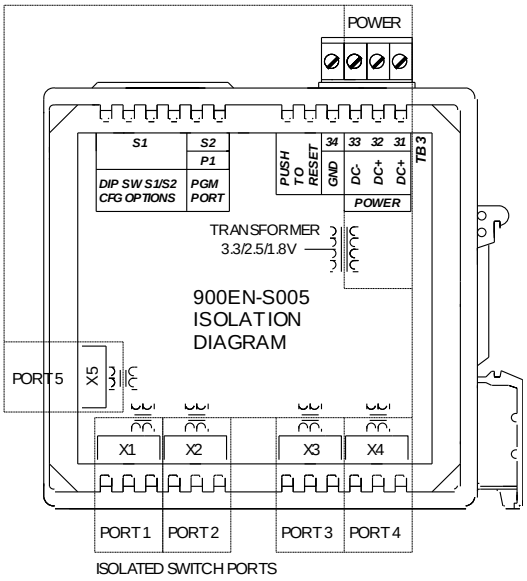
Push Button Reset – Used to reset the module and facilitate in-field reconfiguration. Push this button after making changes to the DIP switches in order to execute any changes.

ISOLATION BARRIERS

Dashed Lines denote isolation barriers.

The switch circuit, the individual network ports, and the power circuit are isolated from each other for safety and increased noise immunity.

Refer to Specifications section for isolation ratings.



BASIC OPERATION

This switch has automatic features that allow it to operate "unmanaged", right out of the box, and there are no special programming or setup procedures required.

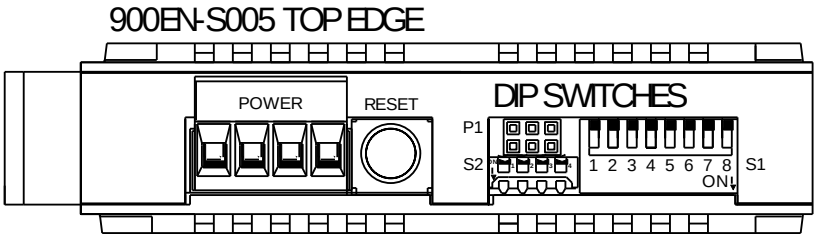
BASIC (DEFAULT) DEVICE OPERATION
Automatic MDI/MDI-X.
Automatic Polarity.
Automatic Half/Full Duplex.
Automatic 10M/100M.
Automatic Address Learning.
Automatic Address Migration.
Automatic Address Aging using 5 minute period (300±75s).
Flow Controls Enabled.
Half-Duplex Back Pressure Applies.
Standard Half-Duplex Back-Off Applies.
Switch will check that frame length conforms to maximum size limit.
R+Y+G LED's indicate Speed 100M ON/10M OFF + Full-Duplex ON/ Collision Blinking + Link ON/Activity Blinking, respectively.

This unit also has advanced features and options that may be selected via DIP switches, or optionally under program control. These features and alternate operating modes are explained in the Technical Reference section at the back of this manual.

BASIC OPERATION

DIP Switch Mode

The default mode of operation for this device is operation in DIP Switch Mode. As shipped from the factory, this unit should have all DIP switches OFF, with the piano-style switch levers of S1 and S2 levers in the up position, as shown in the following drawing (plastic switch cover removed):



DIP SWITCHES S1 & S2 ARE SHOWN AS SHIPPED FROM THE FACTORY, ALL OFF.

This is sufficient for default operation as a 5-port, 10/100Mbps, auto-MDI/MDI-X Ethernet switch.

There are two sets of DIP switches that determine operation: the interface selection switch S2, and the operation options switch S1. By default, both sets of switches are in their OFF positions.

The interface selection switch S2 controls how the switch is to obtain its initial configuration at power-up, the operation of the port LED's, and how the program port interface P1 is to operate. Set S2 switches UP to turn them ON, and DOWN for OFF.

Interface Selection Switch Bank 2 (S2) Operation

DIP	OPERATION	OFF/UP (DEF)	ON/DOWN
1	Configuration Source	Use DIP Switches	Use EEPROM
2	Program Port Vector	SPI to ASIC	I^2C to EEPROM
3	Serial Program Mode	I^2C (EEPROM)	SPI Slave (ASIC)
4	LED Indicator Mode	Mode 0 (R+Y+G): (Speed+FDX/Col+ L/A)	Mode 1 (R+Y+G): (FDX+10ML/A+ 100ML/A)

The option switch bank S1 is used to select optional modes of operation. Set S1 switches DOWN to turn them ON, and UP for OFF as follows:

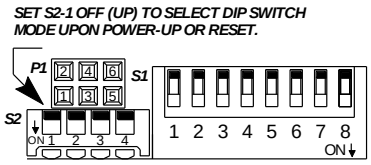
Option Selection Switch Bank 1 (S1) Operation

DIP	OPERATION	OFF/UP (DEF)	ON/DOWN
1	Address Aging	Enabled (300±75s)	Disable (No Aging)
2	Flow Control	Enable Flow Control	Disable Flow Control
3	Half-Duplex Back Pressure	Enable	Disable
4	Collision Frames	Drop Excess > 16	Do Not Drop Excess
5	Half-Duplex Backoff	Disable Aggressive	Enable Aggressive
6	Check Frame Length	Check Max Size	Disable Max Check
7	Force Duplex at Port 4 if AN Off/Failed.	Disabled, Do not Force Duplex	Enable (Port 4 Only)
8	Force Flow Control at Port 4 if AN Off/Failed.	Disabled, Do Not Force Flow Control	Enable (Port 4 Only)

Note: S2-1 must be OFF to cause this switch to use the DIP switch settings of S2-4 and S1-1 through S1-8.

BASIC OPERATION

DIP Switch Mode



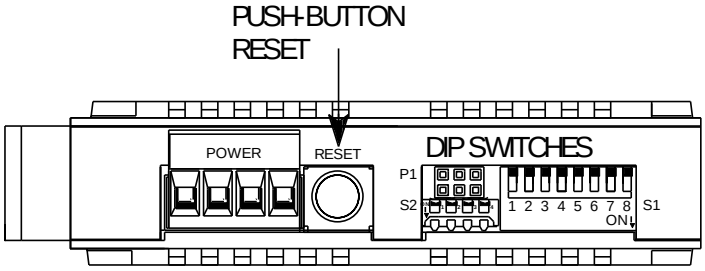
Dip switch S2-1 MUST be OFF to enable module to use the settings of DIP switches S1-4 and S2-1..8.

You MUST reset the module or cycle power for new DIP switch settings to take effect.

You can simply choose to operate this switch with all DIP switches OFF, or you can optionally select alternate modes of operation by setting the DIP switches ON or OFF, as required for your application. Refer to the following table for a definition of each DIP switch function:

IMPORTANT: DIP switch S2-1 MUST remain OFF in order to cause the module to utilize the settings of DIP switches S2-4 and S1-1 through S1-8. If DIP switch S2-1 is instead ON, then the other DIP switches are ignored and the module will utilize the contents of the EEPROM registers to determine its operation.

When making changes to DIP switches, the new settings do not take effect until the module is reset, either by cycling power, or by pushing the reset button after making changes. The reset button is located in the top edge opening adjacent to the power terminals and DIP switches as shown below.



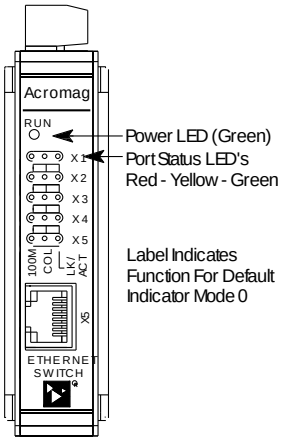
For an explanation of unfamiliar terms or modes of operation, please refer to the Technical Reference section of this manual.

Program Port P1

Note: The 5035-365 cable and its associated Advanced Features 8500-725 users manual have been discontinued.

Socket P1 is located on top of switch bank 2 and is used to provide program access to the internal EEPROM registers which determine operation of this switch in EEPROM Mode (S2-1 ON). Alternately, this connector also provides run-time access to the internal registers of the switch ASIC for operation in SPI Slave Mode. An optional program cable is required to connect your PC to this port (order Acromag cable Model 5035-365). The software required to make use of EEPROM mode is located on the CDROM shipped with your unit. EEPROM Mode is also discussed in the Technical Reference section of this manual.

Port Status LED Indicators



Each port of this module has three port status LED's, red, yellow, and green. The relative function of these LED's is determined by DIP switch S2-4 in DIP Switch Mode (or optionally via bit 1 of register 11 in EEPROM mode, see Technical Reference).

The following table gives the default LED indication in mode 0 (DIP switch S2-4 OFF or bit 1 of register 11 clear), and the optional LED indication mode 1 (DIP switch S2-4 ON or bit 1 of register 11 set):

Port Status LED Indication

Mode	LED 1 (Red)	LED 2 (Yellow)	LED 3 (Green)
0	Speed (On= 100M, Off= 10Mbps)	Full-Duplex+Coll (Constant ON= FDX, Intermittent ON= Collision, Constant OFF= Half-Duplex & No Collision)	Link + Activity (ON)
1	Full-Duplex (ON= FDX, OFF=HDX)	Link Activity (10Mbps Only)	Link Activity (100Mbps Only)

Port Status LED Indicators

The front panel label of the unit reflects LED functionality in default LED Mode 0.

Link/Activity LED

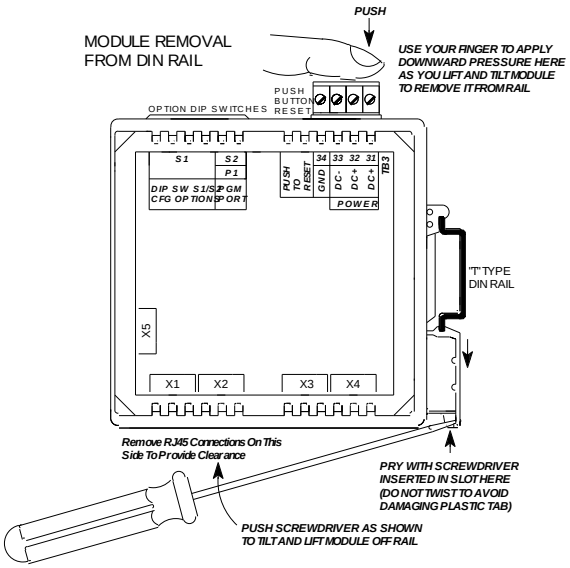
Once auto-negotiation has completed, the Link/Activity LED will be ON to indicate Link status. This LED will blink ON/OFF intermittently to indicate activity when data is being transferred at the port.

Collision LED

If only one ethernet device is connected to a switch port, then a full-duplex connection is formed via auto-negotiation, and no collisions are possible. In this case, the collision LED will be ON to indicate full-duplex, not collision. Collisions may only occur for half-duplex communication with more than one device connected to a switch port. The collision LED will blink intermittently as collisions occur for half-duplex communication.

CONNECTIONS

DIN-Rail Mounting & Removal



When attaching the module to the T-type DIN rail, angle the top of the unit towards the rail and locate the top groove of the adapter over the upper lip of the rail. Firmly push the unit towards the rail until it snaps into place. To remove, first separate the network connections from the bottom side of the module to create a clearance to the DIN mounting area.

Next, while holding the module in place from above, insert a screwdriver into the lower arm of the DIN rail connector and use it as a lever to force the connector down until the unit disengages from the rail (do not twist the screwdriver to avoid damaging the plastic).

CONNECTIONS

Network

For 100Base-TX systems, at a minimum, use data grade Unshielded Twisted-Pair (UTP) wiring that has a 100Ω characteristic impedance and meets the EIA/TIA Category Five wire specifications.

For 10Base-T systems, you may use Category 3, Category 4, or Category 5 UTP cable.

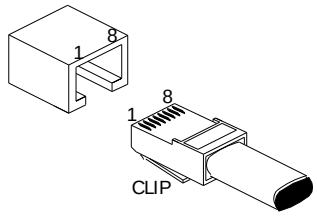
In either case, you are limited to 100 meters between any two devices.

RJ45 MDI AND MDI-X CONNECTIONS

PIN	MDI WIRING	MDI-X WIRING
1	Transmit +	Receive +
2	Transmit -	Receive -
3	Receive +	Transmit +
4	Not Used	Not Used
5	Not Used	Not Used
6	Receive -	Transmit -
7	Not Used	Not Used
8	Not Used	Not Used

Note Crossover Connections

ETHERNET PORT



RJ-45 CONNECTOR

MINIMUM RECOMMENDED CABLE

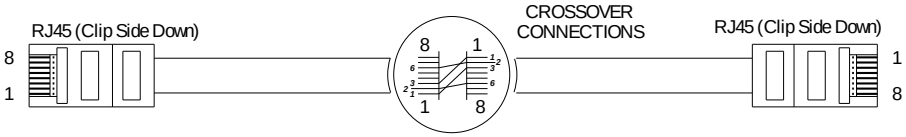
SPEED	DISTANCE	CABLE
10Base-T	100M	CAT 3, CAT 4, or CAT 5 UTP/STP
100Base-T	100M	CAT 5 UTP/STP

A crossover cable simply connects the differential transmit pair on each end, to the receive pair at the opposite end.

Note that network switches and hubs are wired MDI-X by default, while your PC is wired MDI.

This switch does not require use of a crossover cable. *It is documented here for use with Acromag 9xxEN Ethernet I/O modules.*

CROSSOVER CABLE
FOR MDI TO MDI, OR MDI-X TO MDI-X



PINS: 1 TO 3
2 TO 6
3 TO 1
6 TO 2

TIP: You can easily determine if a patch cable is a crossover cable upon inspection by holding both end plugs together in the same direction and reading the wire colors from left to right through the clear portion of the plug. If the wire color arrangement is in the same order, then the cable is a straight cable. Otherwise, it's a crossover cable (*or good cable gone bad*).

Note that all ports of this switch are Automatic MDI/MDI-X and will automatically swap the Tx/Rx channels pairs, as required. As such, a straight-through or crossover cable can be used to connect to any port of this device. However, it is not good practice to use crossover cables when wiring to a switch or hub, as the ports of these devices are already wired MDI-X.

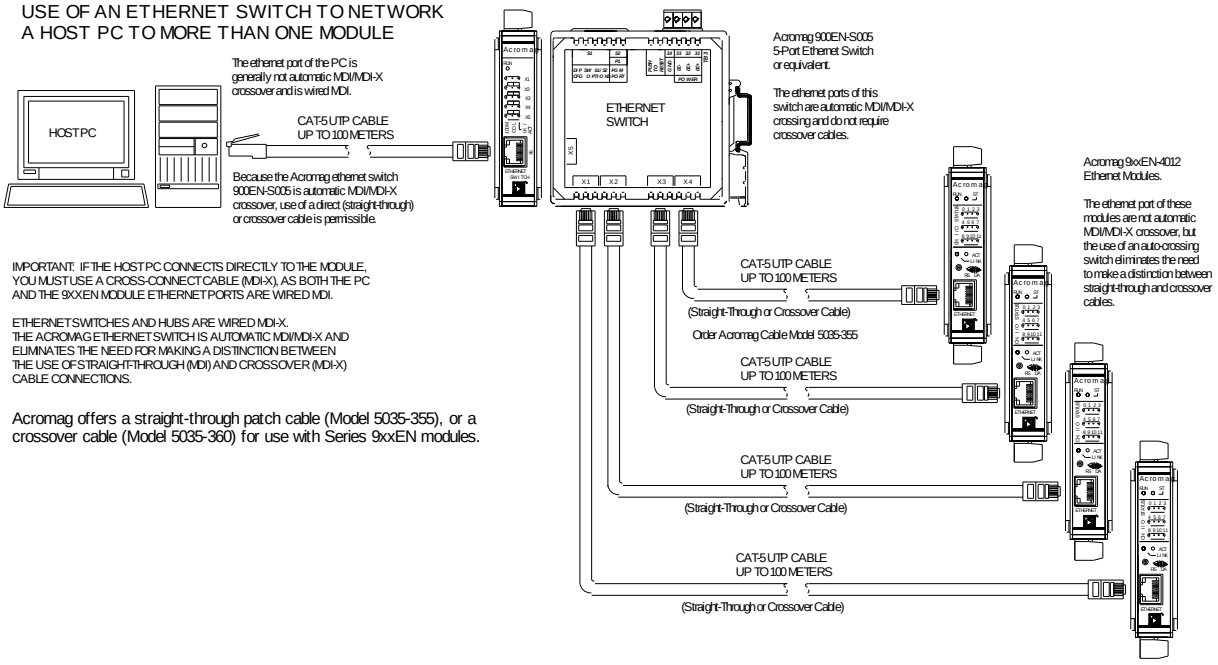
Refer to the Accessory Cables section at the back of this manual for more information on accessory cables including patch and crossover cables available from Acromag and other vendors.

TIP: You can significantly enhance the EMI/RFI performance of your network connections by using Category 5E STP cable (Shielded Twisted Pair) with shielded RJ45 plug connectors. This will also help to protect your installation from damage due to ESD (Electro-Static Discharge). The use of shielded cable is strongly recommended for installations in harsh industrial environments and/or in the presence of strong electrical fields.

CONNECTIONS

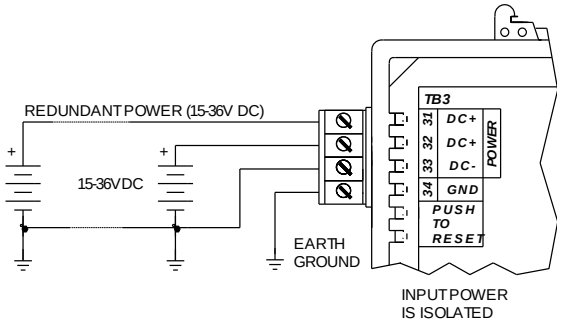
Network

You can use this switch to build a network of Acromag Ethernet modules, similar to that shown below. This drawing shows how to network-connect this switch to a host PC and four Acromag Series 9xxEN Ethernet I/O modules.



Power

✓ Connect 15-36V DC to the power terminals labeled DC+ & DC-. Optionally connect redundant (backup) power to the second DC+ terminal. Observe proper polarity. For supply connections, use No. 14 AWG wires rated for at least 75°C. **CAUTION:** Do not exceed 36VDC peak.



Voltage	Current
15VDC	164mA
18VDC	134mA
24VDC	101mA
36VDC	72mA

IMPORTANT – External Fuse: If unit is powered from a supply capable of delivering more than 1A to the unit, it is recommended that this current be limited via a high surge tolerant fuse rated for a maximum current of 1A or less (for example, see Bel Fuse MJS1).

Optional Program Port (Adjacent To DIP Switch S2)

This connection requires an optional programming cable, Acromag Model 5035-365.

✓ **Connection to program port P1 is not required to achieve basic operation.** Connection to this port is only required if you wish to make use of more advanced programmable features of this device, such as port-based VLAN support, broadcast storm protection, rate limiting, and priority control. An optional accessory cable (Model 5035-365) and software are required to interface with this port. This software is included on the CDROM that contains this manual and shipped with your unit, or it may be optionally downloaded from our web site at www.acromag.com. Refer to the Technical Reference section at the back of this manual for more information regarding advanced features and optional program port connections.

Earth Ground

Warning: *To comply with safety and performance standards, use shielded cable and connect earth ground as noted. Failure to use good wiring and grounding practices may be unsafe and hurt performance.*

✓ Connect Earth Ground as shown in the connection drawings above. Note the additional connection to earth ground at the GND terminal (recommended).

The plastic module housing does not require earth ground.

TROUBLE-SHOOTING

Diagnostics Table

If your problem still exists after checking your wiring and reviewing this information, or if other evidence points to another problem with the unit, an effective and convenient fault diagnosis method is to exchange the module with a known good unit. Acromag's Application Engineers can provide further technical assistance if required. Complete repair services are also available from Acromag.

Check your wiring and refer to this table if you have trouble using this switch.

SYMPTOM	POSSIBLE CAUSE	POSSIBLE FIX
Cannot communicate.	Is Power ON at the module?	Check power. Do any LED's light?
Module Does not recognize new DIP switch settings.	Have you reset the module since making changes?	Push Reset Button or cycle power.
	Have you enabled the DIP switches?	DIP switch S2-1 must be OFF to enable DIP switches.
Module Does not recognize new EEPROM register configuration.	Have you reset the module since writing registers?	Push Reset button or cycle power.
	Have you enabled EEPROM interface	DIP Switch S2-1 must be ON to enable EEPROM. DIP Switch S2-3 must be OFF.
	Signature Byte Registers Have Wrong Value.	Registers 0,1 must be set to 5599H, respectively.
Many Communication Errors.	Is cable segment longer than 100M?	Maximum distance between two nodes is limited to 100 meters using approved cable. Good practice further limits segment length to 80% or 80 meters.
	Network cable may be picking up noise.	Try using Category 5E shielded cable and shielded RJ45 connectors.
Communication appears temporarily lost after hot-	Problem – Sometimes if port connections are hot-	You may wait 5 minutes or simply reset the module after hot-swapping port

swapping port connections.	swapped, the unit may wait until the aging period expires (5 minute default) before it recognizes the new connection.	connections. Optionally, in EEPROM Mode you can enable fast aging (register 3 bit 1), or enable fast aging on a change in link status (recommended, reg. 2 Bit 0).
Erroneous reads In SPI Slave Mode	Common - Poor quality parallel port signals.	Check cable. Reduce cable length. Try another PC.

Miracles.74

Note: *The SPI Mode and interface are reserved for factory use only and operation in this mode is not guaranteed by Acromag.*

SYMPTOM	POSSIBLE CAUSE	POSSIBLE FIX
Cannot Program EEPROM Registers	Wired wrong	Check Program Port wiring. Check connector making good contact at P1. Check that cable 5035-365 is plugged into your PC parallel port
	Wrong interface selection—check position of DIP switches S2-1,2,3.	For I^2C/EEPROM Mode, DIP switch S2-3 must be OFF, DIP switch S2-2 ON, and DIP switch S2-1 ON. For SPI Slave Mode, DIP switch S2-3 must be ON, DIP switch S2-2 OFF, and DIP switch S2-1 ON. Note that DIP switches S1 & S2 have the same convention with respect to the ON position (S2 is ON in downward position).
	Cable Not Connected to LPTx port.	Make sure you connected to your host PC printer port.
	Module Power Off	Module must be powered to read/write registers.

TROUBLE-SHOOTING

Diagnostics Table

Useful Statistics

Network analyzers may be used troubleshoot network and cabling problems and may also compile Management Information Base (MIB) data similar to that shown in the table below. This table gives additional troubleshooting information for common MIB statistics.

STATISTIC	INTERPRETATION/ACTION
RxFragments *A fragment is an ethernet frame which is shorter than the requisite 64 octets and which has an invalid Frame Check Sequence (bad CRC), symbol error,*	Fragments or runts are usually the product of collisions, poor wiring, and electrical interference. Most fragments are a result of normal collision activity on an Ethernet network. For example, when a collision occurs the resulting jam signal, appended to the data on the line before the collision took place, results in a fragment. Thus, fragments can be viewed as indicators of collision activity. However, collisions are not the only source of fragments, as they can also be introduced by

or alignment error.	electrical noise. A high number of fragmented packets can result from interference induced on the network cable, either passing too close to noisy devices, or because of problems with network devices themselves. Check for improper cabling, damaged cable, or cables routed too close to noisy equipment. The use of shielded Cat 5e STP cable may also help.

TROUBLE-SHOOTING

Useful Statistics

STATISTIC	INTERPRETATION/ACTION
RxUndersizePkt	*This counts packets that are less than the requisite 64 octets (including FCS octets), but are otherwise well formed (good Frame Check Sequence).* This is usually the result of software errors. Note that undersized and fragmented packets are also referred to as "runts".
RxOversize	*This counts packets that are longer than 1522 bytes including the FCS octets (or 1536 depending on Max Packet Size set), but are otherwise well formed (valid CRC/FCS).* Oversized or "too long" packets are often caused by a bad transceiver, a malfunction of the jabber protection mechanism of the transceiver, or excessive noise on the cable. A transceiver on the network may be adding bits to the packets transmitted. You can use a network analyzer to identify the rogue transceiver and replace it, the adapter, or the station. A high number of these errors may also be indicative of a speed mismatch between the switch port and devices on this segment.
RxJabbers *Stop that incessant jabbering, shut up and listen!*	*This counts the number of frames larger than the maximum packet size of 1522 bytes (or 1536 bytes, depending on the maximum packet size), and that include CRC, alignment, or symbol errors*. Recall that Ethernet devices use electrical signaling to determine whether or not they can transmit. Jabbers indicate that one or more devices on the network are sending improper electrical signals. This is a critical failure because a jabber condition can effectively halt all traffic on a segment, as all other devices think the network is busy. Jabbering is usually caused by a bad network adapter or NIC card, and in rare cases, outside interference.
RxSymbolError	*This tracks packets received with an invalid data symbol but of legal packet size.*
RxCRCerror	*The CRC is a four byte value appended to a packet. The criterion for CRC error rate is 1 CRC error per 10^8 frames for 100base-T.*

	A high number of CRC errors may indicate poor cable quality or operation in a noisy environment. Use a cable tester, try a different cable, or try using shielded cable.
RxAlignmentError	*This is a count of the number of frames received between 64 and 1522/1536 bytes long that do not have an integral number of octets and include a bad CRC (checksum).* Usually a product of collisions, duplex mismatch, speed mismatch, or bad hardware (NIC, cable, or switch port).

STATISTIC	INTERPRETATION/ACTION
RxControl8808Pkts	*Tracks the number of MAC control frames received by a port with 88-08H in the Ether Type field.*
RxBroadcast TxBroadcastPkts	Broadcast packets are a normal part of network operation. Too many broadcast packets (broadcast storms) can use excessive bandwidth. Broadcast storms occur when network stations create traffic that by its nature generates more traffic. You can use VLAN's to prevent broadcast storms by creating separate broadcast domains, which limit the area of the network each broadcast packet affects. More VLAN's means less proliferation of broadcast packets.
RxMulticast TxMulticastPkts	Multicast packets are a normal part of network operation, but like broadcast packets, too many multicast packets can use excessive bandwidth. You can segment the network into smaller VLAN's and routing between them can help control the over proliferation of multicast messages.
RxJabbers RxOversize RxAlignmentError	A high number of these errors may indicate a faulty node or port. If a port is judged to be OK, then the cable connecting the node may be too long—it must be less than 100M. Otherwise, there may be a duplex mismatch between the switch port and the connected node.
RxCRCerror RxAlignmentError *These stats count the number of times the bits of a frame cannot be divided by 8 (broken into legal octets) and that contain a Frame Check Sequence (FCS) error.*	This is typically caused by turning equipment on or off, and by noise on twisted pair segments. This is normal but should only result in a few errors. A higher amount may also reflect damaged cables, or be the result of interference induced on network cables by passing them too close to noisy devices. The Ethernet standard allows a 1 in 10^8 bit error rate, but you should expect less than 1 in 10^{12} packets. In general, a rate in excess of one error per 1000 packets indicates a serious problem.
TxLateCollision *Similar to collisions as noted below, but detection has failed.*	*Indicates that two devices have transmitted at the same time, but failed to detect the collision. This usually indicates the Slot Time is being exceeded. This is because the time it takes to propagate the signal from one device to the other is greater than*

TROUBLE-SHOOTING

Useful Statistics

	the time it takes to put the entire packet on the network, thus causing the device to fail to sense the other device's transmission until the entire packet is on the network. This is most commonly caused by cabling errors, faulty hardware (NIC, cable, or switch port), excessive segment length, or too many repeaters between devices (more than two). It may also occur as the result of duplex mismatch error.

TROUBLE-SHOOTING

Useful Statistics

STATISTIC	INTERPRETATION/ACTION
TxTotalCollision TxExcessiveCollision TxSingleCollision TxMultipleCollision *These count the number of times packets have collided on the network (i.e. the number of messages retransmitted because of a collision).*	*Collisions are detected by the transmitting station and indicate that two devices happened to detect that the network is idle and tried to transmit at the same time. Since only one device may transmit at a time, both devices must stop sending and attempt to retransmit. The retransmission algorithm attempts to prevent the packets from transmitting at the same time again, but collisions may still occur and this process will repeat itself until the packets finally pass onto the network, or the packets may be discarded after 16 consecutive collisions.* Note that only transmitting hosts can be aware of collisions and that collisions cannot occur for full-duplex communication (one device connected to a switch port). Collisions also result from an over-extended LAN where the cable is too long or where more than two repeaters are used between stations. A high number of collisions is also indicative of a congested network and some nodes may need to be relocated to another segment. A node on the segment may also have a faulty adapter that is not listening before broadcasting and you may have to isolate each network adapter to see if the problem disappears. Guidelines for collision rates are as follows: ● 10% is a normal rate for shared segments. ● 30% is a rate where collisions begin to interfere with performance. ● 70% is judged to be a practical limit where below this the network is considered functional.

TECHNICAL REFERENCE

KEY FEATURES

- **Safety Agency Approvals** – CE, UL, & cUL listed, plus Class I; Division 2; Groups A, B, C, D approvals.
- **Wide-Range DC-Power w/ Redundant Power Connection -** Diode-coupled for use with redundant supplies, and/or battery back-up. An extra power terminal is provided for optional standby backup power.
- **Wide Ambient Operation** – Reliable over a wide temperature range.
- **Hardened For Harsh Environments** - For protection from RFI, EMI, ESD, EFT, & surges. Has low radiated emissions per CE requirements.
- **Adds Support For Double-Shielded RJ45 Connectors & Cable** – Properly terminates cable shield for noise resistance, ESD protection, and lower emissions.
- **Plug-In Terminal Block & DIN-Rail Mount -** Makes mounting, removal, and replacement easy.
- **10Base-T and 100Base-TX Support** – Auto-negotiated 10/100Mbps, half or full duplex with flow controls and compliant to IEEE 802.3u.
- **Fully Isolated** – Individual ports and input power are isolated from each other for safety and increased noise immunity.
- **Auto MDI/MDI-X Crossover & Auto-Polarity** – No special up-link/down-link port or crossover cables are required. This switch eliminates need for crossover cables when connecting your PC to Acromag 9xxEN I/O modules. Further, switch automatically selects the correct plus and minus polarities for the differential Tx/Rx channel pairs.
- **Unmanaged, Stand-Alone Operation** - No PC for basic operation.
- **Wire Speed Receive and Transmit/Non-Blocking Switch** – Allows simultaneous transmission on all ports.
- **Three Programmable LED's Per Port** – Select from two LED modes that combine Link, Activity, Full/Half duplex, & Speed indication.
- **Optional DIP-Switch Programming** – Some options may be selected via a 4-Position and 8-Positon DIP switch on the module.
- **Optional Program Via Parallel Port** – Advanced options may be programmed via connection to host PC parallel port (LPTx). This connection requires an optional cable (Model 5035-365) and software.
- **Broadcast Storm Protection –** Helps unburden switch resources during excessive amounts of broadcast messages.
- **Half-Duplex Back Pressure Flow Controls** – Used to defer transmission by other stations to avoid congestion.
- **Store & Forward Operation For 1024 Frames** - Integrated address look-up supports 1K absolute MAC addresses.
- **Smart Address Management** - Automatic address learning, address aging (300 seconds or disabled), and address migration.
- **Supports Virtual LAN Definitions** - Allows VLAN groups to be defined for added security between groups & applications.
- **Priority Controls -** Queue Priority Management controls with advanced Quality of Service (QoS) supports "DiffServ" and IEEE 802.1p based priority to prioritize different classes of voice, video, and data traffic, plus Port-Based Priority.
- **Integrated 128KB (32Kx32bit) High-Speed SRAM Frame Buffer** - Shared by all 5 ports and supports 1.4Gbps memory bandwidth.
- **Energy Miser** - Individual port power is shut down if no cable is connected to conserve energy.
- **Push-Button Reset Switch** – Enables field reprogramming via DIP switches without cycling power.

HOW IT WORKS

Background - Hubs

To better understand the operation of an Ethernet switch, you need to differentiate it from a hub. An Ethernet hub (or repeater) is a device that simply connects Ethernet nodes. Any message at one hub port is repeated on all ports. That is, hubs forward data packets they receive from a single station to all hub ports. As a result, all port devices connected to a single hub will share the same bandwidth. Then as nodes are added to the network hub, they compete for this finite amount of bandwidth (at 10Mbps or 100Mbps). This can cause data collisions to occur and makes network determinism impossible, particularly on busy networks. Determinism is a term that is used to describe the ability to guaranty that a packet is sent or received in a finite and predictable amount of time. In the past, lack of determinism is the main reason that Ethernet has had problems being accepted for use in critical control applications, as most control systems have a defined time requirement for packet transmission, typically less than 100ms.

Contrast - Switches

A switch (or switching hub) is an intelligent device that is used to more efficiently connect distributed Ethernet nodes than a hub. Unlike a simple hub, a switch provides *targeted* data transfer, as it will forward a data packet to a specific port or network segment, rather than all ports, thus freeing up bandwidth. The ability to target a packet to a specific port increases network throughput and helps to eliminate the collisions that historically make Ethernet non-deterministic.

- Switches act as intelligent repeaters to increase network distance.
- Switches split networks into separate collision domains at each port.
- Switches provides determinism by reducing collisions.
- Switches increases network bandwidth/throughput.
- Switches can provide supplemental error checking.

Introducing The Acromag 900EN-S005

The Acromag 900EN-S005 is a five-port, Ethernet switch that combines integrated buffer memory, five MAC's (Media Access Controllers), five PHY's (Ethernet Physical Layers), and a sophisticated switch engine for small home, office, or industrial applications. It is packaged in a rugged enclosure, suitable for DIN-rail or panel mounting. It operates over a wide temperature range and is designed to withstand the effects of harsh plant floor environments. It also carries Class I, Div 2, Group A, B, C, and D ratings, allowing it to operate in the presence of explosive gasses. The 900EN-S005 also performs additional error checking on data packets to help ensure the integrity of forwarded data. A wide input switching regulator (isolated flyback) provides isolated power to the circuit and the unit includes a redundant power input, for hot standby back-up power should the main supply fail. Each port of this switch functions just like any other Ethernet device. It is able to receive and decode Ethernet frames, test for frame integrity, plus assemble and transmit Ethernet frames.

With Ethernet, any device can try to send a data frame at any time. If two devices happen to send a data frame at the same time, then a collision may occur. The arbitration protocol for carrier transmission access of the Ethernet network is called Carrier Sense Multiple Access with Collision Detect (CSMA/CD). With CSMA/CD, each device will first sense whether the line is idle and available for use. If it is, the device will begin to transmit its first frame. If another device also tries to send a frame at the same time, then a collision occurs and both frames are discarded. Each device then waits a random amount of time and retries its transmission until it is successfully sent.

HOW IT WORKS

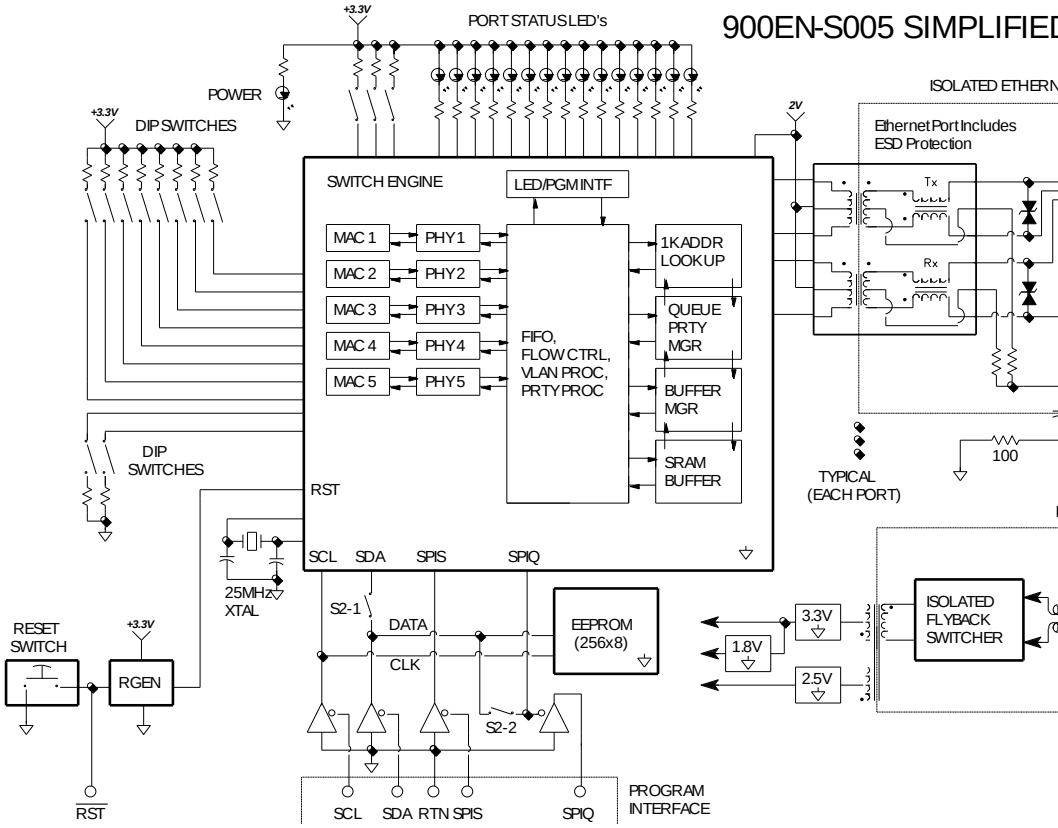
Unlike other Ethernet devices, such as an Ethernet host adapter or Network Interface Card (NIC), the port of a switch does not require its own MAC address. During retransmission of a received packet, the switch port will instead look like the originating device by having assumed its source address. This is why the Ethernet collision domain is said to terminate at the switch port. That is, a two-port switch will effectively break a network into two distinct data links or segments. A five port switch like the Acromag 900EN-S005 can break a network into 5 distinct data links or segments (also called *collision domains*). Since all Ethernet nodes are able to recognize the occurrence of a collision, and since the detection of a collision is principal to the way Ethernet arbitrates media access, large domains containing many nodes can become quite cumbersome. Thus, using an Ethernet switch to subdivide a large network into separate collision domains will certainly help to increase throughput.

Each port of a switch forwards data to another port based on the MAC address contained in the received data packet/frame. In order to know which port to forward a data packet to, the switch will learn and store the MAC addresses of every device it is connected to, along with the associated port number (up to 1024 MAC addresses are stored in high speed SRAM). However, until the switch actually learns the port a particular address resides at (the first packet), it forwards this traffic to all ports. The switch will use this internal look-up table to quickly determine the location (port) of a node, establish a temporary connection between itself and the node, then terminate the connection once a packet is transferred. In this way, it increases network bandwidth and provides the network determinism required for critical control applications.

The current tendency in critical industrial control applications is to connect one Ethernet device per switch port. This will produce the most deterministic mode of operation as the switch can operate full-duplex, with no chance of collisions. This ensures determinism, helping critical control applications to remain predictable and on-time.

This switch uses a *store and forward* algorithm to process Ethernet frames. That is, it first stores the Ethernet frame and examines it for errors before forwarding it to its destination. Although this method may seem to increase the forwarding time (latency) and possibly cause fragmentation, it effectively reduces the occurrence of error frames and improves overall throughput. This is particularly useful when there is heavy network traffic and or greater potential for noise and interference.

Refer to the simplified schematic shown below to gain a better understanding of the circuit. Note that the network transmit and receive channels of each port include transient suppression. Further, the metal shield of the network ports are terminated with an isolation capacitor and TVS, which effectively isolates the shield connection, minimizes emissions, and enhances transient protection.



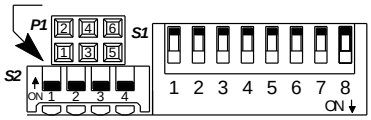
ADVANCED OPERATION

This model operates on three different levels with varying operating modes and methods of reconfiguration. The first level is operation right "out of the box" in DIP Switch Mode. The second level refers to optional operation in EEPROM mode. The third level refers to operation in SPI Slave Mode which is not covered in this manual (reserved for factory use). The second and third levels also require an optional cable (Acromag model 5035-365) and configuration software. This section of the manual will explain some of the alternate operating modes of this device and related terminology. The EEPROM Register Map is also presented which will introduce most of the programmable features of this device. Not all register functions will be supported. Some register functions apply to functionality useful in SPI Slave Mode and this mode is reserved for factory use only.

Operation "Right Out Of The Box" (DIP Switch Mode)

The default mode of operation for this device is DIP Switch Mode and this is already covered in the first part of this manual (Refer to Basic Operation section). Terminology related to this mode is discussed in the Terms and Concepts section at the back of this manual.

SET S2-1 OFF (DOWN) TO SELECT DIP SWITCH MODE UPON POWER-UP OR RESET.



The default mode of operation for this device is sufficient to allow the unit to operate as a 5 port switch, right out of the box, with no special software or hardware switches to configure. DIP switch S2-1 must be OFF to set the unit to DIP Switch Mode and this will cause the unit to initialize itself using the settings of DIP switches S2-4, and S1-1..8 upon reset. For parameters not controlled by a DIP switch, the default settings noted in the EEPROM Register Map will apply.

ADVANCED OPERATION

For most applications, the default (OFF) position of these switches is sufficient for basic operation. If optional settings are desired, these switches are usually set one time at installation, usually with power off, then new settings take effect upon power-on reset, or after pushing the reset button.

Note that you may have to remove a small plastic cover in order to access the DIP switches. This cover can be removed by first removing the enclosure left side cover by gently prying it apart using a flat blade screwdriver, and then sliding the protective cover out. The plastic cover is provided to prevent possible ESD damage and unauthorized in-field access. Always be sure to handle the board at an ESD-safe workstation, or damage to the unit may occur.

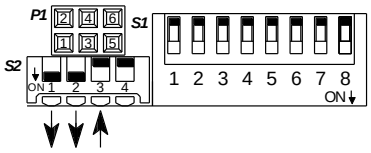
You may set DIP switches S1-4 and S2-1..8 as required by your application, then either apply power to the board (power-on reset), or press the reset button if power is already applied to the board. Reset will cause the new switch settings to take effect. Note that each DIP switch also has an internal EEPROM register that can be used to optionally affect operation in EEPROM Mode. In any case, DIP switch S2-1 MUST be OFF in order to cause the internal switch engine to utilize the settings of the other switches, as opposed to the settings configured in the corresponding EEPROM registers (see Register Map). For options not directly addressed by a DIP switch, the defaults noted in the Register Map will apply—that is, DIP switches cannot be combined with any non-default settings in EEPROM.

The DIP switches determine operation with DIP switch S2-1 set OFF, and only the EEPROM determines operation with DIP switch S2-1 set ON.

EEPROM Mode

EEPROM Mode provides direct read/write access to switch configuration registers in EEPROM memory on the board and causes the switch to utilize these register settings to determine its operation upon power-up or reset. This mode provides more extensive control of available features and options than the DIP switches, such as broadcast storm protection, rate limiting, and port-based VLAN definitions. EEPROM mode is generally used to setup the switch prior to installation, as opposed to using the DIP Switches.

DIP switch S2-1 must be ON to operate in EEPROM Mode. This causes the internal switch engine to initialize itself based on the contents of the EEPROM registers each time it is reset or power is applied.



SET S2-1 & S2-2 ON (DOWN) AND S2-3 OFF (UP) TO SELECT EEPROM MODE UPON POWER-UP OR RESET.

DIP switch S2-2 must be ON and DIP switch S2-3 OFF to make program port P1 use I^2C serial mode to write directly to the EEPROM in order to program it.

IMPORTANT: In order to access the on board EEPROM, you must place the module in EEPROM (I^2C) Mode by setting DIP switch S2-3 to OFF. Additionally, DIP switch S2-2 is set ON to provide direct EEPROM access, and DIP switch S2-1 is set ON to enable initialization via EEPROM.

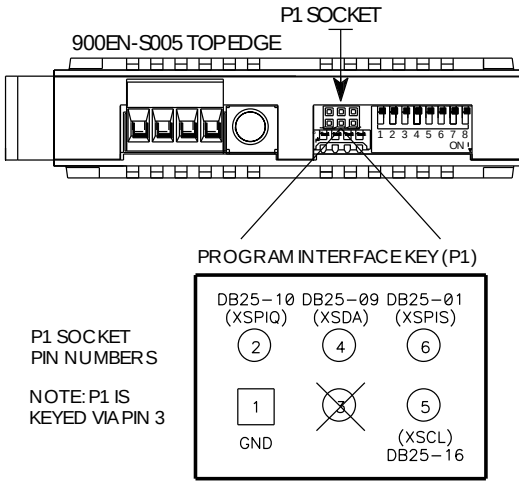
ADVANCED OPERATION

EEPROM Mode

The EEPROM is programmed via program port P1, which rests on top of switch bank 2 as shown at right.

The DB25M parallel port pins of your PC that connect to these pins are also indicated.

Use Acromag Cable Model 5035-365 (sold separately) to connect your PC's parallel port to the module at P1.



You can refer to the Register Map that follows and program the EEPROM configuration registers as required by your application. Simply connect this module's buffered program port to the parallel port of any DOS/Windows based computer using Acromag cable Model 5035-365 (sold separately).

With respect to the EEPROM's I^2C program interface, data start and stop conditions are signaled on the data line as a state transition during clock high time. A high to low transition indicates the start of data, and a low to high transition indicates a stop condition. The actual data that traverses the serial line changes during the clock low time. This interface is compatible with the Atmel AT24C02 EEPROM and further timing and data sequences can be found in the Atmel AT24C02 specification (www.atmel.com). Alternately, you may decide to use your own software to program EEPROM memory (refer to Atmel AT24C02 timing diagrams). In either case, you must use Acromag cable 5035-365 to connect this device to your PC's parallel port (LPT1 or LPT2) in order to accomplish reprogramming in this manner.

EEPROM Program Utilities keeprom.exe & 95m.exe

On the CDROM that shipped with your unit is folder labeled 900EN-S005. In this folder are three other folders labeled Manual, DOSUtility, and WindowsUtility.

DOSUtility contains a DOS program called 95m.exe for reading and writing the contents of EEPROM in the 900EN. A default settings data file called 95m.dat is also provided.

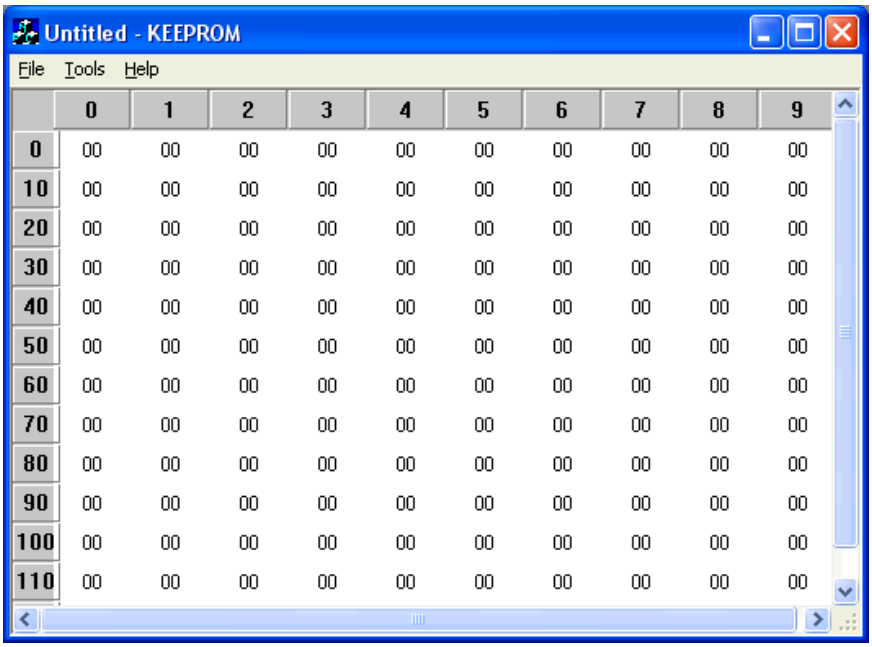
WindowsUtility contains a Windows based program called keeprom.exe for reading and writing the contents of EEPROM. A default settings data file called default95m.dat is also provided.

You may also download these files from our web site at www.acromag.com. Keeprom.exe (or 95m.exe) will allow you to easily upload/download new register data to the EEPROM, as required for your application.

Before continuing, be sure to connect the 900EN-S005 to your PC's DB25 parallel port using Acromag cable Model 5035-365 (sold separately) and turn power on at the switch module.

Note: T and its Advanc 8500-72 have be

After executing the keeprom.exe program, a screen similar to the following will appear:



This screen displays a matrix of 128 buffer cells. It will allow you to read and write any of the 128 register bytes contained in EEPROM in the 900EN. A specific register byte is located at the intersection of a row and column, with the sum of the row and column number being the register number as noted in the EEPROM Register Map. Thus, Byte 0 = Register 0 = Row 0, Column 0. Byte 10 = Register 10 = Row 10, Column 0. Byte 120 = Register 120 = Row 120, Column 0. Each register byte is indicated in hexadecimal format. A decimal-to-hexadecimal-to-binary conversion table is shown at right. Note that it takes two hex digits to represent eight register bits. Use this table and divide each register into two 4-bit numbers in order to determine what to write to a register. Note that any changes you make will not take effect until the next time the module is reset after writing its EEPROM (assuming DIP switch S2-1 is ON to select EEPROM Mode).

EEPROM Programmer Utility keeprom.exe

NUMBER		BINARY			
		2^3	2^2	2^1	2^0
DEC	HEX	8	4	2	1
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1
10	A	1	0	1	0
11	B	1	0	1	1
12	C	1	1	0	0
13	D	1	1	0	1
14	E	1	1	1	0
15	F	1	1	1	1

The following keeprom menu functions are available:

File	**Tools**	**Help**
New Ctrl+N	Verify	About keeprom…
Open…Ctrl+O	Upload	
Save Ctrl+S	Download	
Save As…	Modify	
Exit		

The File functions are used to manage the EEPROM image data files stored on your hard disk.

- Use "File-New" to set the file buffer to all 0's (do this to start from a clean sheet in order to create a new EEPROM image).
- Use "File-Open" to open an existing EEPROM image data file (all image files have file extension ".dat"). A default file named default95m.dat is provided (do not change the contents of this file).

EEPROM Programmer Utility keeprom.exe

- Use "File-Save" to save the data in the file buffer (current screen) to the currently opened EEPROM image data file. If there is no current file opened, a dialog box will appear for typing in a new file name to create a file, or to select an existing file to over-write.
- Use "File-Save As" to save the data in the file buffer (the current screen) to a file to be named. A dialog box will appear prompting for a file name.
- Use "File-Exit" to exit the keeprom program.

The Tools functions are used to manage the EEPROM image data inside the current file buffer.

- Use "Tools-Verify" to compare the data in the file buffer against the data inside the EEPROM of the connected switch module.
- Use "Tools-Upload" to read the data from the EEPROM to the file buffer. The current data in the file buffer will be overwritten with the contents of EEPROM.
- Use "Tools-Download" to write the data in the file buffer to the EEPROM. All the data in EEPROM will be overwritten with the data indicated in the current screen.
- Use "Tools-Modify" to bring up an editing window to modify the data in the file buffer.

The "Help-About" function only provides a method to display the current version number of this software.

To write data to the EEPROM registers, you will need to refer to the EEPROM Register Map that follows. You will have to enter data in "byte" form using two hexadecimal digits to represent the contents of each register. The easiest way to accomplish this is to first use "Tools-Upload" to load the screen buffer with the current EEPROM contents, then use "Tools-Modify" to change specific buffer registers, as required for your application. Then use "Tools-Download" to download the new contents to the EEPROM. In case of error, you may wish to first use "File-Save As" after you upload the EEPROM contents in order to preserve the original contents before making changes. Note that there is no error checking done by this software, it is up to you to make sure that you write the EEPROM registers correctly to affect its operation as required. Be sure to follow your changes with a reset.

EEPROM Register Map

The operative values for most of the advanced features of this device are stored in EEPROM memory in the module. The contents of these registers are loaded upon power-up or after reset, only when the module is operating in EEPROM Mode. A runtime image of these registers are also available in SPI mode (SPI Mode registers do not reside in EEPROM). You can make changes to these internal program registers as required for your application according to the register map that follows.

IMPORTANT: In order to access on-board EEPROM, you must place the module in EEPROM (I^2C) Mode by setting DIP switch S2-3 to OFF. Additionally, DIP switch S2-2 is set ON to provide direct EEPROM access, and DIP switch S2-1 is set ON to enable initialization via EEPROM.

EEPROM Register Map

As part of its initialization routine performed on power-up or after a reset, the internal switch engine will read the contents of 110 EEPROM registers (registers 0-109) to determine its setup when placed in EEPROM mode (DIP Switch S2-1 ON). If however, DIP switch S2-1 is OFF, it will instead use its internal defaults along with the DIP switch settings to determine its setup. In any case, DIP switch S2-1 must be ON in order read the EEPROM. Further, the first 2 bytes stored in EEPROM must be "95" and "00" respectively in order for loading to occur—if these 2 values are incorrect, then all other EEPROM data will be ignored. Any changes to either the module's DIP switches or the EEPROM registers will not take effect until the module is subsequently reset. A reset button is located adjacent to the power terminals to accomplish this, or simply cycle power to reset the unit after making changes.

OFFSET (EEPROM)		REGISTER DESCRIPTION
Decimal	**Hexadecimal**	
0-1	00H-01H	Chip ID Registers (Read Only)
2-11	02H-0BH	Global Control Registers
12-15	0CH-0FH	*Reserved - Do Not Modify*
16-29	10H-1DH	Port 1 Control Registers
30-31	1EH-2FH	Port 1 Status Registers (Read Only)
32-45	20H-2DH	Port 2 Control Registers
46-47	2EH-2FH	Port 2 Status Registers (Read Only)
48-61	30H-3DH	Port 3 Control Registers
62-63	3EH-3FH	Port 3 Status Registers (Read Only)
64-77	40H-4DH	Port 4 Control Registers
78-79	4EH-4FH	Port 4 Status Registers (Read Only)
80-93	50H-5DH	Port 5 Control Registers
94-95	5EH-5FH	Port 5 Status Registers (Read Only)
96-103	60H-67H	TOS Priority Control Registers
104-109	68H-6DH	MAC Address Registers
110-111	6EH-6FH	Indirect Access Control Registers
112-120	70H-78H	Indirect Data Registers
121-122	79H-7AH	Digital Testing Status Registers (Read Only)
123-124	7BH-7CH	Digital Testing Control Registers
125-126	7DH-7EH	Analog Testing Control Registers
127	7FH	Analog Testing Status Register (Read Only)

An explanation of various operating modes and terminology follows the EEPROM Register Map.

Register Map Summary

All EEPROM registers are Read/Write, unless otherwise specified.

Some registers address functionality not supported by this model, or functionality only useful in SPI Slave mode (Managed Mode). These registers are mentioned here in brief in order to prevent inadvertent access and operation.

The DEF settings noted in the Register Map that follows represent the defaults that apply in EEPROM Mode and the contents contained in the default95M.dat file used by the EEPROM program software. In some cases (noted), these defaults will differ in DIP switch Mode.

Register Map

The DEF settings noted in the Register Map represent the defaults that apply in EEPROM Mode and reflect the contents contained in the data file (default95M.dat) used by the EEPROM program software. In some cases (noted), these defaults will differ in DIP switch Mode with all switches OFF.

REG		DESCRIPTION	DEF
0	**00H**	**Chip ID0 Register – Chip Family Identification**	**95H**
	Bit	**Function**	
	7-0	Chip Family (Treat as Read Only) – Contents of this register byte is checked at power-on/reset along with bits 7:4 of register 1. The internal switch engine will use EEPROM register settings to determine its operation if this register contains 95H and bits 7..4 of register 1 contain 0H. Otherwise, it will use internal defaults and ignore the EEPROM contents.	95H
1	**01H**	**Chip ID1 Register / Start Switch:**	**04H**
	Bit	**Function**	
	7-4	Chip Family (Read Only) – "0000" designates "M" series chip (95M) family. The contents of this nibble is checked at power-on/reset along with bits 7:0 of register 0. The internal switch engine will use EEPROM register settings to determine its operation if bits 7..4 of this register contain 0000 and register 0 contains 95H. Otherwise, it will use internal defaults and ignore the EEPROM contents.	0000
	3-1	Read Only - Chip Revision ID (Currently 2).	010
	0	Read/Write - Start Switch For SPI Slave Mode Only: 1=Start switch automatically in SPI Slave Mode; 0=Do Not Start switch in SPI Slave Mode. In SPI Slave Mode, an external master can randomly access an image of registers 0-127 within the ASIC. However, in SPI Mode the system should first configure all desired settings, then enable the switch via this bit. Recall that DIP Switch S2-3 is used to select the serial mode. DIP switch S2-1 is used to enable communication with the EEPROM. If switch S2-3 is OFF, then the I^2C master mode is selected and the internal switch ASIC will start automatically after first trying to read the EEPROM contents. If the EEPROM does not exist or is disabled (DIP switch S2-1 is OFF), the switch ASIC will use default values for all internal parameters. Note that some default values can be set by changing DIP switches and resetting the module. If the EEPROM is present (DIP switch S2-1 is ON), the contents of the EEPROM will be checked. If EEPROM register 0 = 95H and register 1 bits [7:4] = 0000, then the contents of the EEPROM will over-ride register default values and DIP switch settings.	0
2	**02H**	**Global Control 0**	**4CH**
	Bit	**Function**	
	7	*Reserved*	0
	6-4	802.1p Base Priority: Used to classify priority for incoming 802.1Q packets. The "User-Priority" is compared against this 3 bit value. If it is greater than or equal to, then it is classified as high priority. If it is less, then it is classified as low priority.	100
	3	1=Enable PHY MII interface; 0=Tri-state all MII interface outputs. **This model does not implement the MII interface.**	1

Register Map

REG		DESCRIPTION	DEF
2	**02H**	**Global Control 0…continued**	**4CH**
	Bit	**Function**	
	2	Buffer Share Mode: 1=Share buffer pool among all ports and allow any port to use more buffer than allocated when other ports are not busy (default). 0=Restrict each port to 1/5 of available buffer pool.	1
	1	UNH Mode: 1=Switch will drop packets with 8808H in T/L field, or with DA=01-08-C2-00-00-01. 0=Switch will drop packets qualified as flow control packets.	0
	0	Link *Change* Age: 1=A change from "link" to "no link" will cause fast aging (less than 800us) of addresses. After an age cycle is complete, the aging logic will return to normal (300±75 seconds). **Note:** If any port is unplugged, all addresses are automatically aged out. 0=Do not allow fast aging. Aging period remains (300±75 seconds).	1
3	**03H**	**Global Control 1**	**04H**
	Bit	**Function**	
	7	Pass ALL Frames Enable: 1=Switch all packets including bad packets. Used for debugging purposes only and works in conjunction with sniffer mode. 0=Do not switch bad packets.	0
	6	*Reserved*	0
	5	IEEE 802.3x Transmit Flow Control Disable: 1=Do not enable transmit flow control, no matter what the auto-negotiation result is. 0=Enable transmit flow control based on auto-negotiation result. **This function may optionally be controlled via DIP switch S1-2 for both receive and transmit combined, but the Tx/Rx flow control can be programmed independently via bits 5 & 4 of this register.**	0/1
	4	IEEE 802.3x Receive Flow Control Disable: 1=Do not enable receive flow control, no matter what the auto-negotiation result is. 0=Enable transmit flow control based on auto-negotiation result. **This function may optionally be controlled via DIP switch S1-2 for both receive and transmit combined, but the Tx/Rx flow control can be programmed independently via bits 5 & 4 of this register.**	0/1

Register Map

REG		DESCRIPTION	DEF
3	**03H**	**Global Control 1…continued**	**04H**
	Bit	**Function**	
	3	Frame Length Field Check: 1=Check the frame length field in the IEEE packets, and if the actual length does not match, the packet will be dropped (for L < 1500). 0=Do not check frame length.	0
	2	Aging Enable: 1=Enable aging (default aging period is 300±75s). 0=Disable aging. **This function may optionally be controlled via DIP switch 1.**	1/0
	1	Fast Aging Enable: 1=Turn on fast aging (~800us); 0=Standard aging (300±75s). See Note at left.	0
	0	Aggressive Back-Off Enable (Half-Duplex): 1=Enable the more aggressive back-off algorithm in half-duplex mode to enhance performance (this is not an IEEE standard). Default is ON in EEPROM mode and OFF in DIP Switch Mode. 0=Disable aggressive back-off. **This function may optionally be controlled via DIP switch S1-5 which is OFF by default.**	0/1
4	**04H**	**Global Control 2**	**F0H**
	Bit	**Function**	
	7	Unicast Port-VLAN Mismatch Discard. This feature is used for port-VLAN's (see registers 17 and 33). 1=All packets cannot cross VLAN boundary. 0=Unicast packets (excluding unknown/multicast/ broadcast) can cross VLAN boundary.	1
	6	Multicast Storm Protection Disable: 1=Broadcast Storm Protection does not include multicast packets. Only DA=FFFFFFFFFFFF packets will be regulated. 0=Broadcast Storm Protection includes DA=FFFFFFFFFFFF and DA[40]=1 packets.	1
	5	Back Pressure Mode: 1=Carrier sense back-pressure is selected. 0=Collision based back-pressure is selected.	1
	4	Flow Control & Back Pressure Fair Mode: 1=Fair Mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0=In non-fair mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port.	1

Note: *Excessive use of fast aging can make your switch act more like a hub. Recall that a switch will send a message to all switch ports (like a hub does), until it actually learns an address (usually after the first communication). If fast aging is enabled and messages happen to be infrequent (reoccurring after 800us), then the switch will age out a learned address, and revert to sending a subsequent message to all ports, rather than the target port. This makes data transfer less efficient and needlessly increases network traffic.*

Register Map

REG		DESCRIPTION	DEF
4	**04H**	**Global Control 2…continued**	**F0H**
	Bit	**Function**	
	3	No Excessive Collision Drop: 1=Do NOT drop packets after 16 or more collisions. This is the default setting in EEPROM Mode. 0=Drop packets when 16 or more collisions occur. **This function may optionally be configured via DIP switch S1-4 which is OFF by default.**	0/1
	2	Huge Packet Support: 1=Accept packet size up to/including 1916 bytes. Note: This bit setting will over-ride the setting of bit 1 of this register. 0=Maximum packet size will be determined by bit 1 of this register.	0
	1	Legal Maximum Packet Size Check Disable: 1=Accept packet sizes up to/including 1536 bytes. This is default selection in EEPROM mode. 0=Accept packet sizes up to/including 1522 bytes for tagged packets (not including packets w/ STPID from CPU to ports 1-4), or up to/including 1518 bytes for untagged packets. Any packets larger than the specifed maximum are dropped. **This function may optionally be configured via DIP switch S1-6 (ON=1536 bytes) which is OFF by default.**	0/1
	0	Priority Buffer Reserve: 1=Each output queue is pre-allocated 48 buffers to be used exclusively for high-priority packets. It is recommended that this be enabled when the priority queue feature is turned ON. 0=Do not reserve buffers for high priority packets.	0
5	**05H**	**Global Control 3**	**00H**
	Bit	**Function**	
	7	802.1Q VLAN Enable: 1=Enable 802.1Q VLAN mode (Note: VLAN table needs to be setup prior to enabling this mode). 0=Disable 802.1Q VLAN mode.	0
	6	IGMP Snoop Enable For Switch MII Interface: 1=IGMP Snoop enabled; 0=IGMP Snoop disabled. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	5	Enable Direct Mode on MII Interface: 1=Direct Mode on Port 5. This is a special mode for the switch MII interface. Using preamble before MRXDV to direct switch to forward packets and bypass the internal look-up; 0=Normal operation. **This model does not implement the MII interface and this bit should remain set to 0.**	0

Register Map

REG		DESCRIPTION	DEF
5	**05H**	**Global Control 3…continued**	**00H**
	Bit	**Function**	
	4	Enable Pre-Tag on switch MII Interface: 1=Packets forwarded to switch MII interface will be pre-tagged with the source port number (preamble before MRXDV) 0=Normal operation. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	3-2	Priority Scheme Select: 00=Always deliver high priority packets first; 01=Deliver high/low packets at a ratio of 10/1; 10=Deliver high/low packets at a ratio of 5/1; 11=Deliver high/low packets at a ratio of 2/1.	00
	1	Enable "Tag" mask: 1=Last 5 digits in the VID field are used as a mask to determine which port(s) the packet should be forwarded to; 0=No tag masks.	0
	0	Sniff Mode Select: 1=Do Rx AND Tx sniff (both the source port and destination port must match); 0=Do Rx OR Tx sniff (either source port or destination port must match). This is the mode used to implement Rx only sniff.	0
6	**06H**	**Global Control 4**	**00H**
	Bit	**Function**	
	7	Switch MII Back Pressure Enable: 1=Enable half-duplex back pressure on switch MII; 0=Disable back pressure on switch MII interface. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	6	Switch MII Half-Duplex Mode: 1=Enable MII interface for half-duplex mode. 0=Enable MII interface for full-duplex mode. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	5	Switch MII Flow Control Enable: 1=Enable full-duplex flow control on switch MII. 0=Disable full-duplex flow control on switch MII. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	4	Switch MII 10BT: 1=Switch MII interface is in 10Mbps mode. 0=Switch MII interface is in 100Mbps mode. **This model does not implement the MII interface and this bit should remain set to 0.**	0
	3	NULL VLAN ID (VID) Replacement: 1=Replace NULL VID with port VID (12-bits). 0=Do not replace NULL VID.	0
	2-0	Broadcast Storm Protection Rate Bits [10:8]: These 3 bits along with Register 7 determine how many "64-byte blocks" of packet data are allowed on an input port in a preset period. This period is 50ms for 100BT or 500ms for 10BT. The default is 1%	000

Register Map

REG		DESCRIPTION			DEF
7	**07H**	**Global Control 5**			**4AH**
	Bit	**Function**			
	7-0	Broadcast Storm Protection Rate Bits [7:0]: This byte along with 3 bits of the previous register byte determine how many "64-byte blocks" of packet data are allowed on an input port in a preset period. The period is 50ms for 100BT, or 500ms for 10BT. The default is 1% (4AH). **Note:** 148800 frames/second* 0.050s/interval *0.01(1%)= approximately 74 frames/interval=4AH.			4AH
8	**08H**	**Global Control 6**			**24H**
	Bit	**Function**			
	7-0	*Reserved For Factory Testing –Do Not Read/Write.*			24H
9	**09H**	**Global Control 7**			**28H**
	Bit	**Function**			
	7-0	*Reserved For Factory Testing –Do Not Read/Write.*			28H
10	**0AH**	**Global Control 8**			**24H**
	Bit	**Function**			
	7-0	*Reserved For Factory Testing –Do Not Read/Write.*			24H
11	**0BH**	**Global Control 9**			**00H**
	Bit	**Function**			
	7-2	*Reserved For Factory Testing –Do Not Write.*			0
	1	LED Mode->	*0=MODE 0*	*1=MODE 1*	0[1]
		LED 0 (Red)	Speed	Full-Duplex	
		LED 1 (Yel)	Full-Dx/Collision	10MLink/Activity	
		LED 2 (Grn)	Link/Activity	100MLink/Act	
		This function may optionally be selected via DIP switch S2-4 (ON=LED Mode 1). See Note 1.			
	0	Special TPID Mode (Spanning Tree Only): Used for direct mode forwarding from port 5 using spanning tree function. **Spanning tree function is not implemented in this model and this bit should remain set to 0.**			0
12	**0CH**	*Reserved – Do Not Modify*			**00H**
13	**0DH**	*Reserved – Do Not Modify*			**00H**
14	**0EH**	*Reserved – Do Not Modify*			**00H**
15	**0FH**	*Reserved – Do Not Modify*			**00H**

PORT REGISTERS: *The following registers are used to enable features assigned on a per-port basis. The register bit assignments are the same for all 5 ports, but the address of each port is different.*

REG		DESCRIPTION	DEF
16	**10H**	**Port 1 Control 0**	**00H**
	Bit	**Function**	
	7	Broadcast Storm Protection Enable: 1=Enable for ingress packets on the port; 0=Disable broadcast storm protection.	0
	6	Diffserv/DSCP Priority Classification Enable: 1=Enable Diffserv for ingress packets on the port; 0=Disable Diffserv function.	0

Register Map

REG		DESCRIPTION	DEF
16	**10H**	**Port 1 Control 0…continued**	**00H**
	Bit	**Function**	
	5	802.1p Priority Classification Enable: 1=Enable for ingress packets on the port; 0=Disable 802.1p priority classification.	0
	4	Port-Based Priority Classification Enable: 1=Port ingress packets are classified as high priority if "Diffserv" or "802.1p" are not enabled, or if unit fails to classify. 0=Ingress packets on port will be classified as low priority if "Diffserv" or "802.1p" are not enabled, or if unit fails to classify. **Note:** "Difserv", "802.1p", and port priority can all be enabled at the same time. The or'ed result of 802.1p and Diffserv/DSCP overwrites port priority.	0
	3	*Reserved – Do Not Write*	0
	2	Tag Insertion Enable: 1=When packets are output on a port, the switch will add 802.1Q tags to packets without 802.1Q tags when received. The switch will NOT add tags to packets already tagged. The tag inserted is the ingress port VLAN ID "port VID". 0=Disable tag insertion.	0
	1	Tag Removal: 1=When packets are output on a port, the switch will remove 802.1Q tags from packets with 802.1Q tags when received. The switch will NOT modify packets received without tags. 0=Disable tag removal.	0
	0	Priority Port Split Enable: 1=The port output queue is split into high and low priority queues; 0=Single output queue on the port. No priority differentiation even though packets are classified into high or low priority.	0
32	**20H**	**Port 2 Control 0 -**See Port 1 Control 0 Description.	00H
48	**30H**	**Port 3 Control 0 -**See Port 1 Control 0 Description.	00H
64	**40H**	**Port 4 Control 0 -**See Port 1 Control 0 Description.	00H
80	**50H**	**Port 5 Control 0 -**See Port 1 Control 0 Description.	00H
17	**11H**	**Port 1 Control 1**	**1FH**
	Bit	**Function**	
	7	Sniffer Port: 1=Port is a designated "sniffer port" and will transmit packets that are monitored; 0=Port is a normal port.	0
	6	Receive Sniff: 1=All the packets received on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port". 0=No receive monitoring.	0

Register Map

REG		DESCRIPTION	DEF
17	**11H**	**Port 1 Control 1…continued**	**1FH**
	Bit	**Function**	
	5	Transmit Sniff: 1=All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port". 0=No transmit monitoring.	0
	4-0	Port VLAN Membership – Define VLAN ports: 1=Include Port; 0=Exclude Port. Bit 4=Port 5, Bit 3=Port 4, Bit 2=Port 3, Bit 1=Port 2, Bit 0=Port 1. **Note that a port can only communicate within the membership if it is included.**	11111
33	**21H**	**Port 2 Control 1 –**See Port 1 Control 1 Description	**1FH**
49	**31H**	**Port 3 Control 1 –**See Port 1 Control 1 Description	**1FH**
65	**41H**	**Port 4 Control 1 –**See Port 1 Control 1 Description	**1FH**
81	**51H**	**Port 5 Control 1 -**See Port 1 Control 1 Description	**1FH**
18	**12H**	**Port 1 Control 2**	**0EH/ 06H**
	Bit	**Function**	
	7	*Reserved – Do Not Write*	0
	6	Ingress VLAN Filtering: 1=The switch will discard packets whose VLAN ID (VID) port membership in the VLAN table bits [20:16] does not include the ingress port. 0=No ingress VLAN filtering.	0
	5	Discard Non-PVID Packets: 1=Switch will discard packets whose VLAN ID(VID) does not match the ingress port default VID. 0=No packets will be discarded.	0
	4	Force Flow Control: 1=Always enable Rx & Tx flow control on the port, regardless of auto-negotiation result. 0=The flow control is enabled based on auto-negotiation result. **Note:** Setting a port for both half-duplex and forced flow control is an *illegal configuration*. Half-duplex uses another form of flow control (non-standard) called back pressure (see bit 3 below). **Port 4 ONLY – This function may be optionally controlled for port 4 via DIP switch S1-8.**	0
	3	Back Pressure Enable (Half-Duplex Only): 1=Enable port half-duplex back pressure. This is the default setting in EEPROM Mode. 0=Disable port half-duplex back pressure (default). **This function may optionally be configured via DIP switch S1-3 which is OFF by default.**	1/0

Register Map

REG		DESCRIPTION	DEF
18	**12H**	**Port 1 Control 2…continued**	**0EH/ 06H**
	Bit	**Function**	
	2	Transmit Enable (For Spanning Tree Support): 1=Enable packet transmission on the port. 0=Disable packet transmission on the port (not used on this model). **Spanning tree function is not implemented in this model and this bit should remain set to 1.**	1
	1	Receive Enable (For Spanning Tree Support): 1=Enable packet reception on the port. 0=Disable packet reception on the port (not used on this model). **Spanning tree function is not implemented in this model and this bit should remain set to 1.**	1
	0	Learning Disable (For Spanning Tree Support): 1=Disable switch address learning capability (not used on this model). 0=Enable switch address learning. **Spanning tree function is not implemented in this model and this bit should remain set to 0.**	0
34	**22H**	**Port 2 Control 2** -See Port 1 Control 2 Description.	**0EH**
50	**32H**	**Port 3 Control 2** -See Port 1 Control 2 Description.	**0EH**
66	**42H**	**Port 4 Control 2** -See Port 1 Control 2 Description.	**0EH**
82	**52H**	**Port 5 Control 2** -See Port 1 Control 2 Description.	**0EH**

The Port Control 3 and Control 4 registers that follow serve two purposes:
(1) They are associated with the ingress untagged packets and used for egress tagging.
(2) They define default VLAN ID (VID) for the ingress untagged or null-VID-tagged packets and are used for address look-up.

REG		DESCRIPTION	DEF
19	**13H**	**Port 1 Control 3**	**00H**
	Bit	**Function**	
	7-0	Port Default Tag Bits [15:8] Consisting Of: Bits 7-5: User Priority Bits; Bit 4: CFI Bit; Bits 3-0: VLAN Identification VID[11:8]	0
35	**23H**	**Port 2 Control 3** -See Port 1 Control 3 Description.	00H
51	**33H**	**Port 3 Control 3 -**See Port 1 Control 3 Description.	00H
67	**43H**	**Port 4 Control 3 -**See Port 1 Control 3 Description.	00H
83	**53H**	**Port 5 Control 3 -**See Port 1 Control 3 Description.	00H
20	**14H**	**Port 1 Control 4**	**01H**
	Bit	**Function**	
	7-0	Port Default Tag Bits [7:0]: VID[7:0]	0000 0001
36	**24H**	**Port 2 Control 4 -**See Port 1 Control 4 Description.	01H
52	**34H**	**Port 3 Control 4** -See Port 1 Control 4 Description.	01H
68	**44H**	**Port 4 Control 4 -**See Port 1 Control 4 Description.	01H
84	**54H**	**Port 5 Control 4 -**See Port 1 Control 4 Description.	01H

Register Map

REG		DESCRIPTION	DEF
Rate Limiting: *This switch supports hardware rate limiting at its transmit and/or receive ports. Rate limiting is a form of flow control that enforces a strict bandwidth limit by counting the number of bytes to cross a port in one second. You specify the maximum number of bytes in multiples of 32Kbps (32000 bits per second). Port Control 5-11 Registers 21-27 allow you to apply different rate controls for both high priority and low priority packets.*			
21	**15H**	**Port 1 Control 5**	**00H**
	Bit	**Function**	
	7-0	Transmit HIGH Priority Rate Control [7:0]: This byte along with port control 7 bits [3:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be transmitted (in a unit of 32K bits or 4K bytes in a one second period).	0
37	**25H**	**Port 2 Control 5 -**See Port 1 Control 5 Description.	**00H**
53	**35H**	**Port 3 Control 5** -See Port 1 Control 5 Description.	**00H**
69	**45H**	**Port 4 Control 5 -**See Port 1 Control 5 Description.	**00H**
85	**55H**	**Port 5 Control 5 -**See Port 1 Control 5 Description.	**00H**
22	**16H**	**Port 1 Control 6**	**00H**
	Bit	**Function**	
	7-0	Transmit LOW Priority Rate Control [7:0]: This byte along with port control 7 bits [7:4] form a 12-bit field to determine how many "32Kbps" low priority blocks can be transmitted (in a unit of 32K bits or 4K bytes in a one second period).	0
38	**26H**	**Port 2 Control 6 -**See Port 1 Control 6 Description.	**00H**
54	**36H**	**Port 3 Control 6 -**See Port 1 Control 6 Description.	**00H**
70	**46H**	**Port 4 Control 6 -**See Port 1 Control 6 Description.	**00H**
86	**56H**	**Port 5 Control 6 -**See Port 1 Control 6 Description.	**00H**
23	**17H**	**Port 1 Control 7**	**00H**
	Bit	**Function**	
	7-4	Transmit LOW Priority Rate Control [11:8]: This nibble along with port control 6 bits [7:0] form a 12-bit field to determine how many "32Kbps" low priority blocks can be transmitted (in a unit of 32K bits or 4K bytes in a one second period).	0000
	3-0	Transmit HIGH Priority Rate Control [11:8]: This nibble along with port control 5 bits [7:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be transmitted (in a unit of 32K bits or 4K bytes in a one second period).	0000
39	**27H**	**Port 2 Control 7 -**See Port 1 Control 7 Description.	**00H**
55	**37H**	**Port 3 Control 7 -**See Port 1 Control 7 Description.	**00H**
71	**47H**	**Port 4 Control 7 -**See Port 1 Control 7 Description.	**00H**
87	**57H**	**Port 5 Control 7 -**See Port 1 Control 7 Description.	**00H**

Register Map

REG		DESCRIPTION	DEF
24	**18H**	**Port 1 Control 8**	**00H**
	Bit	**Function**	
	7-0	Receive HIGH Priority Rate Control [7:0]: This byte along with Port Control 10 bits [3:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be received (in a unit of 32K bits or 4K bytes in a one second period).	0
40	**28H**	**Port 2 Control 8 -**See Port 1 Control 8 Description.	**00H**
56	**38H**	**Port 3 Control 8 -**See Port 1 Control 8 Description.	**00H**
72	**48H**	**Port 4 Control 8 -**See Port 1 Control 8 Description.	**00H**
88	**58H**	**Port 5 Control 8 -**See Port 1 Control 8 Description.	**00H**
25	**19H**	**Port 1 Control 9**	**00H**
	Bit	**Function**	
	7-0	Receive LOW Priority rate Control [7:0]: This byte along with Port Control 10 bits [7:4] form a 12-bit field to determine how many "32Kbps" low priority blocks can be received (in a unit of 32K bits or 4K bytes in a one second period).	0
41	**29H**	**Port 2 Control 9** -See Port 1 Control 9 Description.	**00H**
57	**39H**	**Port 3 Control 9 -**See Port 1 Control 9 Description.	**00H**
73	**49H**	**Port 4 Control 9 -**See Port 1 Control 9 Description.	**00H**
89	**59H**	**Port 5 Control 9 -**See Port 1 Control 9 Description.	**00H**
26	**1AH**	**Port 1 Control 10**	**00H**
	Bit	**Function**	
	7-4	Receive LOW Priority Rate Control [11:8]: This nibble along with Port Control 9 bits [7:0] form a 12-bit field to determine how many "32Kbps" low priority blocks can be received (in a unit of 32K bits or 4K bytes in a one second period).	0000
	3-0	Receive HIGH Priority Rate Control [11:8]: This nibble along with Port Control 8 bits [7:0] form a 12-bit field to determine how many "32Kbps" high priority blocks can be received (in a unit of 32K bits or 4K bytes in a one second period).	0000
42	**2AH**	**Port 2 Control 10** –Port 1 Control 10 Description.	**00H**
58	**3AH**	**Port 3 Control 10** -Port 1 Control 10 Description.	**00H**
74	**4AH**	**Port 4 Control 10** -Port 1 Control 10 Description.	**00H**
90	**5AH**	**Port 5 Control 10** -Port 1 Control 10 Description.	**00H**

Register Map

REG		DESCRIPTION	DEF
27	**1BH**	**Port 1 Control 11**	**00H**
	Bit	**Function**	
	7	Receive Differential Priority Rate Control: 1=If bit 6 is also "1", this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also "1", this will enable receive rate control on high priority packets at the high priority rate. 0=receive rate control will be based on the low priority rate for all packets on this port.	0
	6	Low Priority Receive Rate Control Enable: 1=Enable port low priority receive rate control. 0=Disable port low priority receive rate control.	0
	5	High Priority Receive Rate Control Enable: 1= If bit 7 is also "1", this will enable the port high priority receive rate control feature. If bit 7 is "0" and bit 6 is "1", all receive packets on this port will be rate controlled at the low priority rate. 0=Disable port high priority receive rate control.	0
	4	Low Priority Receive Rate Flow Control Enable: 1=Flow control may be asserted if the port's low priority receive rate is exceeded. 0=Flow control is not asserted if the port's low priority receive rate is exceeded.	0
	3	High Priority Receive Rate Flow Control Enable: 1=Flow control may be asserted if the port's high priority receive rate is exceeded (to use this, the differential receive rate control must be on, see bit 7). 0=Flow control is not asserted if the port's high priority receive rate is exceeded.	0
	2	Transmit Differential Priority Rate Control: 1=Will do a transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively. 0=Will do transmit rate control on any packets. The rate counters defined in low priority will be used.	0
	1	Low Priority Transmit Rate Control Enable: 1=Enable port's low priority transmit rate control. 0=Disable port's low priority transmit rate control.	0
	0	High Priority Transmit Rate Control Enable: 1=Enable port's high priority transmit rate control. 0=Disable port's high priority transmit rate control.	0
43	**2BH**	**Port 2 Control 11** -Port 1 Control 11 Description.	**00H**
59	**3BH**	**Port 3 Control 11** -Port 1 Control 11 Description.	**00H**
75	**4BH**	**Port 4 Control 11** -Port 1 Control 11 Description.	**00H**
91	**5BH**	**Port 5 Control 11** -Port 1 Control 11 Description.	**00H**

Register Map

Port Control 12 and 13 registers 28 & 29, and Port Status 0 contents can be accessed by MIIM (MDC/MDIO) interface via the standard MIIM register definition.

REG		DESCRIPTION	DEF
28	**1CH**	**Port 1 Control 12**	**5DH**
	Bit	**Function**	
	7	Disable Auto-Negotiation (AN): 1=Disable Auto-Negotiation – Speed and Duplex are decided by bits 6 & 5 of this register. 0=Auto-Negotiation is ON.	0
	6	Force Speed (w/ Auto-Negotiation Off): 1=Force 100baseT if Auto-Neg is disabled via bit 7. 0=Force 10baseT if Auto-Neg is disabled via bit 7.	1
	5	Force Duplex (w/ Auto-Negotiation Off): 1=Force Full-Duplex if Auto-Neg is disabled, or Auto-Neg is enabled but failed. 0=Force Half-Duplex if Auto-Neg is disabled, or Auto-Neg is enabled but failed. **Note that this function may be optionally configured via DIP switch S1-7 for port 4 only (ON=Half-Duplex) following reset.**	0
	4	Advertise Flow-Control Capability: 1=Advertise Flow-Control Capability. 0=Suppress Flow-Control Capability from transmission to link partner.	1
	3	Advertise 100BaseT Full-Duplex Capability: 1=Advertise 100BaseT Full-Duplex capability. 0=Suppress 100BaseT Full-Duplex capability from transmission to link partner	1
	2	Advertise 100BaseT Half-Duplex Capability: 1=Advertise 100BaseT Half-Duplex capability. 0=Suppress 100BaseT Half-Duplex capability from transmission to link partner	1
	1	Advertise 10BaseT Full-Duplex Capability: 1=Advertise 10BaseT Full-Duplex Capability. 0=Suppress 10BaseT Full-Duplex Capability from transmission to Link Partner	0
	0	Advertise 10BaseT Half-Duplex Capability: 1=Advertise 10BaseT Half-Duplex Capability. 0=Suppress 10BaseT Half-Duplex Capability from transmission to Link Partner	1
44	**2CH**	**Port 2 Control 12 (Port 1 Control 12 Description)**	**5FH**
60	**3CH**	**Port 3 Control 12 (Port 1 Control 12 Description)**	**5FH**
76	**4CH**	**Port 4 Control 12 (Port 1 Control 12 Description)**	**5FH**
92	**5CH**	**Port 5 Control 12 (Port 1 Control 12 Description)**	**5FH**

Register Map

REG		DESCRIPTION	DEF
29	**1DH**	**Port 1 Control 13**	**00H**
	Bit	**Function**	
	7	LED Disable: 1=Turn OFF all port status LED's; 0=Normal Operation.	0
	6	Txids: 1=Disable Port Transmitter; 0=Normal Operation.	0
	5	Restart Auto-Negotiation: 1=Restart Auto-Negotiation; 0=Normal Operation.	0
	4	Disable Far-End Fault: 1=Disable far-end fault detection and pattern transmission. 0=Enable far-end fault detection and pattern transmission.	0
	3	1=Power Down; 0=Normal Operation.	0
	2	1=Disable Auto-MDI/MDI-X function. 0=Enable Auto-MDI/MDI-X function.	0
	1	Forced MDI: 1=Force PHY into MDI mode if auto MDI/MDI-X is disabled; 0=Do NOT force PHY into MDI mode.	0
	0	Loopback: 1=Perform "local loopback" (loop back the PHY Tx channel to its Rx channel); 0=Normal operation.	0
45	**2DH**	**Port 2 Control 13 (Port 1 Control 13 Description)**	**00H**
61	**3DH**	**Port 3 Control 13 (Port 1 Control 13 Description)**	**00H**
77	**4DH**	**Port 4 Control 13 (Port 1 Control 13 Description)**	**00H**
93	**5DH**	**Port 5 Control 13 (Port 1 Control 13 Description)**	**00H**
30	**1EH**	**Port 1 Status 0 (READ ONLY)**	**00H**
	Bit	**Function**	
	7	1=Port is MDI; 0=Port is MDI-X.	0
	6	1=Auto-Negotiation (AN) Done; 0=AN Not Done.	0
	5	1=Link Good; 0=Link Not Good.	0
	4	1=Link Partner Flow Control Capable. 0=Link Partner NOT Flow Control Capable.	0
	3	1=Link Partner is 100BT Full-duplex Capable. 0=Link Partner NOT 100BT Full-Duplex Capable.	0
	2	1=Link Partner is 100BT Half-Duplex Capable. 0=Link Partner NOT 100BT Half-Duplex Capable.	0
	1	1=Link Partner is 10BT Full-Duplex Capable. 0=Link Partner NOT 10BT Full-Duplex Capable.	0
	0	1=Link Partner is 10BT Half-Duplex Capable. 0=Link Partner NOT 10BT Half-Duplex Capable.	0
46	**2EH**	**Port 2 Status 0 -**See Port 1 Status 0 Description.	**00H**
62	**3EH**	**Port 3 Status 0 -**See Port 1 Status 0 Description.	**00H**
78	**4EH**	**Port 4 Status 0 -**See Port 1 Status 0 Description.	**00H**
94	**5EH**	**Port 5 Status 0 -**See Port 1 Status 0 Description.	**00H**

Register Map

REG		DESCRIPTION	DEF
31	**1FH**	**(Reserved) Port 1 Status 1 (READ ONLY)** 1=Perform PHY MAC Tx Loopback to Rx); 0=Norm	**00H**
	Bit	**Function**	
	7-1	*Reserved – Do Not Write*	0
	0	Far-End Fault: 1=Far end fault status detected. 0=No far end fault status detected.	0
47	**2FH**	**Port 2 Status 1** –See Port 1 Status 1 Description.	**00H**
63	**3FH**	**Port 3 Status 1** –See Port 1 Status 1 Description.	**00H**
79	**4FH**	**Port 4 Status 1** –See Port 1 Status 1 Description.	**00H**
95	**5FH**	**Port 5 Status 1 -**See Port 1 Status 1 Description.	**00H**

ADVANCED CONTROL REGISTERS 96..103 – *The IPv4 TOS (Type Of Service) priority control registers implement a fully decoded 64-bit DSCP (Differentiated Services Code Point) register used to determine priority from the 6-bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.*

REG		DESCRIPTION	DEF
96	**60H**	**TOS Priority Control Register 0**	**00H**
	Bit	**Function**	
	7-0	DSCP[63:56]	0
97	**61H**	**TOS Priority Control Register 1**	**00H**
	7-0	DSCP[55:48]	0
98	**62H**	**TOS Priority Control Register 2**	**00H**
	7-0	DSCP[47:40]	0
99	**63H**	**TOS Priority Control Register 3**	**00H**
	7-0	DSCP[39:32]	0
100	**64H**	**TOS Priority Control Register 4**	**00H**
	7-0	DSCP[31:24]	0
101	**65H**	**TOS Priority Control Register 5**	**00H**
	7-0	DSCP[23:16]	0
102	**66H**	**TOS Priority Control Register 6**	**00H**
	7-0	DSCP[15:8]	0
103	**67H**	**TOS Priority Control Register 7**	**00H**
	7-0	DSCP[7:0]	0

ADVANCED CONTROL REGISTERS 104..109 – *Registers 104-109 define the switching engine's MAC address. This 48-bit address is used as the source address in MAC pause control frames.*

REG		DESCRIPTION	DEF
104	**68H**	**MAC Address Register 0**	**00H**
	Bit	**Function**	
	7-0	MACA[47:40]	0
105	**69H**	**MAC Address Register 1**	**10H**
	7-0	MAC[39:32]	10H
106	**6AH**	**MAC Address Register 2**	**A1H**
	7-0	MACA[31:24]	A1H

Register Map

REG		DESCRIPTION	DEF
107	**6BH**	**MAC Address Register 3**	**FFH**
	7-0	MACA[23:16]	FFH
108	**6CH**	**MAC Address Register 4**	**FFH**
	7-0	MACA[15:8]	FFH
109	**6DH**	**MAC Address Register 5**	**FFH**
	7-0	MACA[7:0]	FFH
ADVANCED CONTROL REGISTERS 110-120 – Use registers 110 & 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters. For SPI Slave Mode only.			
REG		**DESCRIPTION**	**DEF**
110	**6EH**	**Indirect Access Control 0 (SPI Mode Only)**	**00H**
	Bit	**Function**	
	7-5	*Reserved*	000
	4	Read-High/Write-Low: 1=Read cycle; 0=Write cycle.	0
	3-2	Table Select (SPI Slave Mode Only): 00=Static MAC address table selected. 01=VLAN table selected. 10=Dynamic address table selected. 11=MIB counter selected.	00
	1-0	Indirect Access High – Bits 9-8 of indirect address	00
111	**6FH**	**Indirect Access Control 1 (SPI Mode Only)**	**00H**
	Bit	**Function**	
	7-0	Indirect Address Low: Bits 7-0 of indirect address. **Note:** A write to register 111 will actually trigger a command. Read or write access will be decided by bit 4 of register 110.	0
REG		**DESCRIPTION**	**DEF**
112	**70H**	**Indirect Data Register 8**	00H
	Bit	**Function**	
	7-0	Indirect Data Bits 68-64 (Unused upper 3 bits 000)	00000
113	**71H**	**Indirect Data Register 7**	00H
	7-0	Indirect Data Bits 63-56	0..0
114	**72H**	**Indirect Data Register 6**	00H
	7-0	Indirect Data Bits 55-48	0..0
115	**73H**	**Indirect Data Register 5**	00H
	7-0	Indirect Data Bits 47-40	0..0
116	**74H**	**Indirect Data Register 4**	00H
	7-0	Indirect Data Bits 39-32	0..0
117	**75H**	**Indirect Data Register 3**	00H
	7-0	Indirect Data Bits 31-24	0..0
118	**76H**	**Indirect Data Register 2**	00H
	7-0	Indirect Data Bits 23-16	0..0
119	**77H**	**Indirect Data Register 1**	00H
	7-0	Indirect Data Bits 15-8	0..0
120	**78H**	**Indirect Data Register 0**	00H
	7-0	Indirect Data Bits 7-0	0..0

Register Map

REG		DESCRIPTION	DEF
IMPORTANT: DO NOT WRITE/READ TO/FROM REGISTERS 121-127, AS DOING SO MAY PREVENT PROPER OPERATION. THESE REGISTERS ARE RESERVED FOR FACTORY TESTING ONLY			
121	**79H**	**Digital Testing Status 0 (Read Only)**	00H
	Bit	**Function**	
	7-0	*Reserved - Qm_split Status*	0..0
122	**7AH**	**Digital Testing Status 1 (Read Only)**	00H
	7-0	*Reserved – Dbg[7:0]*	0..0
123	**7BH**	**Digital Testing Control 0**	00H
	7-0	*Reserved – Dbg[12:8]*	0..0
124	**7CH**	**Digital Testing Control 1**	00H
	7-0	*Reserved – Do Not Read/Write*	0..0
125	**7DH**	**Analog Testing Control 0**	00H
	7-0	*Reserved – Do Not Read/Write*	0..0
126	**7EH**	**Analog Testing Control 1**	00H
	7-0	*Reserved – Do Not Read/Write*	0..0
127	**7FH**	**Analog Testing Status (Read Only)**	00H
	7-0	*Reserved – Do Not Read/Write*	0..0

Notes (Register Map):

1. LED Display Modes: Each port of this module has three port status LED's. The relative function of these LED's is determined by DIP switch S2-4 in DIP Switch Mode, or bit 1 of register 11. The following table gives the default LED indication (mode 0, DIP switch S2-4 OFF or bit 1 of register 11 clear), and the optional LED indication mode (mode 1, DIP switch S2-4 ON or bit 1 of register 11 set):

Mode	LED 1 (Red)	LED 2 (Yellow)	LED 3 (Green)
0	Speed (On= 100M, Off= 10Mbps)	Full-Duplex+Coll (Constant ON= FDX, Intermittent ON= Collision, Constant OFF=Half+No Coll)	Link + Activity (ON)
1	Full-Duplex (ON= FDX, OFF=HDX)	Link Activity (10Mbps Only)	Link Activity (100Mbps Only)

SPI Slave Mode

Use of this mode is reserved for factory purposes only and will not be covered in detail here. Acromag makes no guaranty of operation in this mode.

The same socket that is used to program the EEPROM memory also doubles as an SPI interface to the internal switch ASIC. This provides "run-time" access to all of the registers outlined in the EEPROM Mode, plus access to all static MAC entries, the VLAN table, the dynamic MAC address table, and the MIB counters. Note that the SPI interface of this model is used to read and modify the registers in the switch ASIC itself, and does not access or update the EEPROM of the module. As such, changes made in SPI mode will be lost if power is interrupted.

SPI Slave Mode

In SPI Slave Mode, no EEPROM memory is used and ASIC registers are configured via the SPI interface after reset (during run-time). Register 1 provides a start switch bit that is used to start a new configuration, after the registers have been configured. Changes made to registers in SPI mode will be lost if power is interrupted.

IMPORTANT: The SPI connections are limited to short distances and operate at much higher clock speeds than the I^2C interface used to program EEPROM. As such, accessory cable 5035-365 is not sufficient for reliable operation in SPI Mode. This mode is reserved for factory use only and Acromag makes no guaranty of operation in this mode.

Use of the advanced features in SPI Slave Mode is generally beyond the scope of most applications and is not recommended for most users. Additional expertise is required to exploit these features and these topics are not discussed in this manual. Some of these features will only be presented here in brief, because the unit provides these capabilities and to thwart the inadvertent misuse of some registers.

To communicate with a module in SPI Mode, you must set DIP switch S2-1 and S2-3 ON to set the module to SPI Slave Mode (ON). Additionally, make sure DIP switch S2-2 is OFF to enable SPI access.

TERMS AND CONCEPTS

Refer to this section for more information on unfamiliar terms, topics, and operating modes.

Auto MDI/MDI-X Crossover and Auto Polarity

The MDI (Medium Dependent Interface) is the part of the Media Attachment Unit (MAU) that provides the physical and electrical connection to the cabling medium. MDI-X (MDI crossover) is a version of MDI that enables a connection between *like-wired* devices. In practice, MDI ports connect to MDI-X ports via straight-through twisted pair cable, whereas MDI-to-MDI and MDIX-to-MDIX require a crossover cable. With auto-crossover, the port will automatically detect the remote transmit and receive pairs and correctly assign them to the internal transmit and receive channels. Thus, it is not necessary to make a distinction between 1:1 straight-through cable connections, or crossover connections, when wiring to this device. This also eliminates the necessity of having to provide an additional up-link/crossover port on the device, as all ports of the 900EN-S005 are equivalent. Additionally, with auto-polarity correction, this device will detect and correct the plus and minus polarities of the differential transmit and receive channels, as required.

Auto MDI/MDI-X Controls

CONTROL REGISTER	FUNCTION
Port Control 13 bit 2	Set to disable Auto-MDI/MDI-X. Clear to enable Auto-MDI/MDI-X (Default).
Port Control 13 bit 1	Set to force MDI mode at port if auto-MDI/MDI-X is disabled. Clear to not force MDI mode.
Port Status 0 bit 7	Read Only to determine if port is MDI (set), or MDI-X (clear).

TERMS AND CONCEPTS

Auto-Negotiation/ Auto-Sense

This feature allows each port to automatically select the best common mode of operation with another node with respect to speed/duplex and will automatically establish a half or full duplex connection at 10Mbps or 100Mbps as required.

Auto Negotiation Controls

CONTROL REGISTER	FUNCTION
Port Control 12 bit 7	Set to disable Auto-Negotiation, clear to enable. If AN is disabled, speed and duplex are determined by bits 6 and 5 of Port Control 12 register.
Port Control 12 bit 6	If AN is disabled, set to force speed to 100baseT, clear to force 10baseT.
Port Control 12 bit 5	If AN is disabled or if AN is enabled but failed, set to force Full-Duplex, clear to force Half-Duplex.
Port Control 13 bit 5	Set to restart Auto-Negotiation. Clear for normal operation.
Port Status 0 bit 6	Read Only to determine if port auto-negotiation is done (set), or not done (clear).
Port Control 12 Bit 3	Advertise 100baseT Full-Duplex Capability
Port Control 12 Bit 3	Advertise 100baseT Half-Duplex Capability
Port Control 12 Bit 3	Advertise 10baseT Full-Duplex Capability
Port Control 12 Bit 3	Advertise 10baseT Half-Duplex Capability
Port Status 0 Bit 3	Read for 100baseT Full-Duplex Capable.
Port Status 0 Bit 2	Read for 100baseT Half-Duplex Capable.
Port Status 0 Bit 1	Read for 10baseT Full-Duplex Capable.
Port Status 0 Bit 0	Read for 10baseT Half-Duplex Capable.

Automatic Address Management – Learning, Aging, Migration

This switch will automatically learn and store up to 1024 MAC addresses with their port number and timestamp. It will update its look-up table with a new entry if the packet's source address does not already exist in the look-up table, and if the received packet has no errors and is of legal length. If the table is already full, the last entry of the table (oldest) will be deleted first to make room for the new entry. The switch will also monitor whether a station has moved and will update its table with new source port information if a received packet's source address is already in the table, and if the received packet has no errors and is of legal length (auto-migration). The switch will also update the time stamp information of a record whenever the corresponding source address appears. It will use this timestamp to determine the age of a record and if a record is not updated for 5 minutes, the record will be removed from the table (auto-aging). Auto-aging may also be optionally disabled via DIP switch 1 on the board.

Address Management Controls

CONTROL REGISTER	FUNCTION
Global Control 1 Bit 2	Set to enable automatic address aging (default). Normal aging period is 300±75s. Clear to disable aging. ***This is also controlled via DIP switch 1 in DIP Switch Mode.***
Global Control 1 Bit 1	Set to enable fast aging (~800us). Clear for standard aging period of 300±75s.
Global Control 0 Bit 0	Set to cause fast address aging period of 800us for a change from "link" to "no link". After aging cycle is complete, the port will revert to normal aging cycle of 300±75s. Clear to prevent fast aging upon link change.

TIP: *If you hot-swap port connections after applying power, sometimes it may appear the switch has stopped communicating with your device, as it may take up to 5 minutes to recognize the new connection (aging period). You can wait the requisite 5 minutes and the switch will recover on its own, or you can simply reset the module. Optionally, you can either enable fast aging, or enable fast aging when link status has changed to avoid this.*

CSMA/CD

Recall that for half-duplex communication, transmit and receive are possible, but not at the same time. If two stations attempt to simultaneously transmit data along the same network, a collision will occur. Half-duplex Ethernet makes use of **Carrier Sense Multiple Access with Collision Detection (CSMA/CD)** to arbitrate access to the network. *Carrier Sense* requires that all stations must listen for no traffic on the network for a period of time before transmitting data. *Multiple Access* guaranties that all stations on the network have equal access to transmit data and that any station is allowed to repeat the transmit sequence without first waiting for the other stations to transmit their data. *Collision Detection* is the process by which a transmitting station must detect a collision of its data with any other station's transmitting data, should both stations attempt to simultaneously transmit data.

On shared ethernet, any device can try to send a data frame at any time. Normally, each device will first sense whether the line is idle and available for use (channel clear). If it is clear, the device will begin to transmit its first frame. During this transmission, the device will listen for a time to ensure that its transmission is being faithfully produced and that no other device attempts a simultaneous transmission. If another device also happened to send a frame at approximately the same time, then a collision is detected (an abnormal voltage level that exceeds the Collision Detect threshold) and the originating station will attempt to reinforce the collision by applying a JAM signal (frame preamble plus 32 alternating bits). The jam signal causes non-transmitting stations to wait until the jam signal ends prior to attempting to transmit and will signal to all stations sharing the connection to discard the frame. Each competing device then waits a random amount of time (back-off) and retries its transmission until it is successfully sent.

Exponential Backoff

The process by which a host that has experienced a collision on a network waits for an amount of time before attempting to retransmit refers to its back-off. A random back-off minimizes the probability that the same nodes will collide again. Sometimes increasing the back-off period after each collision will also help to prevent repeated collisions, especially when the network is heavily loaded. In dealing with network contention, this switch implements the IEEE Standard 802.3 binary exponential back-off algorithm, plus an optional "aggressive mode" backoff to further enhance performance.

CSMA/CD

Collision Retry

The switch will normally retry a transmission if a collision occurs and drop packets after 16 or more collisions. Optionally, you can choose not to drop packets after 16 or more collisions via DIP switch S1-4 (or Register 4 bit 3). Note that in order for CSMA/CD to function, all of these devices (stations, hubs, etc.) must reside within the same collision domain (e.g. connect to the same switch port).

Illegal Frames

The 900EN-S005 will accept frames up to 1536 bytes (less if VLAN tags are present—1522 for tagged packets or 1518 for untagged packets), or optionally up to 1916 bytes (huge packet support is enabled via Register 4 bit 2), and will discard frames less than 64 bytes (minimum valid packet size). DIP switch S1-6 (or Register 3 bit 3) may be used to disable the maximum frame length check.

Late Collision

After beginning transmission in CSMA/CD, a device listens for a period of time in order to detect a collision (this is the slot time). It listens for an amount of time equivalent to the time it would take to transmit the smallest valid packet in Ethernet (64 bytes or 512 bits of data). However, if a transmit packet has a collision after 512 bit times of the transmission, the packet will be dropped. Late collisions refer to collisions that exceed the slot time.

The occurrence of late collisions is indicative of illegal cable length. Protocol analyzers are often used to detect late collisions and troubleshoot cable problems.

Packet Frame Checking & Collision Controls

CONTROL REGISTER	FUNCTION
Global Control 1 bit 0 *(Also see Switch S1-5 in DIP Switch Mode)*	Half-Duplex Aggressive Back-Off Enable: Set to enable the more aggressive half-duplex back-off (proprietary). Clear for standard IEEE 802.3 binary exponential back-off.
Global Control 1 bit 3	Frame Length Field Check: Set to cause the switch to check the frame length field of the packet and if it doesn't match the measured length, drop the packet. Clear to not verify frame length.
Global Control 2 bit 3 *(Also see DIP Switch S1-4 in DIP Switch Mode)*	Disable Packet Drop For Excessive Collisions: Set to prevent packets from being dropped after 16 or more collisions occur. Clear to drop packets when 16 or more collisions occur.
Global Control 2 bit 2	Huge Packet Enable: Set to allow huge packets up to 1916 bytes long (this over-rides maximum legal packet size set below).
Global Control 2 bit 1 *(Also see Switch S1-6 in DIP Switch Mode)*	Maximum Legal Packet Size: Set to allow packet sizes up to 1536 bytes. Clear to set maximum to 1522 bytes (tagged packets), or 1518 bytes (untagged packets). Packets larger than this maximum will be dropped.

Note that under no conditions will a switch ever try to repair a bad packet, it simply drops bad packets and does not forward them.

CSMA/CD

With CSMA/CD, prior to beginning transmission, a device monitors the link to determine if it is inactive. If the link is active, it will wait before beginning to transmit. There may be other devices on the network that are also waiting to begin transmission at about the same time. If more than one device begins to transmit at the same time, a collision occurs. Each transmitting device continues to listen for a period of time and if the device senses activity during its transmission, it knows that a collision has occurred and a recovery procedure is initiated (collision detection is done by comparing voltage levels).

Slot Time

The *slot time* is the time after a device begins transmitting that it continues to listen for a collision. It is related to the time it would take to transmit 64 bytes or 512 bits of data (this is the minimum packet size with ethernet). Slot time is generally expressed in units of Bit Times. Bit times represent the rate of transmission. For a 10MHz system, the bit time is 100ns. For a 100MHz system, the bit time is 10ns. Therefore, the slot time is 51.2us for a 10BaseT system, and 5.12us for a 100BaseT system.

In order for each station to reliably detect collisions, the minimum transmission time for a complete frame must be at least one slot time. Further, the time required for collisions to propagate the entire network must be less than one slot time. As such, a station cannot finish transmitting a frame before detecting that a collision has occurred (unless the cable length is excessive). This requires that the maximum round-trip delay be less than 512 bit times. Thus, the slot time is also equivalent to the amount of time a device will wait after a collision before retransmitting. The 512 bit slot time effectively establishes the minimum size of an Ethernet frame as 64 bytes. This is why the slot time is sometimes defined as the time it takes to transmit 64 bytes. Note that any frame less than 64 bytes is considered a collision fragment and automatically discarded by receiving stations.

To illustrate how slot time is derived, assume that node A begins to transmit data to node B. This data travels along the cable in time TA. Also assume that some time after node A begins transmission, node B also begins to transmit, perhaps just before the data from node A arrives. Thus, when node A's data arrives at node B, node B knows immediately that a collision has just occurred and can begin recovery operations.

Node A will not know a problem has occurred until data from node B arrives in time TB. That is node A has to wait at least TA + TB before it can be assured that no collision has occurred during its transmission.

The standard also allows for some additional time (TC) necessary to sense the collision. The slot time is approximated by the sum TA+TB+TC. The sum TA + TB is the round trip delay along the cable between the nodes and TA is equal to TB. If the delay characteristics of the connecting cable is known, the maximum cable length can be approximated from the time delay TA.

Slot Time

The size of a network collision domain is often referred to as the *network diameter* and is related to the "round trip" delay limitation of 512 Bit times necessary for effective collision detection with CSMA.

The maximum size or diameter of a collision domain is determined by adding the repeater delays, the cable delay, NIC (Network Interface Card) delays, plus a safety factor of 5 bit times (one way) and making sure that this sum is less than or equal to 512 bit times (round trip). Good design practice also takes into account the collision sense time and by keeping the total delay time less than or equal to 80% of allowable, or about 400 bit times.

The following table gives typical delays (one way) for various Fast Ethernet components:

COMPONENT	MAXIMUM DELAY (us)
Fast Ethernet NIC	0.25us
Fast Ethernet Switch Port	0.25us
Class I Repeater	0.70us
Class II Repeater	0.46us
Cat 5 UTP Cable (per 100M/330ft)	0.55us
Multimode Fibre (per 100M/330ft)	0.50us
Collision Sensing Time	1.12us

Using the information given in the above table, plus a 5 bit time safety factor, you can determine if a given network connection is permissible by making sure that the one way delay between the two furthest nodes is less than half the slot time--25.6us (10BaseT), or 2.56us (100BaseT). Times given above are typical values for 100baseT components. Double these figures for round trip delay times (except collision sense time). You may use these values for feasibility studies, but you should recalculate using the actual time delays of your components as these times will vary between components.

Inter Packet Gap (IPG)

While slot time is the time after a device begins transmission that it listens for a collision, the inter-frame gap is the amount of time after the link becomes inactive that a device must wait before transmitting data on the link. Note that for shared Ethernet, the network has to be silent (no data transfer) for a few microseconds before any node can consider the network idle and start to transmit. This delay time applied between successive data packets is required by the network standard and is called the *interpacket gap time (IPG).* This delay is approximated by the signal propagation time on the cable which allows the "silence" to reach the remote end of the network so that all nodes can detect idle.

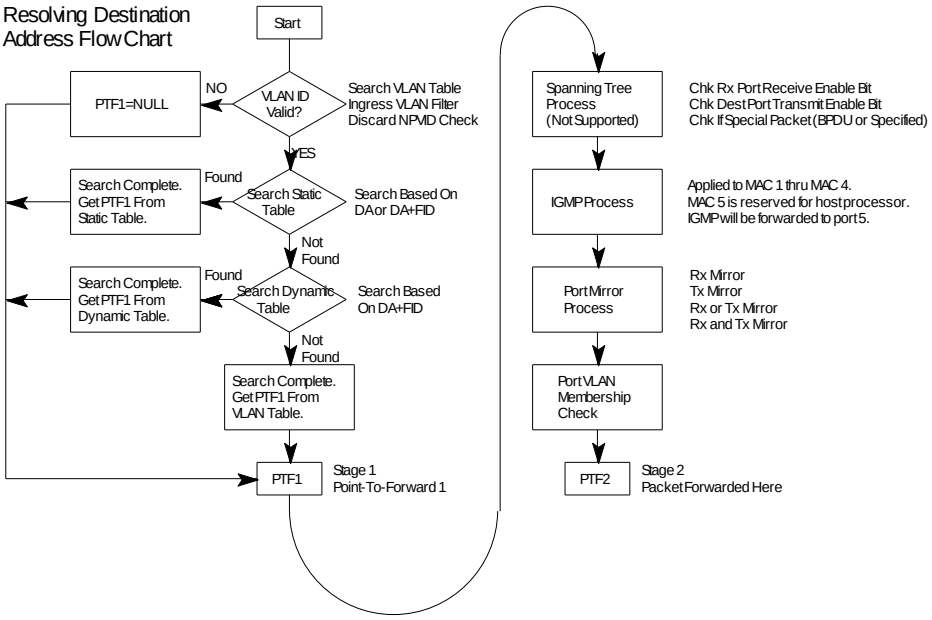
The Bit Time (BT) is simply the reciprocal of the data rate. With respect to the 900EN-S005, when a frame is successfully transmitted, the IPG is 96 bit times and measured between the two consecutive MTXEN (Transmit Enable). If the current packet is experiencing a collision, the 96 bit time IPG is measured from MCRS (Carrier Sense) and the next MTXEN (Transmit Enable).

Inter Packet Gap (IPG)

Network Time Parameter	10BaseT (10MHz)	100BaseT (100MHz)
Bit Time (BT)	100ns	10ns
Slot Time	512BT (51.2us)	512BT (5.12us)
InterPacket Gap Time	9.6us	0.96us

Switch Forwarding

The internal switch engine will forward packets according to a two stage algorithm illustrated in the following flow chart. It first looks up the VLAN ID, static table, and dynamic table for the Destination Address (DA) and resolves to a "port to forward 1" (PTF1). The PTF1 is then modified by the spanning tree (not supported), IGMP snooping, port mirroring, and port VLAN processes to resolve to a "port to forward 2" (PTF2). PTF2 is where the packet will be sent. Not all of these stages are supported by this model.



The 900EN-S005 will <u>not</u> forward the following packets:

- Error packets: Framing errors, FCS errors, alignment errors, and illegal-size packet errors.
- IEEE 802.3x Pause Frames: The switch will intercept these packets and perform the appropriate actions.
- Local Packets (Based on Destination Address Look-up): If the destination port from the look-up table matches the port where the packet was from, the packet is defined as a "local packet" and will not be forwarded.

Traffic Flow Controls

Recall that the flow of traffic on a network can be either half-duplex (one direction at a time), or full-duplex (simultaneous in both directions).

In 1995, the 802.3 Ethernet standard was modified to include provisions for 802.3u 100Mbps Fast Ethernet. Fast Ethernet operates using full-duplex communication in lieu of half-duplex with CSMA/CD. Thus, fast Ethernet implies a point-to-point Ethernet connection between two devices, with no possibility of collisions, allowing the stations at each end to transmit simultaneously (full-duplex).

Similarly, if only one device is connected to a switch port (such as an Ethernet host adaptor or another switch port), this is referred to as *microsegmentation* and full-duplex operation is possible without the occurrence of collisions. If however, a collision domain is shared on a switch port (multiple host adaptors or repeating hubs connected on a segment), then only half-duplex communication is allowed and use of the interconnection medium must be arbitrated among the nodes (using CSMA/CD). Flow controls are methods used to help arbitrate communication along this medium. For full-duplex segments, the *Pause Scheme* is used. For half-duplex segments, the *back pressure* approach is used.

Full-Duplex Flow Control

Full-duplex flow control is enabled by default, but may be disabled via DIP switch S1-2. Per IEEE 802.3x, flow control refers to the use and handling of pause frames to address short term traffic overload on a full-duplex link, for both the transmit and receive channels.

On a receive channel, if a pause control frame is received, the switch will not transmit the next normal frame until the timer (specified in the pause control frame) expires. If another pause frame is received before the original time expires, the timer will be updated with the new time value in the second received pause frame. During the flow control period (timer running), only flow control packets may be transmitted.

On a transmit channel, the switch determines when to invoke flow control based on the availability of switch resources, considering available buffer space, the transmit queues, and the receive queues.

The 900EN-S005 will apply flow control on any port which just received a packet if the destination port resources are being used fully. The switch will also flow control all ports if its receive queue becomes full. A flow control frame (XOFF) will be issued which contains the maximum pause time defined by IEEE 802.3x. Once its required resource is freed up, it will send out the opposite flow control frame (XON) with a zero pause time to turn off the flow control (and thereby turn on transmission to the port). Additionally, hysteresis is employed to prevent the flow control mechanism from being activated and deactivated too many times.

Half-Duplex Flow Control (Half-Duplex Back Pressure)

This module also provides another form of flow control for half-duplex links that is not part of the IEEE 802.3x standard and is called *half-duplex back pressure*. Half-duplex back pressure ensures retransmission of incoming packets if a half-duplex switch port is unable to receive incoming packets.

Recall that for half-duplex, traffic flows in one direction at a time on the network and CSMA/CD arbitration is used. During periods of heavy congestion, a port may apply half-duplex back pressure to help unburden resources. Half-duplex back pressure will use the same conditions as stated for full-duplex flow control to activate or deactivate.

There are two back pressure modes that may be employed for half-duplex—collision-based and carrier-sense.

If the collision-based back pressure mode is enabled and no buffer space is available to the port, the switch will send collision frames across the affected port and cause the transmitting station to resend the packets. The switch can then use this retransmission time to clear its receive buffer by sending packets already in its queue.

For carrier-sense (the method used in 900EN-S005), if back pressure is required, the switch will send preambles to defer transmission by other stations (this is called *carrier sense deference*). After a certain amount of time, the switch will discontinue the carrier sense, then raise the carrier sense quickly, in order to avoid jabber and excessive deference as defined by the IEEE 802.3 standard. The resultant short silent time where no carrier sense is used is done to prevent other stations from sending out packets and will serve to keep the other stations in a carrier sense deferred state. If a port has packets to send while applying this back pressure, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, the carrier sense type back pressure will be activated again, until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further collisions and maintaining carrier sense to prevent the reception of additional packets.

Traffic Flow Controls

CONTROL REGISTER	FUNCTION
Global Control 1 bit 5	Transmit flow control Disable: Set to disable transmit flow control.
Global Control 1 bit 4	Receive flow control Disable: Set to disable receive flow control.
Global Control 2 bit 5	Back Pressure Mode: Set to select carrier-sense back-pressure. Clear for Collision-based back-pressure.

Traffic Flow Controls

Traffic Flow Controls…continued

CONTROL REGISTER	FUNCTION
Global Control 2 bit 4	Flow Control/Back-Pressure Fair Mode: Set to select Fair Mode, clear for Non-Fair Mode. In Fair mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped to prevent the flow control port from being flow controlled for an extended period of time. In non-fair mode, for the same conditions, the flow control port will be flow controlled and this may not be "fair" to the flow control port.
Port Control 2 bit 4	Force Flow Control (Per Port): Set to always enable receive and transmit flow controls regardless of auto-negotiation. Clear to enable flow control based on the auto-negotiation result.
Port Control 2 bit 3	Half-Duplex Back Pressure Enable: Set to enable half-duplex back pressure. Clear to disable (default).

Broadcast Storm Protection

Broadcast packets are addressed to all nodes on a network and are typically forwarded to all ports except the source (ingress) port. What can happen is that if a broadcast, multicast, or unicast message is transmitted at a port, all other ports can become flooded with this transmission and this will burden switch resources (bandwidth and transmit queue space). Broadcast storm protection is a method used to protect a switch port from receiving too many of these "*broadcast"* packets by discarding broadcast packets if their number exceeds a defined threshold in a preset amount of time. When this time expires, the receiving port resumes forwarding broadcast packets until the rate threshold is reached again.

For the Acromag 900EN-S005, this protection may be enabled or disabled on a per port basis. The protection rate is a 12-bit number representing the number of 64-byte blocks of packet data permissible in 50ms (100baseT), or 500ms (10baseT). The maximum broadcast receiving threshold is unlimited when protection is disabled (default).

Broadcast Storm Protection Controls

CONTROL REGISTER	FUNCTION
Port Control 0 bit 7	Protection Enable (Per Port): Set to enable broadcast storm protection.
Global Control 2 bit 6	Multicast Storm Protection Disable: Set to exclude multicast packets (Dest. Address= FFFFFFFFFFFF) from storm protection.
Global Controls 4 (bits 2-0) & 5 (bits 7-0)	Protection Rate (12-bits): Sets the number of 64-byte blocks of packet data permissible on an input port in 50ms (100baseT), or 500ms (10baseT).

Rate Limiting

Rate limiting is a form of flow control that is used to enforce a strict bandwidth limit which allows you to specify the maximum number of bytes a port can send and/or receive. This switch supports fixed rate limiting independently at its receive and transmit channels on a per port basis. The port will drop bytes that exceed the rate limit you specify, separately for receive and/or transmitted data. Fixed rate limiting applies to all types of traffic on a port, and in priority or non-priority environments.

Programmable rate limiting allows separate transmit and receive rate limits to be set at each port. It may also set different rate limits for high and low priority packets. You specify the maximum number of bytes in bits per second (bps). The rate limiting feature works over one second intervals. The rate limit starts from 0Kbps up to the line rate in multiples of 32Kbps (32768bps). At the beginning of each interval, the internal counter is cleared to 0 and the rate limit function starts to count the number of bytes during this one second interval. If the number of bytes exceeds the programmed limit, the switch will stop receiving packets, and/or stop transmitting packets, at the port until the one second interval expires.

If the rate limit is programmed greater than or equal to 128Kbps, and the byte counter is 8Kbytes below the limit, this flow control will still be triggered. If the rate limit is programmed lower than 128Kbps, and the byte counter is 2Kbytes below the limit, the flow control will also be triggered. If priority is enabled, you can apply different rate controls for both high priority and low priority packets (see Port Control 5-11 Registers 21-27).

Rate Limiting Controls

CONTROL REGISTER	FUNCTION
Port Control 11 bit 0	High Priority Transmit Rate Control Enable: Set to enable. Clear to disable.
Port Control 11 bit 1	Low Priority Transmit Rate Control Enable: Set to enable. Clear to disable.
Port Control 11 bit 2	Transmit Differential Priority Rate Control: Set to perform transmit rate control on both high and low priority packets using high and low priority rate counters. Clear to perform transmit rate control on any packets using low priority rate counter.
Port Control 11 bit 3	High Priority Receive Rate Flow Control Enable: Set to assert flow control if the high priority receive rate is exceeded (differential receive rate control bit 7 must also be set). Clear to not assert flow control if the high priority receive rate is exceeded.
Port Control 11 bit 4	Low Priority Receive Rate Flow Control Enable: Set to assert flow control if the low priority receive rate is exceeded. Clear to not assert flow control if the low priority receive rate is exceeded.
Port Control 11 bit 5	High Priority Receive Rate Control Enable: Set to enable the port high priority receive rate control feature (differential receive rate control bit 7 must also be set). Clear to disable port high priority receive rate control.

Rate Limiting

Rate Limiting Controls…continued

CONTROL REGISTER	FUNCTION
Port Control 11 bit 6	Low Priority Receive Rate Control Enable: Set to enable the port low priority receive rate control. Clear to disable port low priority receive rate control.
Port Control 11 bit 7	Receive Differential Priority Rate Control: Set to enable receive rate control on port for low priority packets at low priority rate (if bit 6 is also set), or to enable receive rate control on high priority packets at high priority rate (if bit 5 is also set). Clear to perform receive rate control using the low priority rate for all packets on this port.
Port Control 5 bits 7-0 and Port Control 7 bits 3-0.	Transmit HIGH Priority Rate Control: A 12-bit number that sets how many "32Kbps" high priority blocks can be transmitted (in a unit of 32K bits or 4K bytes) in a one second period.
Port Control 6 bits 7-0 and Port Control 7 bits 7-4.	Transmit LOW Priority Rate Control: A 12-bit number that sets how many "32Kbps" low priority blocks can be transmitted (in a unit of 32K bits or 4K bytes) in a one second period.
Port Control 8 bits 7-0 and Port Control 10 bits 3-0.	Receive HIGH Priority Rate Control: A 12-bit number that sets how many "32Kbps" high priority blocks can be received (in a unit of 32K bits or 4K bytes) in a one second period.
Port Control 9 bits 7-0 and Port Control 10 bits 7-4.	Receive LOW Priority Rate Control: A 12-bit number that sets how many "32Kbps" low priority blocks can be received (in a unit of 32K bits or 4K bytes) in a one second period.

Priority Controls

The Acromag 900EN-S005 can discern priority via three different means at its input port: on a per-port basis, via the 802.1p frame tag, and by viewing the DSCP (TOS) field in the IPv4 header. Note however, in order for any priority control to be effective, the high and low priority queues must be separately enabled at the input point or destination port.

Priority Using The Per-Port Method

Each port has a general Enable Port Priority bit that when set, specifies that the port has high-priority traffic and all traffic from this switch port is considered high-priority in the destination queue. This is most useful for IP phone applications mixed with other types of traffic data where the IP phone is connected to a specific port. In this case, the IP phone traffic would be high priority (outgoing) to the WAN (Wide Area Network). The incoming phone traffic is all the same priority to the IP phone.

Priority Using The 802.1p Method

Each port has an "Enable Port 802.1p Priority" bit that when set, directs that the 802.1p priority tag (3 bits) be used to determine a received frame's priority. A 3-bit value is defined in bits 6..4 of Global Control 0 register which is used to classify the priority of incoming packets. In this method, the inbound traffic port examines the priority field in the tag, compares it to the 3-bit value, and determines if it is of high or low priority.

Priority Controls

That is, the packet's "user-priority" is compared against this value. If it is greater than or equal to it, the packet is classified as high priority. If it is less than it, it is classified as low priority.

There is also a global Priority Classification register that is used to set the high or low priority status of each 3-bit 802.1p tag field (a set bit specifies high priority for the corresponding tag value). In this method, the inbound traffic port examines the priority field in the tag and determines if it is of high or low priority. This method works best when used with ports that have mixed data and media traffic flow.

Priority Using The IPv4 Diffserv/DSCP Method

Diffserv is another per-frame method of determining outbound traffic priority. The Diffserv method uses the TOS field in the IP header as a Differentiated Services Code Point (DSCP) to determine high and low priority on a per code point basis. Each fully decoded code point can have either high or low priority and a wider spectrum of priority flow can be defined with this larger code space. The most significant 6 bits of the IP header TOS field are fully decoded into 64 possibilities and each resultant singular code is compared against the corresponding bit in the DSCP register. If the register bit is 1, the priority is high, and low if 0. Each port has an enable port DSCP bit that when set, causes the DSCP field of the IP header to determine the high or low priority. There is also a global DSCP Priority Points register (64 bits) that is used to fully decode the priority of the 6 bit DSCP field of the IP header.

When setting up a priority scheme, other controls are also available to regulate traffic, such as: the Priority Scheme bits which control the interleaving of high and low priority frames. This is a global (all ports) transmit buffer high/low interleave control (see register 5 bits 3-2). Options allow high/low ratios of 2:1, 5:1, 10:1, up to delivering all high priority packets first.

Another global priority control is the Priority Buffer Reserve bit that when set, will allocate 48 buffers per output port for high priority traffic only. A separate buffer share bit can also be used to cause all ports to share the available buffer pool and allow any port to use more than its allocated amount (1/5 of available buffer space) when the other ports are not busy.

On an individual port basis, we have the Enable Diffserv/DSCP, Enable 802.1p, and Enable Port-Based Priority bits described above, plus an Enable Port Queue Split that splits the transmit queue of the desired port for high and low priority traffic. Note that default high priority classification is a VLAN tag value greater than 4, and low priority being 3 or less (this applies if the 802.1 global priority classification is clear or not defined).

Priority Controls

Priority Controls *(Also See Priority Controls of Rate Limiting)*

CONTROL REGISTER	FUNCTION
General Priority	
Global Control 2 Bit 0	Priority Buffer Reserve: Set to pre-allocate 48 output buffers to each output queue exclusive to high priority packets (enable this when priority queue feature is enabled).
Global Control 3 Bits 3-2	Transmit Buffer Priority Scheme High/Low Interleave Select: 00=Always deliver high priority packets first; 01=Deliver high/low packets at a ratio of 10/1; 10=Deliver high/low packets at a ratio of 5/1; 11=Deliver high/low packets at a ratio of 2/1.
Port Control 0 Bit 0	Port Split Enable For Priority: Set to split the port transmit queue into separate high and low priority queues. Clear for a single output queue with no priority differentiation.
802.1p Priority	
Port Control 0 Bit 5	802.1p Priority Classification Enable (Per Port): Set to enable 802.1p priority classification for ingress packets. Clear to disable.
Global Control 0 Bits 6-4	802.1p Base Priority Class: This 3-bit value that is used to classify priority of incoming packets by comparing it against the "User-Priority". Packet is high priority if user priority is greater than or equal to this number, and low priority if less than this number.
Port-Based Priority	
Port Control 0 Bit 4	Port-Based Priority Classification Enable: Determines which ports have high priority traffic. Set to classify port ingress packets as high priority if "Diffserv" or "802.1p" are not enabled, or if unit fails to classify. Clear to classify port ingress packets as low priority if "Diffserv" or "802.1p" are not enabled, or if unit fails to classify. Note that "Difserv", "802.1p", and port-based priority can all be enabled at the same time. The or'ed result of 802.1p and Diffserv/DSCP overwrites port-based priority.
Diffserv/DSCP Priority	
Port Control 0 Bit 6	Diffserv/DSCP Priority Classification Enable (Per Port): Set to enable Diffserv/DSCP priority classification for ingress packets. Uses DSCP field in IP header to decide high or low priority. Clear to disable Difserv/DSCP.
TOS Priority Control Registers 96-103	A 64-bit fully decoded DSCP (Differentiated Services Code point) for the IPv4 TOS (Type Of Service) priority control that is used to determine packet priority from the 6-bit TOS field of the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

Virtual LAN Support (Port-Based VLAN)

This model provides support for port-based Virtual Local Area Networks (VLAN). Tag-based VLAN controls require the use of SPI Slave Mode, which is not covered in this manual and is reserved for factory use. Thus, this section will focus on the more common port-based VLAN definitions which can be preprogrammed in EEPROM Mode, then take effect at power-up or following the next reset.

A Virtual LAN (VLAN) is an exclusive broadcast domain or network segment that allows multiple nodes (members) at different physical locations, on different LAN's or segments, to communicate with each other as if they were on a common LAN. VLAN's subdivide a physical network and isolate network segments via logical grouping, as opposed to physical grouping. This is normally done in an effort to constrain overall traffic flow, limiting VLAN messages to only the members that need to share this information. This effectively frees up bandwidth on the network, as broadcast messages may target specific work groups that happen to share the same physical network.

Recall that each switch port forms a different physical network segment or broadcast domain. Port-based VLAN's allow the end stations at different switch ports of the same switch to be included in a "virtual network segment" by grouping together one or more ports of the switch.

For the 900EN, the port membership is predefined when the switch is configured in EEPROM mode, then takes effect following startup. Then packets that the switch receives and identifies as belonging to a port-based VLAN are forwarded only over the ports assigned to that VLAN. However, once the port-based VLAN membership is set, if a VLAN member moves from one port to another, the VLAN membership must be reconfigured as this type of VLAN does not migrate when a cable is changed between ports.

To contrast port-based VLAN controls, a 802.1q tag-based VLAN makes use of VLAN control information stored in the VLAN header of an IEEE 802.3 packet frame. This allows the tag-based VLAN to span beyond the boundary of a single switch, to other segments connected to other switches. On the other hand, the port-based VLAN is defined on the switch itself and does not use information contained in the packet frame to define its membership, thus it is restricted to the ports of the same switch. In this respect, only the switch itself knows a VLAN's architecture, while the segments connected to the switch ports have no way of knowing the VLAN definition even exists. This is the key difference between port and tag based Virtual LAN's.

The following table lists the register controls of the 900EN that are specific to port-based VLAN's only (refer to the Register Map).

Virtual LAN Support (Port-Based VLAN)

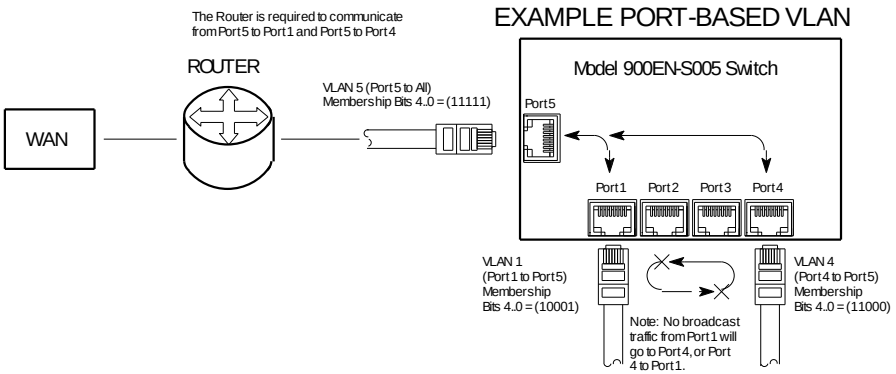
Summary of 900EN-S005 Port-Based VLAN Control Registers

CONTROL REGISTER	FUNCTION
Global Control 3 Bit 7 **802.1Q VLAN Enable**	0=Disable 802.1Q VLAN mode in order to use port-based VLAN definitions. 1=Enable 802.1Q Tag-Based VLAN Mode (the VLAN table must be setup first). *You must disable 802.1Q VLAN mode to use port-based VLAN definitions.*
Global Control 2 Bit 7 **Unicast Port-Based VLAN Mismatch Discard**	Used with port-based VLAN's to restrict or unrestrict the passing of unicast packets. 1=Restrict ALL packet types (including unicast) from crossing VLAN boundary. 0=Permit Unicast packets (excluding unknown/ multicast/broadcast) to cross VLAN boundary. **Note:** Unicast packets are delivered to a single destination node. Multicast packets are delivered to a number of destination nodes. Broadcast packets are delivered to all destination nodes.
Port Control 1 Bits 4-0 **Port VLAN Membership** *Note that any port can only communicate within the VLAN membership if included.*	Use these flags to specify which ports belong to the VLAN at this port. Set to include a port, clear to exclude a port. You must also include this port (the ingress port). The five ports of this switch are applied to bits 4..0 as follows: Bit 4=Port 5, Bit 3=Port 4, Bit 2=Port 3, Bit 1=Port 2, Bit 0=Port 1. The port this control applies to is the input/ ingress port for the VLAN, while the membership defines the other ports as output/egress port(s) of the VLAN.

For the 900EN-S005, a port-based VLAN is setup by programming the Port VLAN Membership bits of the Port Control 1 register in EEPROM. The concept of VLAN "membership" is taken from the perspective of the input/ingress port and which output/egress port(s) it sees directly through the switch. The Port Control 1 register you use corresponds to the ingress port of the VLAN you define (you still have to set its membership bit though), while the other bits define the membership of that VLAN (as output/egress ports). Because the VLAN is defined at the input/ingress port with respect to its output/egress port(s), if you wish to allow two separate ports to talk to each other (both directions), then you must define the egress for both ports separately. Note that a port can only communicate within its VLAN membership and all multicast frames (one sender to a group), and broadcast frames (one sender to everybody on the network) will honor the VLAN configuration and not cross the VLAN boundary. Whether unicast frames also honor the VLAN membership is separately determined via bit 7 of the Global Control 2 register.

Virtual LAN Support (Port-Based VLAN)

For example, if port 1 is to participate in a VLAN with port 5, then bits 0 and 4 of the Port 1 Control 1 Register must be set. If port 4 is to participate in a second VLAN with port 5, then bits 3 and 4 of the Port 4 Control 1 register must be set. Note that port 5 belongs to both VLAN's in this example as an egress port. As such, none of the broadcast traffic at port 1 will go to port 4, and none of the broadcast traffic at port 4 will go to port 1. Further, incoming messages at ports 1 and 4 will be forwarded to port 5 only. However, incoming messages at port 5 will not be forwarded to ports 1 or 4, as port 5 is the egress port for VLAN's at ports 1 and 4. If you wanted port 5 to have two-way communication with ports 1 or 4, then you would have to define a third VLAN at port 5 and set bits 0, 3, and 4 of the Port 5 Control 1 Register.



Unlike the tag-based VLAN definition, in a port-based VLAN the packet forwarding decision is based solely on the destination MAC address and its associated port. Normally, a switch determines the VLAN membership of a data frame it receives by reading a portion of the data frame's tag header and/or examining the configuration of the port that received the transmission. A four-byte field in the header is used to identify a VLAN and this identification indicates what VLAN the frame belongs to. If the frame has no tag header, the switch then checks the VLAN settings of the port on which the packet was received. If the switch port has been configured to support a port-based VLAN, it assigns the port's VLAN identification to the new frame before forwarding it. Optionally, VLAN tags can be added or removed on a per port basis just as with tag-based VLAN's, but the switch doesn't use these tags to make its switching decision as it does with tag-based VLAN's.

SPECIFICATIONS

This device is a DIN-rail mount, five-port, industrial Ethernet switch. It is provided as an accessory for use with Acromag 9xxEN Ethernet I/O modules and may be used to increase effective network bandwidth and help to ensure determinism for industrial control applications. The 900EN-S005 has been designed for wide-ambient operation and is hardened for harsh environments, with protection from RFI, EMI, ESD, EFT, and surges. It also emits low radiation per strict CE requirements. Its plug-in terminal blocks and DIN-Rail mount make mounting, removal, and replacement easy. Port-to-port and port-to-power isolation enhances safety and increases noise immunity. It is CE, UL, and cUL listed, with Class I, Division 2, Groups A, B, C, and D approvals, making it suitable for use in the presence of explosive gases. Units are DC-powered, reverse polarity protected, and include redundant supply support.

Model Number

900EN-S005

The ProfiBus model prefix "900" denotes the Series 900. The "EN" suffix denotes Ethernet. The four digit suffix of this model number represents the following options, respectively: "S" = Switch; "00" = Default; "5" = 5 Ports.

Ethernet Interface

Connector: Five shielded RJ-45 sockets, 8-pin, 10BaseT/100BaseTX.
Wiring: Ports are wired MDI-X and include automatic MDI-X/MDI crossover.
Data Rate: Auto-negotiated, 10Mbps or 100Mbps.
Duplex: Auto-negotiated, Full or Half Duplex.
Compliance: IEEE 802.3, 802.3u, 802.3x.
Port Status Indicators: Three LED's per port – red, yellow, and green. Two indication modes combine speed, link status, activity indication, and duplex indication. The LED indication mode is programmed via DIP switch S2-4, or via bit 1 of EEPROM register 11.
Memory Bandwidth: 1.4Gbps.
Maximum Message Length/Frame Size: 1536 bytes (default), or select 1522 bytes with VLAN and 1518 bytes without VLAN. Also supports huge packets (1916 bytes).
Illegal Frame Detection: Frames less than 64 bytes and more than maximum (see above) are discarded.
Flow Control: IEEE 802.3x flow control on both transmit an receive is enabled (default) and may be optionally disabled.
Half-Duplex Back Pressure (Non IEEE 802.3 standard): Uses carrier sense deference during heavy traffic to unburden resources. Enabled by default and may be optionally disabled.
Half-Duplex Backoff: Binary exponential per IEEE 802.3 (less aggressive default). Optional more aggressive backoff may be enabled.
Address Learning: Automatic, storage of up to 1K (1024) MAC addresses.
Address Aging: Automatic, enabled by default (5 minutes), can be optionally disabled.
Address Migration: Automatic.
Frame Retry w/Collision: Will drop frame after 16 collisions (default operation), or may be optionally disabled for continuous retry.
Late Collision Detection: Transmit packet is dropped if collision occurs after 512 bit times of transmission (may optionally be disabled). Late collisions are usually indicative of illegal cable length.
Register Memory: 512 bytes, Atmel AT24C02 or compatible EEPROM. See EEPROM Register Map for definition.

Ethernet Interface

Frame Buffer: 64K Bytes (16Kx32 Bits) of SRAM shared across all 5 ports for frame storage (providing 512 buffers of 128 Bytes each). Resource is shared among 5 ports, or optionally, allocated one-fifth per port. A single frame can vary from 64 Bytes up to 1536 Bytes. This is effective storage for as little as 42 messages, or as much as 1024 messages.

Communication Distance: The distance between two devices on an Ethernet network is generally limited to 100 meters using recommended copper cable. Distances may be extended using hubs, switches, or fiber optic transmission. However, the total round trip delay time must not exceed 512 bit times for collision detection to work properly.

Broadcast Storm Protection: Disabled (default), but may optionally select a maximum receive threshold for multicast/broadcast messages. Broadcast packets are discarded if they exceed the configured threshold within a preset amount of time (refer to Advanced Operation for more detailed information).

Priority: Transmit all high priority before any low priority (default) with a variable high:low interleave (optional). Optionally select DiffServ, 802.1p, and port-based priority controls (refer to Advanced Operation for more detailed information).

Virtual LAN: Supports port-based Virtual LAN definitions using EEPROM Mode (refer to Advanced Operation for more detailed information).

Broadcast storm protection, priority selection, and Virtual LAN definitions require configuration software and an optional cable (Model 5035-365) in order to program.

Program Interface – DIP Switches

This is the default mode of operation. A bank of 8 DIP switches (S1) and 4 DIP switches (S2) allows some operating parameters of this device to be modified and optional modes of operation selected. These switches are located in the top opening adjacent to the power terminals and reset button. DIP switch S2-1 must be OFF to enable use of DIP switches S2-4 and S1-1..8. In this mode, DIP switch settings are combined with the defaults noted for the operating parameters not directly covered by a DIP switch (see Register Map). Refer to Basic Operation for more information on using the DIP switches to configure operation.

Program Interface – EEPROM/I^{2}C

This I^{2}C interface provides direct read/write access to switch configuration registers in EEPROM memory on board for more extensive control of available features and options than the DIP switches alone. Access to this interface is provided via socket P1, which is nested in the opening with the DIP switches. Use this interface to set up the switch prior to installation. An optional program cable is required to connect this module to the host PC parallel port (Acromag cable Model 5035-365). Refer to the EEPROM Mode section of this manual for more information on available features.

Connector (P1): This buffered combination I^{2}C/SPI interface uses the same connector and cable as for SPI access (Acromag Cable Model 5035-365). DIP switch S2-3 must be OFF and switch S2-2 ON to provide EEPROM access. DIP switch S2-1 must be ON to cause the module to use the EEPROM settings (as opposed to the other DIP switches) upon power-up or after a reset.

EEPROM: Atmel AT24C02 or equivalent, 2K (256x8bits) serial EEPROM. Refer to EEPROM Mode of Advanced Operation for information on programming.

Signals (P1 Program Interface): Socket P1 combines I^{2}C, SPI, and ground signals for EEPROM programming, or optional run-time operation in SPI Slave Mode. The following signals are supported:

Program Interface – EEPROM/I²C

P1 Program Interface

P1 PIN	SIGNAL	DESCRIPTION
1	GND	Logic Ground (logic ground is internally coupled to earth ground at TB3-4 via a 100Ω resistor).
2	XSPIQ	Buffered SPI serial data output in SPI Mode (not used in I²C EEPROM mode). This output connects to parallel port connector DB25 pin 10.
3	*NA*	*Keyed Polarity Pin (optional buffered Reset(L) trigger input with key removed).*
4	XSDA	Buffered serial data input in SPI slave mode, or serial data output in I²C EEPROM mode. SDA connects to parallel port connector DB25 pin 9.
5	XSCL	Buffered I²C Clock Line. Input clock up to 5MHz in SPI Slave Mode. Output clock at 81KHz in I²C EEPROM master mode. SCL connects to parallel port connector DB25 pin 16.
6	XSPIS	Buffered SPI Slave Select (active-low). A high-to-low transition initiates the SPI start of data transfer in SPI slave mode. When high, the switch ASIC is deselected and SPIQ is held in a high impedance state. SPIS buffer input ties to parallel port connector DB25 pin 1.

Program Interface – SPI Slave Mode

This mode of operation requires that a host PC be connected to the module during runtime (not recommended). This mode provides access to all registers, plus all static MAC entries, the VLAN table, dynamic MAC address table, and the MIB counters. Use of the SPI interface in SPI Slave Mode is reserved for factory use only and is not covered in this manual.

Note: This mode is provided for experimentation and troubleshooting purposes and is reserved for factory use only. Acromag makes no guaranty of operation in this mode.

Connector (P1): This buffered combination I²C/SPI interface uses the same connector as for EEPROM access. DIP switch S2-1 and S2-3 must be ON, and switch S2-2 OFF to utilize the SPI mode.

Signals (P1 Program Interface): Socket P1 combines I²C, SPI, and ground signals for EEPROM programming, or optional run-time operation in SPI Slave Mode. Refer to the signal table above for EEPROM/I²C interface signal descriptions.

SPI Bus Speed: Up to 5MHz. A high speed SPI master is recommended to prevent internal counter overflow. **NOTE:** A high rate of read errors in SPI mode is commonly caused by weak parallel port signals and poor cabling. Interface cable 5035-565 is not sufficient for reliable operation in SPI Mode and Acromag makes no guaranty of operation in this mode.

Enclosure and Physical

Dimensions: 1.97 inches wide, 4.15 inches tall, 4.55 inches deep. Refer to the dimensions drawing at the front of this manual.

DIN Rail Mount: Type EN50022; "T" rail (35mm).

I/O Connectors: Removable plug-in type terminal blocks rated for 15A/300V; AWG #12-24 stranded or solid copper wire.

Network Connector: 8-pin RJ-45 connector socket with metal shield. Note that shield is bypassed to earth ground at the ground (G) terminal via an isolation capacitor (1000pF) and transient voltage suppressor. The shield is also isolated from the RJ-45 pin circuits.

RJ45 Pin	Signal	Description (MDI-X)
1	Tx+	Transmit Positive
2	Tx-	Transmit Negative
3	Rx+	Receive Positive
4	Not Used	Connects to Pin 5
5	Not Used	Connects to Pin 4
6	Rx-	Receive Negative
7	Not Used	Connects to Pin 8
8	Not Used	Connects to Pin 7

Enclosure and Physical

Case Material: Fiber-reinforced polycarbonate PC-F thermoplastic, UL94 V0 inflammability class, black color; general purpose NEMA Type 1 enclosure.
Printed Circuit Boards: Military grade FR-4 epoxy glass.
Shipping Weight: 1 pound (0.45 Kg) packed.

Agency Approvals

Safety Approvals: : UL Listed (USA & Canada). Hazardous Locations- Class I, Division 2, Groups A, B, C, D. Consult factory.
ATEX Certified: Assessment by TUV Rheinland of North of America, Inc. per
ATEX Directive 94/9/EC.
Ex II 3 G
Ex nA T4-25°C< Ta < +70°C
TUVNA 07 ATEX 7145X
X= Special Conditions
1) "WARNING-EXPLOSION HAZARD-DO NOT MAKE OR BREAKCONNECTIONS IN HAZARDOUS LOCATIONS OR AREAS"
2) "Warning: Must be installed in suitable enclosure with an Ingress Protection of IP54 minimum, in Hazardous Locations or Areas"

Environmental

Operating Temperature: -25°C to +70°C (-13°F to +158°F).
Storage Temperature: -40°C to +85°C (-40°F to +185°F).
Relative Humidity: 5 to 95%, non-condensing.
Power Requirements: Non-polarized 15-36V DC SELV (Safety Extra Low Voltage), 2.6W. Observe proper polarity. See table for current. Current shown assumes 25°C and all ports are connected.

Supply	900EN-S005 Current Draw
12V	195mA Typical, 215mA Maximum
15V	149mA Typical, 164mA Maximum
18V	122mA Typical, 134mA Maximum
24V	92mA Typical, 101mA Maximum

CAUTION: *Do not exceed 36VDC peak, to avoid damage to the module.*

External Fuse: *Select a high surge tolerant fuse rated for 1A or less to protect unit.*

36V	65mA Typical, 72mA Maximum

Isolation: Power and network circuits are isolated from each other for common-mode voltages up to 250VAC, or 354V DC off DC power ground, on a continuous basis (will withstand 1500VAC dielectric strength test for one minute without breakdown). Complies with test requirements of ANSI/ISA-82.01-1988 for voltage rating specified.

Installation Category: Designed to operate in an Installation in a Pollution Degree 2 environment with an installation category (over-voltage category) II rating.

Electromagnetic Interference Immunity (EMI): Product has demonstrated resistance to digital upset (state change) with interference from switching solenoids, commutator motors, and drill motors.

Environmental

Electromagnetic Compatibility (EMC) -

Immunity Per European Norm BS EN 61000-6-2:2005:

Electrostatic Discharge (ESD) Immunity: 4KV direct contact and 8KV air-discharge to the enclosure port per IEC61000-4-2.

Radiated Field Immunity (RFI): 10V/M, 80 to 1000MHz AM, 1.4 to 2GHz 3V/M, and 2 to 2.7GHz 1V/M, per IEC61000-4-3.

Electrical Fast Transient Immunity (EFT): 2KV to power, and 1KV to signal I/O per IEC61000-4-4.

Conducted RF Immunity (CRFI): 10Vrms, 150KHz to 80MHz, per IEC61000-4-6.

Surge Immunity: 0.5KV per IEC61000-4-5.

Emissions Per European Norm BS EN 61000-6-4:2007

Radiated Frequency Emissions: 30 to 1000MHz per CISPR16 Class A

EMC – CE Marked

Electromagnetic Compatibility (EMC): CE marked, per EMC Directive 2004/108/EC. Consult factory.

Immunity per BS EN 61000-6-2:

1) Electrostatic Discharge Immunity (ESD), per IEC 61000-4-2.
2) Radiated Field Immunity (RFI), per IEC 61000-4-3.
3) Electrical Fast Transient Immunity (EFT), per IEC 61000-4-4.
4) Surge Immunity, per IEC 61000-4-5.
5) Conducted RF Immunity (CRFI), per IEC 61000-4-6.

Emissions per BS EN 61000-6-4:

1) Enclosure Port, per CISPR 16.
2) Low Voltage AC Mains Port, Per CISPR 16.
3) Telecom / Network Port, per CISPR 22.

WARNING: This is a Class A product. In a domestic environment, this product may cause radio interference in which the user may be required to take adequate measures.

Controls & Indicators

Power Indicator: Green LED ON indicates power (internal +3.3V rail OK).

Port Status Indicators: Three LED's per port – red, yellow, and green. Two indication modes combine speed, link status, activity indication, and duplex indication. The LED indication mode is programmed via DIP switch S2-4, or via bit 1 of EEPROM register 11.

Mode	LED 1 (Red)	LED 2 (Yellow)	LED 3 (Green)
0 (Default)	Speed (On= 100M, Off= 10Mbps)	Full-Duplex+Coll (Constant ON= FDX, Intermittent ON= Collision, Constant	Link + Activity (ON)

		OFF=Half+No Coll)	
1	Full Duplex (ON= FDX, OFF=HDX)	Link Activity (10Mbps Only)	Link Activity (100Mbps Only)

Controls:

Reset Switch: This momentary push-button is located adjacent to the power terminals and is used to reset the module and facilitate in-field reconfiguration via the DIP switches. Push this button after making changes to DIP switch settings in order to excecute the changes.

DIP Switches: A 12-position DIP switch is located in the top opening next to the power terminals and reset button and is used to select alternate modes of operation. Refer to Basic Operation for more information.

ACCESSORY CABLES

The minimum cable required for full operation of this device is Category 5. The term "Category" refers to classifications of UTP (Unshielded Twisted Pair) and STP (Shielded Twisted Pair) cables. There are 3 main categories of cable – Category 3, Category 4, and Category 5. The differences in classification is found in their electrical performance and this is documented in the TIA/EIA 568-A standard.

This device is designed for use in harsh industrial environments. Acromag recommends the use of shielded cable when wiring to this device. Select STP (Shielded Twisted Pair) cable rather than UTP (Unshielded Twisted Pair). The use of shielded cable will help protect the data being transmitted from harmful EMI (Electromagnetic Interference) and RFI (Radio Frequency Interference). It will also help to lower your radiated emissions by keeping the cable from emitting EMI and RFI.

TIP: *In our own tests for radiated emissions, the use of STP/shielded cable instead of UTP/unshielded cable lowered emissions by as much as 7dB.*

There are two types of cable conductors: solid cable and stranded cable. Stranded cables are more flexible than solid cables. But since attenuation is higher for stranded cables than solid conductor cables, these are generally reserved for short runs and patch applications less than 6 meters.

Currently there are two types of shielding employed in Category 5 STP cable: single-shielded and double-shielded. Both of these cables have the same core and jacket as UTP cables, but also include a thin foil outer shield that covers all four twisted-wire pairs. Variations may include a drain wire that encircles the outer jacket. A double-shielded version adds an outer wire screen that surrounds the foil shield and also functions as a drain wire. The drain wire or wire screen typically makes contact at each end of the cable with the metal shield around special RJ45 plug connectors. This shield then makes contact with the metal shield of shielded RJ45 sockets. The socket shield may make direct contact with earth ground, or it may be capacitively coupled to earth ground. In the Acromag 9xxEN modules, it makes contact with earth ground via a high voltage capacitor and transient voltage suppressor. In addition to separately isolating the shield, this helps to minimize radio frequency and electromagnetic interference, and has the added benefit of protection from ESD (Electro-Static Discharge).

Further, Acromag recommends the use of *enhanced* Category 5 cable (CAT-5e). Category 5e cable has a greater number of turns-per-inch in its twisted pairs and its performance is also more suitable for applications that make use of all four wire pairs for simultaneous bidirectional data transmission (full-duplex). Acromag offers the following cable accessories:

Patch Cable & Crossover Cable

Cable Model 5035-355 – A yellow, 3 foot long, single-shielded Category 5e STP patch cable with an RJ45 plug at both ends.
Cable Model 5035-360 – A green, 5 foot long, single-shielded Category 5e STP crossover cable with an RJ45 plug at both ends. This cable performs the Ethernet crossover function and is used to connect a PC directly to an Acromag Series 9xxEN I/O module.

You may obtain cable in other lengths and colors as required for your application from other vendors. For example, shielded CAT-5e cable is available from the following vendors:

- L-com Connectivity Products, www.L-com.com
- Pro-Link, www.prolink-cables.com

Patch Cable & Crossover Cable

For very noisy environments or in the presence of strong electrical fields, you can obtain double-shielded CAT-5e cable and shielded RJ45 plugs from the following vendors:

- L-com Connectivity Products, www.L-com.com, see cable model TFSC2004 and shielded plug T8P8CSR.
- Regal Electronics, www.regalusa.com, see shielded plug model 1003B-8P8CSR-C5.

Complete premium double-shielded Category 5e standard and crossover cables in variable lengths can be obtained from Lumberg at www.lumbergusa.com (refer to their etherMate line). For example, specify RJ45S-RJ45S-656/B/3M for a double-shielded, 3 meter straight cable. Specify RJ45S-RJ45S-656/BX/3M for a double-shielded, 3 meter crossover cable.

Programming Cable 5035-365

This module has many advanced programmable features. If you wish to take advantage of these features, you will need to purchase the following programming cable from Acromag:

Cable Model 5035-365 – A 4 foot long, 6-wire IDC cable with a 6-pin header at one end (2 rows of 3 pins with pin 3 removed) and a DB25M connector at the other end. This cable is used to connect between the parallel port of a personal computer and the program port of the 900EN-S005. Use this cable to write to EEPROM of the switch (EEPROM Mode), or to access the runtime registers of the switch in SPI Slave Mode. Additional software is required to use this cable and is located on the CDROM shipped with your unit. A diagram of this cable and interface is provided below.

Note: The 5035-365 cable and its associated Advanced Features 8500-725 users manual have been discontinued.

If you need to service this cable, or you wish to build your own cable, you can obtain the necessary parts from other vendors. For the 6-wire IDC cable and header assembly, see Samtec part number HCMD-03-S-50.00-02 (www.samtec.com). The DB25M IDC connector is a common part that can be obtained from many vendors including 3M (www.3M.com), and Kycon (www.kycon.com).