AN1983
APPLICATION NOTE

Recommendations For OCE-Lite Based Debug in Super10 Applications

1 - INTRODUCTION

The purpose of this note is to give indications on how to design Super10 based applications, to ease OCE-Lite debugging task.

The intended audiences of this note are SOC designers, hardware application designers, hardware/ software development engineers and all peoples involved in the development of an application based on embedded Super10 System-On-Chip (SOC).

The Super10 is an enhanced ST10 microcontroller core optimized for real-time performance and System-On-Chip applications, from STMicroelectronics. This third generation of 16-bit microcontroller core provides high bandwidth system throughput and full DSP instructions that have been optimized for real-time applications.

1.1 - Additional Documentation

[1] Instruction set is covered in the Super10 Instruction Set Reference Guide.

[2] Memory organization, registers description and core features are explained in the Super10 User's Manual.

[3] Basic peripherals are detailed in the Super10 Standard Peripherals User's Manual.

[4] The embedded Super10 IP is described in the Super10 Megacell M3XX Specification.

[5] All electrical timing specifications and the product pin out can be found in the datasheet of your specific product with embedded Super10.

[6] Application Note AN1981, “Recommendations for Real-time Debugging Using Bondout Chip in Super10 Applications” from STMicroelectronics.

[7] Application Note AN912/1098, “A simple guide to development tools” from STMicroelectronics.

[8] The Nexus 5001™ Forum Standard for a Global Embedded Processor Debug Interface, "IEEE-ISTO-5001™-1999".

[9] The IEEE Standard Test Access Port and Boundary-Scan Architecture, “IEEE Std 1149.1-1990”.

[10] Super10 OCE-Lite datasheet.

[11] Application Note AN1982, “From ST10 to Super10” from STMicroelectronics.

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2 - EMULATION AND DEVELOPMENT TOOLS

Emulation and Development Tools are available from several third party vendors, and three debug solutions are proposed for the embedded Super10 SOC :

– Bondout chip based emulation (Refer to [6]).

– Embedded OCE-Lite based debug.

– Embedded “Nexus“ OCE based debug. (Refer to [8]).

These solutions allow different levels of debug and visibility and this note covers OCE-Lite debugger only.

Historically the Bondout chip emulators were the first in place and even if this kind of tools have no equivalent for real time debug, they also have limitations:

– High number of pins required for emulation on the customer SOC.

– Possible core discrepancy between bondout and customer SOC.

– Potential high frequency limit.

– Issue with addition of “on-chip” peripheral into more integrated customer SOC.

This has pushed STMicroelectronics to define a new tool generation, consisting in “on chip” embedded OCE based.

Main benefits of embedded cell for emulation are :

– Very few emulation hardware constraints on the target application board.

– Limited emulation hardware constraints at the SOC level.

– Use of customer SOC during debug, meaning also the real silicon debug.

– Possible debug after application crash down.

For more information please refer to [7].

2.1 - OCE-Lite Presentation

2.1.1 - Benefits

– Embedded on the device.

– Extremely small silicon area, meaning lower cost.

– Requires only an advanced IEEE1149.1’ connector (5 JTAG pins + Reset signal) on the target application board.

– Non intrusive considering the Super10 CPU activity.

– No SOC resources reserved by the debugger.

– A debug session can start on the fly, even after a crash down of an application.

– Independent of the “on-chip” peripheral integration.

– Independent of the CPU frequency.

2.1.2 - Specific Features (Refer to [10])

– Nexus class 1 compliance (Refer to [8]).

– Optional Nexus features such as memory access (read-write access to the complete Super10 address space either in debug mode or on the fly).

– Debug mode (break) entered upon debugger request or watchpoint trigger.

– Programmable debug level versus interrupt level.

– Software breakpoint.

– Stepping while in debug mode.

– "break-before-make" capability on Instruction Pointer watchpoints.

– Two watchpoint units, each of them consisting of:
  - Two instruction pointer compare units with range combination capability
  - Two data compare units including data address, value and access type parameters
  - 16 bit event counter
  - Independent Instruction Pointer compare units and data compare units.
  - Watchpoints can be cascaded to build complex trigger conditions
– One event input and event output.
– On the fly debugger accesses to memory and registers.
– Code downloading capability, controlled by the debugger software on the emulator host.

2.1.3 - Limitations

– No trace visibility.
– No profiling capability.

2.2 - Debugger Features

OCE-Lite debuggers are principally composed of a hardware and a software module. The main task of the hardware is mostly to bridge between the host machine interface and the embedded OCE-Lite JTAG port.

Concerning the debugger software on the debugger host, it is up to the debugger manufacturer to implement all OCE-Lite features in order to provide debugger users as much as possible with high class and comfortable debugging.

Refer to your OCE-Lite debugger User's Manual to know exactly the available features of your debugger.

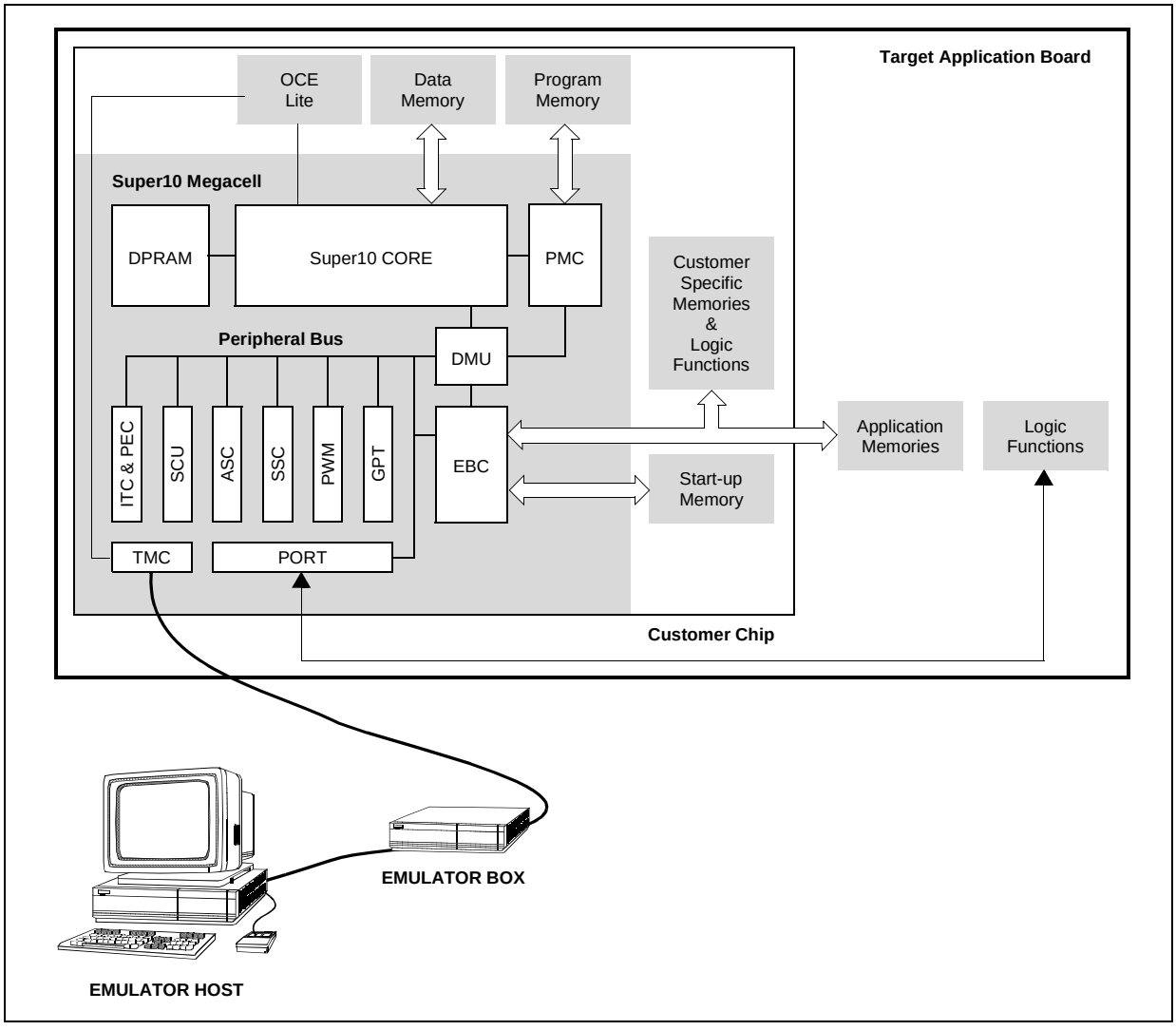
2.3 - OCE-Lite Based Debugger and Tool Chain Description

When an OCE-Lite debugger is connected to a target application board, the building of the hardware chain is detailed in the figure below.

The basic principle of the embedded debugger is based on the use of the customer chip itself during the debug session, meaning that:

– The execution of the application code is fully controlled by the debugger software (thank to OCE-Lite break features, watchpoint features, etc...).
– Code or data downloading is possible if "on-chip" RAM memory (or on target application board) is available.

Figure 1 : OCE-Lite Debugger Tool Chain



2.3.1 - Debug Mode

There is no particular setting to switch to debug mode. Simply connecting the debugger on the target application board will allow the debugger software (running the debugger host) to enable the OCE-Lite, and then to control the core activities (breaking, stepping, reading or writing memories, etc…)

Even if the customer chip has started in standalone mode, or even if the customer chip has crashed (post mortem (1) analysis process) the debugger software is always able to be connected and to extract information from the Super10 Megacell.

Note: 1. A post mortem analysis is necessary when the application behavior is no more controlled by the embedded Super10 Megacell SOC. For an undetermined reason, the execution of the application code is stopped and usually the application is considered as crashed. Connecting an OCE-Lite debugger at this stage will allow development engineers to recover registers values, variables values, Super10 CPU system flags etc…, allowing them to determine the reason(s) of the crash.

3 - EMULATION CONSTRAINT ON SOC DESIGN

Please refer to [4] for OCE-Lite integration in a SOC.

3.1 - Debug Link Pin Count

The main constraint that customer will have to face at the SOC design stage is the number of pin allowed to the debug link.

It is the customer responsibility to decide if optional debug signals (concerning advanced debug features) can be removed from his SOC pinning .

Nexus class 1 compliance, requires to OCE-Lite embedded block to provide the following signals :

– Five JTAG signals which are TDI, TDO, TCK ,TMS and TRST_n

– Chip RESET input

So 6 pins is the minimum required number of SOC pins for OCE-Lite debug.

For enhanced OCE-Lite debug features the following signals can be added:

– RDY_n

– EVTI_n and EVTO_n

– CLOCKOUT

So 10 pins is the maximum possible number of SOC pins for OCE-Lite debug.

4 - EMULATION CONSTRAINT ON TARGET APPLICATION BOARD DESGIGN

Following the overview of the precautions in designing the SOC at customer's chip level, this chapter summarizes the recommendations concerning the design of the target application board.

4.1 - Debugger Connection & Adapter Board

Concerning the connection of his OCE-Lite debugger to the target application board the customer has several choices:

– Applications without strong dimensional limitation:
  - Place directly an OCE-Lite (Nexus class 1 compliance) connector on his target application board.

– Applications with strong dimensional limitation:
  - Place very high density and size adapted connector(s) on the target application board, in order to carry OCE-Lite debugger signals. Then an adapter board design will allow to connect to an OCE-Lite debugger.

    This adapter board is of course a good opportunity to route back to a logic analyzer others signals, in order to ease the debug stage.

4.2 - Nexus Class 1 Compliant Connector

4.2.1 - Signals Description

The table below describes shortly each signal required in the Nexus 5001 Forum™ Standard for class 1 compliance. For complete description, refer to [8].

Group	Name	Brief Description (Target Application Board Side)
Mandatory pins at SOC level	TDI	Test (Access Port) Data In, this serial input is used by the SOC to receive data from the OCE-Lite debugger.
	TDO	Test (Access Port) Data Out, this serial output is used by the SOC to transmit data to the OCE-Lite debugger.
	TCK	Test (Access Port) Clock (33 MHz max according to [8]), this input line is the SOC 's TAP controller clock.
	TMS	Test (Access Port) Mode select, this input line is used by the SOC 's TAP controller to work.
	TRST_n	Test (Access Port) Reset, this input line is concerning : – SOC 's TAP controller reset. – SOC 's OCE-Lite reset.
	RESET_n	This input line is used by the OCE-Lite debugger to reset the SOC on the target application board. Note : no particular caution if the SOC's reset pin is a bidirectionnal pin. The Nexus 5001 Forum™ Standard advise tools vendors to implement (on the tool side) an open drain output. In such a case a tool is able to detect that the application is under reset.

Group	Name	Brief Description (Target Application Board Side)
NOT mandatory pins at SOC level. * Refer to comment below the table	RDY_n	Ready pin: this output line is used by the SOC for flow control and tell the OCE-Lite debugger that the action requested has been executed (in order to speed up data transfer).
	EVTI_n	Event IN: this input line is used by the SOC to break on an external event.
	EVTO_n	Event Out : this output line is used by the SOC for breakpoint occurrence indication.
	CLOCKOUT	This is the system clock from the customer SOC.
Mandatory pin at Application board level	VREF	This signal is used to establish the signaling level of the debug interface of the application. VREF is necessarily at the customer SOC VDD-IO level.
	Ground	
NOT mandatory pin at Application board level	I/O Vendor defined	Unused by Super10 OCE-Lite. Referring to [8], this pin is reserved to MCU/MPU manufacturer, for proprietary feature of the debug link. Tool vendors should design their tools such that they are able to work with this signal (than can be configured as an input or output depending on the MCU/MPU targeted).

** Comment concerning the NOT mandatory pins at SOC level. RDY_n, and CLOCKOUT need carefulness, because they can be involved into the debugger operating mode so that their removal could be a problem with debugger requiring them to operate. Then to avoid non-working situation it is fundamental to verify with the Development Tool vendor, what are the mandatory signal for it' s OCE-Lite debugger to work.*

4.2.2 - Connector Pinning & Type

OCE-Lite connector is conform to the “Connector A” described in "IEEE-ISTO-5001T-1999" ([8]), and is consisting of the following pin arrangement.

Signal-Name	I/O	Pin	Pin	I/O	Signal-Name
RESET_n	IN	1	2	—	VREF
EVTI_n	IN	3	4	—	GND
TRST_n	IN	5	6	—	GND
TMS	IN	7	8	—	GND
TDI	IN	9	10	—	GND
TCK	IN	11	12	—	GND
TDO	OUT	13	14	—	GND
CLOCKOUT	OUT	15	16	—	GND
EVTO_n	OUT	17	18	—	GND
RDY_n	OUT	19	20	—	Unused by Super10 OCE_Lite

Mechanically the standard is as well defining the "Connector A".

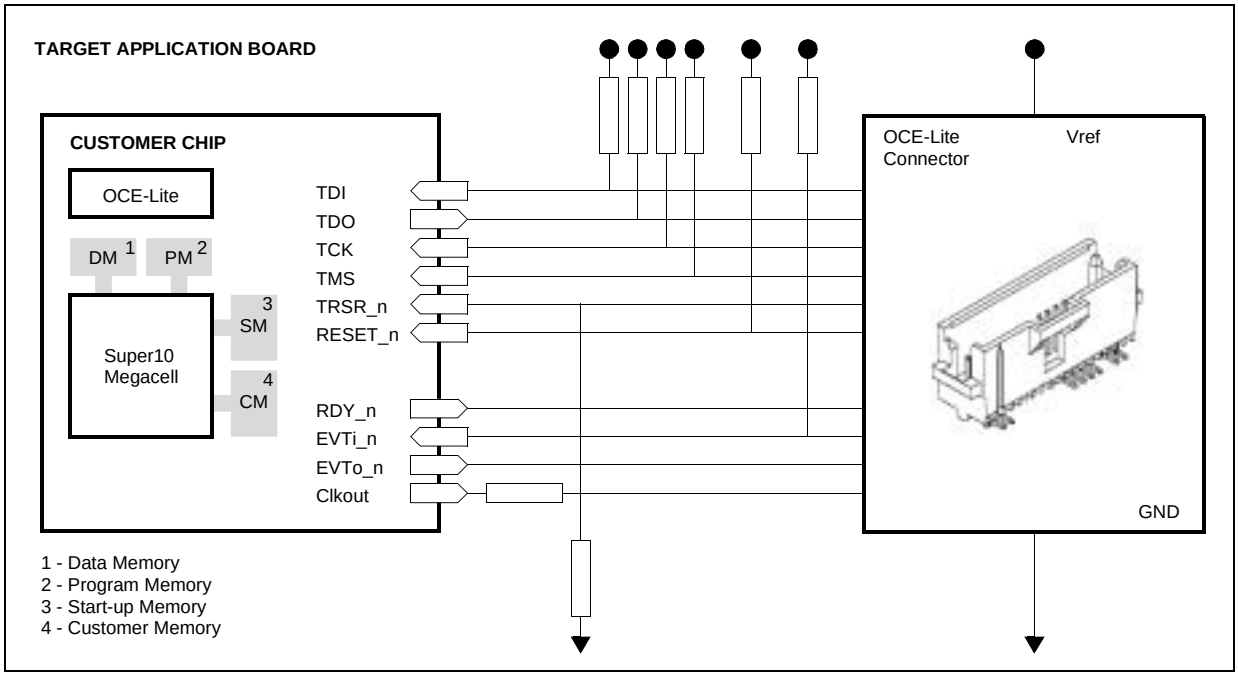
On the application side, the AMP, System 50, 20-pin, board mounted connector is recommended. The part number (P/N) is 104549-2. This is a vertical, surface mount type header with a shroud and two mounting holes.

For compatible connectors use, the constraint is that this must mate with the recommended connector on the debugger side that is the AMP Ribbon Cable Connector System (P/N 111196-4).

4.3 - Implementation Considerations

In a standard manner on the target application board, take caution to pull up (10KΩ resistor) all the “active low” inputs signals (EVTI_n, RESET_n) and IEEE 1149.1 signals (TDI, TDO, TMS and TCK). Concerning TRST_n signal, pull down resistor (10KΩ) will insure continuous OCE-Lite reset when the debugger is not connected.

Figure 2 : OCE-Lite Debug Detailed Implementation



4.4 - High Speed Signal

A very particular attention must be taken if the optional signal CLOCKOUT is routed back to the debugger.

Due to the Super10 Megacell high working frequency capability (>100MHz), CLOCKOUT signal use around or over 100MHz should be avoided as much as possible to avoid EMI & RFI generation. If for lower frequencies this signal could be accepted, it is important to place on this signal a tiny zero ohm SMD resistor (as close as possible to the customer SOC pin) to permit the microstrip cut in high frequency.

At the target application board layout stage apply the following guidelines on CLOCKOUT signal :

– Trace length reduced as much as possible.

– Layers to layers paths reduced as much as possible (multi layers PCB).

– Using ground shield all around the trace.

– Using ground filled layers.

– Using matched controlled impedance connectors if possible.

5 - GLOSSARY

Name	Meaning
CPU	Central Processing Unit
DSP	Digital Signal Processing
EMI & RFI	ElectroMagnetic Interferences & Radio Frequency Interferences
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Join Test Action Group
MHz	Mega-Hertz
OCE	On Chip Emulation
PCB	Printed Circuit Board
RAM	Random Access Memory
ROM	Read Only Memory
TAP	Test Access Port
SMD	Surface Mount Device
SOC	System On Chip
VDD-IO	Typical I/O supply voltage (to differentiate from Typical Core supply voltage)

5.1 - Definitions

In this application note:

– An application is an electronic system using an embedded Super10 System-On-Chip, and running the Super10 software to be debug.

– A target application board is PCB embedding a Super10 System-On-Chip.

Table 1. Revision History

Date	Revision	Description of Changes
June 2004	1	First Issue

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