TMC304(TEG3) User's Manual

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(Chip designed in 1994)

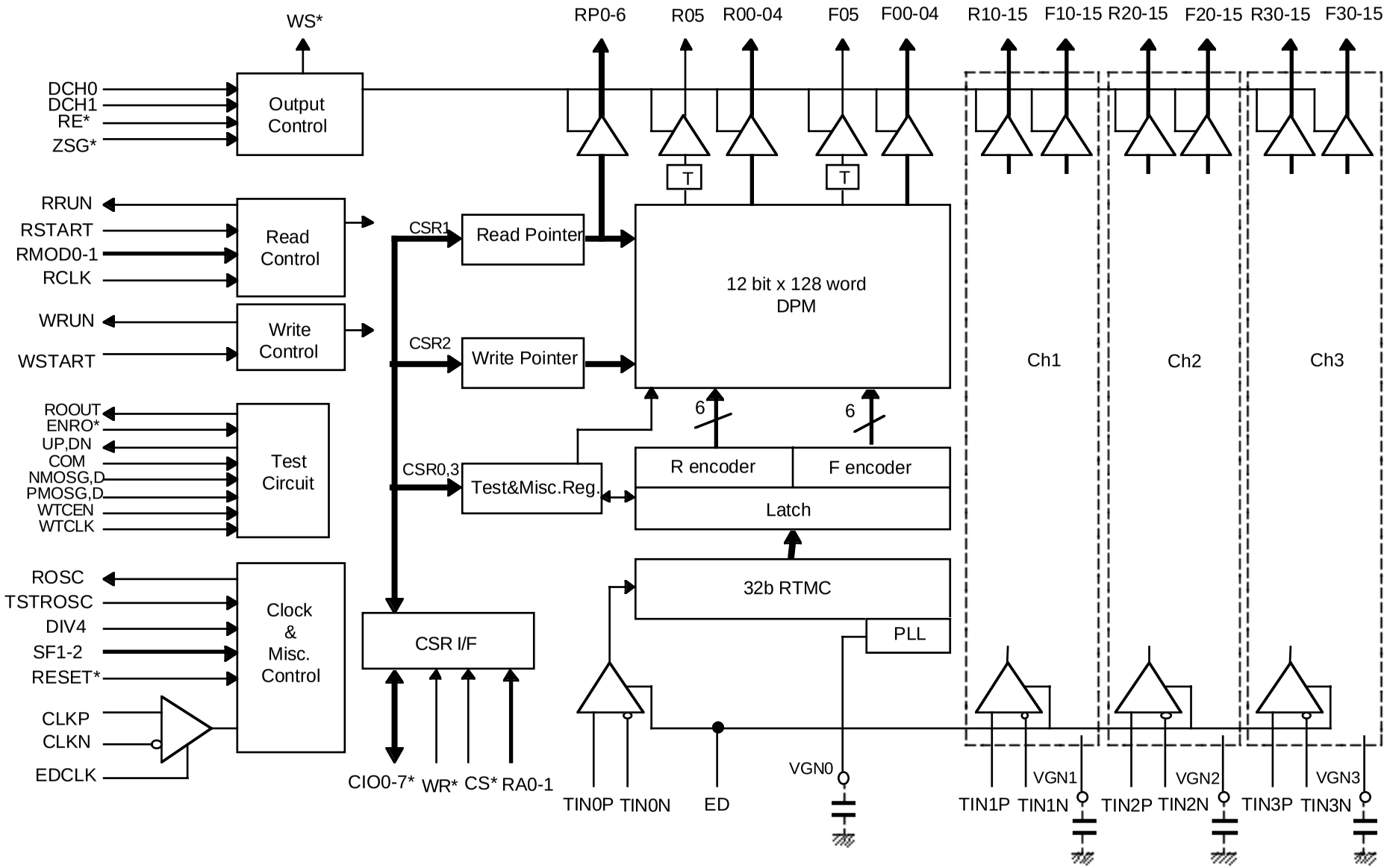
TMC304 (previous name TMCTEG3) is a low-power and high-resolution multi-hit Time to Digital Converter chip. Input signals are digitized at TMC (Time Memory Cell) circuits in (clock period)/32 (0.78 ns @40MHz) time bin. The 32 bits of digitized data is then encoded into a hit bit and 5-bit data, and stored in memories. The memory is dual port memory so write and read can be performed at the same time and there is no dead time for data conversion. There are 128 words of dual port memories, and the chip can store 2.56 μs to 12.8 μs data depend on the system clock frequency.

If user wants to suppress zero data at the output, signal correspond to the hit tag bit can be used as a strobe signal to next level buffer.

To stabilize the internal delay element, PLL circuit is used. User can select 10 - 50 MHz system clock (x1 mode) or 2.5 - 12.5 MHz clock (x4 mode). There are 4 Control and Status Registers (CSR's) which can be read and write from 8 bit CSR bus. TMC304 chip has 4 input channels.

MAIN FEATURES

• Least Time Count	: 0.6 - 3.1 ns/bit
• Time Resolution	: RMS = 250 ps (@40 MHz)
• Integral Linearity Error	: < 80 ps @40MHz
• Differential Linearity Error	: < 60 ps @40MHz
• Stability	: (3.0 - 3.6 V. 0 - 70 ˚C)
• System Clock Frequency	: 10 - 50 MHz (x1 mode)
	2.5 - 12.5 MHz (x4 mode)
• No. of Channels	: 4 Channels
• Recording depth	: 128 clock cycle (2.56 - 12.8 μs)
• Double Hit Resolution	: 25 - 32 ns
• Readout mode	: (i) Synchronous read mode (individual channel zero suppress)
	(ii) Synchronous read mode (all channel zero suppress)
	(iii) Asynchronous read mode (4 channel access)
	(iv) Asynchronous read mode (1 channel access)
• Data format	: dual edge encode (hit tag + 5 bit)
• Supply Voltage	: 3.3 V (3.0 - 3.6V)
• Process	: 0.5 μm CMOS Sea-of-Gate
• Power Dissipation	: ~ 50 mW/Channnel (@40MHz, Input=1MHz)
• Package	: 0.5 mm lead pitch, 144 pin plastic QFP
[• Test Circuits	: Ring Oscillator, NMOS and PMOS transistors.]



TMC304(TEG3) Block Diagram

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INTRODUCTION

A. Fine-Time Measurement

The measurement of the fine time is based on a 32 tap ring oscillator as shown in Fig. 1. The circuit of the ring oscillator is modified to generate even number of equaly spaced timing signals and named “Asymmetric Ring Oscilator” [1]. The frequency of the oscillator is stabilized with a PLL(Phase Locked Loop) circuit. The level of the external signal is stored to latches at every

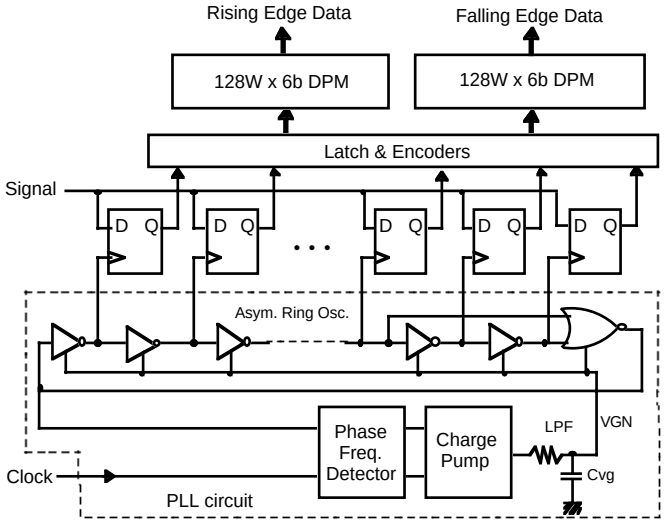

Fig. 1 TMC core circuit.

PIN DESCRIPTION

[I = Input, DI = Differential Input, O = Normal Output, TO = Three State Output; PU = with internal pull-up resistor, PD = with internal pull-down resistor, * = negative logic]

TMC pins

- EDCLK [I] : When this signal is High level, CLKP/CLKN pins are connected to a differential input receiver. When this signal is Low level, the CLKP pin is connected to a single ended input buffer and the CLKN is disconnected from the internal circuit.

- CLKP,CLKN [DI/I] : System clock inputs. In a differential input mode, CLKP act as a non-inverting input and CLKN act as a inverting input. In a single end mode, CLKP pin is used as the clock input.

- DIV4 [I] : Divide by 4 selection. When this signal is high, the internal oscillation clock is divided by 4 before the phase comparator of the PLL. Thus the internal clock frequency has 4 times higher frequency of the system clock.

- RESET* [I] : This input pin is used to reset all the internal circuit. When RESET* is asserted, internal registers and circuit are initialized. The PLL circuit does not be affected in the reset operation when DIV4 is low. When “divide by 4” mode is selected (DIV4=High), phase lock is lost at the reset.

- CIO0*~CIO7* [I,TO] : These I/O pins are data lines for control bus which read and write the CSR registers.

- CS* [I] : This signal is a strobe signal for the control bus.

- RA0~1 [I] : These pins are used as address line to the control bus.

- WR* [I] : This pin is a Read/Write* select signal in the control bus.

- ED [I] : When this signal is High level, TINxP/TINxN (x=0..3) pins are connected to a differential input receiver. When this signal is Low level, the TINxP pin is connected to a single ended input buffer and the TINxN pin is disconnected from internal circuit.

- TIN0P ~ TIN3P,TIN0N~3N [DI/I] : Inputs for time measuring signals. In differential input mode, TINxP act as a non-inverting input and TINxN act as a inverting input. In single end mode, TINxP is used for the input of clock.

- Rxy (x=0..3, y=0..5) [TO] : These signals are output of rising edge data. The "x" denotes channel number and the "y" denotes bit number. Bit 0 to 4 indicate encoded data and bit 5 indicates a hit tag. Timing characteristic of the bit 5 is controlled by ZSG* signal, and user can select pulse or level output. The three-state output buffer is controlled by a RE* signal.

- Fxy (x=0..3, y=0..5) [TO] : These signals are output of falling edge data. The "x" denotes channel number and the "y" denotes bit number. Bit 0 to 4 indicate encoded data and bit 5 indicates a hit tag. Timing characteristic of the bit 5 is controlled by ZSG* signal, and user can select pulse or level output. The three-state output buffer is controlled by a RE* signal.

- RP0-RP6 [TO] : These pins provide the Read Pointer value with synchronous to the Rxy and Fxy. The three-state output buffer is controlled by RE* signal.

- RE* [I] : This input controls the three-state output buffers of Rxy, Fxy and RP0-6. When RE* is asserted those output buffers are enabled as shown below. When RE* is negated, those output has high impedance.

RE*	RMODE	DCH0, 1	R0y, F0y	R1y, F1y	R2y, F2y	R3y, F3y	RP0-RP6
1	x	x	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
0	0, 1, 2	x	enabled	enabled	enabled	enabled	enabled
0	3	0	enabled	Hi Z	Hi Z	Hi Z	enabled
0	3	1	Hi Z	enabled	Hi Z	Hi Z	enabled
0	3	2	Hi Z	Hi Z	enabled	Hi Z	enabled
0	3	3	Hi Z	Hi Z	Hi Z	enabled	enabled

• RMOD1~0 [I] : These pins select readout mode as shown below.

RMODE	Readout mode
0	Synchronous read mode (individual channel zero suppress)
1	Synchronous read mode (all channel zero suppress)
2	Asynchronous read mode (4 channel access)
3	Asynchronous read mode (1 channel access)

RMODE = [RMOD1,RMOD0]

RMODE=0 is a synchronous read mode and data will appear at the output at every clock cycle. Each channel has its own hit tag bit.

RMODE=1 is almost same as the RMODE0 but the R05 indicates ORed signal of all 4 channel hit tag of the rising edge. The F05 indicates ORed signal of all 4 channel hit tag of the falling edge. In addition, the R15 indicates ORed signal of all 4 channel hit tag of both rising and falling edge. All other Rx5 signals have same value as in the RMODE=0.

RMODE=2 is an asynchronous read mode, and all 4 channel data are read out simultaneously controlled by RCLK. In the asynchronous mode, data recording should be stopped when reading.

RMODE=3 is an asynchronous read mode. In the asynchronous mode, data recording should be stopped when reading. The data readout is done for each channel selected by DCH0 and DCH1. Readout timing is controlled by RCLK.

• DCH1~0 [I] : These signals select readout channel when readout mode is 3.

• RCLK [I] : This signal is used to control the data readout timing in the asynchronous read mode (RMODE=2 or 3).

• ZSG* [I] : This signal controls the timing characteristics of the hit tag outputs (Rx5, Fx5). When this signal is asserted, the hit tag outputs become pulsed output and can be used to strobe non-zero data. When this bit is negated, the hit tag outputs has same timing characteristics as other data line.

• WSTART [I] : This signal starts write cycle of the TMC.

• WRUN [O] : This signal indicates the start of the write cycle in the TMC. This is a synchronized signal with the system clock.

• RSTART [I] : This signal starts readout cycle of the dual port memory.

• RRUN [O] : This signal indicates the start of the readout cycle of the dual port memory. This is a synchronized signal with the system clock.

• VGN0-VGN3 [O] : These pins are outputs of PLL loop filter, and must be connected to external capacitors of ~6800 pF.

- SF1 - SF2 [I] : Selection of the PLL loop filter value.These pins should be connect to Vdd.
- WS* [O] : Write strobe signal. This signal can be used as a strobe signal of the data (Rxy, Fxy and RP0-6).

Test purpose pins (expert only)

[Following pins are used for test purpose. Normal user can leave those pins open.]

- DN [O] : PLL down signal.
- UP [O] : PLL up signal.
- ROSC [O] : TMC ring oscillator clock output. You can check internal clock signal throgh this pin when TSTROSC pin is connected to high level. There is a PLL circuit for each channel, and you can select the channel by DCH0-1 signals as shown below.

TSTROSC	DCH1	DCH0	ROSC
1	0	0	Ch0 PLL Clock
1	0	1	Ch1 PLL Clock
1	1	0	Ch2 PLL Clock
1	1	1	Ch3 PLL Clock
0	x	x	0

- TSTROSC [I, PD] : Enable oscillator test. When this signal is asserted, PLL oscillator output select by DCH0 and 1 is connected to ROSC pin. In addition the selected signal is also supplied to the read pointer to check the frequency.
- ENRO* [I, PU] : Enable radiation test ring oscillator.
- ROOUT [O] : Ring oscillator output for radiation damage test.
- WTCEN [I, PD] : WTCLK enable.
- WTCLK [I, PD] : Write test clock.
- NMOSG, NMOSD, PMOSG, PMOSD, COM : Test transistor connections. Each pis has input protection circuit.

CSR Registers

CSR registers bit assignment

bit	7	6	5	4	3	2	1	0
CSR0	SHIFT (R/W:0)	MTEST (R/W:0)	**NRPSYN** (R/W:0)	**ENRPUP** (R/W:0)	- (R/W:0)	TCH1 (R/W:0)	TCH0 (R/W:0)	F/R* (R/W:0)
CSR1	0	**Read Pointer register [RPR]** (R/W:0)						
CSR2	0	**Write Pointer Register [WPR]** (R/W:0)						
CSR3	SOUT (R:0)	SIN (R/W:0)	Test Data Register [TDR] (R/W:0)					

(R/W: x) --- (Readable/Writeable: Initial value)

* CSR0 : Miscellaneous control.

- NRPSYN [read/write]: Disable synchronous count up of the read pointer with write pointer. When NRPSYN="0", the read pointer is incremented synchronous to the system clock when write cycle started. If the NRPSYN="1", this automatic count up is inhibited.

- ENRPUP [read/write] : Enable automatic count up of the read pointer after asynchronous readout. When ENRPUP="1" and in asynchronous read mode (RMODE=2 or 3), the read pointer is incremented after negation of the RCLK.

---------- [Following bits are used to test chip. Normal user should not set these bits.]

- F/R* [read/write]: Test data select, =0 rising edge, =1 falling edge.

- TCH0~1 [read/write]: Test channel select. TCH = [TCH1,TCH0].

- MTEST : Memory Test select. When this bit is set, output of the Test Data Register (TDR) is connected to the input of the DPM and the input of TDR is connected to the output of encoder logic selected by TCH bits and F/R* bit.

- SHIFT : Enable Shift In/Out. When this bit is set, the value of the SIN bit is shifted into the encode register which is selected by CH bits at the end of CSR3 read/write operation..[read/write]

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* CSR1 : Read Pointer Register

- RPR [read/write]: Read Pointer Register. This is a 7-bit loadable up-counter which outputs are connected to the read addresses of the Dual Port Memory (DPM). The read pointer is set through this register and read back present value of the read pointer.

* CSR2 : Write Pointer Register

- WPR [read/write]: Write Pointer Register. This is a 7-bit up loadable up-counter which outputs are connected to the write addresses of the Dual Port Memory (DPM). The write pointer is set through this register and read back present value of the write pointer.

* CSR3 : Test Data Register

[This register is used to test chip. Normal user should not set this register.]

- TDR [read/write]: Test Data Register.
- SIN [read/write] : Serial Input bit.
- SOUT [read only] : Serial output bit

Data Encoding Scheme

Digitized data at TMC circuit is encoded before the write operation to the dual port memory. The data encoding scheme is shown in the following table . Bit position at which the data is changed from "0" to "1" is encoded in the rising edge data, and bit position of "1" to "0" is encoded in the falling edge data. Hit tag bit shows the existence of those transition.

In addition to the transition encoding, user can get all "0" or all "1" information by taking the encoded data at no hit tag. This may help more understanding of the signal behavior.

Rising Edge

0	1	2	3	4	5	…	row data	…	30	31	next cycle 0	[Rx5] Hit Tag	[Rx4..0] Encoded Data	Comment
0	0	0	0	0	0	•	•	•	0	0	0	0	0	all 0
1	d	d	d	d	d	•	•	•	d	d	d	0	1	all 1 /no R edge
0	1	x	x	x	x	•	•	•	x	x	x	1	0	edge at 0-1
x	0	1	x	x	x	•	•	•	x	x	x	1	1	edge at 1-2
d	d	0	1	x	x	•	•	•	x	x	x	1	2	edge at 2-3
d	d	d	0	1	x	•	•	•	x	x	x	1	3	edge at 3-4
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
d	d	d	d	d	d	•	•	•	0	1	x	1	30	edge at 30-31
d	d	d	d	d	d	•	•	•	d	0	1	1	31	edge at 31-0

Falling Edge

0	1	2	3	4	5	…	row data	…	30	31	next cycle 0	[Fx5] Hit Tag	[Fx4..0] Encoded Data	Comment
1	1	1	1	1	1	•	•	•	1	1	1	0	0	all 1
0	u	u	u	u	u	•	•	•	u	u	u	0	1	all 0 /no F edge
1	0	x	x	x	x	•	•	•	x	x	x	1	0	edge at 0-1
x	1	0	x	x	x	•	•	•	x	x	x	1	1	edge at 1-2
u	u	1	0	x	x	•	•	•	x	x	x	1	2	edge at 2-3
u	u	u	1	0	x	•	•	•	x	x	x	1	3	edge at 3-4
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
u	u	u	u	u	u	•	•	•	1	0	x	1	30	edge at 30-31
u	u	u	u	u	u	•	•	•	1	1	0	1	31	edge at 31-0

d..d = no rising edge
u..u = no falling edge
x = don't care

TMC304 Pin Assignments

Pin No	Signal Name
1	VDD
2	CIO0*
3	CIO1*
4	CIO2*
5	CIO3*
6	VSS
7	CIO4*
8	CIO5*
9	CIO6*
10	CIO7*
11	ZSG*
12	VSS
13	R00
14	R01
15	R02
16	R03
17	R04
18	VDD
19	R05
20	(ROOUT)
21	WS*
22	RRUN
23	TIN0N
24	TIN0P
25	TIN1N
26	TIN1P
27	VSS
28	ED
29	TIN2N
30	TIN2P
31	TIN3N
32	TIN3P
33	VSS
34	VDD[PMOSD]
35	VDD[PMOSG]
36	(COM)

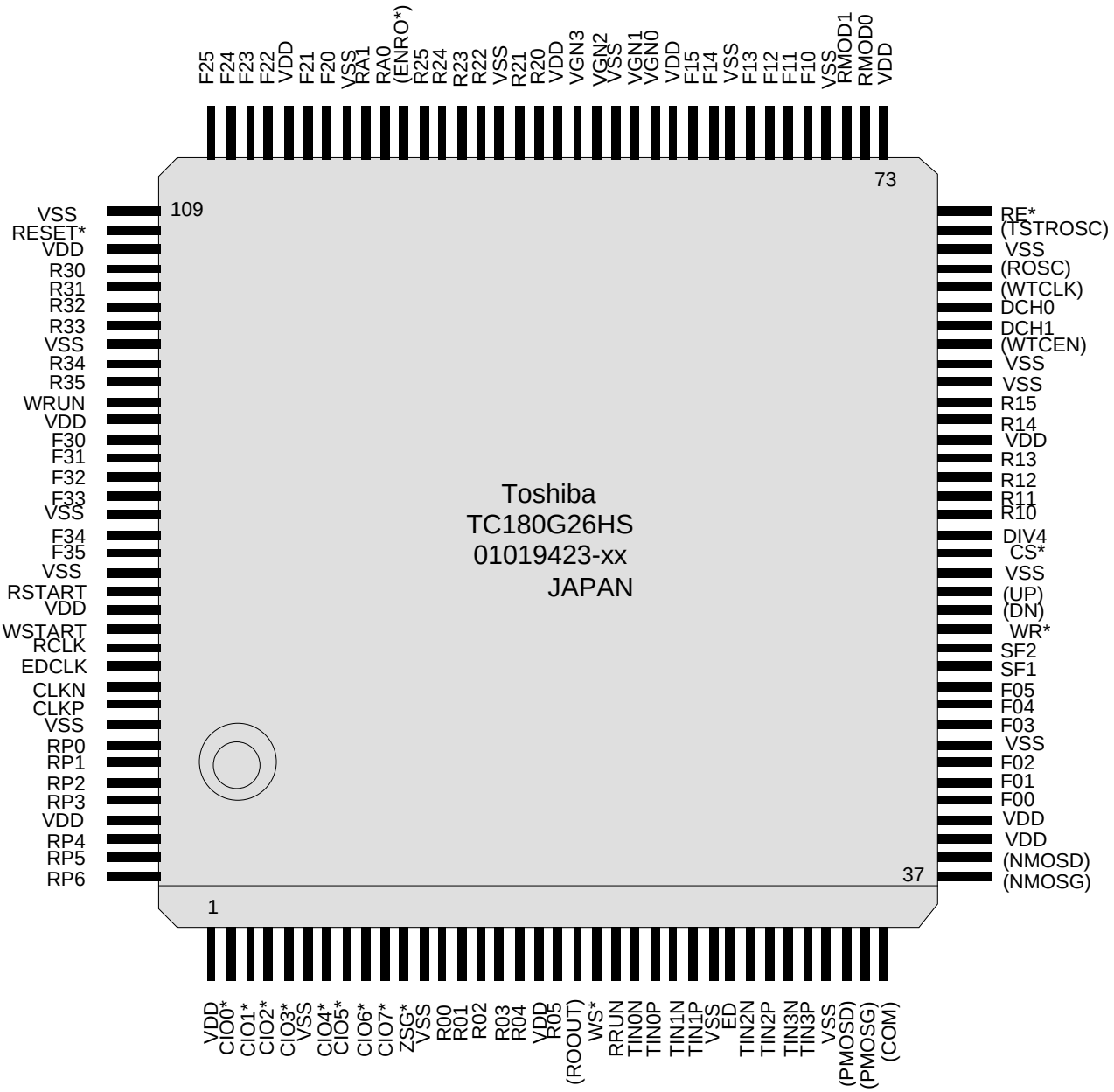
Pin No	Signal Name
37	VSS[NMOSG]
38	VSS[NMOSD]
39	VDD
40	VDD
41	F00
42	F01
43	F02
44	VSS
45	F03
46	F04
47	F05
48	SF1
49	SF2
50	WR*
51	(DN)
52	(UP)
53	VSS
54	CS*
55	DIV4
56	R10
57	R11
58	R12
59	R13
60	VDD
61	R14
62	R15
63	VSS
64	VSS
65	(WTCEN)
66	**DCH1**
67	**DCH0**
68	(WTCLK)
69	ROSC
70	VSS
71	(TSTROSC)
72	RE*

)

Pin No	Signal Name
73	VDD
74	RMOD0
75	RMOD1
76	VSS
77	F10
78	F11
79	F12
80	F13
81	VSS
82	F14
83	F15
84	VDD
85	VGN0
86	VGN1
87	VSS
88	VGN2
89	VGN3
90	VDD
91	R20
92	R21
93	VSS
94	R22
95	R23
96	R24
97	R25
98	(ENRO*)
99	RA0
100	RA1
101	VSS
102	F20
103	F21
104	VDD
105	F22
106	F23
107	F24
108	F25

Pin No	Signal Name
109	VSS
110	RESET*
111	VDD
112	R30
113	R31
114	R32
115	R33
116	VSS
117	R34
118	R35
119	WRUN
120	VDD
121	F30
122	F31
123	F32
124	F33
125	VSS
126	F34
127	F35
128	VSS
129	RSTART
130	VDD
131	WSTART
132	RCLK
133	EDCLK
134	CLKN
135	CLKP
136	VSS
137	RP0
138	RP1
139	RP2
140	RP3
141	VDD
142	RP4
143	RP5
144	RP6

* --- negative logic
( ) -- Test Signals (leave open)



n.c.=non connection, ( ) = Test Signals (leave open)

TMCTEG3 Pin Assignment (Top View)

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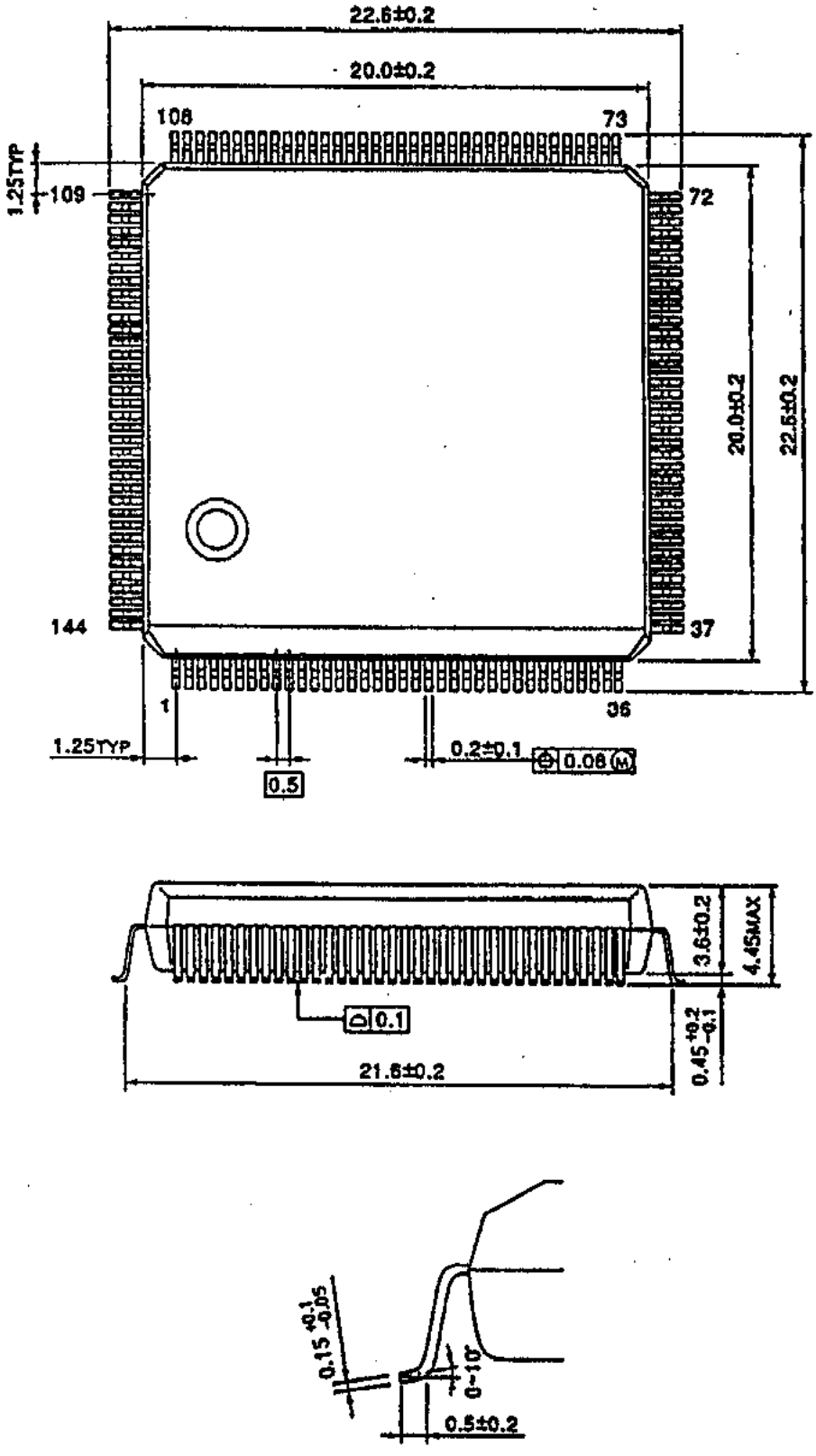


QFP144 Shrink 144-pin Plastic Flat Package (unit : mm)

• Maximum Ratings

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	-0.3 to +5.0 V
V_{IN}	Input Voltage	-0.3 to VDD+0.3 V
I_{IN}	Input Current	±10 mA
T_{STG}	Storage Temperature	-40 to +125 ˚C

• Recommended Operating Condition (V_{SS} = 0V)

Symbol	Parameter	Value
V_{DD}	DC Supply Voltage	3.0 to 3.6 V
Ta	Ambient Temperature	0 to +70 ˚C

• DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input High Voltage		V_{DD} x 0.8		
V_{IL}	Input Low Voltage		V_{DD} x 0.2		
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	-10	10	µA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	-10	10	µA
V_{OH}	High-Level Output Voltage	RRUN, WRUN, ROSC I_{OH} = -4 mA (B4)	2.4		V
		All Signals except above. I_{OH} = -8 mA (B8)	2.4		V
V_{OL}	Low-Level Output Voltage	RRUN, WRUN, ROSC I_{OH} = 4 mA (B4)		0.4	V
		All Signals except above I_{OH} = 8 mA (B8)		0.4	V
I_{OZ}	3-state Output Leakage Current		-10	10	µA
I_{DDS}	Quiescent Device Current	$V_{IN} = V_{DD}$ or V_{SS}		60	µA

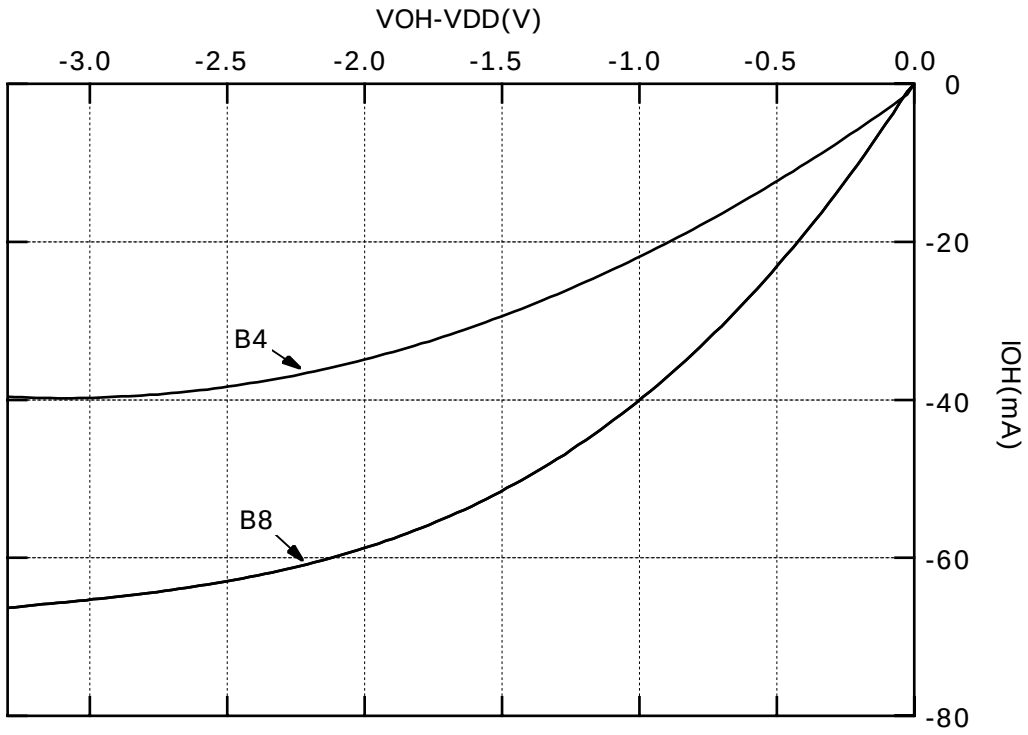


Fig.1 Output High Level Current Characteristic
(VDD=3.3V, Ta=25 °C, typ)

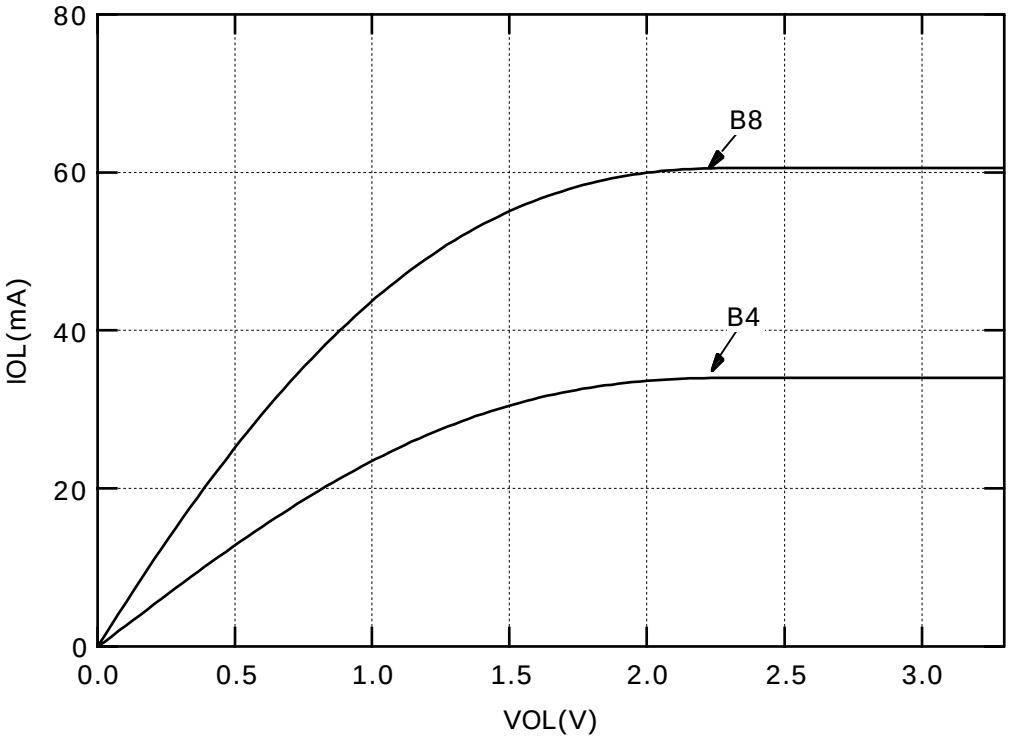


Fig. 2 Output Low Level Current Characteristic
(VDD=3.3V, Ta=25 °C, typ)

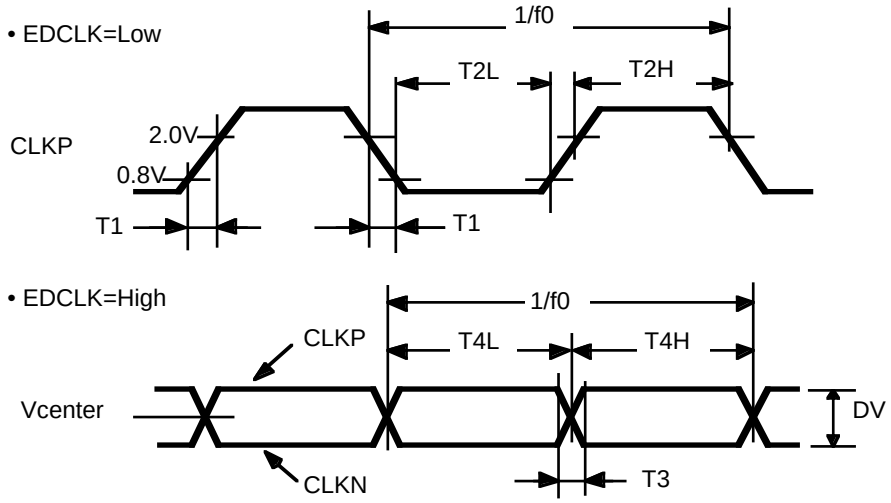
[AC Characteristics]

(VDD = 3.3 V, Ta = 25 ˚C. ROSC, WRUN, RRUN : Cload = 25 pF, All other output signals : Cload = 50 pF)

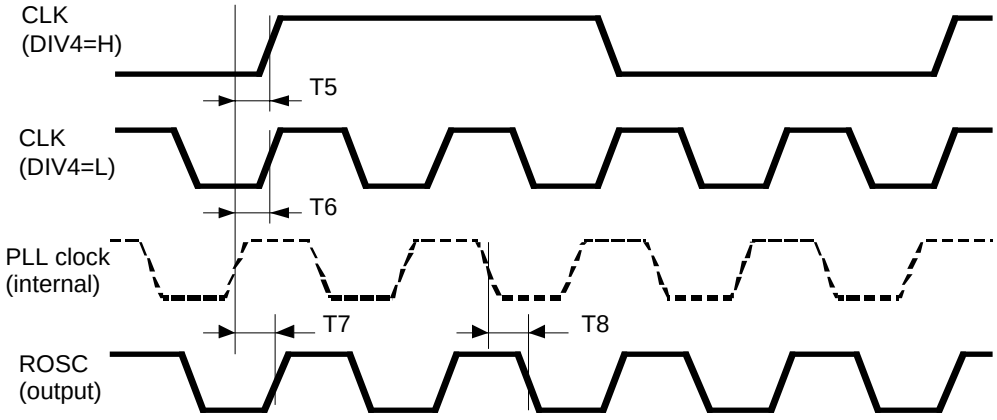
• Clock Signal Characteristics

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
f0	CLK frequency	DIV4=L	10	-	50	MHz
		DIV4=H	2.5	-	12.5	MHz
T1	CLK rise and fall time	EDCLK=L	-	-	3.0	ns
T2L/T2H	CLK duty factor	EDCLK=L	0.6	1.0	1.4	
Vcenter	Center voltage of differential clock	EDCLK=H	1.4	-	2.6	V
ΔV	Differential clock amplitude	EDCLK=H	100	-	-	mV
ΔV/T3	CLK rise and fall rate	EDCLK=H	-	-	1	V/ns
T4L/T4H	CLK duty factor	EDCLK=H	0.6	1.0	1.4	
T5	External clock and PLL clock phase offset	DIV4=1	- 4	- 1.7	1	ns
T6	External clock and PLL clock phase offset	DIV4=0	- 3	- 0.7	2	ns
T7	Rising edge delay between ROSC output and PLL clock	TSTROSC=1	2.5	4.2	6.3	ns
T8	Falling edge delay between ROSC output and PLL clock	TSTROSC=1	2.8	4.7	7.1	ns

[Clock Waveforms]



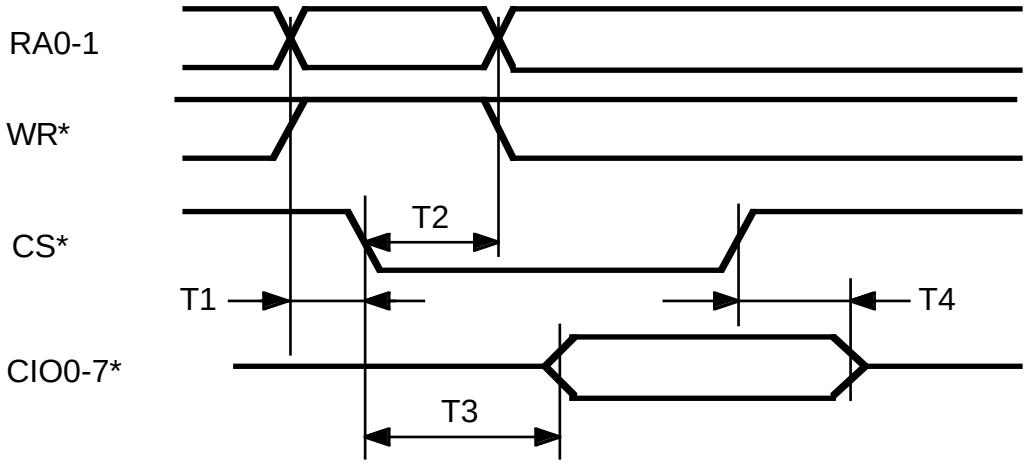
[Clock Offsets]



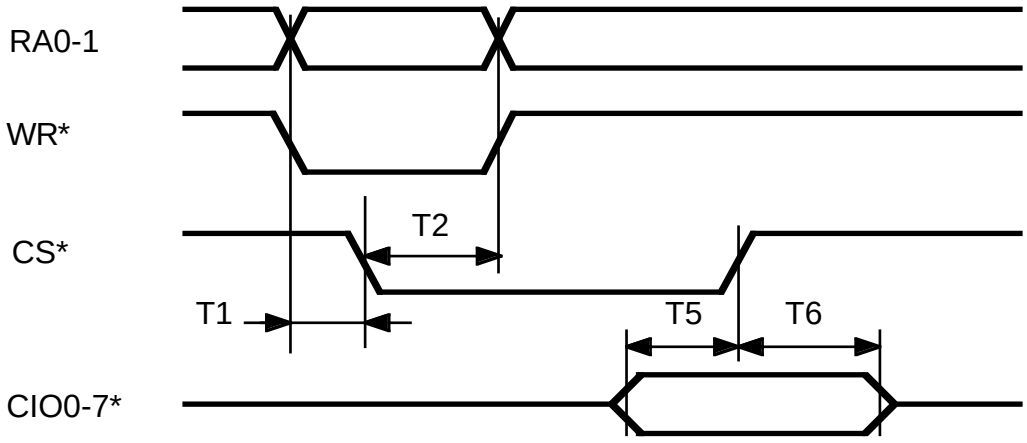
• **CSR Access Timing**

Symbol	Characteristics	Min	Typ	Max	Unit
T1	RA, WR* setup time	1.0	-	-	ns
T2	RA, WR* hold time	2.0	-	-	ns
T3	CS* asserted to CIO* asserted	4.4	-	12	ns
T4	CS* negated to CIO* negated	2.8	-	8	ns
T5	CIO* setup time	0.0	-	-	ns
T6	CIO* hold time	3.0	-	-	ns

[CSR Read Cycle Timing Diagram]



[CSR Write Cycle Timing Diagram]

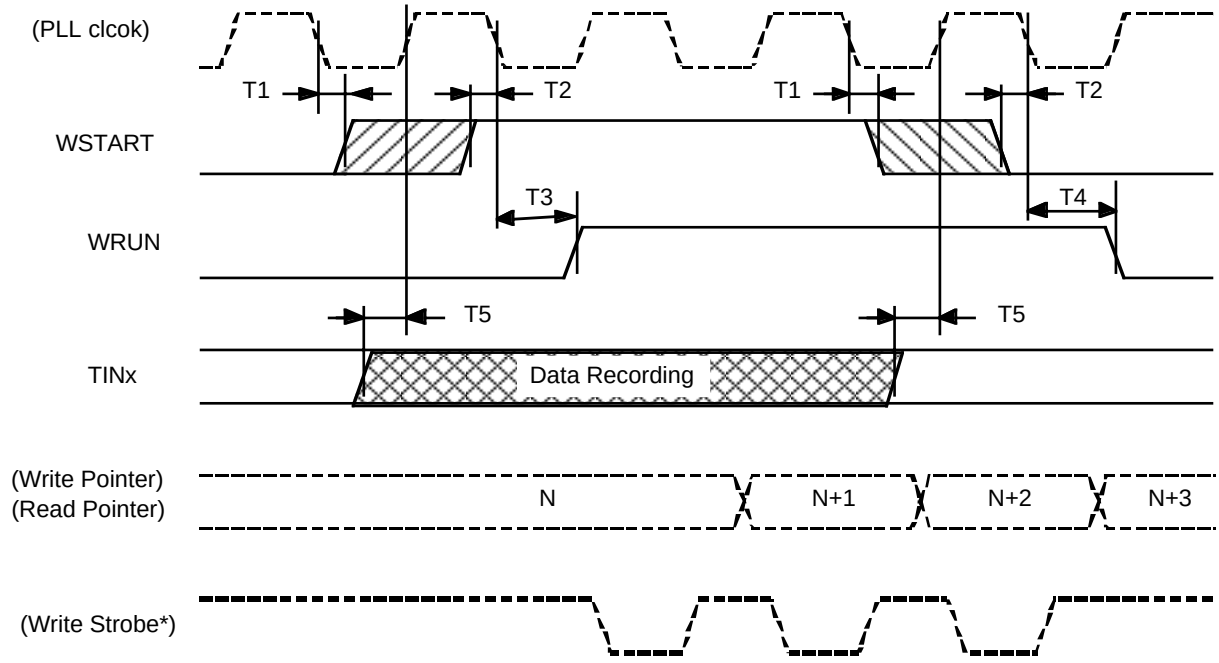


• Input Recording Timing

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	WSTART safety area start timing (*)		-	-	1.5	ns
T2	WSTART safety area end timing (*)		-	-	0.1	ns
T3	WRUN assert timing		2.8	-	7.1	ns
T4	WRUN negate timing		2.9	-	7.3	ns
T5	Input recording timing	Δt=bit width	-	7Δt	-	ns

(*) If WSTART is asserted outside of this safety area, it is not guaranteed that the input recording will start from the next cycle. User can identify the start of recording by checking WRUN signal., or synchronize the WSTART signal to CLK signal if necessary.

[Input Recording Timing]

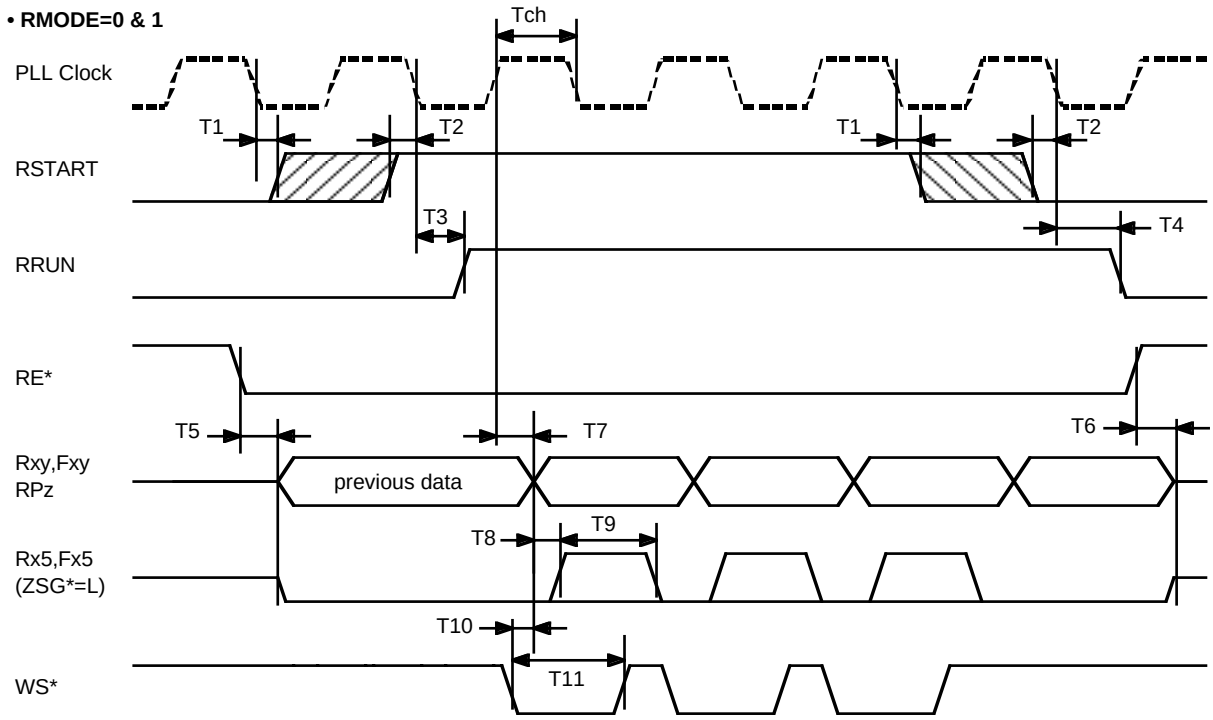


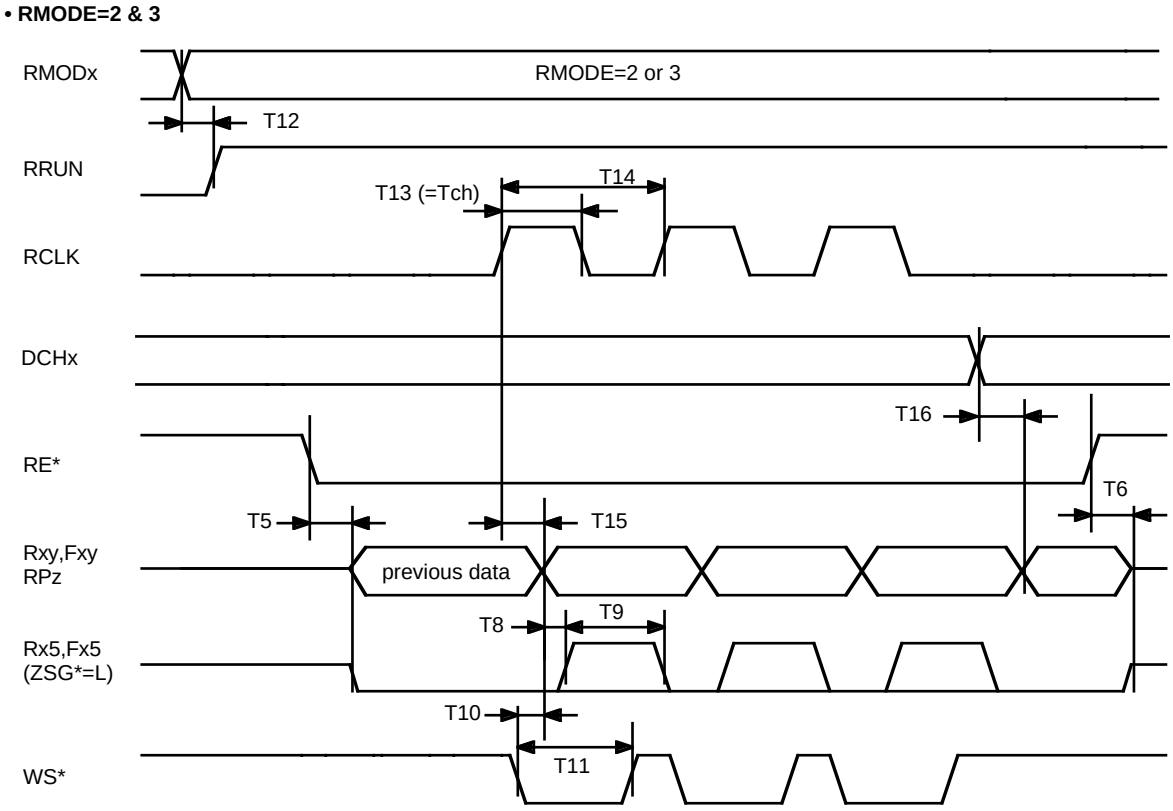
( ) -- Internal Signal

• Readout Timing

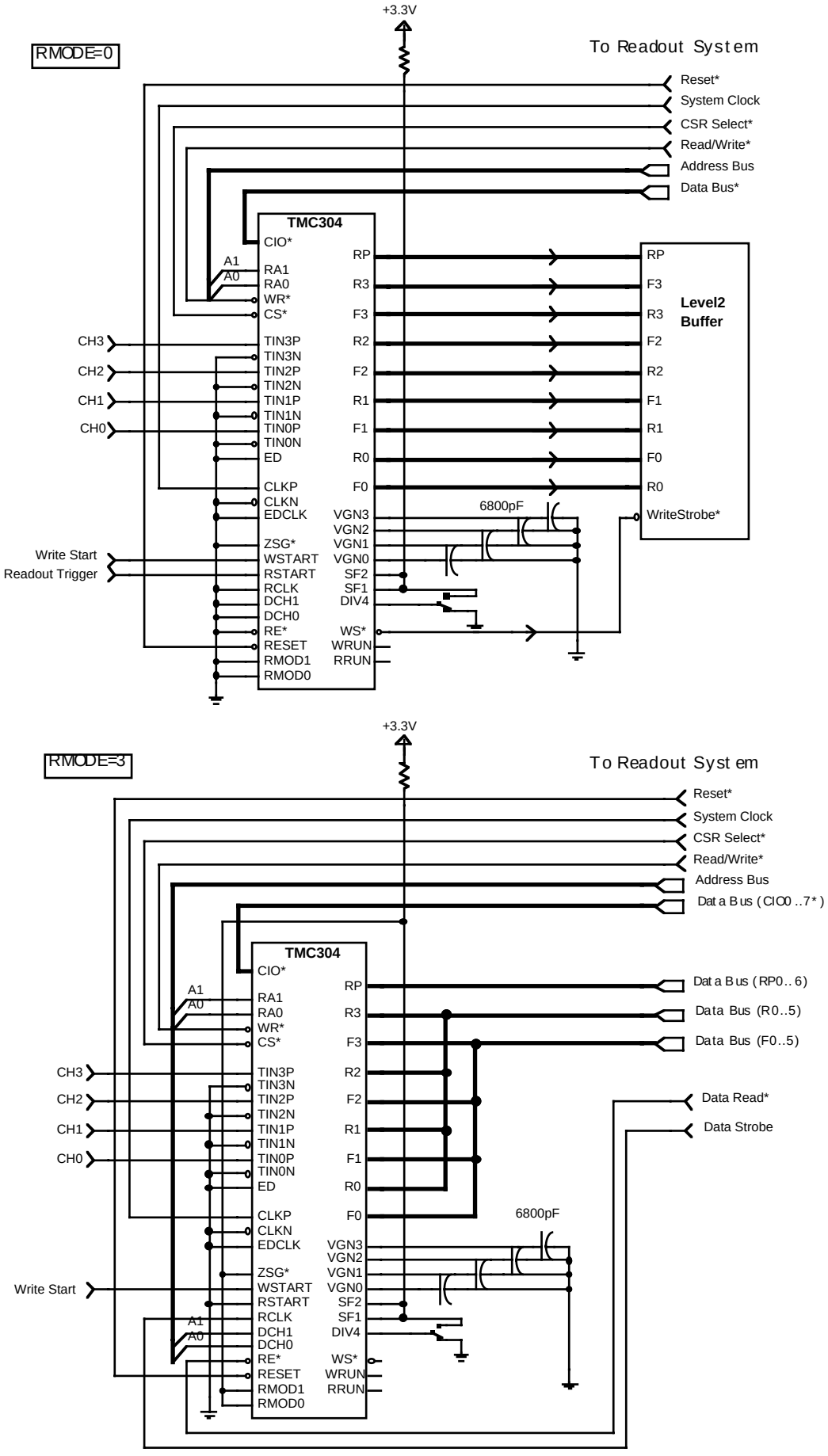
Symbol	Characteristics	Condition	Min	Max	Unit
T1	RSTART safety area start timing (*)	RMODE=0 or 1	-	1.1	ns
T2	RSTART safety area end timing (*)	RMODE=0 or 1	-	0.3	ns
T3	RRUN assert timing	RMODE=0 or 1	3.1	7.8	ns
T4	RRUN negate timing	RMODE=0 or 1	2.9	7.4	ns
T5	RE* assert to data line enable time		3.4	9.5	ns
T6	RE* negate to data line disable time		3.0	10.2	ns
T7	PLL clock high to data assert time	RMODE=0 or 1	3.9	10.5	ns
T8	Data change to Rx5, Fx5 assert time	ZSG*=L	0.8	3.8	ns
T9	Rx5, Fx5 pulse width (**)		Tch+0.8	Tch+2.3	ns
T10	WS* assert to data change time		0.8	3.3	ns
T11	WS* pulse width (**)		Tch+0.1	Tch+0.4	ns
T12	RMOD to RRUN assert time	RMODE=2 or 3	3.1	7.6	ns
T13	RCLK high pulse width (=Tch)	RMODE=2 or 3	5	-	ns
T14	RCLK cycle time	RMODE=2 or 3	20	-	ns
T15	RCLK high to data assert time	RMODE=2 or 3	4.1	11.6	ns
T16	DCHx to channel data change time	RMODE=3	3.7	8.5	ns

(*) If RSTART is asserted outside of this safety area, it is not guaranteed that the readout will start from the next cycle. User can identify the start of reading by checking RRUN signal., or synchronize the RSTART signal to CLK signal if necessary.
(**) Tch : Clock high time of PLL clock(RMODE=0 or 1) or RCLK(RMODE=2 or 3).





Readout Timing



Exapmles of signal connections.