IOS-320

12-Bit High-Density Analog Input Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The I/O Server Module IOS-320 is a 12-bit, high-density, single-size IOS analog input board with the capability to monitor 20 differential or 40 single-ended analog input channels. The IOS-320 utilizes state of the art Surface Mounted Technology (SMT) to achieve its high channel density. It offers a variety of features which make it an ideal choice for many industrial and scientific applications as described below.

Important Note: The following IOS model are accessories to the IOS Server Models: IOS-7200, IOS-7200-WIN, IOS-7400, and IOS-7400-WIN; which are cULus Listed. This equipment is suitable for use in Class I, Division 2, Groups A, B, C, and D or non-hazardous locations only.

Model	Operating Temperature Range
IOS-320	-40 to 85^{o}C

KEY ANALOG INPUT FEATURES

- **High Channel Count -** Monitors up to 20 differential, or 40 single-ended analog inputs (acquisition mode and channels are selected via a programmable control register). Up to four units may be mounted on a carrier board providing up to 80 differential inputs, or 160 single-ended inputs in a single system slot.
- **12-bit Accuracy -** Contains an enhanced, 12-bit, successive approximation Analog to Digital Converter (ADC) with a 4.5uS conversion time.
- **High Speed -** The recommended maximum system throughput rate is 100KHz.
- **Multiple Input Range –** A Hardware DIP switch allows for selectable ranges for both bipolar and unipolar voltage inputs: -5 to +5V, -10 to +10V, and 0 to +10V.
- **Programmable Gain -** Gains of 1, 2, 4, and 8 are programmable via the control register.
- **Software/Hardware Trigger -** Input acquisition can be triggered via software, or by an external hardware input for synchronization to external events.
- **Precision References -** On-board, high-precision voltage references provide the means for accurate and reliable software calibration of the module.
- **Conduction Cooled Module** - I/O modules employ advanced thermal technologies. A thermal pad and module cover wicks heat away from the module and transfers the energy to a heat spreading friction plate. Heat moves to the enclosure walls where it is dissipated by the external cooling fins.

I/O SERVER MODULE INTERFACE FEATURES

- **High density -** Single-size, industry standard, IOS module footprint. Four units mounted on a carrier board provide up to 80 differential or 160 single-ended channels.
- **Local ID** - Each IOS module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **16-bit I/O** - Control register Read/Write and A/D Conversion/Read are performed through 16-bit data transfer cycles.

I/O SERVER MODULE SOFTWARE

IOS MODULE Win32 DRIVER SOFTWARE

Acromag provides a software product (sold separately) to facilitate the development of Windows Embedded Standard applications interfacing with I/O Server Modules installed on Acromag Industrial I/O Server systems. This software (Model IOSSW-DEV-WIN) consists of a low-level driver and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic.NET, Borland C++ Builder and others. The DLL functions provide a high-level interface to the IOS carrier and modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

IOS MODULE LINUX SOFTWARE

Acromag provides a software product (sold separately) consisting of Linux® software. This software (Model IOSSW-API-LNX) is composed of Linux libraries designed to support applications accessing I/O Server Modules installed on Acromag Industrial I/O Server systems. The software is implemented as a library of “C” functions which link with existing user code.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

BOARD CONFIGURATION

The board may be configured differently, depending on the application. All allowable jumper settings are discussed in the following sections. Jumper locations are shown in the drawing in the end of this manaul.

Power should be removed from the board when configuring hardware jumpers, installing IOS modulesIP's, cables, termination panels and field wiring. Refer to the Analog Input Connection Diagram on page 15 and IOS documentation for IOS configuration and assembly instructions.

Default Hardware Jumper Configuration

A board shipped from the factory is configured as follows:

- Analog input range is configured for a 10V bipolar input span (i.e. an ADC input range of -5 to +5 Volts).
- Internal ±12 Volt power supplies are used (sourced from P1 connector).
- Programmable software control register bits are set at logic low during power-up reset. The control register should be programmed to the desired gain, mode, and channel configuration before starting ADC analog input acquisition.

Analog Input Range Hardware Jumper Configuration

The ADC input range is programmed via hardware DIP switch. The DIP switch controls the input voltage span and the selection of unipolar or bipolar input ranges. The configuration of the DIP switch for the different ranges is shown in table 2.1. A switch selected as "ON" would be positioned to the side of the DIP labeled "ON". The DIP switch location is shown in the Jumper Locations drawing on page 14.

The selection of internal or external analog power supplies is accomplished via hardware jumpers J1 and J2. J1 (J2) controls the selection of either the internal +12 (-12) Volt supply sourced from P1 connector, or the external +15 (-15) Volt supply sourced from the P2 connector. The configuration of the jumpers for the different supplies is shown in the table 2.2. "IN" means that the pins are shorted together with a shorting clip. "OUT" means the clip has been removed. For a detailed drawing refer to the Jumper Locations drawing on page 14.

Table 2.1: Analog Input Range Selections/DIP Switch Settings

Desired ADC Input Range* (VDC)	Required Input Span (Volts)	Required Input Type	Switch Settings ON	Switch Settings OFF
-5 to +5	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 to +10**	20	Bipolar	2,5,6,9	1,3,4,7,8
0 to +10**	10	Unipolar	1,3,4,7	2,5,6,8,9

* Assuming a gain of 1.

** These ranges can only be achieved with ±15V external power supplies. The input ranges will be clipped if ±12V supplies are used, typically to ±9 V maximum inputs.

Table 2.2: Power Supply Selections (Pins of J1 and J2)

Power Supply Selection*	J1/J2 (1&2)	J1/J2 (2&3)
±12 Volt (Internal, P1)	IN	OUT
±15 Volt (External, P2)	OUT	IN

* Internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts).

WARNING: J3 IS USED FOR FACTORY CALIBRATION ONLY! TREAT THESE PINS AS DO NOT CONNECTS. CONNECTING THSE PINS MAY DAMAGE THE BOARD.

Control Register Configuration

The control register is software configurable. There are no hardware jumpers associated with it. Control register bits are defined as logic low at reset and must be programmed to the desired gain, acquisition mode, and channel configuration, before starting ADC analog input acquisition (refer to Section 3 for details).

Analog Input Data Format

The analog input data will appear as Straight Binary for all input ranges. The following tables indicate the relationship between data format (bipolar vs. unipolar) and the ideal analog input voltage to the module.

Table 2.3: Unipolar Straight Binary Analog Data Format*

Analog Input Voltage (Volts)	Unipolar Straight Binary Data (Hex)
9.9976	FFF0
9.9951	FFE0
. .	. .
0.0024	0010
0.0000	0000

* For Table 2.3 it is assumed that the analog input range (unipolar) is 0 to +10 Volts (i.e. with a programmable gain of 1). The 12-bit straight binary data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are zero and should be ignored in calculations made with the data returned from the IOS module.

Table 2.4: Bipolar Straight Binary Analog Data Format*

Analog Input Voltage (Volts)	Bipolar Straight Binary Data (Hex)
4.9976	FFF0
4.9951	FFE0
. .	. .
0.0024	8010
0.0000	8000
-0.0024	7FF0
. .	. .
-4.9976	0010
-5.0000	0000

* For Table 2.4 it is assumed that the analog input range (bipolar) is -5 to +5 Volts (i.e. with a programmable gain of 1). The straight binary, 12-bit data is left-justified within the 16-bit word. The 4 Least Significant Bits (LSB's) are zero and should be ignored in calculations made with the data returned from the IOS module.

CONNECTORS

IOS Field I/O Connector (P2)

P2 provides the field I/O interface connector for mating IOS modules to the carrier board. The field and logic side connectors are keyed to avoid incorrect assembly. P2 pin assignments are unique to each IOS model (see Table 2.5) and correspond to the pin numbers of the front-panel, field I/O interface connector on the carrier board).

In Table 2.5, channel designations are abbreviated to save space. For example, single-ended channel 0 is abbreviated as "SCH00"; the +input for differential channel 0 is abbreviated as "+DCH00". Both of these labels are attached to pin 1, but only one applies according to whether the input is single-ended or differential (i.e. if your inputs are applied differentially, follow the differential channel labeling for each channel's + and - input leads).

Table 2.5: IOS-320 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Numbe r
SCH00/+DCH00	1	SCH32/-DCH12	26
SCH20/-DCH00	2	SCH13/+DCH13	27
SCH01/+DCH01	3	SCH33/-DCH13	28
SCH21/-DCH01	4	SCH14/+DCH14	29
SCH02/+DCH02	5	SCH34/-DCH14	30
SCH22/-DCH02	6	SCH15/+DCH15	31
SCH03/+DCH03	7	SCH35/-DCH15	32
SCH23/-DCH03	8	SCH16/+DCH16	33
SCH04/+DCH04	9	SCH36/-DCH16	34
SCH24/-DCH04	10	SCH17/+DCH17	35
SCH05/+DCH05	11	SCH37/-DCH17	36
SCH25/-DCH05	12	SCH18/+DCH18	37
SCH06/+DCH06	13	SCH38/-DCH18	38
SCH26/-DCH06	14	SCH19/+DCH19	39
SCH07/+DCH07	15	SCH39/-DCH19	40
SCH27/-DCH07	16	SENSE	41
SCH08/+DCH08	17	SENSE	42
SCH28/-DCH08	18	COMMON	43
SCH09/+DCH09	19	COMMON	44
SCH29/-DCH09	20	RESERVED	45
SCH10/+DCH10	21	RESERVED	46
SCH30/-DCH10	22	-15V DC	47
SCH11/+DCH11	23	*Ext Trigger	48
SCH31/-DCH11	24	+15V DC	49
SCH12/+DCH12	25	SHIELD	50

* Indicates an Active-Low Signal

Analog Input Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the IOS module and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references. See page 14 for analog input connections for differential and single-ended inputs.

Single-ended inputs only require a single lead (+) per channel, with a shared "sense" (reference) lead for all channels, and can be used when a large number of input channels come from the same location (e.g. printed circuit board). The channel density doubles when using single-ended inputs, and this a powerful incentive for their use. However, caution must be exercised since the single "sense" lead references all channels to the same common which will induce noise and offset if they are different.

The IOS-320 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed (12-bits or more). Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IOS-320 input module.

External Trigger Input

The external trigger signal on P2 is an active-low input which may be used for synchronizing the ADC conversion of analog inputs from several IOS modules to external events. The external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. Note that the IOS-320 provides 125ns of debounce on the external trigger input. The conversion is triggered on the falling edge of a normally high signal.

The trigger pulse must be low for a minimum of 250nS to guarantee acquisition. The external trigger may remain low for an indefinite period of time. However, it must return to a high state for a minimum of 250nS prior to a subsequent trigger. See Section 3 for programming information.

3.0 PROGRAMMING INFORMATION

ID SPACE- (Read Only, 32 even-byte addresses)

Each IOS module contains an identification (ID) PROM that resides in the ID space.. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IOS" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IOS-320 ID information does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the even addresses in a 64 byte block. The IOS-320 ID space contents are shown in Table 3.1. Note that the base-address for the IOS module ID space (see your carrier board instructions) must be added to the addresses shown to properly access ID space. Execution of an ID space read requires 0 wait states.

Table 3.1: IOS-320 ID Space Identification (ID)

Hex Offset From ID Base Address	Numeric Value (Hex)	Field Description
00	49	
02	50	
04	41	
06	43	
08	A3	Acromag ID Code
0A	32	IOS Model Code[1]
0C	00	Not Used (Revision)
0E	00	Reserved
10	00	Not Used
12	00	Not Used
14	0C	Total Number of ID Bytes
16	2E	CRC
18 to 3E	00	Not Used

Notes (Table 3.2):
1. The IOS model number is represented by a two-digit code within the ID space (the IOS-320 model is represented by 32 Hex).

I/O SPACE ADDRESS MAP

This board is addressable in the I/O Server Module space to control the acquisition of analog inputs from the field. The I/O space may be as large as 64, 16-bit words (128 bytes), but the IOS-320 only uses a portion of this space. The I/O space address map for the IOS-320 is shown in Table 3.2. Note the base address for the IOS module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on a 16-bit word basis (D0..D15).

Table 3.2: IOS-320 I/O Space Address Memory Map

Base Add+ (Hex)	High Byte D15 D08	Low Byte D07 D00	Base Add+ (Hex)
01	R/W - Control Register		00
03 ↓ 0F	Repeated Control Register[1]		02 ↓ 0E
11	W - ADC Convert Command		10
13 ↓ 1F	Repeated ADC Convert Command[1]		12 ↓ 1E
21	R - Read ADC Data		20
23 ↓ 2F	Repeated Read ADC Data[1]		22 ↓ 2E
31 ↓ 3F	Not Used[2]		30 ↓ 3E
41 ↓ 4F	Reserved[2]		40 ↓ 4E
51 ↓ 7F	Not Used[2]		50 ↓ 7E

Notes (Table 3.1):
1. Registers appear in multiple locations in the memory map because of simplified address decoding (these locations can be ignored).
2. The IOS will respond to addresses that are “Not Used” with an active IOS module acknowledge ACK*. The board will return “0” for all address reads that are not used or reserved.

Control Register - (Read/Write, Base + 00H)

The IOS-320 Control Register reflects and controls analog input channel data acquisition functions. This register must be written/read, one word (D16) at a time. Execution of a Control Register read (write) requires 0 (1) wait states. At reset all bits are set to 0. The function of each bit is described as follows:

High Byte

MSB D15	D14	D13	D12	D11	D10	D09	LSB D08
CTRIG	Data Ready	Not used	Not used	Not used	Not used	MODE 1	MODE 0

Low Byte

MSB D07	D06	D05	D04	D03	D02	D01	LSB D00
GSEL 1	GSEL 0	Not used	SEL HIGH	CH3	CH2	CH1	CH0

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Bit 15: When read, the CTRIG bit indicates whether an ADC conversion has been triggered, either by software command or external trigger input. If the bit reads high, the conversion could be taking place or has been completed. CTRIG is cleared by reading the ADC data. Writing to this bit position will have no effect.

Bit 14: The Data Ready bit indicates if an ADC convert command has completed and valid data resides in the ADC Data Register. If the bit reads high, then valid data awaits in the ADC data register from the previous conversion. Data Ready is cleared by reading the ADC data register. Writing to this bit position will have no effect.

Bits 13-10: Not used - if read will return data written to those bit positions.

Bits 9 & 8: Control the input acquisition mode as described in the following table:

Acquisition Mode	MODE1 Bit (D09)	MODE0 Bit (D08)
Differential Input CH0-19 & CAL0-3	0	0
Single-ended Input CH0-19	0	1
Single-ended Input CH20-39	1	0
Auto Zero Input*	1	1

* Auto Zero input is enabled by the mode bits, overriding all channel selection bits.

Bits 7 & 6: Control the programmable gain setting as described in the following table:

Desired Gain Setting	GSEL1 Bit (D07)	GSEL0 Bit (D06)
1	0	0
2	0	1
4	1	0
8	1	1

Bit 5: Not used - if read will return data written to the bit position.

Bit 4: The SEL HIGH bit acts as the MSB for analog input channel selection. As such, its action is grouped with that of bits 3-0 (see following).

Bits 3-0: Control the selection of analog input channels per the following table. Note that the SEL HIGH bit and MODE bits are also shown to completely define the channel selection. When MODE 1 & MODE 0 are both 0, differential channels 0-19 and calibration voltages 0-3 may be selected; when MODE 1 is 0 and MODE 0 is 1, single-ended channels 0-19 may be selected; when MODE 1 is 1 and MODE 0 is 0, single-ended channels 20-39 may be selected; when both MODE 1 & MODE 0 are 1, the Auto Zero input is selected regardless of any other bit levels.

Desired Chan.	SEL HIGH Bit D04	CH3 Bit D03	CH2 Bit D02	CH1 Bit D01	CH0 Bit D00	Mode 1 Bit D09	Mode 0 Bit D08
0	0	0	0	0	0	0	0/1
1	0	0	0	0	1	0	0/1
2	0	0	0	1	0	0	0/1
3	0	0	0	1	1	0	0/1
4	0	0	1	0	0	0	0/1
5	0	0	1	0	1	0	0/1
6	0	0	1	1	0	0	0/1
7	0	0	1	1	1	0	0/1
8	0	1	0	0	0	0	0/1
9	0	1	0	0	1	0	0/1
10	0	1	0	1	0	0	0/1
11	0	1	0	1	1	0	0/1
12	0	1	1	0	0	0	0/1
13	0	1	1	0	1	0	0/1
14	0	1	1	1	0	0	0/1
15	0	1	1	1	1	0	0/1
16	1	0	0	0	0	0	0/1
17	1	0	0	0	1	0	0/1
18	1	0	0	1	0	0	0/1
19	1	0	0	1	1	0	0/1
CAL0	1	0	1	0	0	0	0
CAL1	1	0	1	0	1	0	0
CAL2	1	0	1	1	0	0	0
CAL3	1	0	1	1	1	0	0
20	0	0	0	0	0	1	0
21	0	0	0	0	1	1	0
22	0	0	0	1	0	1	0
23	0	0	0	1	1	1	0
24	0	0	1	0	0	1	0
25	0	0	1	0	1	1	0
26	0	0	1	1	0	1	0
27	0	0	1	1	1	1	0
28	0	1	0	0	0	1	0
29	0	1	0	0	1	1	0
30	0	1	0	1	0	1	0
31	0	1	0	1	1	1	0
32	0	1	1	0	0	1	0
33	0	1	1	0	1	1	0
34	0	1	1	1	0	1	0
35	0	1	1	1	1	1	0
36	1	0	0	0	0	1	0
37	1	0	0	0	1	1	0
38	1	0	0	1	0	1	0
39	1	0	0	1	1	1	0
Auto Zero	X	X	X	X	X	1	1

ADC Convert Command - (Write, Base + 10H)

The ADC Convert Command is a write only register (will not respond to reads) that is used to trigger a conversion. The data written to this location should be all ones to reduce digital noise, although the write action alone is sufficient to trigger the conversion. Note that a write to this register during an A/D conversion will have no effect. Execution of this command requires 1 wait state.

D15...D00
FFFF

NOTE: "FFFF" means that all bits are programmed as ones.

Read ADC Data - (Read, Base + 20H)

Use the Read ADC Data command to read the results of the last ADC conversion. This command should be used following the ADC Convert command or an external trigger input. Bit 15 (CTRIG) in the Control Register can be used to determine if a conversion has been triggered, either by software command or external trigger input. Bit 14 (Data Ready) in the Control Register can be used to determine if a conversion has been completed. If the Read ADC Data command is executed while the ADC conversion is taking place, then the IOS-320 will institute wait states until the data is available (up to 4.5 uS) before providing the ADC data and completing the cycle. Execution of the read command requires 2 wait states, if the ADC conversion completed prior to initiating the read command. The execution of this command will reset the CTRIG and Data Ready bits in the Control Register.

The 12-bits of data are left-justified within the 16-bit word. The four LSB's will always read as 0. Data format is Straight Binary. A Reset will set all bits of this register to ‘0’.

MSB D15 → D4	LSB D03 → D0
ADC DATA	0 0 0 0

PROGRAMMING CONSIDERATIONS FOR ACQUIRING ANALOG INPUTS

The IOS-320 provides two different methods of analog input acquisition to give the user maximum flexibility for each application. The following sections describe the features of each and how to best use them.

Using the Separate ADC Convert and Read Commands

Use of the separate convert and read commands is a straightforward and accurate way to acquire data. This method is useful for most applications.

<u>Programming Example (Separate ADC Convert & Read)</u>

NOTE: For this example it is assumed that the external trigger input is <u>NOT</u> being used to trigger conversions.

1. Write to the control register to configure the acquisition mode, gain, and channel selections.
2. Delay to allow for input settling.
3. Execute the ADC Convert command.
4. Write to the control register to configure the acquisition mode, gain, and channel selections for the next acquisition - if they are different. This may be done while the conversion is in progress because the ADC is in the hold mode.
5. The ADC conversion takes several microseconds. This time can be put to use for other purposes (e.g. calibration of ADC channel data).
6. Read ADC Data - if the conversion is still in progress, the read command will generate wait states until it can deliver the data.
7. Repeat steps 3-6 as required to acquire additional analog input samples. Note that the input settling delay does not have to be inserted, since writing to the control register to configure for the next acquisition, immediately after initiating the previous conversion, will allow the input to adequately settle before the next conversion is started. The overlapping of these tasks with the ADC conversion cycle is what gives rise to "pipelined" operation and maximum system throughput.

Using External Conversion Triggers

External hardware triggers are generated by the user via an external TTL compatible input through the field I/O connector (see Section 2) - make sure that all pertinent voltage and pulse width constraints are met. The conversion is initiated on the falling edge of the external trigger signal. This type of conversion triggering is useful for synchronizing the ADC conversion of analog inputs (e.g. several IOS-320's) to external events. Precise time intervals between conversions can be achieved with an external timing device. Note that external triggers that occur during an A/D conversion cycle will be ignored.

<u>Programming Example (External Conversion Trigger)</u>

NOTE: For this example it is assumed that the external trigger input <u>is</u> being used to trigger conversions.

1. Write to the control register to setup the acquisition mode, gain, and channel selections.
2. Delay to allow for input settling.
3. Poll Bit 15 (CTRIG) in the control register to determine when an ADC conversion has been triggered (this assumes some prior knowledge in the application program that a hardware external trigger will occur for a particular channel's conversion).
4. Read ADC Data - if the conversion is still in progress, the read command will generate wait states until it can deliver the data. The Read ADC Data command will reset the CTRIG bit in the control register to prepare for the next external trigger.
5. Repeat steps 3-4 for acquisition of the same input. Otherwise, repeat steps 1-4 as required.

USE OF CALIBRATION SIGNALS

Reference signals for analog input calibration have been provided to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends. A comparison of the uncalibrated and software calibrated performance is shown to illustrate the importance of the software calibration.

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Programmable Gain Amplifier (PGA) and the Analog to Digital Converter (ADC). The untrimmed PGA and ADC have the following performance:

PGA206AU @25°C:
Linearity Error is ±0.005% Maximum (i.e. 1/4 LSB).
Offset Error RTI is ±1mv Typical; ±2.5mV Maximum.
Gain Error is 0.01% typical, 0.1% maximum for all gains.

(ADC) ADS8508 @25°C:
Linearity Error is ± 0.5 LSB Maximum.
Unipolar Zero Error is ± 5 mV Maximum.
Bipolar Zero Error is ± 1 mV Maximum.
Full Scale Calibration Error is ± 0.5% of span, Maximum.

Table 3.3: Maximum Overall Uncalibrated Error at 25°C

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Offset Error (±LSB)	Max Gain Error (±LSB)
-5 to +5	1	-5 to +5	1.43	22.53
-2.5 to +2.5	2	"	"	"
-1.25 to +1.25	4	"	"	"
-0.625 to +0.625	8	"	"	"
-10 to +10	1	-10 to +10	0.72	"
-5 to +5	2	"	"	"
-2.5 to +2.5	4	"	"	"
-1.25 to +1.25	8	"	"	"
0 to +10	1	0 to +10	3.08	24.58
0 to +5	2	"	"	"
0 to +2.5	4	"	"	"
0 to +1.25	8	"	"	"

Note that the worst case non-linearity error is ±0.75 LSB (the sum of the ½ LSB non-linearity of the ADC and the ¼ LSB non-linearity of the PGA).

Calibrated Performance

Very accurate calibration of the IOS-320 can be accomplished by using calibration voltages present on the board. The four voltages and the analog ground reference are used to determine the endpoints of a straight line which defines the analog input characteristic. The calibration voltages are precisely adjusted at the factory to provide optimum performance, as detailed in the following table:

Calibration Signal	Ideal Value (Volts)	Maximum Tolerance @25°C (Volts)	Maximum Temperature Drift (ppm/°C)
Auto Zero	0.0000	±0.0002	0
CAL0	4.9000	±0.0005	±15
CAL1	2.4500	±0.0005	±20*
CAL2	1.2250	±0.0004	"
CAL3	0.6125	±0.0002	"

* Worst case temperature drift is the sum of the ±15 ppm/°C drift of the calibration voltage reference plus the ±5 ppm/°C drift of the resistors in the voltage divider.

The calibration voltages are used with the auto zero signal to find two points that determine the straight line characteristic of the analog front end for a particular range. The recommended calibration voltage selection for each range is summarized in the following table:

Table 3.4: Recommended Calib. Voltages For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Rec. Low Calib. Voltage "$Volt_{CALLO}$" (Volts)	Rec. High Calib. Voltage "$Volt_{CALHI}$" (Volts)
-5 to +5	1	-5 to +5	0.0000 (A. Z.)	4.9000 (CAL0)
-2.5 to +2.5	2	"	"	2.4500 (CAL1)
-1.25 to +1.25	4	"	"	1.2250 (CAL2)
-0.625 to +0.625	8	"	"	0.6125 (CAL3)
-10 to +10	1	-10 to +10	"	4.9000 (CAL0)
-5 to +5	2	"	"	4.9000 (CAL0)
-2.5 to +2.5	4	"	"	2.4500 (CAL1)
-1.25 to +1.25	8	"	"	1.2250 (CAL2)
0 to +10	1	0 to +10	0.6125 (CAL3)	4.9000 (CAL0)
0 to +5	2	"	"	4.9000 (CAL0)
0 to +2.5	4	"	"	2.4500 (CAL1)
0 to +1.25	8	"	"	1.2250 (CAL2)

The following equation (1) is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the calibration voltages and range constants.

$$\text{Corrected\_Count} = \left[\frac{4096 * m}{\text{Ideal\_Volt\_Span}}\right] * \left[\text{Count\_Actual} + \frac{(\text{Volt}_{CALLO} * \text{Gain}) - \text{Ideal\_Zero}}{m} - \text{Count}_{CALLO}\right] \quad (1)$$

where, "m" represents the actual slope of the transfer characteristic as defined in equation 2:

$$m = \text{Gain} * \left[\frac{\text{Volt}_{CALHI} - \text{Volt}_{CALLO}}{\text{Count}_{CALHI} - \text{Count}_{CALLO}}\right] \quad (2)$$

Gain	=	The Programmable Gain Amplifier Setting Used (See Table 3.4)
Volt_{CALHI}	=	High Calibration Voltage (See Table 3.4)
Volt_{CALLO}	=	Low Calibration Voltage (See Table 3.4)
Count_{CALHI}	=	Actual ADC Data Read With High Calibration Voltage Applied
Count_{CALLO}	=	Actual ADC Data Read With Low Calibration Voltage Applied
Ideal_Volt_Span	=	Ideal ADC Voltage Span (See Table 3.5)
Count_Actual	=	Actual Uncorrected ADC Data For Input Being Measured
Ideal_Zero	=	Ideal ADC Input For “Zero” (See Table 3.5)

Table 3.5: Ideal Voltage Span and Zero For Input Ranges

Input Range (Volts)	PGA Gain	ADC Range (Volts)	"Ideal_Volt_Span" (Volts)	"Ideal_Zero" (Volts)
-5 to +5	1	-5 to +5	10.0000	-5.0000
-2.5 to +2.5	2	"	"	"
-1.25 to +1.25	4	"	"	"
-0.625 to +0.625	8	"	"	"
-10 to +10	1	-10 to +10	20.0000	-10.0000
-5 to +5	2	"	"	"
-2.5 to +2.5	4	"	"	"
-1.25 to +1.25	8	"	"	"
0 to +10	1	0 to +10	10.0000	0.0000
0 to +5	2	"	"	"
0 to +2.5	4	"	"	"
0 to +1.25	8	"	"	"

The calibration parameters (Count_{CALHI} and Count_{CALLO}) for each active input range should be determined at startup and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 16) of the calibration parameters should be taken via the ADC and averaged to reduce the measurement uncertainty.

Calibration Programming Example 1

Assume that the input range is -10 to +10 volts. Channel 0 is connected differentially, and corrected input channel data is desired. From Tables 3.4 & 3.5, several calibration parameters can be determined:

Gain = 1 (From Table 3.4)
Volt_{CALHI} = 4.9000 volts (CAL0; From Table 3.4)
Volt_{CALLO} = 0.0000 volts (Auto Zero; From Table 3.4)
Ideal_Volt_Span = 20.0000 volts (From Table 3.5)
Ideal_Zero = -10.0000 volts (From Table 3.5)

The calibration parameters (Count_{CALHI} and Count_{CALLO}) remain to be determined before uncorrected input channel data can be taken and corrected.

1. To prepare to measure Count_{CALLO}, write to the Control Register (@Base + 00H) to setup the auto zero acquisition mode and PGA gain = 1 by writing 0300H. Note that "not used" and "don't care" bits are set to zero.
2. Delay to allow for input settling.
3. Execute ADC Convert Command (@Base + 10H).
4. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
5. Repeat steps 3 and 4 several times (e.g. 16) and take the average of the ADC results. Save this number as Count_{CALLO}.
6. To prepare to measure Count_{CALHI}, write to the Control Register (@Base + 00H) to setup the CAL0 acquisition mode and PGA gain = 1 by writing 0014H. Note that "not used" bits are set to zero.
7. Delay to allow for input settling.
8. Execute ADC Convert Command (@Base + 10H).
9. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
10. Repeat steps 8 and 9 several times (e.g. 16) and take the average of the ADC results. Save this number as Count_{CALHI}.
11. Calculate m = actual_slope from equation 2, since all parameters are known.

    It is now possible to correct input channel data from any input channel using the same input range (i.e. -10 to +10 volts with a PGA gain = 1). Repeat steps 1-11 periodically to re-measure the calibration parameters (Count_{CALHI} and Count_{CALLO}) as required.

12. To prepare to measure channel 0 differentially, write to the Control Register (@Base + 00H) to setup the differential input channel 0 acquisition mode and PGA gain = 1 by writing 0000H. Note that "not used" bits are set to zero.
13. Delay to allow for input settling.
14. Execute ADC Convert Command (@Base + 10H).
15. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word. This data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. Calculate the calibrated value "Corrected_Count". This is the desired, corrected value for input channel 0.
16. Repeat steps 12-15 to re-measure channel zero's data as desired.

Calibration Programming Example 2

Assume that the input range is 0 to +1.25 volts. Channel 39 is connected single-ended, and corrected input channel data is desired. From Tables 3.4 and 3.5, several calibration parameters can be determined:

Gain = 8 (From Table 3.4)
$Volt_{CALHI}$ = 1.2250 volts (CAL2; From Table 3.4)
$Volt_{CALLO}$ = 0.6125 volts (CAL3; From Table 3.4)
Ideal_Volt_Span = 10.0000 volts (From Table 3.5)
Ideal_Zero = 0.0000 volts (From Table 3.5)

The calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) remain to be determined before uncorrected input channel data can be taken and corrected.

1. To prepare to measure $Count_{CALLO}$, write to the Control Register (@Base + 00H) to setup the CAL3 acquisition mode and PGA gain = 8 by writing 00D7H. Note that "not used" bits are set to zero.
2. Delay to allow for input settling.
3. Execute ADC Convert Command (@Base + 10H).
4. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
5. Repeat steps 3 and 4 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALLO}$.
6. To prepare to measure $Count_{CALHI}$, write to the Control Register (@Base + 00H) to setup the CAL2 acquisition mode and PGA gain = 8 by writing 00D6H. Note that "not used" bits are set to zero.
7. Delay to allow for input settling.
8. Execute ADC Convert Command (@Base + 10H).
9. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word.
10. Repeat steps 8 and 9 several times (e.g. 16) and take the average of the ADC results. Save this number as $Count_{CALHI}$.
11. Calculate m = actual_slope from equation 2, since all parameters are known.

    It is now possible to correct input channel data from any input channel using the same input range (i.e. 0 to +1.25 volts with a PGA gain = 8). Repeat steps 1-11 periodically to re-measure the calibration parameters ($Count_{CALHI}$ and $Count_{CALLO}$) as required.

12. To prepare to measure channel 39 single-ended, write to the Control Register (@Base + 00H) to setup the single-ended input channel 39 acquisition mode and PGA gain = 8 by writing 02D3H. Note that "not used" bits are set to zero.
13. Delay to allow for input settling.
14. Execute ADC Convert Command (@Base + 10H).
15. Execute Read ADC Data Command (@Base + 20H). Note that the 12-bit data is left-justified within the 16-bit word. This data represents the uncorrected "Count_Actual" term in equation 1. Since all parameters on the right hand side of equation 1 are known. Calculate the calibrated value "Corrected_Count". This is the desired, corrected value for input channel 39.
16. Repeat steps 12-15 to re-measure channel 39's data as desired.

Error checking should be performed on the "Corrected_Count" value to make sure that calculated values below 0 or above 4095 are restricted to those end points. Note that the software calibration cannot recover signals near the end points of each range which are clipped off due to the uncalibrated hardware (e.g. PGA and ADC).

The maximum corrected (i.e. calibrated) error is summarized in Table 3.6 as the worst case accuracy possible for each range. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25^{o}C. Typical accuracies are significantly better.

Table 3.6: Maximum Overall Calibrated Error @25°C

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Error ± LSB(% Span)
-5 to +5	1	-5 to +5	1.8 (0.044)
-2.5 to +2.5	2	"	2.1 (0.051)
-1.25 to +1.25	4	"	2.5 (0.061)
-0625 to +0.625	8	"	2.9 (0.071)
-10 to +10	1	-10 to +10	2.8 (0.069)
-5 to +5	2	"	1.8 (0.044)
-2.5 to +2.5	4	"	2.1 (0.051)
-1.25 to +1.25	8	"	2.5 (0.061)
0 to +10	1	0 to +10	3.2 (0.078)
0 to +5	2	"	2.2 (0.055)
0 to +2.5	4	"	3.1 (0.076)
0 to +1.25	8	"	5.1 (0.125)

4.0 THEORY OF OPERATION

This section describes the functionality of the IOS-320 circuitry. Refer to the IOS-320 block diagram on page 15 as you study the following paragraphs.

ANALOG INPUTS

The field I/O interface (via the carrier board) is through connector P2. Field analog inputs are non-isolated. This means that the field analog return and logic common have a direct electrical connection. Care must be taken to avoid ground loops and excessive common mode voltage (see Section 2 for connection recommendations). These can cause measurement error, and with extreme abuse, circuit damage.

Analog inputs and calibration voltages are selected via CMOS analog multiplexers (MUX's). A software programmable control register contains gain, acquisition mode (e.g. single-ended or differential) and channel selection information to control the multiplexers. Up to 40 single-ended inputs can be monitored, where each channel's +input is individually selected along with a single sense lead for all channels. Up to 20 differential inputs can be monitored, where each channel's + and - inputs are individually selected. Single-ended and differential channels cannot be mixed (i.e. they must all be single-ended or differentially wired). A Programmable Gain (Instrumentation) Amplifier (PGA) takes as input the selected channel's + and - inputs (or + and sense) and outputs a single-ended voltage proportional to it. The gain can be 1, 2, 4, or 8, and is selected through the control register.

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The output of the PGA feeds the Analog to Digital Converter (ADC). The A/D Converter is a state of the art, 12-bit, successive approximation converter with a built-in Sample and Hold (S/H) circuit. The S/H goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the A/D Converter has accurately digitized the input. Then it returns to the sample mode to acquire the next channel. Once a conversion has been started, the control register can be updated for the next channel. This allows the input to settle for the next channel while the previous channel is converting, which gives rise to the pipelined mode of operation (and maximum system throughput).

A miniature DIP switch on the board control the range selection for the A/D Converter (-5 to +5, -10 to +10, or 0 to +10 Volts) as detailed in Section 2. DIP switch selection should be made prior to powering the unit. Thus, all channels will use the same A/D Converter range. However, the analog input range can vary on an individual channel basis depending on the programmable gain selection.

The logic interface provides ±12 Volt supplies to the analog circuitry. The -10 to +10 and 0 to +10 Volt A/D Converter ranges will be clipped if these supplies are used, typically to ±9 Volt maximum inputs. The user has the option of providing ±15 Volt external supplies to fully utilize input ranges to ±10 Volts. These supplies are selected via hardware jumpers J1 and J2 as detailed in Section 2. Note that jumper selection should be made prior to powering the unit. Further, internal and external supplies should not be mixed (e.g. do not use +12 Volts with -15 Volts).

The board contains four precision voltage references and a ground (autozero) reference for use in calibration. These provide considerable flexibility in obtaining accurate calibration for any desired ADC range and gain combination, when compared to fixed hardware potentiometers for offset and gain calibration of the ADC and PGA. The calibration signals are selected (multiplexed into the PGA) like any other input channel.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IOS with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes
- Frequently Asked Questions (FAQ’s)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Physical Configuration................Single I/O Server Module
Length.................................. 4.030 in. (102.36 mm).
Width....................................1.930 in. (49.02 mm)
Board Thickness...................0.062 in. (1.59 mm)
Height…………………….......0.500 in. (12.7 mm)
Connectors:
P1 (IOS Logic Interface)... ......50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O)........................50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%)........................90mA Typical, 210mA Maximum
+12 Volts (±5%) from P1 or....15mA Typical, 25mA Maximum
+15 Volts (±5%) from P2.........(See Note 1)
-12 Volts (±5%) from P1 or.....13mA Typical, 25mA Maximum
-15 Volts (±5%) from P2..........(See Note 1)

Note:
1. The ±12 volt power supplies are normally supplied through P1 (logic interface connector). Optionally (jumper selectable on the IOS), the user may connect external ±15 volt supplies through the field I/O interface connector, P2.

ENVIRONMENTAL

Operating Temperature................ -40 to +85°C
Relative Humidity........................5-95% non-condensing
Storage Temperature...................-40 to +125°C
Non-Isolated.................................Logic and field commons have a direct electrical connection.
Radiated Field Immunity (RFI)......Complies with EN61000-4-3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less then ±0.25% of FS.
Conducted RF Immunity (CRFI)....Complies with EN61000-4-6 3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with error less then ±0.25% of FS.
Electromagnetic Interference Immunity (EMI)...........................No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Electrostatic Discharge Immunity (ESD)...........................Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) and Level 2 (4KV enclosure port contact discharge) and European Norm EN50082-1.
Surge Immunity...........................Not required for signal I/O per European Norm EN50082-1.
Electric Fast Transient Immunity EFT............................ Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.
Radiated Emissions................... Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

ANALOG INPUTS

Input Channels (Field Access).....40 Single-ended or 20 Differential Ended.
Input Signal Type.........................Voltage (Non-isolated).
Input Ranges (DIP switch selectable):
Bipolar -5 to +5 Volts............(See Note 2).
Bipolar -10 to +10 Volts.........(See Notes 2 & 3).
Unipolar 0 to +10 Volts..........(See Notes 2 & 3).
Programmable Gains...................x1, x2, x4, x8.

Input Overvoltage Protection.........±32 Volts with power applied, -35V to +55 Volts unpowered.
Input Resistance..........................1000 MΩ, Typical.
Input Bias Current.........................1nA Typical.
Common Mode Rejection Ratio.....80dB Typical, 60Hz.
CH-to-CH Rejection Ratio............80dB Typical, 60Hz.
A/D Resolution............................12-bits.
Data Format (left-justified)……….Straight Binary.
No Missing Codes.......................No Missing Codes 12-bit ADC.
A/D Integral Linearity Error..........±1/2 LSB Maximum.

System Accuracy (See Note 4).... The maximum corrected (i.e. calibrated) error is summarized in the following table as the worst case accuracy possible for each range. It is the sum of error components due to ADC quantization of the low and high calibration signals, PGA and ADC linearity error, and the absolute errors of the recommended calibration voltages at 25°C. Typical accuracies are significantly better.

Maximum Overall Calibrated Error @ 25°C

Input Range (Volts)	PGA Gain	ADC Range (Volts)	Max Error ±LSB (% Span)
-5 to +5	1	-5 to +5	1.8 (0.044)
-2.5 to +2.5	2	"	2.1 (0.051)
-1.25 to +1.25	4	"	2.5 (0.061)
-0625 to +0.625	8	"	2.9 (0.071)
-10 to +10	1	-10 to +10	2.8 (0.069)
-5 to +5	2	"	1.8 (0.044)
-2.5 to +2.5	4	"	2.1 (0.051)
-1.25 to +1.25	8	"	2.5 (0.061)
0 to +10	1	0 to +10	3.2 (0.078)
0 to +5	2	"	2.2 (0.055)
0 to +2.5	4	"	3.1 (0.076)
0 to +1.25	8	"	5.1 (0.125)

Settling Time (20V step)................5.2uS to 0.01% of FSR.
A/D Conversion Time...................4.5uS Maximum.
A/D Triggers.................................External and Software.
Maximum Conversion Rate...........200KHz Maximum.
Recommended Conversion Rate..100KHz Maximum.
Input Noise...................................0.2 LSB rms, Typical.
Temperature Coefficient...............See specification of calibration voltages.

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Programmable Calibration Voltages follow:

Calib. Signal	Ideal Value (Volts)	Maximum Tolerance @25°C (Volts)	Max Temperature Drift (ppm/°C)
Auto Zero	0.0000	±0.0002	0
CAL0	4.9000	±0.0005	±15
CAL1	2.4500	±0.0005	±20*
CAL2	1.2250	±0.0004	"
CAL3	0.6125	±0.0002	"

* Worst case temperature drift is the sum of the ±15 ppm/°C drift of the calibration voltage reference, plus the ±5 ppm/°C drift of the resistors in the voltage divider.

Notes:

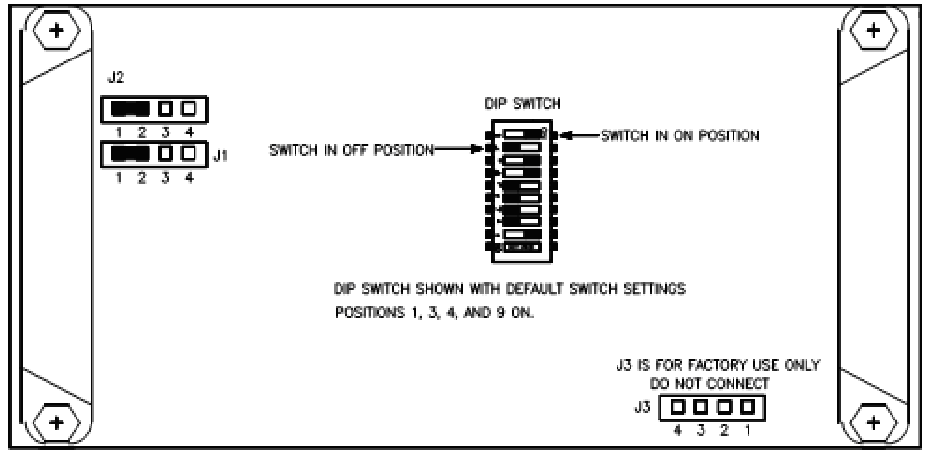
2. Range assumes the programmable gain is equal to one. Additional ranges are created with other gains. Divide the listed range by the programmable gain to determine the actual input range. Input signal ranges may actually fall short of reaching the specified endpoints due to hardware limitations. For example, if an input may reach zero volts or less, a bipolar input range should be selected.
3. These ranges can only be achieved with ±15 Volt external power supplies. The input ranges will be clipped if ±12 Volt supplies are used, typically to ±9 Volt maximum inputs.
4. Follow the input connection recommendations of Section 2, because input noise and non-ideal grounds can degrade overall system accuracy. For critical applications multiple input samples can be averaged to improve performance. Accuracy is specified for the software conversion command. Use of the external hardware trigger input with software polling may degrade accuracy. Accuracy versus temperature depends on the temperature coefficient of the calibration voltage.

Access Times (8MHz Clock):

ID PROM Read......................0 wait states (250ns cycle).
Control Register Read............0 wait states (250ns cycle).
Control Register Write............1 wait state (375ns cycle).
Conversion Request (Write)...1 wait states (375ns cycle).
Read ADC Data (Note 5)........2 wait states (500ns cycle).

Note:

5. The 2 wait states specified assume that the previous conversion has been completed, and that data is available to be read. If a conversion is in progress, the command will institute wait states until the data can be delivered. This could take up to 4.5uS (32 wait states), maximum.



COMPONENT SIDE VIEW

ANALOG INPUT RANGE SELECTION (DIP Switch Settings)

DESIRED ADC INPUT RANGE * (VDC)	REQUIRED INPUT SPAN (VOLTS)	REQUIRED INPUT TYPE	SWITCH SETTINGS ON	SWITCH SETTINGS OFF
-5 TO +5**	10	Bipolar	1,3,4,9	2,5,6,7,8
-10 TO +10***	20	Bipolar	2,5,6,9	1,3,4,7,8
0 TO +10***	10	Unipolar	1,3,4,7	2,5,6,8,9

* ASSUMING A GAIN OF 1

** THE BOARD IS SHIPPED WITH THE DEFAULT DIP SWITCH SETTING FOR THE -5 TO +5 VOLT ADC INPUT RANGE AS SHOWN IN THE ABOVE DIAGRAM.

*** THESE RANGES CAN ONLY BE ACHIEVED WITH +/-15 VOLT EXTERNAL POWER SUPPLIES. THE INPUT RANGES WILL BE CLIPPED IF +/-12 VOLT SUPPLIES ARE USED, TYPICALLY TO +/-8.5 VOLT MAXIMUM INPUTS.

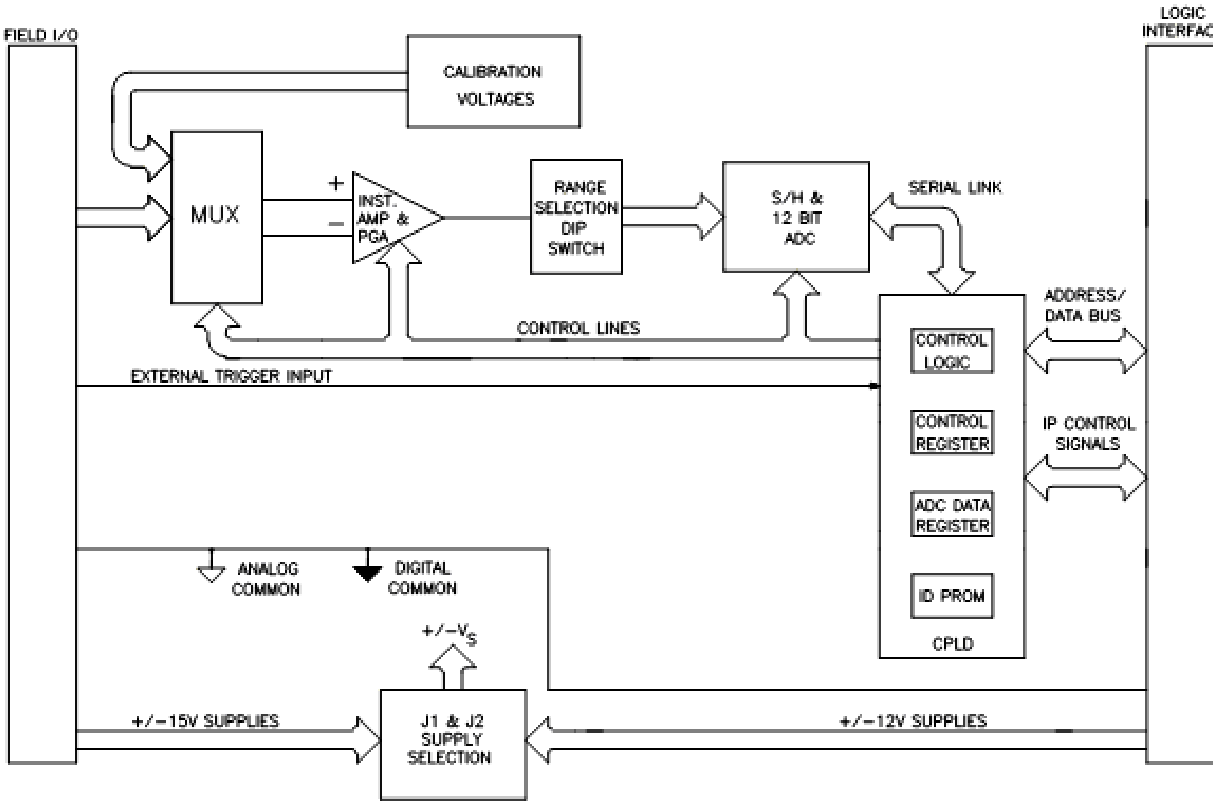
POWER SUPPLY SELECTIONS (PINS OF J1 AND J2)

POWER SUPPLY SELECTION *	J1 (1 & 2)	J1 (2 & 3)	J2 (1 & 2)	J2 (2 & 3)
+/-12 VOLT (INTERNAL)**	IN	OUT	IN	OUT
+/-15 VOLT (EXTERNAL)	OUT	IN	OUT	IN

* INTERNAL AND EXTERNAL SUPPLIES SHOULD NOT BE MIXED (E.G. DO NOT USE +12 VOLTS WITH -15 VOLTS).

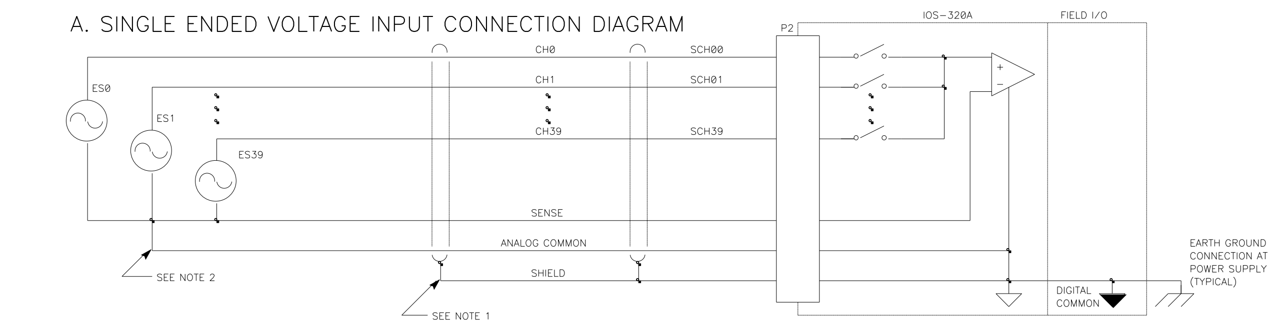
** THE BOARD IS SHIPPED WITH THE DEFAULT JUMPER SETTING FOR +/- 12 VOLT SUPPLIES AS SHOWN IN THE DIAGRAM ABOVE.

IOS-320 JUMPER LOCATIONS

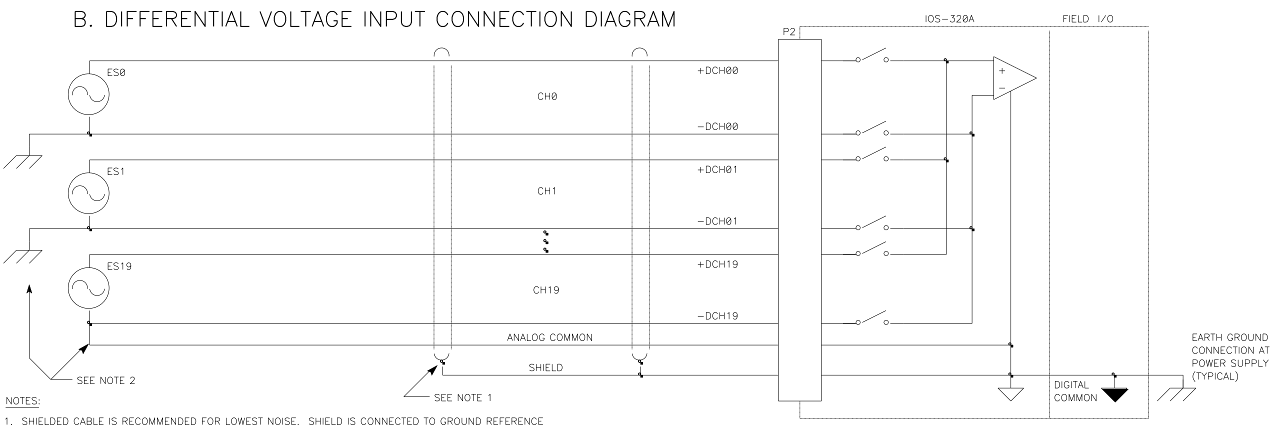


IOS–320 BLOCK DIAGRAM

A. SINGLE ENDED VOLTAGE INPUT CONNECTION DIAGRAM



B. DIFFERENTIAL VOLTAGE INPUT CONNECTION DIAGRAM



NOTES:

1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.
3. EXTERNAL SUPPLIES CAN BE USED BY JUMPERING, IT IS RECOMMENDED THAT THE SUPPLY COMMONS BE CONNECTED TO ANALOG COMMON.