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SSL4120 resonant power supply control IC with PFC

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Document information

Info	Content
Keywords	SSL4120, converter, LED driver, lighting, resonant, converter, PFC, burst mode
Abstract	The SSL4120 integrates a controller for Power Factor Correction (PFC) and a controller for a half-bridge resonant converter (HBC). It provides the drive function for the discrete MOSFET for the up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration. The resonant controller part is a high-voltage controller for a zero voltage switching LLC resonant converter. The resonant controller includes a high-voltage level shift circuit and several protection features such as overcurrent protection, open-loop protection, capacitive mode protection and a general-purpose latched protection input. In addition to the resonant controller, the SSL4120 also contains a Power Factor Correction (PFC) controller. The efficient PFC operation is achieved using quasi-resonant operation at high-power levels and quasi-resonant operation with valley skipping at lower power levels. Overcurrent protection, overvoltage protection and demagnetization sensing, ensures safe operation in all conditions. The proprietary high-voltage BCD Powerlogic process makes direct start-up possible from the rectified universal mains voltage in an efficient way. A second low voltage Silicon-On-Insulator (SOI) IC is used for accurate, high speed protection functions and control. The PFC and resonant controller combination in one IC makes the SSL4120 suitable for lighting, LED drivers, high-power and slim converter applications. This application note describes the SSL4120 functions used in the typical applications.

Table 1. Revision history

Rev	Date	Description
v.1	20121127	first release

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

1.1 Scope and setup

This application note discusses the SSL4120 functions for applications in general. Because the SSL4120 provides extensive functionality, many subjects are discussed.

Each section or paragraph in this application note can be read as a standalone explanation with few cross-references to other parts of the application note or the data sheet. This leads to some repetition between the application note and the SSL4120 data sheet. In most cases, typical values are given to enhance the readability.

- Section 1 "Introduction"
- Section 2 "SSL4120 highlights and features"
- Section 3 "Pin overview with functional description"

  An overview of the SSL4120 pins with a summary of the functionality.
- Section 4 "Application diagram and block diagrams"
- Section 5 "Supply functions"

Section 6, 7, 8, 9 and 10 describe the main functions of the SSL4120, providing an in-depth explanation of the issues relating to the subject. The functions are written from an application point of view.

- Section 6 "MOSFET drivers GATEPFC, GATELS and GATEHS"
- Section 7 "PFC functions"
- Section 8 "HBC functions"
- Section 9 "Burst mode operation"
- Section 10 "Protective functions"

  An overview of the protection functions of the SSL4120 with an extended explanation and related issues on the subject. These functions are described and seen from an applications point of view.
- Section 11 "Miscellaneous advice and tips"

  A collection of subjects related to PCB design and debugging are discussed, including proposals for the way of working.
- Section 12 "Application examples and topologies"

  This section contains examples of applications (circuit diagrams) and possible topologies.

Remark: All values provided throughout this document are typical values unless otherwise stated.

1.2 Related documents

Additional information and tools can be found in other SSL4120 documents such as:

- SSL4120 data sheet
- UM10575 demo board user manual

2. SSL4120 highlights and features

2.1 Resonant conversion

Today's market demands high-quality, reliable, small, lightweight and efficient power supplies.

In principle, the higher the operating frequency, the smaller and lighter the transformers, filter inductors and capacitors can be. On the other hand, the core, switching and winding losses of the transformer increase at higher frequencies and become dominant. This effect reduces the efficiency at a high frequency, which limits the minimum size of the transformer.

The corner frequency of the output filter usually determines the bandwidth of the control loop. A well-chosen corner frequency allows high operating frequencies to achieve a fast dynamic response.

Pulse-Width Modulated (PWM) power converters, such as flyback, up and down converters, are widely used in low and medium power applications. A disadvantage of these converters is that the PWM rectangular voltage and current waveforms cause turn-on and turn-off losses that limit the operating frequency. The rectangular waveforms also generate broadband electromagnetic energy that can produce ElectroMagnetic Interference (EMI).

A resonant DC-to-DC converter produces sinusoidal waveforms and reduces the switching losses, which provide the possibility of operation at higher frequencies.

Recent environmental considerations have resulted in a need for high efficiency performance at low loads. Burst mode operation of the resonant converter can provide the improved efficiency when the converter is required to remain active. The burst mode operation can also provide a higher range of a current controlled output.

Why resonant conversion?

- high power
- high-efficiency
- EMI friendly
- compact

2.2 Power factor correction conversion

Most switch mode power supplies result in a non-linear impedance (load characteristic) to the mains input. Current taken from the mains supply occurs only at the highest voltage peaks and is stored in a large capacitor. The energy is taken from this capacitor storage, in accordance with the switch mode power supply operation characteristics.

Government regulations dictate special requirements for the load characteristics of certain applications. Two main requirements can be distinguished:

- Mains harmonics requirements EN61000-3-2 Class C
- Power factor (real power/apparent power)

The requirements work towards a more resistive characteristic of the mains load and a low total harmonic distortion (THD) for lighting devices.

Measures are required regarding the input circuit of the power supply to fulfill these requirements. Passive (often a series coil) or active (often a boost converter) circuits can be used to modify the mains load characteristics.

An additional market requirement for the added mains input circuit is that it works with a good efficiency and have a low cost.

Using a boost converter to meet these requirements provides the benefit of a fixed DC input voltage when combined with a resonant converter. The fixed input voltage makes design of the resonant converter easier, especially for wide mains input voltage range applications. In addition, the fixed input voltage makes it possible to obtain a higher efficiency.

2.3 SSL4120 resonant power supply control IC with PFC

The SSL4120 integrates two controllers, one for Power Factor Correction (PFC) and one for a half-bridge resonant converter (HBC). It provides the drive function for the discrete MOSFET for the up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

The resonant controller part is a high-voltage controller for a zero voltage switching LLC resonant converter.

The resonant controller includes a high-voltage level-shift circuit and several protection features such as overcurrent protection, open-loop protection, capacitive mode protection and a general-purpose latched protection input.

In addition to the resonant controller, the SSL4120 also contains a Power Factor Correction (PFC) controller. Especially developed for Lighting applications that require low harmonic distortion of the mains current. Efficient PFC operation is provided using functions such as:

- quasi-resonant operation at high-power levels
- quasi-resonant operation with valley skipping at lower power levels

In addition, the IC includes overcurrent protection, overvoltage protection and demagnetization sensing ensures safe operation in all conditions.

The proprietary high-voltage BCD Powerlogic process makes direct start-up possible from the rectified universal mains voltage in an efficient way. A second internal low-voltage SOI die is used for accurate, high-speed protection functions and control.

The SSL4120 controlled PFC and resonant converter topology is flexible and enables a broad range of applications for wide input AC mains voltages (85 V to 305 V). The combination of PFC and resonant controller in one IC makes the SSL4120 suitable for compact power supplies with a high-level of integration and functionality.

2.4 Features

2.4.1 General features

- Integrated power factor controller and resonant controller
- Universal mains supply operation
- High level of integration, resulting in a low external component count and a cost effective design
- Enable input. Also allows enabling of PFC only
- On-chip high-voltage start-up source
- Standalone operation or IC supply from external DC supply

2.4.2 Power factor controller features

- Boundary mode operation with on-time control for highest efficiency
- Valley/zero voltage switching for minimum switching losses
- Frequency limitation to reduce switching losses
- Accurate boost voltage regulation
- Burst mode switching with soft-start and soft-stop

2.4.3 Resonant half-bridge controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap timing
- Burst mode switching

2.4.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output overvoltage protection or external temperature protection
- Protection timer for time-out and restart
- OverTemperature Protection (OTP)
- Soft-start and soft-restart for both converters
- Undervoltage protection for mains (brownout), boost, IC supply and output voltage
- Overcurrent regulation and protection for both converters
- Accurate overvoltage protection for boost voltage
- Capacitive mode protection for resonant converter

2.5 Protection features

The SSL4120 provides several protection functions that combine detection with a response to solve the problem. Regulating the frequency, because of overpower or bad half-bridge switching, can solve the problem or keep the IC operating safely until it is stopped and restarted (timer function).

2.6 Typical applications

- Lighting
- LED drivers
- High-power converters
- Slim converters

3. Pin overview with functional description

Table 2. Pinning overview

Pin	Name	Functional description
1	COMPPFC	Frequency compensation for the PFC control loop. Externally connected filter with typical values: 150 nF (33 kΩ + 470 nF) and connected to V_{mains} using a capacitor to modulate the PFC on-time.
2	SNSMAINS	Sense input for V_{mains}. Externally connected to resistive divided V_{mains}. This pin has four functions: • V_{mains} enable level: $V_{start(SNSMAINS)}$ = 1.15 V • V_{mains} stop level (brownout): $V_{stop(SNSMAINS)}$ = 0.9 V • V_{mains} compensation for the PFC control-loop gain bandwidth • Fast latch reset: $V_{rst(SNSMAINS)}$ = 0.75 V The mains enable and mains stop level enable and disable the PFC. Enabling and disabling of the resonant controller is based on $V_{SNSBOOST}$. $V_{SNSMAINS}$ must be an averaged DC value, representing V_{mains}. Do not use the pin for sensing the V_{mains} phase. Open pin detection is implemented as an internal current source (33 nA).
3	SNSAUXPFC	Sense input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. It is −100 mV level with a time-out of 50 μs. Connect the T_{PCF} auxiliary winding using an impedance to the pin to prevent damage of the input (for example, from lightning surges). Recommended is a 5.1 kΩ series resistor. Open pin detection is implemented as an internal current source (33 nA).
4	SNSCURPFC	Current sense input for PFC. This input is used to limit the maximum peak-current in the PFC core. The PFCSENSE is a cycle-by-cycle protection. The PFC MOSFET is switched off when $V_{SNSCURPFC}$ reaches 0.5 V. The internal logic controls a 60 μA internal current source connected to the pin. This current source is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise in burst mode. The pin is also used to enable the PFC. The PFC only starts when the internal current source (60 μA) is able to charge the soft-start capacitor C_{SSPFC} to 0.5 V. A minimum soft-start resistor of 12 kΩ is required to guarantee enabling of the PFC. C_{SSPFC} provides the soft-start and soft-stop timing in combination with its parallel resistor R_{SSPFC}.
5	SNSOUT	Input for indirectly sensing the output voltage of the resonant converter. It is normally connected to an T_{HBC} auxiliary winding and is also an input for HBC or PFC + HBC burst mode. This pin has four functions related to internal comparators: • OVP: V_{SNSOUT} > 3.5 V, latched • UVP: V_{SNSOUT} < 2.3 V, protection timer • Hold HBC: V_{SNSOUT} < 1.0 V, stop switching HBC (burst mode) • Hold HBC and PFC: V_{SNSOUT} < 0.4 V, stop switching HBC and PFC (burst mode) The pin also contains an internal current source of 100 μA. Initially, the current source generates up to 1.5 V across an external impedance > 20 kΩ to avoid unintended burst mode operation.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
6	SUPIC	IC voltage supply input and output of the internal HV start-up source. All internal circuits are directly or indirectly (via SUPREG) supplied from this pin, except for the high-voltage circuit. The buffer capacitor on SUPIC can be charged in several ways: • Internal High-Voltage (HV) start-up source • T_{HBC} auxiliary winding supply or capacitive supply from switching half-bridge node • External DC supply, for example a standby supply The IC enables operation when V_{SUPIC} reaches the 22 V (for HV-start) or 17 V (for external supply) start level. It stops operation under 15 V and a shutdown reset is activated at 7 V.
7	GATEPFC	Gate driver output for PFC MOSFET.
8	PGND	Power ground. Reference (ground) for HBC low-side and PFC driver.
9	SUPREG	Output of the internal regulator: 10.9 V. Internal IC functions such as the MOSFET drivers use this supply. It can also be used to supply an external circuit. SUPREG can provide a minimum of 40 mA. SUPREG becomes operational after V_{SUPIC} has reached its start level. The IC starts full operation when V_{SUPREG} has reached 10.7 V. SUPREG UVP: If V_{SUPREG} drops under 10.3 V after start, the IC stops operating and the current from SUPIC is limited to 5.4 mA, to allow recovery.
10	GATELS	Gate driver output for low side MOSFET of HBC.
11	n.c.	Not connected, high-voltage spacer.
12	SUPHV	High-voltage supply input for internal HV start-up source. In a standalone power supply application, this pin is connected to the boost voltage V_{boost}. SUPIC and SUPREG are charged with a constant current by the internal start-up source. SUPHV operates at a voltage above 25 V. Initially the charging current is low (1.1 mA). When V_{SUPIC} exceeds the short circuit protection level of 0.65 V, the generated current increases to 5.1 mA. When V_{SUPIC} reaches 22 V a start operation is initiated and the source is switched off. During start operation, an auxiliary supply takes over the supply of SUPIC. If the takeover is not successful, the SUPHV source is reactivated and a restart is made (V_{SUPIC} under 15 V).
13	GATEHS	Gate driver output for high-side MOSFET of HBC.
14	SUPHS	High-side driver supply connected to an external bootstrap capacitor between HB and SUPHS. The supply is obtained using an external diode between SUPREG and SUPHS.
15	HB	Reference for the high-side driver GATEHS. Pin HB is an input for the internal half-bridge slope detection circuit for adaptive non-overlap regulation and Capacitive mode protection. It is externally connected to a half-bridge node between the MOSFETs of HBC.
16	n.c.	Not connected, high-voltage spacer.
17	SNSCURHBC	Sense input for the momentary current of the HBC. If the voltage level representing the primary current is too high, internal comparators increase regulation to a $f_{sw(HBC)}$ frequency ($V_{SNSCURHBC} = \pm0.5$ V) or protect ($V_{SNSCURHBC} = \pm1$ V) by switching immediately to $f_{sw(soft\text{-}start)HBC}$. The additional current from SNSCURHBC can compensate protection level variations due to V_{boost} variations. This current leads to a voltage offset across the external series resistor $R_{SNSCURHBC}$. The current measurement resistor R_{CURHBC} and the series resistance. $R_{SNSCURHBC}$ (1 kΩ typ), provides the total series resistance.
18	SGND	Signal ground, reference for IC.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
19	CFMIN	HBC oscillator pin. The value of the external capacitor determines the minimum switching frequency of the HBC. In combination with R_{RFMAX}, it sets the operating frequency range. A triangular voltage waveform is generated C_{CFMIN} ($V_{l(CFMIN)}$ = 1 V and $V_{u(CFMIN)}$ = 3 V) to facilitate switching timing. A fixed minimum charge/discharging current of 150 μA determines the minimum frequency. During special conditions, the charge/discharging current is reduced to 30 μA to slow down the charging temporarily. An internal function limits the operating frequency to 670 kHz.
20	RFMAX	HBC oscillator frequency pin. The value of the resistor R_{RFMAX} connected between this pin and ground, determines the frequency range. Both the minimum and maximum frequencies of the HBC are preset. C_{CFMIN} sets the minimum frequency. The absolute maximum frequency is internally limited to 670 kHz. In addition to the 150 μA fixed current on the CFMIN pin, V_{RFMAX} and the connected resistor value, controls the variable part of C_{CFMIN} charging/discharging current. V_{RFMAX} can vary between 0 V (minimum frequency) and 2.5 V (maximum frequency). SNSFB and the SSHBC/EN function drive V_{RFMAX} (HBC switching frequency). The protection timer is started when the voltage level is above 1.88 V. An error is assumed when the HBC is operating at high frequency for a longer time.
21	SNSFB	Sense input for HBC output regulation feedback by voltage. Sinking a current from SNSFB creates the feedback regulation voltage on the SNSFB pin. V_{SNSFB} is produced when this current is passed through a 1.5 kΩ internal resistor which is internally connected to 8.4 V. The regulation voltage range is from 4.1 V to 6.4 V. The SNSFB pin controls the maximum and minimum frequencies. The SNSFB range is limited to 65 % of the maximum frequency preset using R_{RFMAX}. The provision of open-loop detection activates the protection timer when V_{SNSFB} exceeds 7.7 V.

Table 2. Pinning overview *…continued*

Pin	Name	Functional description
22	SSHBC/EN	Combined soft-start/protection frequency control of HBC and IC enable input (PFC or PFC + HBC). Externally connected to a soft-start capacitor and an enable pull-down function. This pin has three functions: • Enable PFC ($V_{SSHBC/EN}$ > 1 V) and PFC + HBC ($V_{SSHBC/EN}$ > 2 V) • HBC frequency sweep during soft-start from 3.2 V to 8 V • HBC frequency control during protection between 8 V to 3.2 V Seven internal current sources operate the frequency control, depending on which one of the following actions is required: • Soft-start and HB OVP: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA) • CMR: high/low discharge (1800 μA/440 μA) • General: bias discharge (5 μA)
23	RCPROT	Timer presetting for time-out and restart. The values of an externally connected resistor R_{RCPROT} and capacitor C_{RCPORT} determine the timing. A 100 μA charge current activates the timer during certain protection events: • OCR using the SNSCURHBC pin • HFP using the RFMAX pin • OLP using the SNSFB pin • UVP using the SNSOUT pin When the level of 4 V is reached, the protection is activated. R_{RCPROT} discharges C_{RCPROT} and at a level of 0.5 V, a restart is made. If an SCP (SNSBOOST) occurs, C_{RCPROT} is quickly charged by 2.2 mA. After it reaches the 4 V level, C_{RCPROT} is discharged after which a new start is initiated.
24	SNSBOOST	Sense input for boost voltage regulation (output voltage of the PFC stage). It is externally connected to a resistive divided boost voltage V_{boost}. This pin has four functions: • SNSBOOST pin short-circuit protection: $V_{SCP(SNSBOOST)} \leq 0.4$ V • Regulation of PFC output voltage: $V_{reg(SNSBOOST)} = 2.5$ V • PFC soft-OVP (cycle-by-cycle): $V_{OVP(SNSBOOST)} \geq 2.63$ V • Start function: HBC enable: $V_{start(SNSBOOST)} = 2.3$ V • Brownout function: HBC disable: $V_{UVP(SNSBOOST)} = 1.6$ V

4. Application diagram and block diagrams

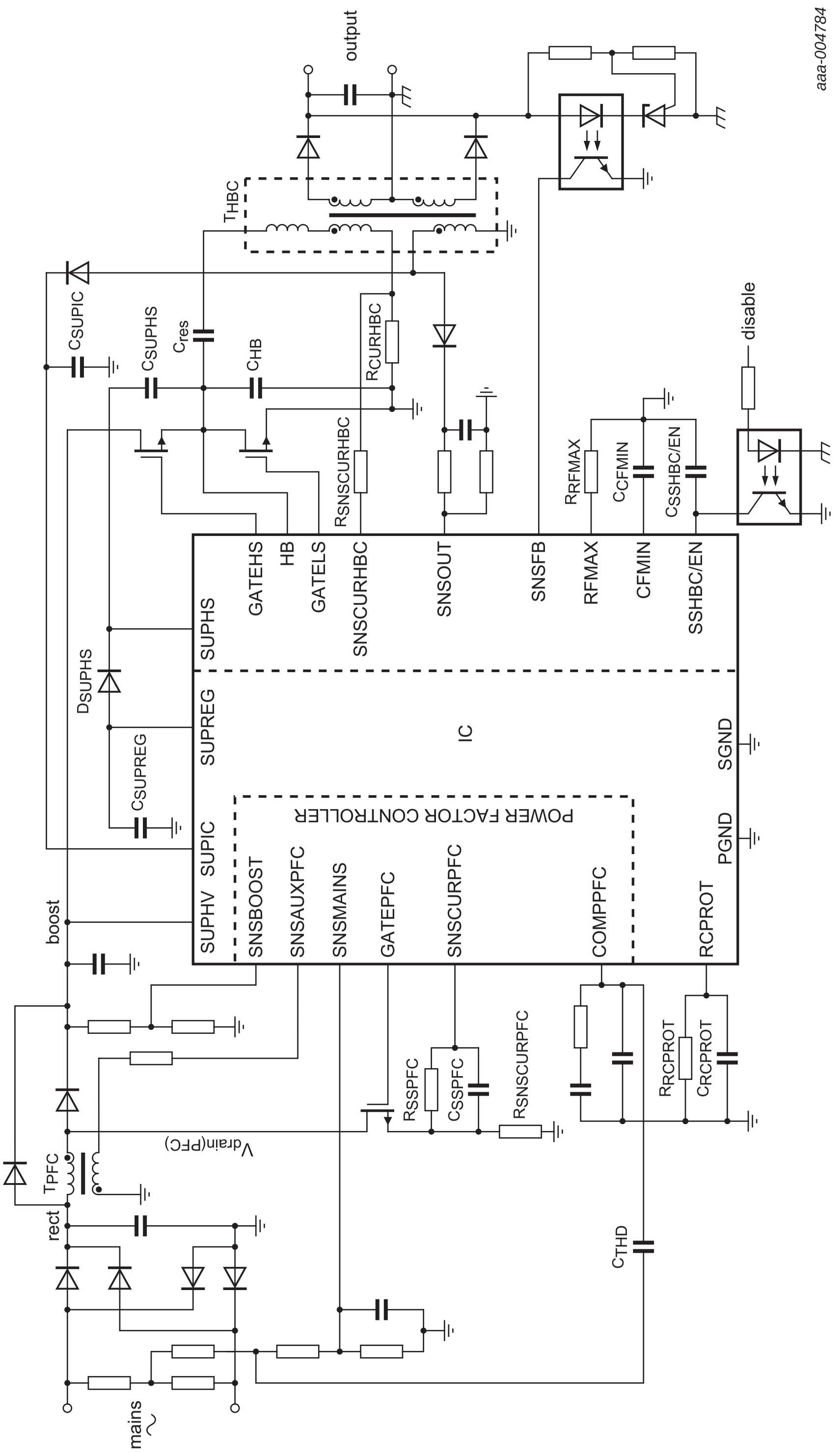

Fig 1. SSL4120 basic application diagram

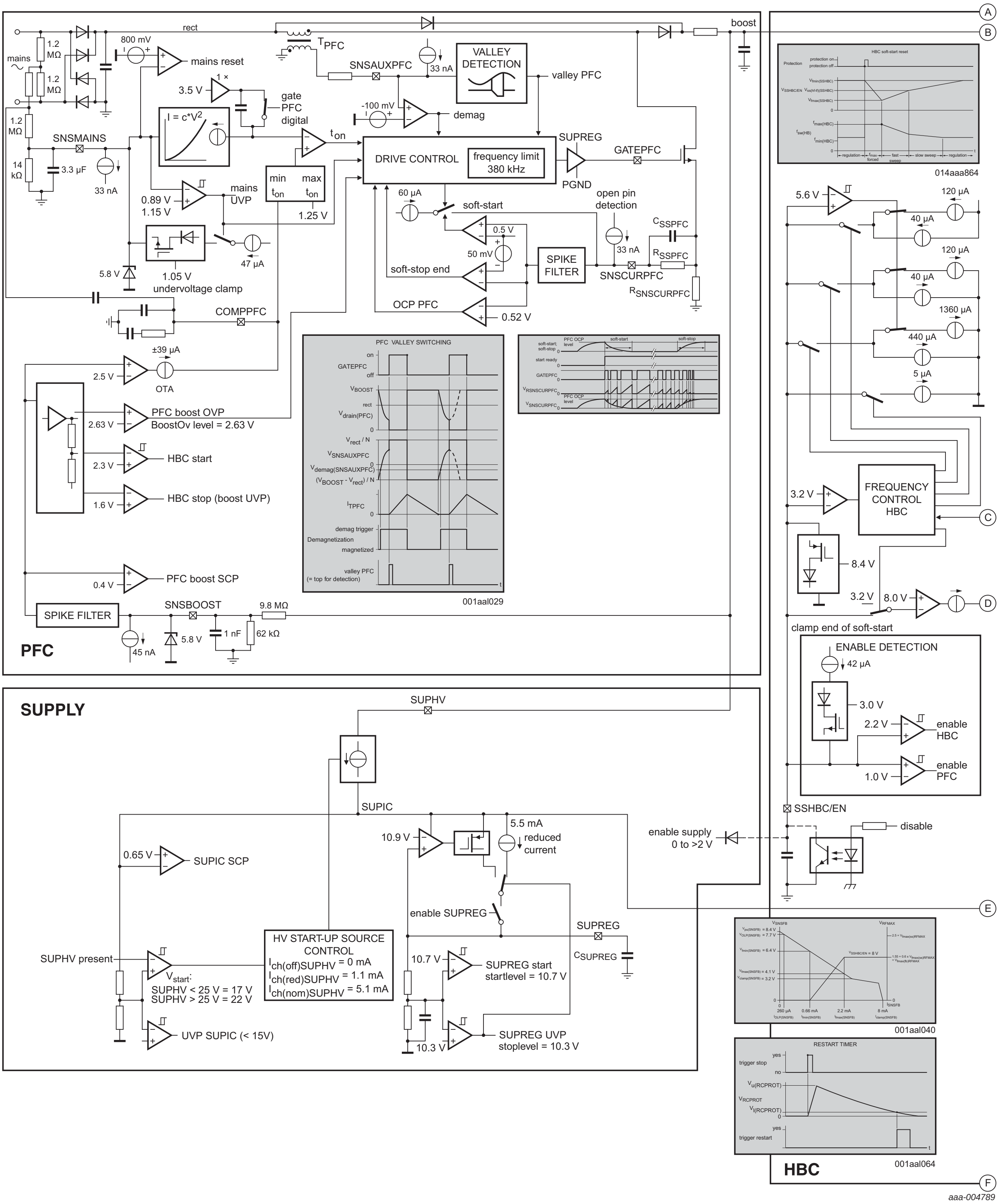

Fig 2. SSL4120 block diagram (part 1)

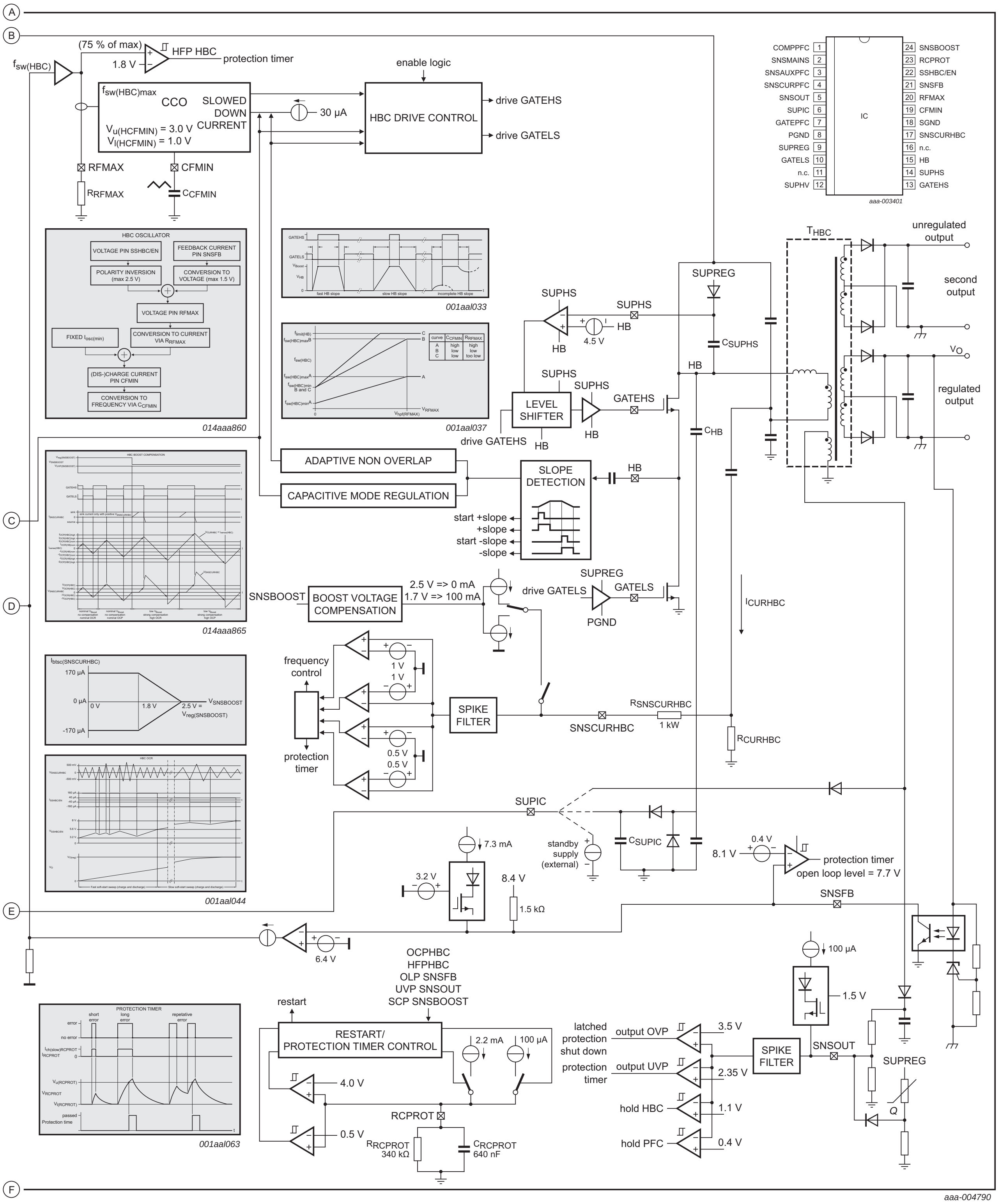

Fig 3. SSL4120 block diagram (part 2)

5. Supply functions

5.1 Basic supply system overview

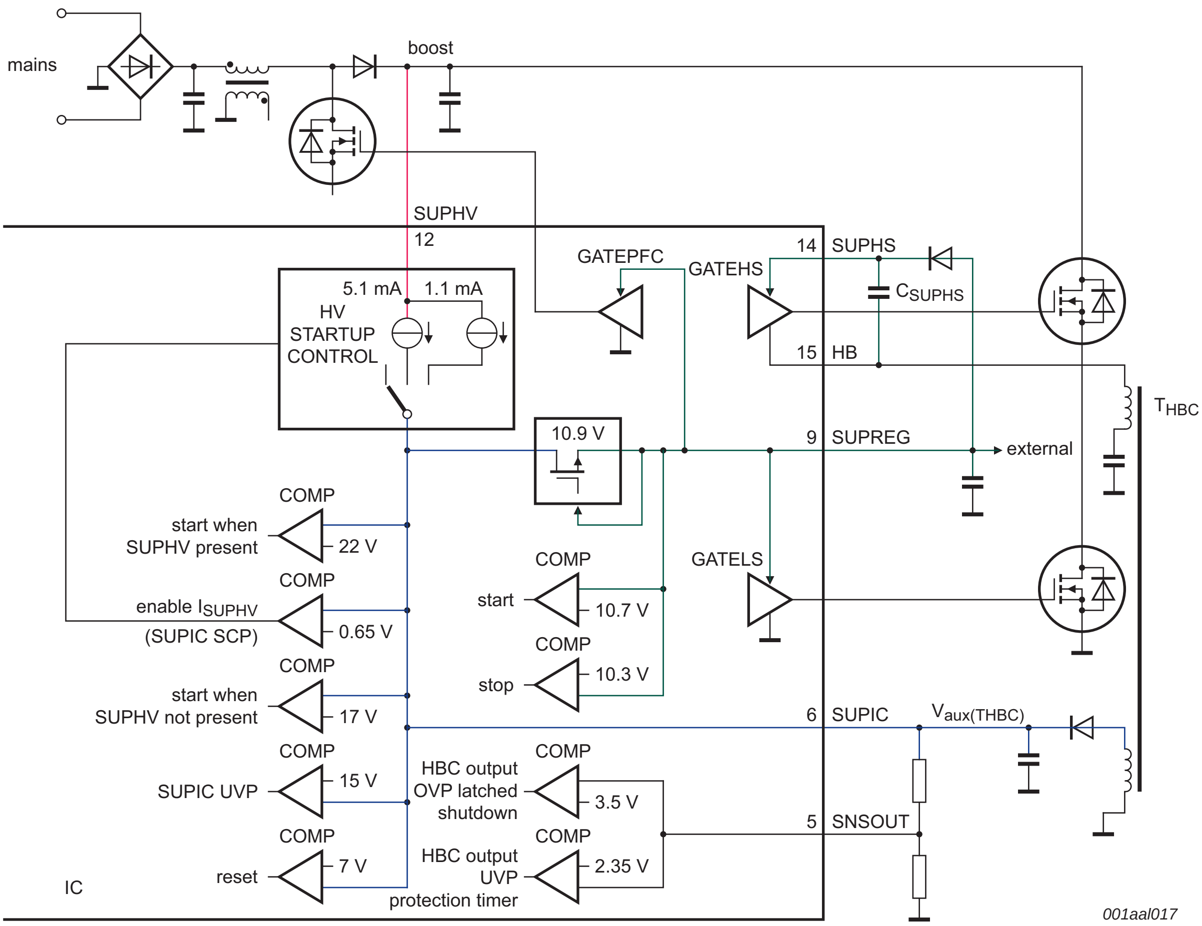

Fig 4. Basic overview internal IC supplies

5.1.1 SSL4120 supplies

The main supply for the SSL4120 is SUPIC.

SUPHV can be used to charge SUPIC for starting the supply. During operation, a supply voltage is applied to SUPIC and the SUPHV source is switched off. The SUPHV source is only switched on again at a new start-up.

The internal regulator SUPREG generates a fixed voltage of 10.9 V to supply the internal MOSFET drivers: GATEPFC, GATELS and GATEHS. A bootstrap function with an external diode is used to make supply SUPHS.This is used to supply GATEHS.

SUPIC and SUPREG also supply other internal SSL4120 circuits.

5.1.2 Supply monitoring and protection

The supply voltages are internally monitored to determine when to initiate certain actions, such as starting, stopping or protection.

In several applications, V_{SUPIC} can also be used to monitor the HBC output voltage by protection input SNSOUT. The applications include, for example, using an auxiliary winding construction T_{HBC} as shown in Figure 4.

5.2 Low voltage IC supply (SUPIC pin)

SUPIC is the main IC supply. Except for the SUPHV circuit, all internal circuits are either directly or indirectly supplied from this pin.

5.2.1 SUPIC start-up

Connect SUPIC to an external buffer capacitor. This buffer capacitor can be charged in several ways:

- Internal high-voltage (HV) start-up source
- Auxiliary supply, for example, from a winding on T_{HBC}
- External DC supply, for example, from a standby supply

The IC starts operating when V_{SUPIC} and V_{SUPREG} reach the start level. The start level value of V_{SUPIC} depends on the condition of the SUPHV pin.

5.2.1.1 $V_{SUPHV} \geq 25$ V

$V_{SUPHV} \geq 25$ V is typically in a standalone application where the HV start-up source initially charges SUPIC. The V_{SUPIC} start level is 22 V. The large difference between the start and stop levels (15 V) allows sufficient discharge time for capacitor C_{SUPIC} to take over the IC supply by the T_{HBC} auxiliary supply.

5.2.1.2 SUPHV not connected/used

SUPHV not connected or used is the case when the SSL4120 is supplied from an external DC supply. The V_{SUPIC} start level is now 17 V. During start-up and operation, the IC is continuously supplied by the external DC supply. Do not connect the SUPHV pin in this kind of application.

5.2.2 SUPIC stop, UVP and SCP

The IC stops operating when V_{SUPIC} drops under 15 V which is the UnderVoltage Protection (UVP) of SUPIC. While in the process of stopping, the HBC continues until the low-side MOSFET is active, before stopping the PFC and HBC operation.

V_{SUPIC} has a low-level detection at 0.65 V to detect a short circuit to ground. This level also controls the current source from the SUPHV pin.

5.2.3 SUPIC current consumption

The SUPIC current consumption depends on the state of the SSL4120.

- Disabled IC state:

  When the IC is disabled via the SSHBC/EN pin, the current consumption is low at 250 μA.
- SUPIC charge, SUPREG charge, thermal hold, restart and shutdown state:

  Only a small part of the IC is active during the charging of SUPIC and SUPREG before start-up, a restart sequence or shutdown after activation of protection. The PFC and HBC are disabled. The current consumption from SUPIC in these states is low at 400 μA.
- Boost charge state:

  PFC is switching and HBC is still off. The high-voltage start-up source current is large enough to supply SUPIC. The current consumption is therefore, under the maximum current (5.1 mA) that SUPHV can deliver.
- Operating supply state:

  Both the PFC and HBC are switching. The current consumption is larger. The MOSFET drivers are dominant in the current consumption (see Section 5.5.5), especially during HBC soft-start, when the switching frequency is high and during normal operation. Initially, the stored energy in the SUPIC capacitor delivers the SUPIC current. After a short time, the supply source on SUPIC takes over.

5.3 SUPIC using the T_{HBC} auxiliary winding supply

5.3.1 Start-up by V_{SUPHV}

In a standalone power supply application, the IC can be started using a high-voltage source (rectified mains voltage) when the SUPHV high-voltage input is connected to V_{boost} (PFC output voltage).

The internal HV start-up source, which delivers a constant current from SUPHV to SUPIC, charges the SUPIC and SUPREG. SUPHV is operational at a voltage > 25 V.

When V_{SUPIC} is under the short-circuit protection level (0.65 V), the current from SUPHV is low (1.1 mA). This feature limits the dissipation in the HV start-up source when SUPIC is shorted to ground.

During normal conditions, V_{SUPIC} quickly exceeds the protection level and the HV start-up source switches to normal current (5.1 mA). The HV start-up source switches off when V_{SUPIC} has reached the start level (22 V). The current consumption from SUPHV is low (7 μA) when switched off.

When V_{SUPIC} has reached the start level (22 V), SUPREG is charged. When V_{SUPREG} reaches the level of 10.7 V, it enables operation of HBC and PFC.

The T_{HBC} auxiliary winding supply must take over the supply of SUPIC before it discharges to the SUPIC undervoltage stop level (15 V).

5.3.2 Block diagram for SUPIC start-up

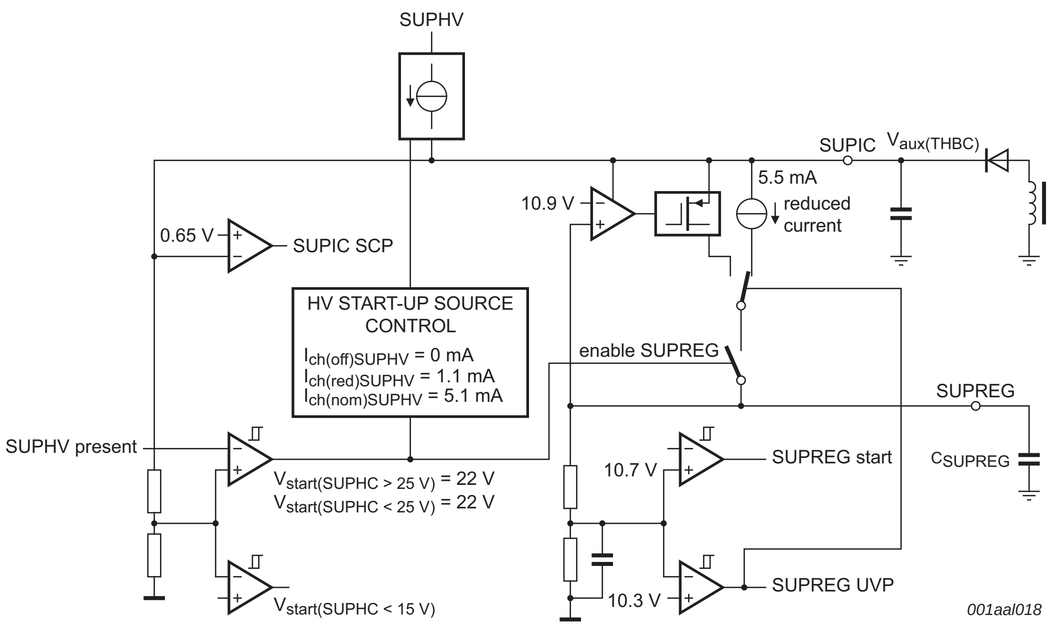

Fig 5. Block diagram: SUPIC and SUPREG start-up with SUPHV and T_{HBC} auxiliary winding supply

5.3.3 Auxiliary winding on the HBC transformer

A T_{HBC} auxiliary winding can be used to obtain a supply voltage for SUPIC during operation. As SUPIC has a wide operational voltage range (15 V to 38 V), it is not a critical parameter for constant voltage outputs.

But:

- V_{SUPIC} must be low for low-power consumption.
- The T_{HBC} auxiliary winding supply must be an accurate representation of V_O to use the auxiliary winding voltage for the IC supply and HBC output voltage measurement (using SNSOUT). Physically place the T_{HBC} auxiliary winding on the secondary output side to ensure a good coupling.
- When mains insulation is included in T_{HBC}, it can affect the auxiliary winding construction. Triple insulated wire is needed when the T_{HBC} auxiliary winding is placed on the transformer construction secondary area.

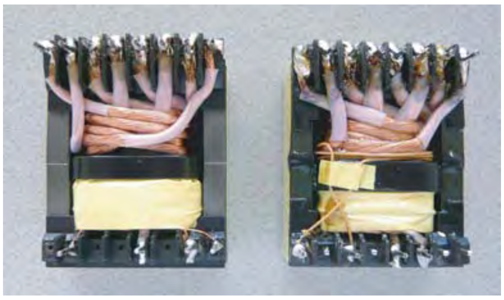

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Fig 6. T_{HBC} auxiliary winding on primary side (left) and secondary side (right)

5.3.3.1 SUPIC and SNSOUT using T_{HBC} auxiliary winding

The SNSOUT input provides a combination of four functions:

- HBC output OVP: V_{SNSOUT} > 3.5 V, latched
- HBC output UOP: V_{SNSOUT} < 2.35 V, protection timer
- Hold HBC: V_{SNSOUT} < 1.1 V, stop switching HBC (burst mode)
- Hold HBC and PFC: V_{SNSOUT} < 0.4 V, stop switching HBC and PFC (for burst mode)

Remark: A more detailed explanation of the SNSOUT functions can be found in Section 10.3.1 and Section 10.3.2.

Often, a circuit is used which combines SUPIC and output voltage monitoring using SNSOUT, with one T_{HBC} auxiliary winding. But an independent construction for SUPIC and SNSOUT is also possible. This construction can be used in a situation where SUPIC is supplied by a separate standby supply and the T_{HBC} auxiliary winding is used only for output voltage sensing. It is also possible not to use SNSOUT for output sensing but as a general-purpose protection input. See Section 10.3.3 for more information.

In a combined SUPIC and SNSOUT function using one T_{HBC} auxiliary winding, some issues must be addressed to get a good output voltage representation for SNSOUT measurement.

The advantage of a good coupling/representation of the T_{HBC} auxiliary winding with the output windings is also that a stable auxiliary voltage is obtained for SUPIC. A low SUPIC voltage value can be designed more easily for lowest power consumption.

5.3.3.2 Auxiliary supply voltage variations by output current

At high (peak) current loads, the voltage drop across the series components of the HBC output stage (resistance and diodes) is compensated using regulation. The compensation results in a larger voltage on the windings at higher output currents because of the higher currents which cause an increased voltage drop across the series components. The T_{HBC} auxiliary winding supply shows that this variation is caused due to the HBC output.

5.3.3.3 Voltage variations by auxiliary winding position: primary side component

Due to a less optimal position of the auxiliary winding, V_{SNSOUT} and/or SUPIC can contain a certain amount of undesired primary voltage component. This component can seriously endanger the feasibility of the SNSOUT sensing function.

The coupling of the auxiliary winding with the primary winding must be as small as possible to avoid a primary voltage component on the auxiliary voltage. Place the auxiliary winding on the secondary winding/windings and as physically remote as possible from the primary winding. The differences in results are shown in Figure 7 using comparison of secondary side position.

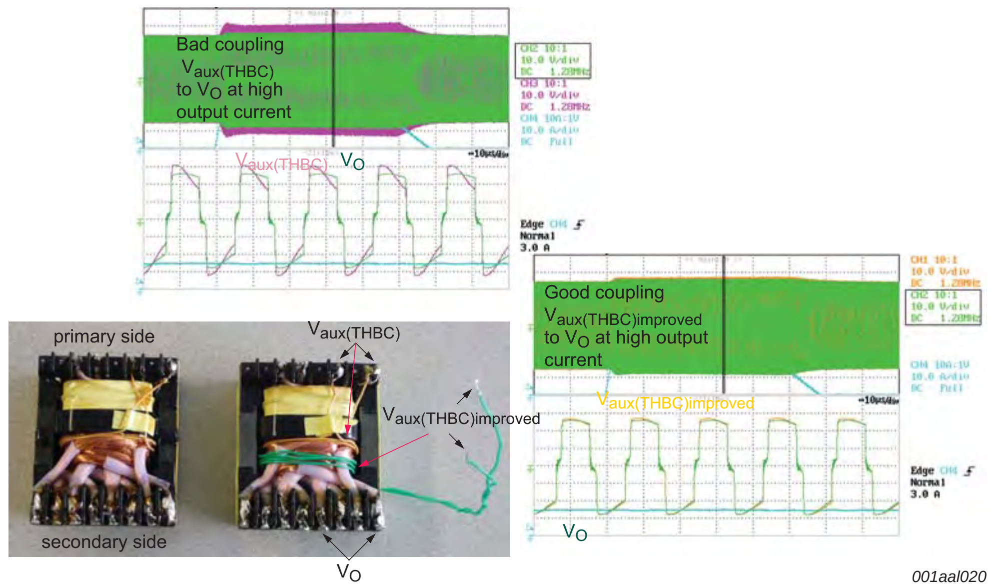


Fig 7. Position the T_{HBC} auxiliary winding for good output coupling

5.3.4 Difference between HB output UVP on SNSOUT and HBC OCP/OCR on SNSCURHBC

In a system that uses output voltage sensing with the SNSOUT function, there can be an overlap in functionality in an output overpower or output short-circuit situation. In such a situation, often both the SNSOUT HBC output UVP and the HBC OCP/OCR on SNSCURHBC, activate the protection timer.

There are basic differences between both functions:

- SNSOUT monitors (indirectly) the HBC output voltage or another external protection circuit (such as NTC temperature measurement)
- HBC OCP/OCR monitors the power in the HBC by sensing the primary current in detail

SNSOUT is a more general usable protection input while SNSCURHBC is designed for HBC operation. In addition, SNSOUT also offers three other functions:

- HBC output OVP (latched)
- hold HBC (for burst mode)

- hold HBC + PFC (for burst mode)

5.4 SUPIC supply by external voltage

5.4.1 Start-up

When the SSL4120 is supplied by an external DC supply, the SUPHV pin can remain unconnected. The V_{SUPIC} start level is now 17 V.

When V_{SUPIC} exceeds 17 V, the internal regulator is activated and charges SUPREG.

At $V_{SUPREG} \geq 10.7$ V, GATELS is switched on for the bootstrap function to charge SUPHS. And at the same time the PFC operation is internally enabled. When all enable conditions are met, the SSL4120 starts the PFC function. When V_{boost} reaches approximately 90 % ($V_{SNSBOOST} \geq 2.3$ V) of its nominal value, the HBC starts.

5.4.2 Stop

Operation of the SSL4120 can be stopped by switching off the external source for SUPIC. When V_{SUPIC} drops under 15 V, operation is stopped.

When shut down because of a triggered protection, the state is reset by internal logic when V_{SUPIC} drops under 7 V.

5.5 SUPREG

SUPIC has a wide voltage range for easy application. SUPIC cannot be directly used to supply the internal MOSFET drivers because of this feature, as the allowed gate voltage of many external MOSFETs would be exceeded.

The SSL4120 contains an integrated series stabilizer to avoid this issue and to create a few other benefits. The series stabilizer generates an accurate regulated voltage on C_{SUPREG}.

This stabilized V_{SUPREG} is used for:

- Supply of internal PFC driver
- Supply of internal low-side HBC driver
- Supply of internal high-side driver via external components
- Reference voltage for optional external circuits

The series stabilizer for SUPREG is enabled after SUPIC has been charged. In this way, optional external circuitry at SUPREG does not consume from the start-up current during the charging of SUPIC. C_{SUPIC} acts as a buffer at charge of SUPREG and start-up of the IC.

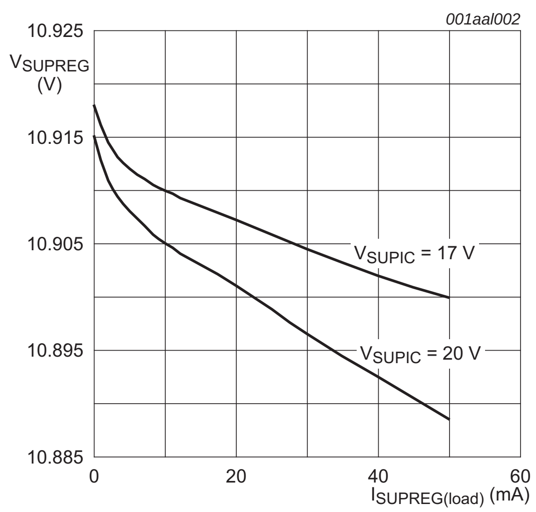
V_{SUPREG} must reach $V_{start(SUPREG)}$ before the IC starts operating to ensure that the external MOSFETs receive sufficient gate drive if V_{SUPIC} is also above its start level.

The SUPREG has an UnderVoltage Protection. When V_{SUPREG} drops under the 10.3 V, two actions take place:

- The IC stops operating to prevent unreliable switching due to too low gate driver voltage. The PFC controller stops switching immediately, but the HBC continues until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to 5.4 mA. If an overload occurs at SUPREG in combination with an external DC supply for SUPIC, the dissipation reduces in the series stabilizer.

In principle, SUPREG can only source current.

The drivers of GATELS and GATEPFC are supplied using V_{SUPREG} and draw current from it during operation depending on the operating condition. Some change in value can be expected due to current load and temperature:



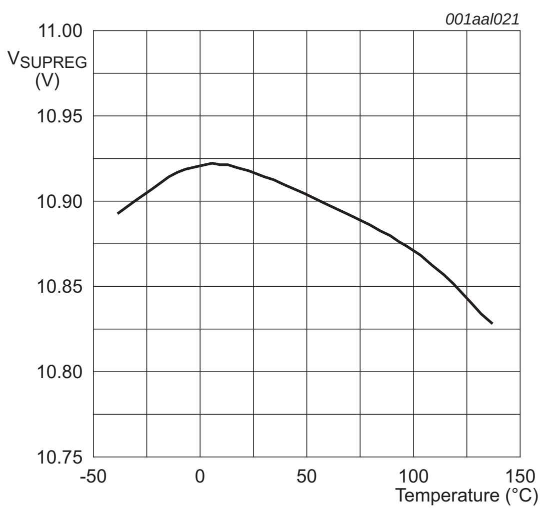


Fig 8. Typical V_{SUPREG} characteristics for load and temperature

5.5.1 Block diagram of SUPREG regulator

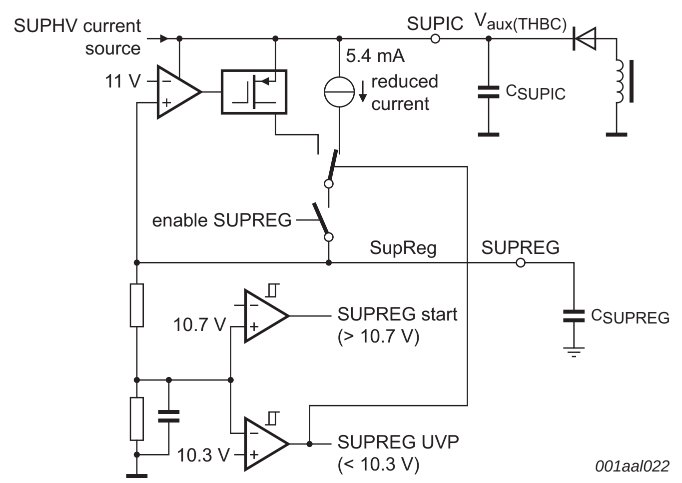


Fig 9. Block diagram of internal SUPREG regulator

5.5.2 SUPREG during start-up

SUPREG is supplied by SUPIC. SUPIC is the unregulated external power source that provides the input voltage for the internal voltage regulator that provides SUPREG.

At start-up V_{SUPIC} must reach a specific voltage level before SUPREG is activated:

- Using the internal HV supply, SUPREG is activated when $V_{SUPIC} \geq 22$ V
- Using an external low voltage supply, SUPREG is activated when $V_{SUPIC} \geq 17$ V

5.5.3 Supply voltage for the output drivers: SUPREG

The SSL4120 has a powerful output stage for GATEPFC and GATELS to drive large MOSFETs. These internal drivers are supplied by SUPREG that provides a fixed voltage.

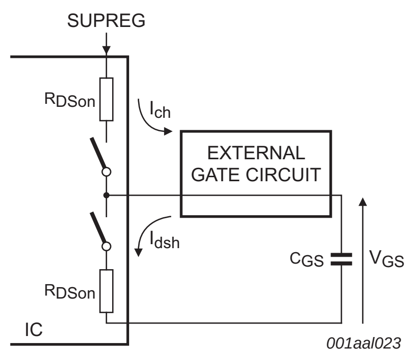


Fig 10. Simplified model of MOSFET drive

It can be seen from Figure 10 that current is drawn from SUPREG when the external MOSFET is switched on by charging the gate to a high voltage.

The shape of the current from SUPREG at switch-on is related to:

- The supply voltage for the internal driver (10.9 V)
- The characteristic of the internal driver
- The gate capacitance C_{GS} to be charged
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

Remark: The switching moments of GATEPFC and GATELS are independent in time. The charging of SUPHS for GATEHS is synchronized in time with GATELS but has a different shape because of the bootstrap function.

5.5.4 Supply voltage for the output drivers: SUPHS

The high-side driver is supplied by an external bootstrap buffer capacitor. The bootstrap capacitor is connected between the high-side reference pin HB and the high-side driver supply input pin SUPHS. While V_{HB} is low, an external diode from SUPREG charges this capacitor. Selecting a suitable external diode minimizes the voltage drop between SUPREG and SUPHS. This selection is especially important when using a MOSFET which needs a large amount of gate charge and/or when switching at high frequencies.

Instead of using SUPREG as the power source for charging C_{SUPHS}, another supply source can be used. In such a construction, it is important to check for correct start/stop sequences and to prevent the voltage exceeding the maximum value of V_{HB} +14 V.

Remark: The current taken from SUPREG to charge V_{SUPHS} differs for each cycle in time and shape from the current taken by the GATEPFC and GATELS drivers.

5.5.4.1 Initial charging of C_{SUPHS}

At start-up, the bootstrap function charges C_{SUPHS} when GATELS is set HIGH to switch on the low-side MOSFET. While C_{SUPHS} is being charged, GATELS is switched on for charging and the PFC operation is started. The time between start charging and start HBC operation is normally sufficient to charge C_{SUPHS} completely. Start HBC operation is when $V_{SNSBOOST}$ reaches 2.3 V which is approximately 90 % of nominal V_{boost}.

5.5.4.2 Current load on SUPHS

The current taken from SUPHS consists of two parts:

- Internal MOSFET driver GATEHS
- Internal circuit to control GATEHS (37 μA, quiescent current)

Figure 11 shows that the current taken by the GATEHS driver occurs at switch-on. The shape of the current from SUPHS at switch-on is related to:

- The value of the supply voltage for the internal driver
- The characteristic of the internal driver
- The gate capacitance to be charged
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

V_{SUPHS} can vary.

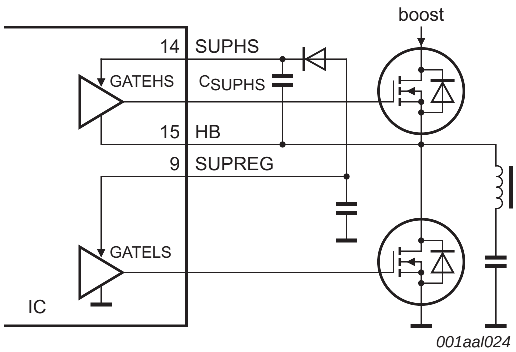


Fig 11. Typical application of SUPHS

5.5.4.3 Lower voltage on SUPHS

During normal operation, each time the Half-Bridge (HB) node is switched to ground level, the bootstrap function charges C_{SUPHS}. V_{SUPHS} is normally lower than V_{SUPREG} (or other bootstrap supply input) because of the voltage drop across the bootstrap diode.

The voltage drop across the bootstrap diode is directly related to the amount of current that is required to charge C_{SUPHS}. The resulting V_{SUPHS} also has a relationship to the time available for charging.

A large voltage drop occurs when an external MOSFET with a large gate capacitance is switched at high frequency (high current and a short time).

During burst mode operation, a low voltage on SUPHS can occur. In burst mode, there are (long) periods when switching does not occur. Therefore C_{SUPHS} is not charged. The circuit supplied by SUPHS slowly discharges C_{SUPHS} during this time. When a new burst starts, V_{SUPHS} is lower than during normal operation. During the first switching cycles C_{SUPHS} is recharged to its normal level. During burst mode, at low output power, the switching frequency is normally rather high which limits a fast recovery of V_{SUPHS}.

Although in most applications the voltage drop is limited, it is an important issue for evaluation. It can influence the selection of the best diode type for the bootstrap function and the value of C_{SUPHS}.

5.5.5 SUPREG power consumed by the MOSFET drivers

During operation the drivers GATEPFC, GATELS and GATEHS charging the gate capacitances of the external MOSFETs are a major part of the power consumption from SUPREG. The amount of energy required in time is linear to the switching frequency. Often, for the MOSFETs used, the total charge is specified for certain conditions. With this specification, an estimation can be made for the amount of current needed from SUPREG.

5.5.5.1 GATELS and GATEHS (driving a total of two MOSFETs)

$$\Delta I_{SUPIC(HBC)} = 2 \times Q_{gate(HBC)} \times f_{sw(HBC)} \quad (1)$$

Example:

- $Q_{gate(HBC)}$ = 40 nC
- $f_{sw(HBC)}$ = 100 kHz

$$\Delta I_{SUPIC} = 2 \times 40\ nC \times 100\ kHz = 8\ mA$$

Remark: The calculated value is higher than the practical value in general because the switching operation deviates from the MOSFET specification for Q_{gate}.

5.5.5.2 GATEPFC

$$\Delta I_{SUPIC(PFC)} = Q_{gate(PFC)} \times f_{sw(PFC)} \quad (2)$$

Example:

- $Q_{gate(PFC)}$ = 40 nC
- $f_{sw(PFC)}$ = 100 kHz

$$\Delta I_{SUPIC(PFC)} = 40\ nC \times 100\ kHz = 4\ mA$$

5.5.6 SUPREG supply voltage for other circuits

The regulated voltage of SUPREG can also be used as a regulated supply for an external circuit. The load of the external circuits affects the start-up (time) and the total load (IC and external circuit) of SUPREG during operation.

5.5.6.1 Current available for supplying an external circuit from SUPREG

The total current available from SUPREG is a minimum of 40 mA. Determine how much current the IC requires and the amount of current required by the external circuit.

$I_{SUPREG(external)}$ = 40 mA – $I_{SUPREG(IC)}$

With respect to the IC, by far the greatest amount of current from SUPREG is consumed by the MOSFET drivers (GATELS, GATEHS and GATEPFC). Other circuit parts in the IC, consume a maximum of 3 mA.

$I_{SUPREG(IC)}$ = $I_{SUPREG(drivers)}$ + $I_{SUPREG(external)}$

$I_{SUPREG(IC)}$ = $I_{SUPREG(drivers)}$ + 4 mA max

$I_{SUPREG(drivers)}$ is estimated using the method provided in Section 5.5.5

5.5.6.2 An estimation by measurement

While supplying the circuit from an external power supply, the SUPIC current used can be assumed as a first approximation of how much SUPREG current the IC circuits draw. An estimation can be made of the power available for external circuits using this value.

Remark: The highest power consumption value is reached when the MOSFET drivers are switching at the highest frequency.

Example:

$I_{SUPIC(IC)max(measured)}$ = 18 mA

$I_{SUPREG(IC)}$ = $I_{SUPIC(IC)max(measured)}$ = 18 mA

$I_{SUPREG(external)}$ = 40 mA – $I_{SUPREG(IC)}$ = 40 mA – 18 mA = 22 mA

Remark: V_{SUPREG} must remain above the undervoltage protection level of 10.3 V to maintain full functionality. During start-up, high external current loads can lead to problems.

5.6 Value of the capacitors on SUPIC, SUPREG and SUPHS

Some practical examples are provided in Section 12.

5.6.1 Value of C_{SUPIC}

5.6.1.1 General

Use two types of capacitors on SUPIC. An SMD ceramic type with a smaller value located close to the IC and an electrolytic type with the major part of the capacitance.

5.6.1.2 Start-up

A larger capacitor is needed when the HV source initially provides the supply before it is taken over by the auxiliary winding. The capacitor value must be large enough to handle the start-up before the T_{HBC} auxiliary winding supply takes over the supply of SUPIC.

Example:

- $I_{SUPIC(start\text{-}up)}$ = 10 mA
- $\Delta V_{SUPIC(start\text{-}up)}$ = 22 V – 15 V = 7 V
- $\Delta t_{Vaux(HBC)>15V}$ = 70 ms

$$C_{SUPIC} > I_{SUPIC(start\text{-}up)} \times \frac{\Delta t_{Vaux(HBC)>15\ V}}{\Delta V_{SUPIC(start\text{-}up)}} = 10\ mA \times \frac{70\ ms}{7\ V} = 100\ \mu F \quad (3)$$

5.6.1.3 Normal operation

The main purpose of the capacitors on SUPIC for normal operation is to keep the current load variations (for example, gate drive currents) local.

5.6.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an T_{HBC} auxiliary winding and start-up from an HV source. While in burst mode, there is a long period during which the T_{HBC} auxiliary winding is not able to charge C_{SUPIC} because the HBC is not switching (time between two bursts). Therefore, the capacitor value of C_{SUPIC} must be large enough to keep the voltage above 15 V. This voltage prevents activating the SUPIC undervoltage stop level.

Example:

- $I_{SUPIC(burst\text{-}off)}$ = 4 mA
- $\Delta V_{SUPIC(burst)} = V_{aux(THBC)burst} - 15\ V = 19\ V - 15\ V = 4\ V$
- $\Delta t_{burst\text{-}off}$ = 25 ms

$$C_{SUPIC} > I_{SUPIC(burst-off)} \times \frac{\Delta t_{burst-off}}{\Delta V_{SUPIC(burst)}} = 4\ mA \times \frac{25\ ms}{4\ V} = 25\ \mu F \quad (4)$$

5.6.2 Value of C_{SUPREG}

C_{SUPREG} must not be larger than C_{SUPIC} to support charging of C_{SUPREG} during an HV source start. This prevents a severe voltage drop on SUPIC due to the charge of C_{SUPREG}. If SUPIC is supplied by an external (standby) source, this method is not important.

SUPREG is the supply for the current of the gate drivers. Keeping current peaks local is achieved using an SMD ceramic capacitor supported by an electrolytic capacitor. This combination is necessary to provide sufficient capacitance to prevent a voltage drop during high current loads. C_{SUPREG} must be much larger than the (total) MOSFETs capacitance that is driven to prevent significant voltage drop. The MOSFET capacitance includes the SUPHS parallel load and capacitor bootstrap construction.

When considering the internal voltage regulator, C_{SUPREG} must be ≥ 1 µF. Often a much larger value is used for the reasons mentioned previously.

5.6.3 Value of C_{SUPHS}

C_{SUPHS} must be much larger than the gate capacitance to support charging the gate of the high side MOSFET. This size is to prevent a significant voltage drop on SUPHS by the gate charge. When burst mode is applied, C_{SUPHS} is discharged by 37 µA during the time between two bursts.

6. MOSFET drivers GATEPFC, GATELS and GATEHS

The SSL4120 provides three outputs for driving external high-voltage power MOSFETs:

- GATEPFC for driving the PFC MOSFET
- GATELS for driving the low side of the HBC MOSFET
- GATEHS for driving the low side of the HBC MOSFET

6.1 GATEPFC

The SSL4120 has a strong output stage for PFC to drive a high-voltage power MOSFET. It is supplied by the fixed voltage from V_{SUPREG} = 10.9 V.

6.2 GATELS and GATEHS

Both drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to pin PGND and is supplied from SUPREG. The high-side driver is floating, referenced to HB, the connection to the midpoint of the external half-bridge. The high-side driver is supplied using C_{SUPHS} that is supplied from an external bootstrap function via SUPREG. The bootstrap diode charges C_{SUPHS} when the low-side MOSFET is on.

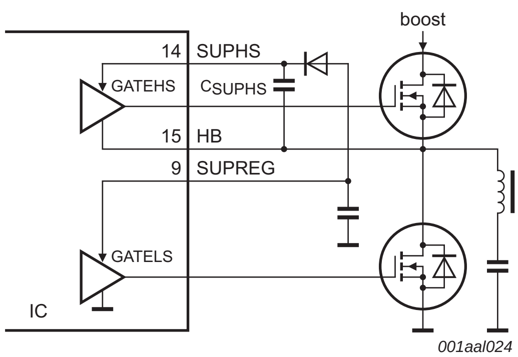


Fig 12. GATELS and GATEHS drivers

Both HBC drivers have a strong current source capability and an extra strong current sink capability. In HBC operation, fast switch-on of the external MOSFET is not critical, as the HB node swings automatically to the correct state after switch-off (zero-voltage switching). Fast switch off however, is important to limit switching losses and prevent delay especially at high frequency.

6.3 Supply voltage and power consumption

See Section 5.5.3 and Section 5.5.5.for a description of the supply voltages and power consumption by the MOSFET drivers.

6.4 General subjects on MOSFET drivers

6.4.1 Switch on

The time to switch on depends on:

- The supply voltage for the internal driver
- The characteristic of the internal driver
- The gate capacitance to be charged
- The gate threshold voltage for the MOSFET to switch on
- The external circuit to the gate

6.4.2 Switch off

The time to switch off depends on:

- The characteristic of the internal driver
- The gate capacitance to be discharged
- The voltage on the gate just before discharge
- The gate threshold voltage for the MOSFET to switch off
- The external circuit to the gate

Because the timing for switching off the MOSFET is more critical than switching it on, the internal driver can sink more current than it can source. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes a compromise is made between fast switching and EMI effects. A gate circuit between the driver output and the gate can be used to optimize the switching behavior.

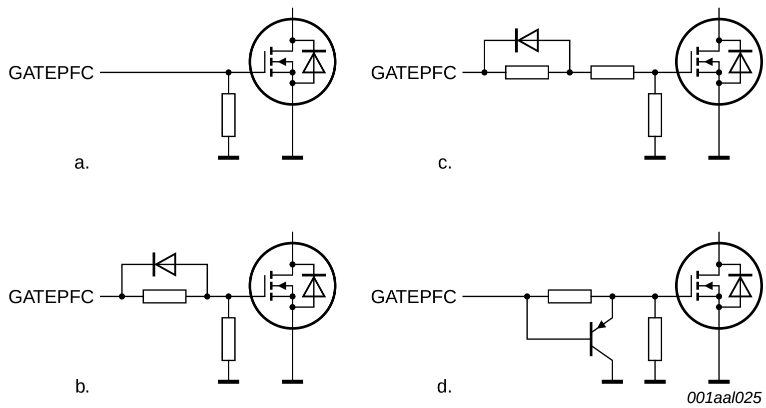


Fig 13. Gate circuits examples

Switching on and off the MOSFETs using the drivers can be modeled by alternating charge and discharge of a (gate-source) MOSFET capacitance through a resistor (R_{DSon} of the internal gate driver).

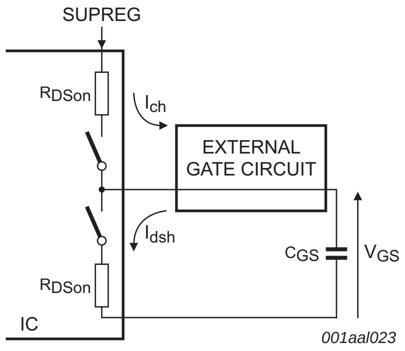


Fig 14. Simplified model of a MOSFET drive

6.5 Specifications

The main function of the internal gate drivers is to source current and sink current to switch on and off the external MOSFET switch.

The amount of current that can be sunk and sourced is specified to show the capability of the internal driver.

The simplified model in Figure 14 demonstrates that the charge and discharge current values are dependent on the conditions of the supply and gate voltages. The value of the source current is highest when the supply voltage is highest and the gate voltage 0 V. The value of the sink-current is highest when the gate voltage is highest.

Table 3. PFC and HBC driver specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PFC driver (pin GATEPFC)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	–0.5	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V	-	0.7	-	A
		$V_{GATEPFC}$ = 10 V	-	1.2	-	A
HBC high-side and low-side driver (pins GATEHS and GATELS)						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	–310	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 4 V	-	–310	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V	-	560	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	1.9	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 2 V	-	560	-	mA
		$V_{GATELS} - V_{PGND}$ = 11 V	-	1.9	-	A

The supply voltage from SUPREG to GATEPFC and GATELS is constant at 10.9 V. The supply voltage for GATEHS is lower and depends on the operating conditions (see Section 5.5.4).

6.6 Mutual disturbance of PFC and HBC

The charge and discharge currents for the MOSFET gate of the PFC and HBC are independently driven in time. Due to these current peaks being high, they can give disturbance on control and sense signals. As both the PFC and HBC controllers are integrated in the SSL4120. The large GATEPFC and GATELS driver currents can also give mutual interference to the controller operation.

Design the gate circuits and PCB layout (see Section 11.1) to prevent the interference. The construction shown in Figure 12 and Figure 13 helps keep the fast and high switch off current local for a high-power MOSFET.

7. PFC functions

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 380 kHz which reduces switching losses by valley skipping. This reduction is mainly near the zero crossings of the mains voltage and effective at low mains input voltage and medium/low output load condition. The 380 kHz limit is high enough to reach low harmonic distortion of the mains input current as required by lighting devices.

The PFC is designed as a boost converter with a fixed output voltage. An advantage of a fixed boost is that the HBC can be designed to a high input voltage which makes the HBC design easier.

Another advantage of the fixed boost is the possibility to use a smaller boost capacitor C_{boost} value or to have a significant longer hold-up time.

In the SSL4120 system, the PFC is always active. The PFC is switched on first when the mains voltage is present. The HBC is switched on after the C_{boost} is charged to approximately 90 % of its normal value.

The system can be operated in burst mode for improved efficiency at low output loads. During this mode, the HBC determines the on/off sequences and the PFC can be made to burst simultaneously for even better efficiency results.

7.1 PFC output power and voltage control

The PFC of the SSL4120 is t_{on} controlled and therefore it is not necessary to measure the mains phase angle. The on-time is kept constant for the mains voltage and load condition during the half-sine wave to ensure a good Power Factor (PF) and Mains Harmonics Reduction (MHR).

Using a constant t_{on}, the switching current to the PFC output is proportional to the sine waveform input voltage.

An essential PFC coil design parameter is the highest peak current. This current occurs at the lowest input voltage and maximum output power.

The maximum peak current $I_{p(PFC)max}$ for a PFC operating in critical conduction mode can be calculated with the following equation:

$$I_{p(PFC)max} = \frac{2 \times \sqrt{2} \times P_{i(max)}}{V_{mains(min)}} = \frac{2 \times \sqrt{2} \times \dfrac{P_{O(nameplate)}}{\eta}}{V_{mains(min)}} \qquad (5)$$

Example:

- Efficiency $\eta = 0.9$
- $P_{O(nameplate)} = 250$ W
- $V_{mains(min)} = 90$ V
- $I_{p(PFC)max} = 8.73$ A

- $I_{p(PFC)max}$ + 10 % = 9.60 A[1]

7.2 PFC regulation

7.2.1 Sensing V_{boost}

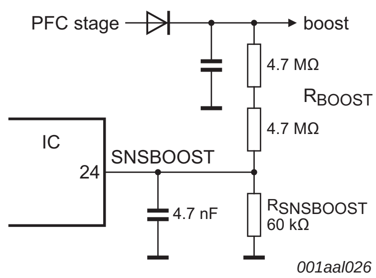


Fig 15. PFC output regulation example: SNSBOOST

V_{boost} is set with a resistor divider between boost and the SNSBOOST pin. When in regulation, $V_{SNSBOOST}$ is kept at 2.5 V.

The resistor divider can have a total value up to 10 MΩ to limit power loss.

$R_{SNSBOOST}$ can be calculated using the following equation:

$$R_{SNSBOOST} = \frac{R_{boost} \times V_{reg(SNSBOOST)}}{V_{boost} - V_{reg(SNSBOOST)}} \quad (6)$$

Example:

- R_{boost} = 4.7 MΩ + 4.7 MΩ = 9.4 MΩ
- V_{boost} = 394 V

$$R_{SNSBOOST} = \frac{R_{boost} \times V_{reg(SNSBOOST)}}{V_{boost} - V_{reg(SNSBOOST)}} = \frac{9.4\ M\Omega \times 2.5\ V}{394\ V - 2.5\ V} = 60\ k\Omega \quad (7)$$

Use a capacitor on SNSBOOST to prevent wrong measurements due to MOSFET switching noise, mains surge events or ESD events. Also, for this reason, place the measurement resistor and the filtering capacitor close to the IC in the PCB layout.

7.2.2 SNSBOOST open and short-circuit pin detection

The PFC does not start switching until $V_{SNSBOOST}$ is above 0.4 V. This feature serves as short-circuit protection for V_{boost} and SNSBOOST pin itself.

1. The SSL4120 PFC, operates in Quasi-Resonant (QR) mode with valley detection providing good efficiency. Valley detection needs additional ringing time within every switching cycle. This time for ringing adds short periods of no power transfer to the output capacitor. The system must compensate the no-power transfer with a higher peak current. A rule of thumb is that the peak current in QR mode is a maximum of 10 % higher than the calculated peak current in critical conduction mode.

An internal current source draws a small amount of current from SNSBOOST. The circuit prevents switching when the pin is left open as $V_{SNSBOOST}$ remains lower than 0.4 V. This combination also creates an Open-Loop Protection (PFC boost OLP) when, for example, a resistor in the boost divider network is disconnected.

7.2.3 PFCCOMP in the PFC voltage control loop

The SNSBOOST pin senses the PFC output voltage and $R_{SNSBOOST}$ controls it. The internal error amplifier with a reference voltage of 2.5 V senses $V_{SNSBOOST}$. The amplifier converts the input error voltage with a transconductance g_m = 80 μA/V to its output. This output is available at COMPPFC for adding an external loop compensation network. The current from the error amplifier results in a loop voltage $V_{COMPPFC}$. $V_{COMPPFC}$ in combination with $V_{SNSMAINS}$, determines the PFC switching-on time.

A compensation network, typically comprising one resistor and two capacitors at pin COMPPFC, is used to stabilize the PFC control loop.

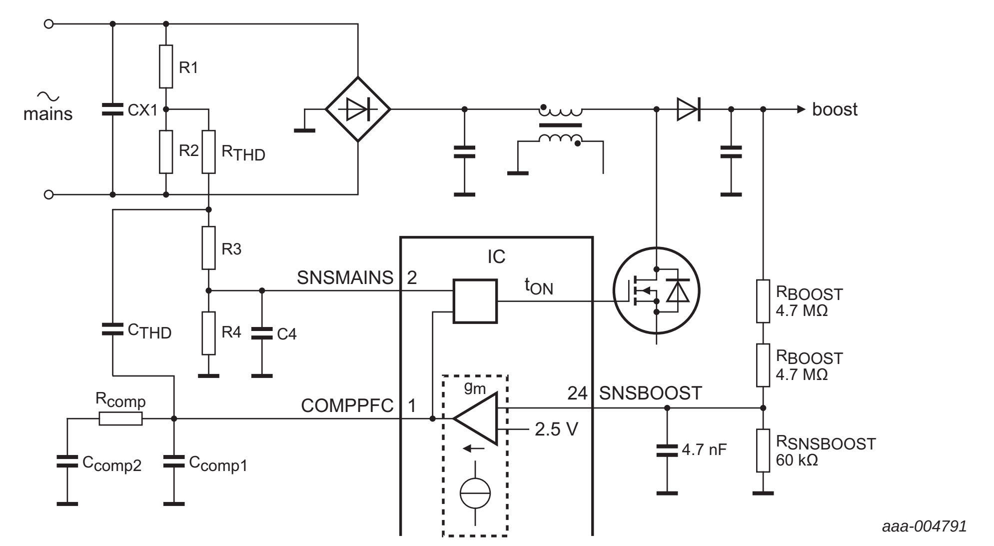


Fig 16. Basic PFC voltage control loop with PFCCOMP and on-time modulation

The transfer function has a pole at 0 Hz, a zero by R_{comp}/C_{comp2} and a pole again by C_{comp1}/C_{comp2}. Set the zero frequency to 10 Hz while the next pole frequency is at 40 Hz. The zero point and pole frequencies of the compensation network can be calculated as follows:

$$f_z = \frac{1}{2\pi \times R_{comp} \times C_{comp2}} \tag{8}$$

$$f_p = \frac{C_{comp1} + C_{comp2}}{2\pi \times R_{comp} \times C_{comp1} \times C_{comp2}} \tag{9}$$

The choice also concerns a trade-off between power factor and transient behavior. A lower regulation bandwidth leads to a better power factor but the transient behavior becomes poorer. A higher regulation bandwidth leads to a better transient response but a poorer power factor.

7.2.4 Mains compensation in the PFC voltage control loop

The mathematical equation for the transfer function of a power factor corrector, contains the square of V_{mains}.

$$K(V_{mains}) = \frac{A}{V_{mains}^2} \quad (10)$$

In a typical application, this results in a low bandwidth for low V_{mains}. While at high V_{mains} the MHR requirements can be hard to meet.

The SSL4120 contains a correction circuit to compensate for the V_{mains} influence. SNSMAINS measures the average V_{mains} which is used for internal compensation. Figure 17 shows the relationship between $V_{SNSMAINS}$, $V_{COMPPFC}$ and the on-time. With this compensation, it is possible to keep the regulation loop bandwidth constant over the complete V_{mains} range. This feature yields a fast transient response on load steps, while still complying with Class-C MHR requirements.

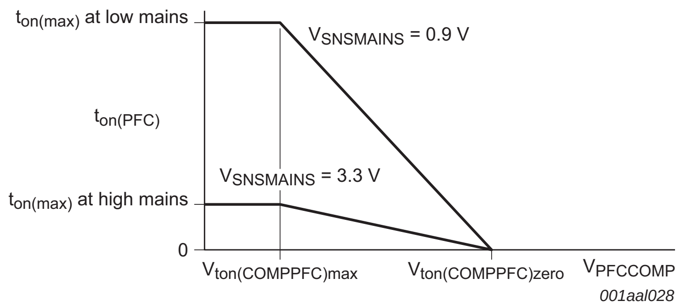


Fig 17. Relationship between on-time $V_{SNSMAINS}$ and $V_{COMPPFC}$

7.3 PFC demagnetization and valley sensing

When the MOSFET drain voltage is at its minimum (valley switching), the PFC MOSFET is switched on for the next stroke. This valley switching reduces switching losses and EMI (see Figure 18).

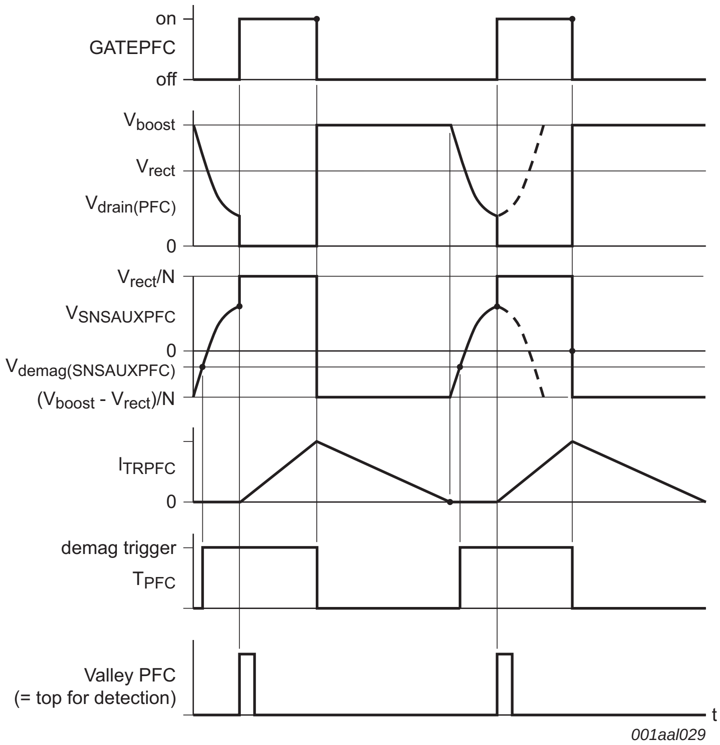


Fig 18. PFC demagnetization and valley sensing

SNSAUXPFC detects the valleys. An auxiliary winding on the PFC coil provides a measurement signal on SNSAUXPFC. It gives a reduced and inverted copy of the MOSFET drain voltage. When a valley of the $V_{drain(PFC)}$ (top at $V_{SNSAUXPFC}$) is detected, the MOSFET is switched on.

If no top (valley at the drain) is detected on $V_{SNSAUXPFC}$ within 4 μs after demagnetization is detected, the MOSFET is forced to switch on.

7.3.1 PFC auxiliary sensing circuit

Add a 5 kΩ series resistor to SNSAUXPFC to protect the internal circuit of the IC against excessive voltage, for example during lightning surges. In the PCB layout, place this resistor close to the IC to prevent disturbances causing incorrect switching.

It is important to maintain valley detection even at low ringing amplitudes. Set $V_{SNSAUXPFC}$ as high as possible, while taking into account its absolute maximum rating of ±25 V.

The number of turns of the auxiliary winding on the PFC coil can be calculated using the following equation:

$$N_{aux(PFC)max} = \frac{V_{SNSAUXPFC(max)}}{V_{L(PFC)max}} \times N_{PFC} = \frac{25\ V}{415} \times 52 = 3.13 \rightarrow 3\ turns \qquad (11)$$

Where:

- $V_{SNSAUXPFC(max)}$ is the absolute maximum voltage rating

- $V_{L(PF)max}$ is the maximum voltage across the PFC primary winding
- N_{PFC} is the number of turns on the PFC coil (for this example, a value of 52 is used)

The V_{boost} level at PFC boost OVP determines the maximum voltage across the PFC primary winding and can be calculated using the following equation:

$$V_{L(PFC)max} = \frac{V_{OVP(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{boost} = \frac{2.63\ V}{2.5\ V} \times 394\ V = 415\ V \quad (12)$$

In this example, a design value of 394 V is used for nominal V_{boost}.

When a PFC coil with a higher number of auxiliary turns is used, a resistor voltage divider can be placed between the auxiliary winding and SNSAUXPFC. The total resistive value of the divider must be less than 10 kΩ to prevent delay of the valley detection in combination with parasitic capacitances.

7.3.2 PFC frequency limit

$f_{sw(PFC)}$ is limited to 380 kHz to minimize the switching losses. If the frequency for quasi-resonant operation is above the 380 kHz limit, the system switches over to Discontinuous conduction mode. The PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching). One or more valleys are skipped, when necessary to keep $f_{sw(PFC)}$ under 380 kHz (valley skipping).

The maximum off-time is limited to 50 μs after the last PFC gate signal to ensure proper control of the PFC MOSFET under all circumstances.

7.4 PFC OverCurrent Regulation and Protection (PFC OCR/OCP)

The maximum peak current which switched using the external MOSFET, is limited cycle-by-cycle by sensing the voltage across a measurement resistor R_{CURPFC}. The SNSCURPFC pin measures the voltage which is limited to 0.5 V. At this voltage level, the MOSFET is switched off.

Take a small voltage margin into account to avoid false triggering of the PFC OCR.

R_{CURPFC} can be calculated with Equation 13:

$$R_{CURPFC} = \frac{V_{OCR(PFC)} - V_{margin}}{I_{L(PFC)max}} = \frac{0.52\ V - 0.1\ V}{8.73\ A} = 48\ m\Omega \quad (13)$$

$V_{SNSCURPFC}$ senses an initial voltage peak at the moment the PFC MOSFET switches on, because its (parasitic) capacitances are discharged. SNSCURPFC has a leading edge blanking of 310 ns to mask this event, so it does not react to this initial peak.

7.4.1 PFC soft-start and soft-stop

The PFC has a soft-start function and a soft-stop function to prevent transformer noise/rattle at start-up or during burst mode operation. The soft-start slowly increases the primary peak current at the start of operation. The soft-stop function slowly decreases the transformer peak current before operation is stopped.

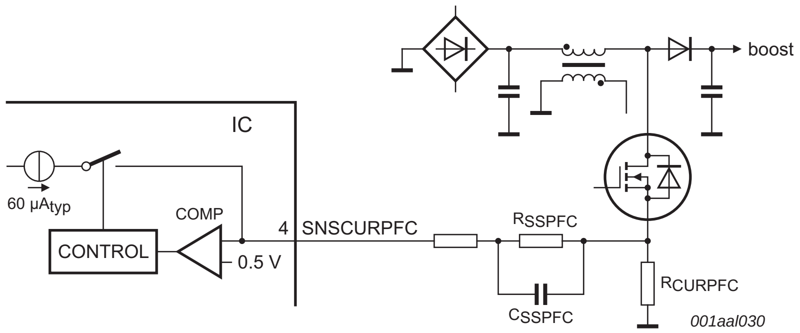


Fig 19. PFC soft-start and soft-stop set-up

R_{SSPFC} and a C_{SSPFC} between SNSCURPFC and R_{CURPFC} set both functions.

7.4.1.1 Soft-start

Before start of operation, an internal current source of 60 μA charges the capacitor to $V_{SNSCURPFC}$ = 60 μA × R_{SSPFC}. When $V_{SNSCURPFC}$ exceeds the internal start voltage of 0.5 V, the operation is started. Select $R_{SSPFC} \geq 12$ kΩ to ensure that the start voltage level is reached.

At start-up, the current source is stopped and $V_{SNSCURPFC}$ drops as R_{SSPFC} discharges C_{SSPFC}. During this discharge, each cycle's peak current increases until C_{SSPFC} is discharged completely and the normal peak current regulation level (PFC OCR/OCP) is reached. R_{CURPFC} sets the PFC OCR/OCP level.

The soft-start period is calculated using Equation 14:

$$\tau_{soft-start(PFC)} = R_{SSPFC} \times C_{SSPFC} \quad (14)$$

7.4.1.2 Soft-stop

Soft-stop is achieved by switching on the internal current source of 60 μA again.

The current charges C_{SSPFC} and the increasing capacitor voltage decreases the peak current. When $V_{SNSCURPFC}$ reaches 0.5 V, the operation is stopped.

$V_{SNSCURPFC}$ is only measured during the off-time of the PFC power switch to prevent measurement disturbances during soft-stop.

7.4.2 SNSCURPFC open and short protection

When the SNSCURPFC pin is open, SNSCURPFC is charged to 0.5 V by the internal current source of 60 μA for soft-start. The PFC does not start switching because of OCP.

When the SNSCURPFC pin is short circuit to ground, the PFC cannot start operation as the start level of 0.5 V has not been reached.

7.5 PFC boost OverVoltage Protection (OVP)

An overvoltage protection circuit is built in to prevent boost overvoltage during load steps and mains transients. When $V_{SNSBOOST}$ exceeds 2.63 V, the switching of the power factor correction circuit is stopped. The PFC resumes switching when $V_{SNSBOOST}$ drops under 2.63 V.

When the resistor between pin SNSBOOST and ground is open, OVP also triggers. In this situation, the internal current source of 45 nA increases $V_{SNSBOOST}$ to the PFC boost OVP protection level.

The voltage value at which PFC boost OVP becomes active can be calculated with the following equation:

$$V_{OVP(boost)} = \frac{V_{OVP(SNSBOOST)}}{V_{reg(SNSBOOST)}} \times V_{boost} = \frac{2.63\ V}{2.5\ V} \times 394\ V = 415\ V \quad (15)$$

In the example, a design value of 394 V is used for nominal V_{boost}.

7.6 PFC mains UnderVoltage Protection (brownout protection)

$V_{SNSMAINS}$ is sensed continuously to prevent the PFC operating at very V_{mains} input voltages. When $V_{SNSMAINS}$ drops under 0.89 V, the switching of the PFC is stopped. This mains undervoltage protection is sometimes referred to brownout protection.

$V_{SNSMAINS}$ must be an average DC value that represents the V_{mains}. The system works best with a time constant of approximately 150 ms for pin SNSMAINS. When $V_{SNSMAINS}$ drops, it is internally clamped to 1.05 V, which is 0.1 V under the start level of 1.15 V. This level allows a fast restart when V_{mains} returns after a mains dropout. The PFC (re)starts when $V_{SNSMAINS}$ exceeds the start level of 1.15 V. In the following calculations, the R_{THD} value is assumed to be zero to simplify the equations.

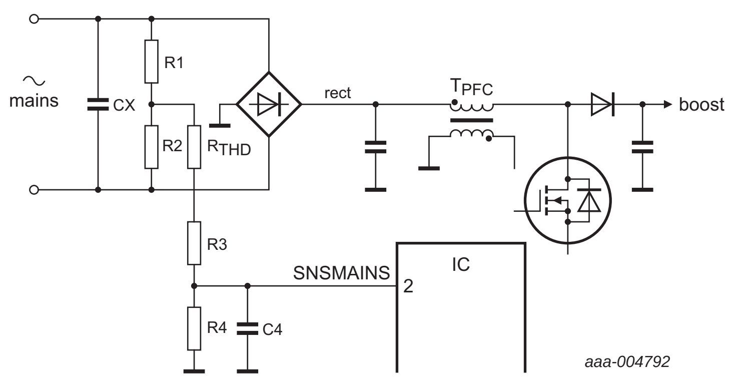


Fig 20. SNSMAINS circuitry

7.6.1 Undervoltage or brownout protection level

The AC input voltage is measured using R1 and R2. Each resistor alternately senses half the sine cycle, both resistors have the same value.

A typical resistor value of 2 MΩ can be applied for R1and R2 to keep the bleeder loss low.

The average voltage sensed is calculated as follows:

$$V_{mains(avg)} = \frac{2\sqrt{2}}{\pi} \times V_{mains(RMS)} \tag{16}$$

The SNSMAINS brownout protection (RMS) voltage level is calculated with Equation 17:

$$R_v = \frac{R1 \times R2}{R1 + R2} \tag{17}$$

$$V_{bo(mains)} = 2 \times \frac{\pi}{2\sqrt{2}} \times V_{UVP(SNSMAINS)} \times \left(\frac{R_v + R3}{R4} + 1\right) \tag{18}$$

Example:

Required: $V_{bo(mains)}$ = 66 V (AC), with:

- $V_{UVP(SNSMAINS)}$ = 0.89 V
- R1 = R2 = 2 MΩ → R_V = 1 MΩ

$$V_{bo(mains)} = 2 \times \frac{\pi}{2\sqrt{2}} \times 0.89 \times \left(\frac{R_v + R3}{R4} + 1\right) \tag{19}$$

$$66 = 1.9771 \times \left(\frac{1\ \mathrm{M}\Omega + R3}{R4} + 1\right) \tag{20}$$

R3 = 560 kΩ, R4 = 47 kΩ

The time constant for a recommended time constant of 150 ms, with C4 = 3300 nF:

$$t_{SNSMAINS} = R4 \times C4 = 47\ k\Omega \times 3300\ nF = 155\ ms$$

7.6.2 Discharging the mains input capacitor

There is often an application requirement to discharge the X-capacitors in the EMC input filter within a certain time. The replacement values of R1, R2, R3 and R4 determine the resistance required for discharging the X-capacitors in the input filter. The replacement value can be calculated with Equation 21:

$$R_{dch} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} \tag{21}$$

Example:

Required: t_{dch} < 600 ms, with:

- R1 = R2 = 2 MΩ
- R3 = 560 kΩ
- R4 = 47 kΩ

$$R_{dch} = R1 + \frac{R2 \times (R3 + R4)}{R2 + R3 + R4} = 2\ M\Omega + \frac{2\ M\Omega \times (560\ k\Omega + 47\ k\Omega)}{2\ M\Omega + 560\ k\Omega + 47\ k\Omega} = 2465\ k\Omega \tag{22}$$

Where:

- CX = 220 nF

- The time constant equals: $t_{dch} = R_{dch} \times CX = 2465\ k\Omega \times 220\ nF = 542\ ms$

7.6.3 SNSMAINS open pin detection

The SNSMAINS pin, which senses V_{mains}, has an integrated protection circuit to detect an open pin. When the pin is not connected, a 33 nA internal current source either pulls the pin down under the stop level of 0.9 V or keeps it under the start level of 1.15 V.

When the SNSMAINS pin is shorted to ground, the results are similar.

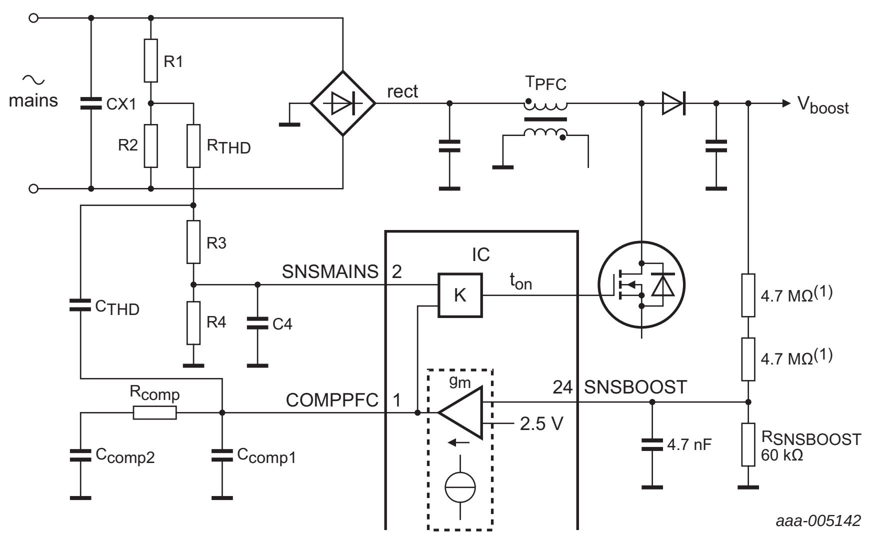
7.7 PFC on-time modulation to reach low THD

When V_{mains} is near 0 V, the energy in the PFC inductor is low because the peak current follows the mains voltage.

$$E_{inductor} = \frac{1}{2}LI^2 \qquad (23)$$

Before the PFC stage can transfer energy to the bus capacitor, the (parasitic) capacitances on the drain of the PFC MOSFET must be first charged from almost 0 V to the boost voltage of 400 V to 450 V.

$$E_{capacitor} = \frac{1}{2}CV^2 \qquad (24)$$



(1) R_{BOOST} is the total of both resistors

Fig 21. SNSMAINS and COMPFC circuitry with THD improvement

The total (parasitic) capacitance on the PFC MOSFET drain consists of:

- MOSFET output capacitance C_{oss}
- Discrete dV/dt limiting capacitance
- Total inter-winding capacitance of the PFC transformer primary winding

To prevent the mains current dropping to zero, the PFC gate drive signal on-time is increased near to V_{mains} zero crossings. As a result, the peak current increases near to V_{mains} zero crossings and the PFC inductor energy increases. The on-time is increased by reducing $V_{COMPPFC}$.

The modulation signal is tapped from the mains voltage via resistor R_{THD} and injected into C_{comp1} via capacitor C_{THD}.

Find the best R_{THD} and C_{THD} value using experimentation. However, the total value of R3 and R_{THD} must be equal to the value for R3 as calculated in Section 7.6.

In the example from Section 7.6, R3 is calculated 560 kΩ with R_{THD} = 0 Ω. During the tuning of the THD and mains harmonics ensure that the sum of R3 and R_{THD} is 560 kΩ.

A good starting value for C_{THD} is 1 nF and R_{THD} equal to R3.

C_{THD} sets the amount of modulation. Adjusting R_{THD} and R3 makes it possible to change slightly the modulation phase and the energy for each harmonic can be levelled to meet the Class-C mains harmonics requirements.

8. HBC functions

8.1 Boost UVP

The IC begins HBC operation when V_{boost} is higher than approximately 90 % of $V_{boost(nom)}$ to ensure proper working of the HBC.

$V_{SNSBOOST}$ is sensed continuously. When $V_{SNSBOOST}$ drops under 1.6 V, switching of the HBC is stopped when the low-side MOSFET is on. The HBC (re)starts when $V_{SNSBOOST}$ exceeds the start level of 2.3 V.

8.2 HBC switch control

The internal control for the MOSFET drivers, determines when the MOSFETs are switched on and off. It uses the input from several functions.

1. An internal divider is used to provide the alternating switching of high-side and low-side MOSFET for every oscillator cycle.
2. The adaptive non-overlap (see Section 8.3) sensing on HB determines the switch-on moment.
3. The oscillator (see Section 8.4) determines the switch-off moment.
4. Several protection and enable functions determine when the resonant converter is switching.

8.3 HBC adaptive non-overlap

8.3.1 Inductive mode (normal operation)

The high efficiency of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft-switching. A small non-overlap time (also called dead time) is required between the on-time of the high-side MOSFET and low-side MOSFET to allow soft-switching. During this non-overlap time, the primary resonant current charge or discharges the capacitance of the half-bridge between ground and V_{boost}. After the charge or discharge, the body diode of the MOSFET starts conducting and because the MOSFET drain voltage is zero, there are no switching losses.

This mode of operation is called Inductive mode because the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

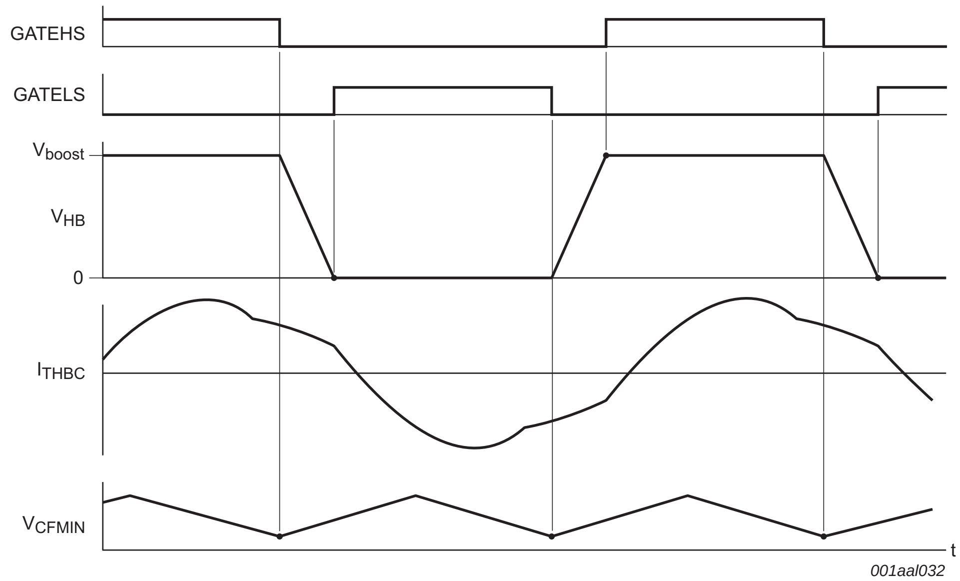


Fig 22. Inductive mode HBC switching

The time required for the transition of V_{HB} depends on the amplitude of the resonant current at the moment of switching. There is a (complex) relationship between the amplitude, $f_{sw(HBC)}$, V_{boost} and V_O. Ideally the IC switches on the MOSFET when the transition of V_{HB} has reached its end value. It must not wait longer, especially at high output load, to prevent a swing back of V_{HB}.

The adaptive non-overlap function of the SSL4120 provides an automatic measurement and control function that decides when to switch on. As it uses actual measurement input, the control adapts for operation changes in time.

Because of this adaptive non-overlap function, it is not necessary to preset a fixed non-overlap time, which is always a compromise between different operating conditions.

The adaptive non-overlap function senses the slope at V_{HB} after one MOSFET has been switched off. Normally, the slope V_{HB} starts directly. Once the transition of the HB node is complete, the slope ends. The adaptive non-overlap function detects the slope end and the other MOSFET is switched on. As a result, the non-overlap time is automatically adjusted to the best value which provides the lowest switching loss. Even if the V_{HB} transition cannot be fully completed.

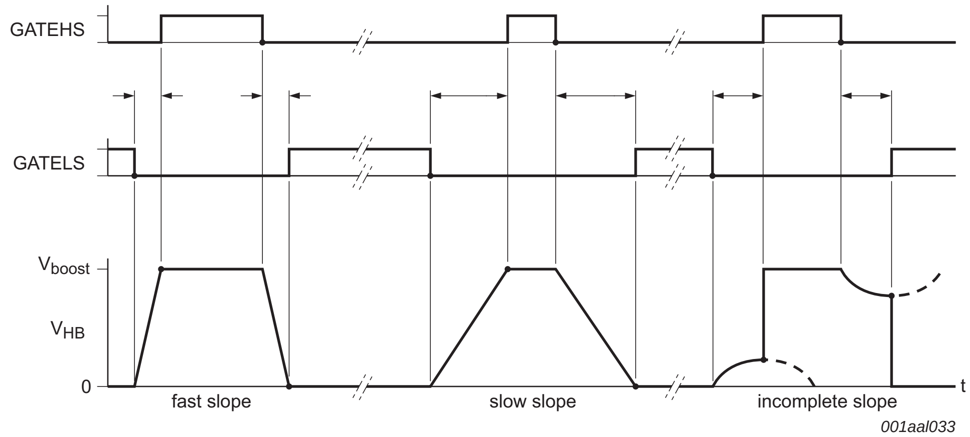


Fig 23. Adaptive non-overlap switching during normal operating conditions

The non-overlap time depends on the V_{HB} slope, but has an upper and lower time limit. An integrated minimum non-overlap time (160 ns max.) prevents accidental cross conduction in all conditions. The maximum non-overlap time is limited to the charging time of the oscillator. If the V_{HB} slope takes more time than the charging of the oscillator (25 % of V_{HB} switching period), the MOSFET is forced to switch on. In this case, the MOSFET is not soft-switching. The maximum non-overlap time limitation ensures that at a high $f_{sw(HBC)}$, the MOSFET on-time is at least 25 % of the V_{HB} switching period.

8.3.2 Capacitive mode

During error conditions (for example, output short circuit, load pulse too high) or special start-up conditions, $f_{sw(HBC)}$ can become lower than the resonance frequency. The resonant tank then has a capacitive impedance. In capacitive mode, the V_{HB} slope does not start after the MOSFET has switched off. It is not preferred to switch on the other MOSFET. The lack of soft-switching increases dissipation in the MOSFETs. The conducting body diode in the MOSFET at the switching moment can damage or even destroy the device quickly.

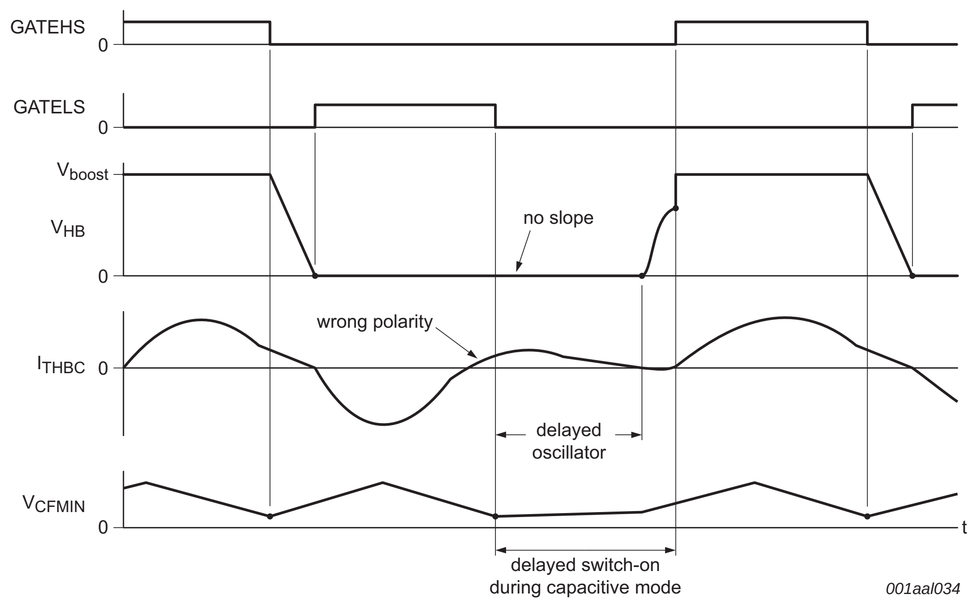


Fig 24. Capacitive mode HBC switching

The adaptive non-overlap system of the SSL4120 always waits until the slope at the half-bridge node starts. It guarantees safe/best switching of the MOSFETs in all circumstances. In Capacitive mode, it can take half the resonance period before the resonant current changes back to the correct polarity and starts charging the half-bridge node. The oscillator remains in its slow charging current mode until the half-bridge slope starts to allow this relatively long waiting time (see also Section 8.4.2 and Figure 28).

The MOSFET is forced to switch on when the half-bridge slope does not start at all and the slowed-down oscillator reaches the high level.

The Capacitive Mode Regulation (CMR) function increases $f_{sw(HBC)}$ to bring the converter from Capacitive mode to Inductive mode operation again.

8.3.3 Capacitive Mode Regulation (CMR)

The adaptive non-overlap function prevents the harmful switching in Capacitive mode. However, an extra action is executed, which results in the CMR to end the Capacitive mode operation and return to Inductive mode operation.

Capacitive mode is detected when the V_{HB} slope does not start shortly (690 ns) after the MOSFET is switched-off. At detection of capacitive mode, $f_{sw(HBC)}$ is increased quickly. Discharging $C_{SSHBC/EN}$ with a high current (1800 μA) from the moment $t_{no\text{-}slope}$ = 690 ns has passed before the half-bridge slope starts to increase $f_{sw(HBC)}$. The resulting $f_{sw(HBC)}$ increase regulates the HBC back to the border between Capacitive mode and Inductive mode.

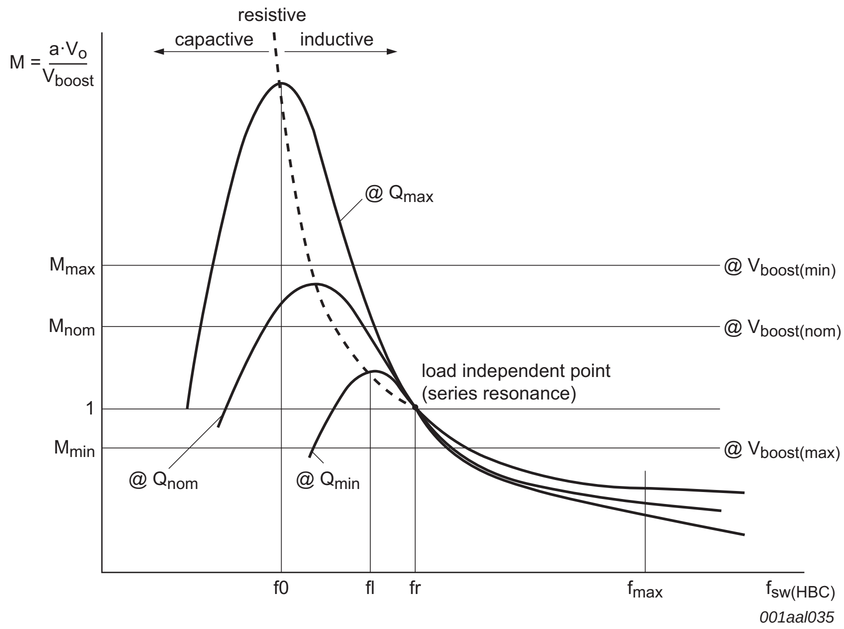
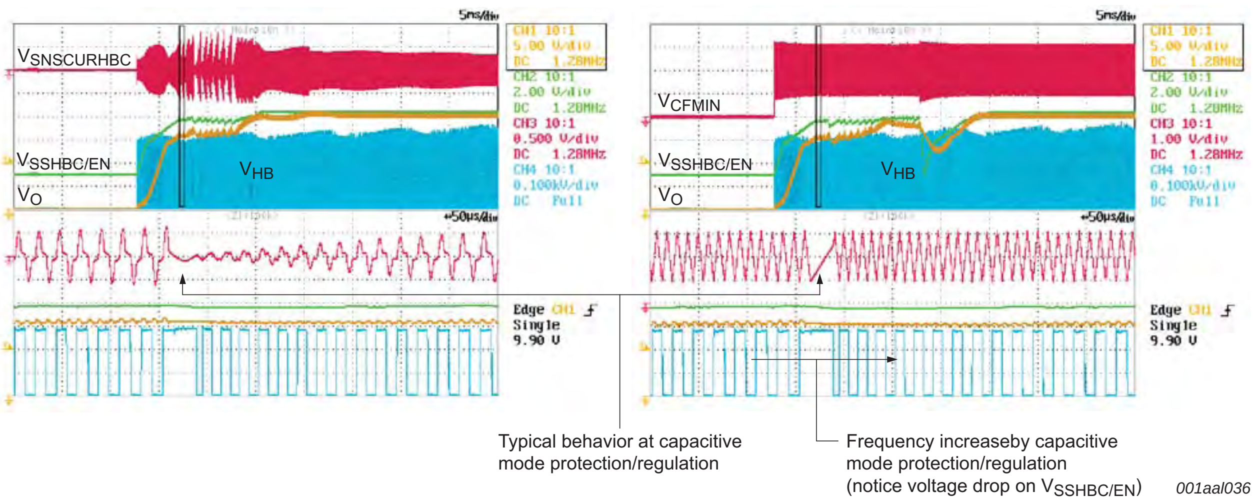


Fig 25. Capacitive/Inductive HBC operating frequencies

The typical slowing of the oscillator in combination with the discharging of $C_{SSHBC/EN}$ can identify a CMR in the SSL4120.



Oscilloscope traces contain normal time-base (top) and zoomed view (bottom)

Fig 26. Typical protection and regulation behavior in capacitive mode (during bad start-up)

8.4 HBC oscillator

The slope controlled oscillator determines $f_{sw(HBC)}$. The oscillator generates a triangular voltage waveform at the external C_{CFMIN} on the pin.

8.4.1 Presets

Two external components determine the frequency range:

- C_{CFMIN}
  Sets the minimum frequency in combination with an internally trimmed current source.
- R_{RFMAX}
  Sets the frequency range and, in combination with C_{CFMIN}, the maximum frequency.

The oscillator frequency depends on the charge and discharge current of C_{CFMIN}. The charge and discharge current consists of a fixed part which determines $f_{min(HBC)}$. In addition, a variable part which depends on the R_{RFMAX} value and V_{RFMAX}.

- V_{RFMAX} is 0 V when the oscillator frequency is minimum.
- V_{RFMAX} is 2.5 V when the oscillator frequency is maximum.
- The value of R_{RFMAX} determines the relationship between V_{RFMAX} and the frequency. It also determines the maximum frequency when V_{RFMAX} = 2.5 V.

The maximum frequency of the oscillator is independent of the settings on CFMIN and RFMAX and is limited internally to a minimum of 500 kHz. Figure 27 shows the relationship between V_{RFMAX} and $f_{sw(HBC)}$ for three different values of C_{CFMIN} and R_{RFMAX}.

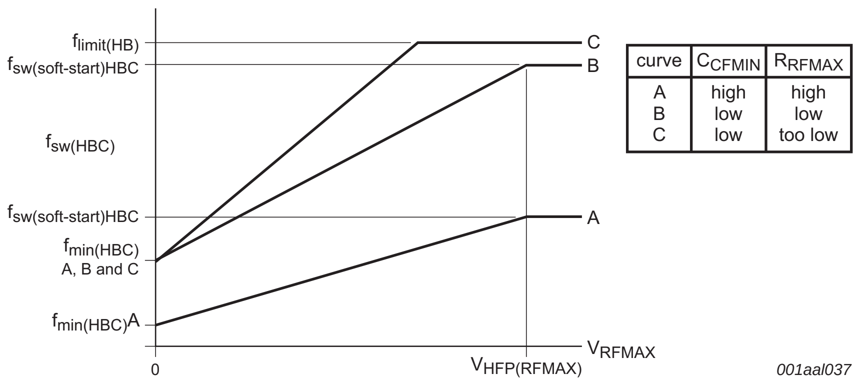


Fig 27. Frequency relationships

8.4.2 Operational control

During operation, the state of the half-bridge node HB controls the oscillator is. An internal slope detection circuit monitors V_{HB}.

The charge current of the oscillator is initially set to a low value of 30 μA. After the start of the half-bridge slope has been detected, the charge current is increased to the normal value corresponding to the operating frequency. Feedback via the SNSFB pin controls the working frequency. Normally, the half-bridge slope starts directly after the switch-off of the MOSFET, the time with the low oscillator current (30 μA) being negligible.

The similarity between GATELS and GATEHS when switching, is that the oscillator signal determines the switch off moment. The V_{HB} sensing circuit determines the switch on moment.

As V_{HB} sensing determines when to switch on, the time between switching one MOSFET off and the other one on, is adaptive. Adaptive non-overlap time (or adaptive dead time) has no influence on the oscillator signal.

The oscillator frequency control comprises time determination between the gate switch off moments (including a small period in which the oscillator current is only 30 μA).

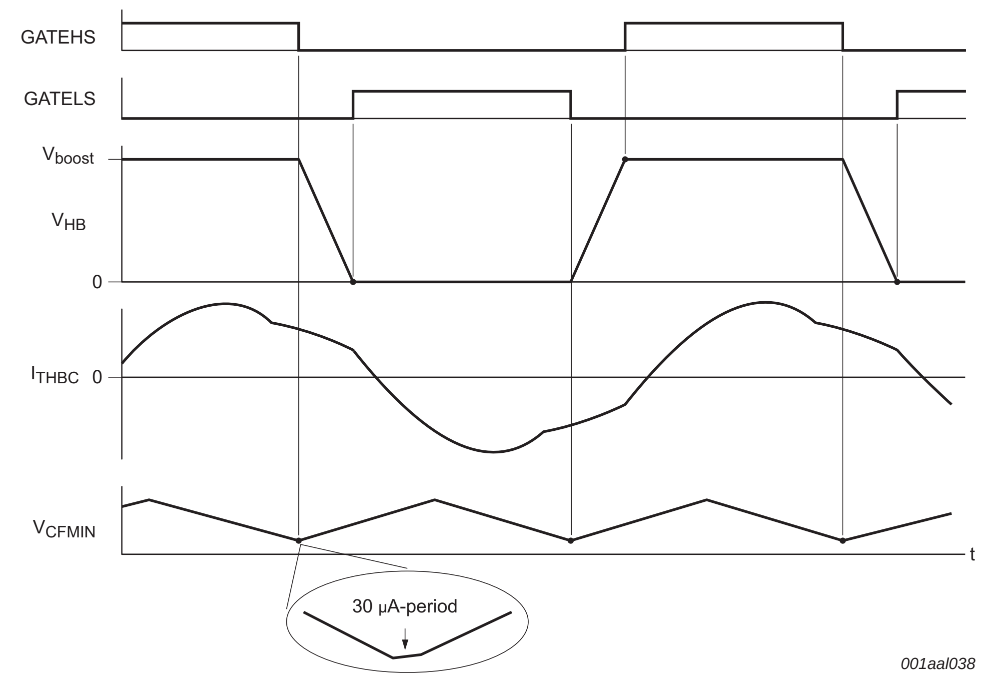


Fig 28. Timing overview of the oscillator and HBC drive

8.4.3 CFMIN and RFMAX

This section explains the method of calculating the values for the C_{CFMIN} and R_{RFMAX}.

8.4.3.1 CFMIN minimum frequency setting

$$f_{osc} = 2 \times f_{sw(HBC)} \quad (25)$$

$$t_{ch} \approx t_{dch} \approx \frac{t_{osc}}{2} \quad (26)$$

$$\Delta V_{osc(CFMIN)} = V_{u(CFMIN)} - V_{l(CFMIN)} = 3\ V - 1\ V = 2\ V \quad (27)$$

$$I_{osc(min)} = 150\ \mu A \quad (28)$$

$$C_{CFMIN} = \frac{I_{osc(min)}}{2 \times 2 \times f_{sw(HBC)min} \times \Delta V_{osc(CFMIN)}} = \frac{150\ \mu A}{8 \times f_{sw(HBC)min}} \quad (29)$$

Example:

Requirement: $f_{sw(HBC)min}$ = 57 kHz

$$C_{CFMIN} = \frac{150\ \mu A}{2 \times 2 \times 57\ kHz \times 2} = \frac{0.00015}{456000} = 329\ pF \quad (30)$$

8.4.3.2 RFMAX maximum frequency setting

$$I_{osc(max)} = 4.7 \times I_{RFMAX(max)} + I_{osc(min)} \quad (31)$$

$$I_{RFMAX(max)} = \frac{V_{fmax(soft-start)RFMAX}}{R_{RFMAX}} \quad (32)$$

$$R_{RFMAX} = \frac{V_{fmax(soft-start)RFMAX}}{I_{RFMAX(max)}} = \frac{2.5\ V}{I_{RFMAX(max)}} \quad (33)$$

Analog to the situation with $I_{osc(min)}$:

$$f_{sw(soft-start)HBC} = \frac{I_{osc(max)}}{4 \times C_{CFMIN} \times \Delta V_{osc(CFMIN)}} = \frac{4.7 \times I_{RFMAX(max)} + I_{osc(min)}}{4 \times C_{CFMIN} \times 2} \quad (34)$$

$$I_{RFMAX(max)} = \frac{8 \times C_{CFMIN} \times f_{sw(soft-start)HBC} - I_{osc(min)}}{4.7} \quad (35)$$

$$I_{RFMAX(max)} = \frac{8 \times C_{CFMIN} \times f_{sw(soft-start)HBC} - 150\ \mu A}{4.7} \quad (36)$$

$$R_{RFMAX} = \frac{2.5\ V}{I_{RFMAX(max)}} = \frac{11.75}{8 \times C_{CFMIN} \times f_{sw(soft-start)HBC} - 150\ \mu A} \quad (37)$$

Example:

Requirement: $f_{sw(soft\text{-}start)HBC}$ = 180 kHz and C_{CFMIN} = 330 pF

$$I_{RFMAX(max)} = \frac{8 \times 330\ pF \times 180\ kHz - 150\ \mu A}{4.7} = \frac{(475\ \mu A - 150\ \mu A)}{4.7} = 69.15\ \mu A \quad (38)$$

$$R_{RFMAX} = \frac{2.5\ V}{69.15\ \mu A} = 36\ k\Omega \quad (39)$$

Remark: The average multiplication factor is 4.7. There is a small deviation in value depending on other parameters and presetting conditions. Practical verification of the result is advised.

8.4.4 RFMAX and High Frequency Protection (HFP)

Normally, the converter does not operate continuously at the preset maximum frequency. This maximum frequency is only used for a short time during soft-start or temporary fault/overload conditions.

When the operating frequency remains at, or close to, maximum frequency for a longer period, a fault condition is assumed and a protection activated.

The HFP senses V_{RFMAX}. This voltage indicates the actual operating frequency. When the frequency is higher than approximately 75 % of the frequency range (V_{RFMAX} = 1.83 V), the protection timer is started.

Remark: During normal regulation, the maximum frequency leads to only 60 % of the present range and V_{RFMAX} is 1.5 V maximum.

8.5 HBC feedback (SNSFB)

A typical power supply application contains mains insulation in the HBC. On the secondary (mains insulated) side, the V_O is compared to a reference and amplified. The SSL4120 is normally placed on the primary side. The output of the error amplifier is transferred to the primary side via an OPTO coupler. The output of the OPTO coupler on the primary side can be connected directly to SNSFB.

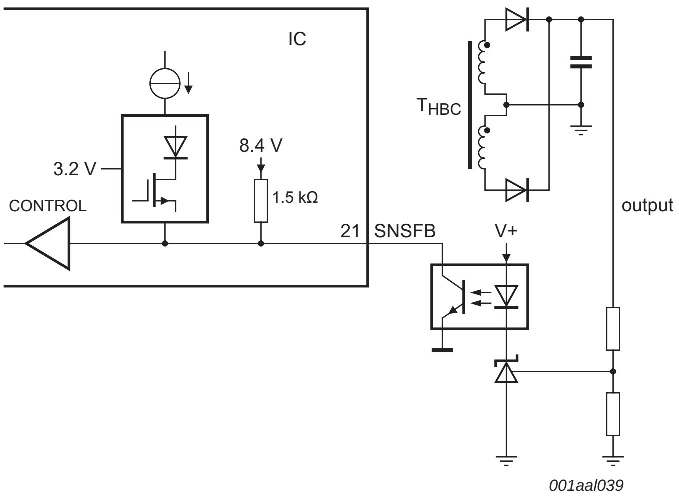


Fig 29. Typical basic SNSFB application

The SNSFB pin supplies the OPTO coupler from an internal voltage source of 8.4 V via an internal series resistor of 1.5 kΩ. This internal series resistance allows spike filtering by an external capacitor at the pin if needed.

The feedback input has a threshold current of 0.66 mA. At this level, $f_{sw(HBC)} = f_{min(HBC)}$ and the 0.66 mA ensures sufficient bias current for correct operation of the optocoupler. $f_{max(soft-start)HBC}$ is reached at 2.2 mA. The frequency range during regulation $f_{max(fb)HBC}$ is approximately 60% of the preset range $f_{max(soft-start)HBC} - f_{min(HBC)}$. The remaining upper part of the frequency range ($f_{sw(HBC)} > f_{max(fb)HBC}$) is only used during soft-start or protection using the SSHBC/EN pin.

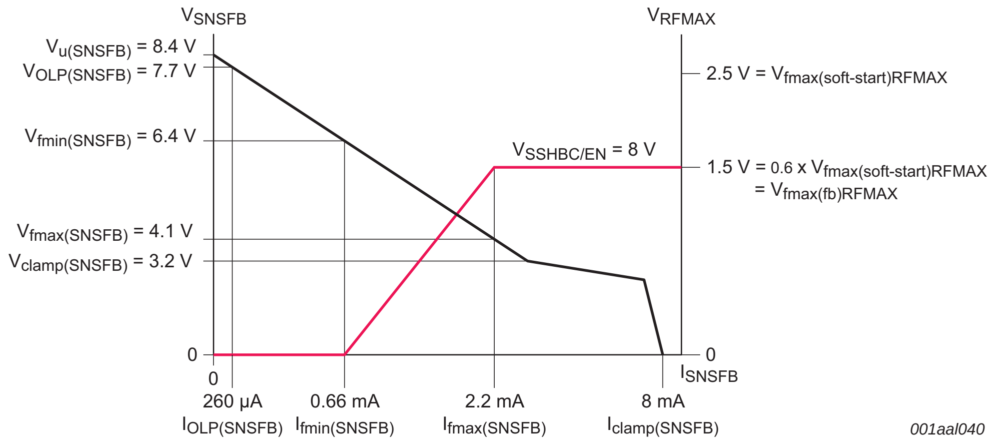
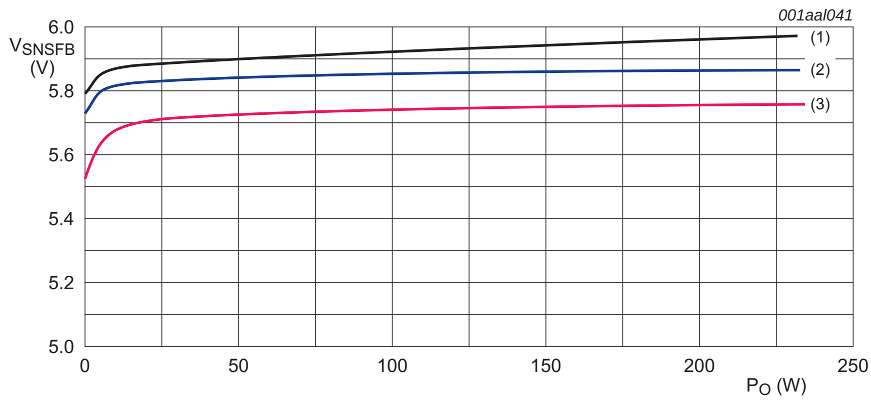


Fig 30. SNSFB V-I characteristics



(1) V_{boost} = 310 V (DC)

(2) V_{boost} = 350 V (DC)

(3) V_{boost} = 390 V (DC)

Fig 31. Examples of V_{SNSFB} to P_o characteristics

8.5.1 HBC Open-Loop Protection (OLP)

The resonant controller of the SSL4120 contains an Open-Loop Protection (OLP). This protection monitors V_{SNSFB}. When it exceeds 7.7 V, the protection timer is started.

In normal operating conditions, the OPTO coupler current is between 0.66 mA and 2.2 mA which pulls down V_{SNSFB}. Due to a fault in the feedback loop, the current can become less than 260 µA which leads to OLP.

8.6 SSHBC/EN soft-start and enable

The SSHBC/EN pin provides the following three functions:

- It enables the PFC ($V_{SSHBC/EN}$ > 1.2 V); PFC and HBC ($V_{SSHBC/EN}$ > 2.2 V)
- It performs an HBC frequency sweep during soft-start from 3.2 V to 8 V
- It provides HBC frequency control during protection

Seven internal current sources operate the frequency control depending on the required action.

- Soft-start + OverCurrent Protection: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA)
- Capacitive mode regulation: high/low discharge (1800 μA/440 μA)
- General: bias discharge (5 mA)

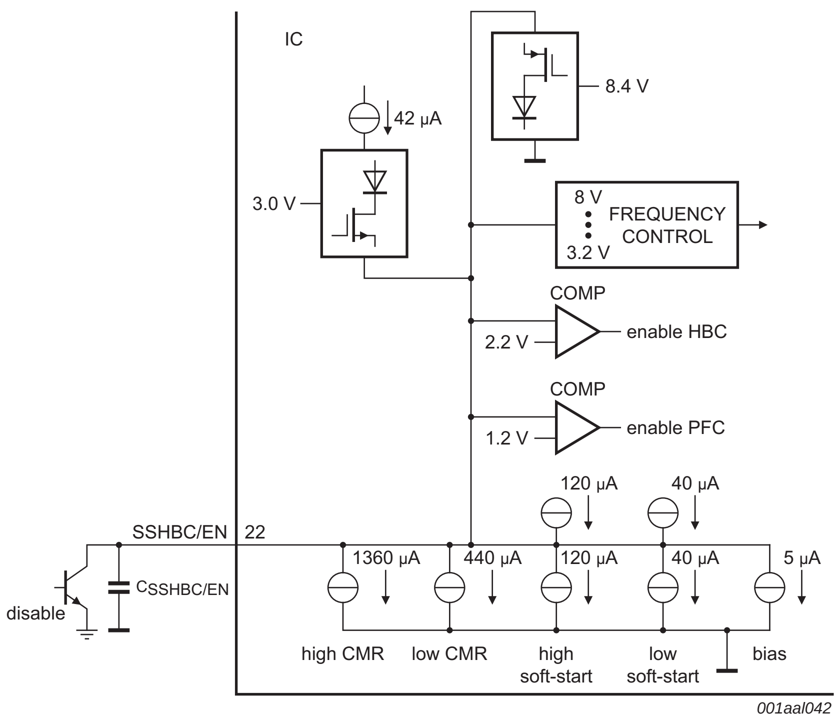


Fig 32. SSHBC/EN: overview of sources, clamps and levels

8.6.1 Switching on and off using an external pull-down function

The SSHBC/EN can be used to switch on and off the converters using an external pull-down function.

This function is often driven using a microcontroller from the secondary side of an optocoupler. The main power supply (PFC and HBC) can be switched off for Standby mode and switched on for normal operation. A separate standby supply must supply the microcontroller functions during Standby mode. It is also possible to switch/keep off the HBC and have the PFC operational.

The SSL4120 also offers the possibility to switch on/off using the SNSOUT function. This function is intended for burst mode operation where the duration of the on-states and off-states are short.

8.6.1.1 Switching on and off using SSHBC/EN

When a voltage is present at pin SUPHV or pin SUPIC, a current from the SSHBC/EN pin charges $C_{SSHBC/EN}$. If the pin is not pulled-down, this current increases $V_{SSHBC/EN}$ to 8.4 V. Since $V_{SSHBC/EN}$ is above the level to enable the operation of PFC (1.2 V) and PFC + HBC (2.2 V), the IC is enabled.

The IC can be disabled by pulling down $V_{SSHBC/EN}$ under 1.2 V. The PFC controller stops switching immediately, but the HBC continues until the low-side stroke is active. The pull-down current must be larger than $I_{pu(SSHBC/EN)}$ = 42 μA.

PFC only active

Only the HBC is disabled when $V_{SSHBC/EN}$ is pulled under the $V_{en(IC)SSHBC/EN}$ = 2.2 V while keeping it above $V_{en(PFC)SSHBC/EN}$ = 1.2 V. The low-side power switch of the HBC is on when the HBC is disabled via the SSHBC/EN pin.

HBC only active

The SSL4120 is not designed to provide this operating mode but it can be realized by forcing a $V_{SNSBOOST}$ higher than 2.63 V (but under 5 V). In this way, the PFC output overvoltage protection is activated and PFC operation stopped. The HBC operates because $V_{SNSBOOST}$ exceeds its start level of 2.3 V boost UVP.

This operating mode is not likely to be required in an application, but it is useful for starting up and debugging purposes during analyses or evaluation.

8.6.1.2 Hold and continue

The SNSOUT function can be used to start and stop the PFC and HBC. This method is intended for burst mode operation to switch off the converters for only a short time. It is possible to operate only the HBC in burst mode or both HBC and PFC simultaneously. The possibilities are similar to SSHBC/EN with the main difference being that HBC continues without soft-start (see Section 9.1).

8.6.2 Soft-start HBC

SSHBC/EN provides the soft-start function for the resonant converter.

The relationship between $f_{sw(HBC)}$ and output current/power is not constant. It is highly dependent on the V_O and V_{boost} voltage and the relationship can be complex. The SSL4120 has a soft-start function to ensure that the resonant converter starts or restarts with safe HBC currents.

The soft-start function forces a start at high HBC frequency so that currents are acceptable in all conditions. The soft-start slowly decreases $f_{sw(HBC)}$ until the output voltage regulation has taken over the frequency control. The limitation of the output current during start-up also limits the output voltage rise and prevents an overshoot.

During soft-start, in parallel to the soft-start frequency sweep, the SNSCURHBC function monitors the primary current and can activate regulation (OCR) in a (temporary) overpower situation.

The soft-start uses $V_{SSHBC/EN}$ as an input. $C_{SSHBC/EN}$ sets the timing (duration) of the soft-start event.

As $V_{SSHBC/EN}$ is also used as enable input, the soft-start functionality is above the enable related voltage levels (see Figure 33).

8.6.2.1 Soft-start voltage levels

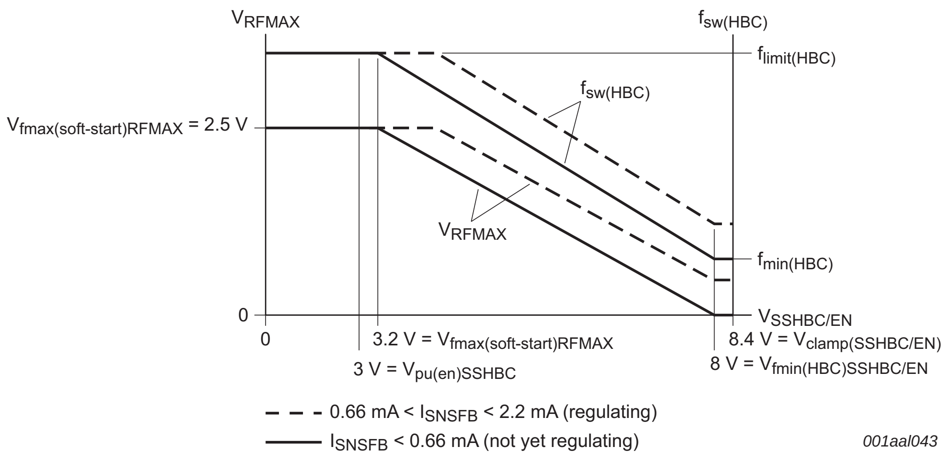


Fig 33. $f_{sw(HBC)}$ related to SSHBC/EN voltage

At start-up, $V_{SSHBC/EN}$ is low which corresponds to the $f_{max(soft-start)HBC}$. During the soft-start procedure, the external capacitor C_{SSHBC} is charged, $V_{SSHBC/EN}$ rises and the $f_{sw(HBC)}$ decreases. The contribution of the soft-start function ends when $V_{SSHBC/EN}$ is above 8 V.

$V_{SSHBC/EN}$ is clamped at 8.4 V and remains at that level during normal operation.

When $V_{SSHBC/EN}$ is reduced during protection or regulation, the voltage is clamped at 3.0 V. The clamping provides a quick response so that the $f_{sw(HBC)}$ can be reduced again. Under 3.2 V the discharge current is reduced to 5 μA.

8.6.2.2 SSHBC/EN charge and discharge

Initially, at start-up the soft-start external capacitor $C_{SSHBC/EN}$ is only charged to obtain a decreasing frequency sweep from $f_{max(soft-start)HBC}$.

Besides the soft-start function, SSHBC/EN is also used for regulation purposes such as OCR. Therefore the voltage on $C_{SSHBC/EN}$ can vary by charging and discharging it by internal current sources.

For example, in case OCR, a continuous alternation between charging and discharging $C_{SSHBC/EN}$ capacitor occurs. $V_{SSHBC/EN}$ can be regulated in this way overruling the signal on the feedback input SNSFB.

The charge and discharge current can have a high value ±160 μA or a low value ±40 μA. The SSL4120 two-speed soft-start sweep allows a combination of a resonant converter short start-up time and stable regulation loops such as OCR.

In some cases, there can be a situation where OCR is activated during the soft-start sequence. This results in a feedback controlled or corrected soft-start.

The fast charge/discharge speed is used for the upper frequency range where $V_{SSHBC/EN}$ < 5.6 V. In the upper frequency range, the current and power in the converter do not react strongly to frequency variations.

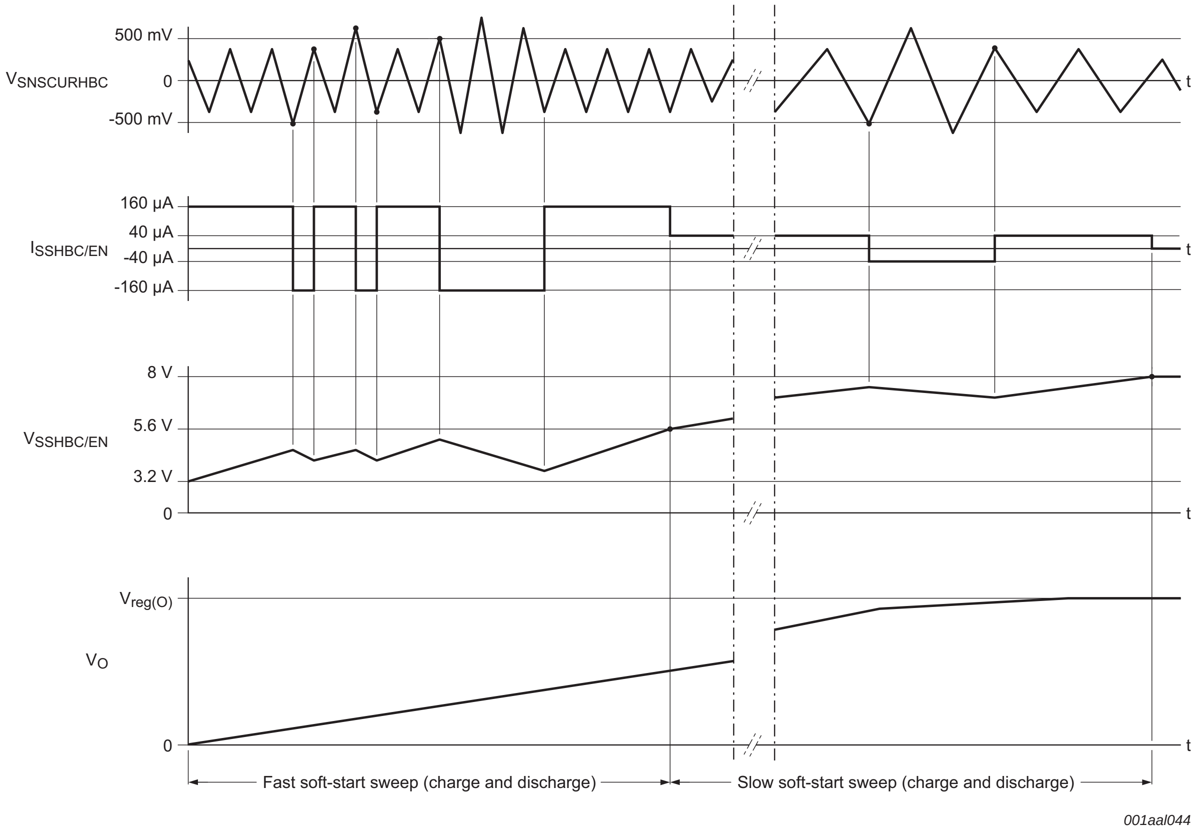


Fig 34. OverCurrent Regulation (HBC output OCR) during start-up

The slow charge and discharge speed is used for the lower frequency range where $V_{SSHBC/EN}$ is above 5.6 V. In the lower frequency range, the current in the converter reacts strongly to frequency variations.

Burst mode

The soft-start capacitor $C_{SSHBC/EN}$ is not charged or discharged during the non-operation time in burst mode operation. $V_{SSHBC/EN}$ does not change during this time.

8.6.2.3 SNSFB, SSHBC/EN and soft-start reset - operating frequency control

The SNSFB and SSHBC/EN pins can simultaneously control $f_{sw(HBC)}$. SSHBC/EN is dominant to provide protection and soft-start capability. Additionally, there is an internal soft-start reset mechanism that overrules both SNSFB and SSHBC/EN control inputs and immediately sets the HBC frequency to $f_{max(soft-start)HBC}$.

8.6.2.4 Soft-start reset

Some protections require a fast correction of the HBC operating frequency to a higher value but they do not require switching stops. OCP is an example (see Table 4).

When OCP is active, the oscillator control input is disconnected $C_{SSHBC/EN}$. $f_{sw(HBC)}$ is immediately set to maximum. In most cases, changing to $f_{max(soft\text{-}start)HBC}$ restores safe switching operation. When $V_{SSHBC/EN}$ drops under 3.2 V, the control input of the oscillator reconnects to $C_{SSHBC/EN}$ and normal soft-start sweep follows. Figure 35 shows the soft-start reset and the two-speed frequency downward sweep.

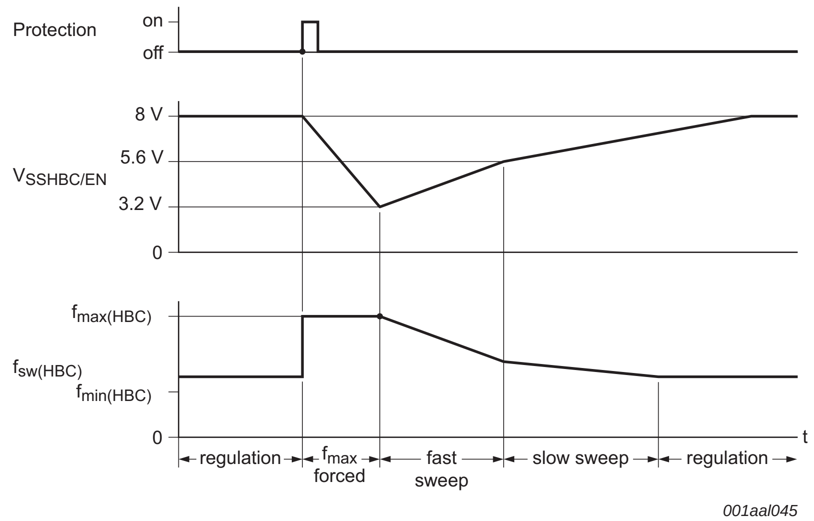


Fig 35. Soft-start reset and two-speed soft-start

The soft-start reset is also used to ensure a safe start-up at maximum frequency $f_{soft\text{-}start(HBC)}$ when the HBC is enabled using SSHBC/EN or after a restart. The soft-start reset is not used when the operation has been stopped for burst mode.

8.7 HBC overcurrent protection and regulation

Measurement of the primary resonant current indicates the level of output power that the converter generates. During a fault or output overload condition, this current often increases considerable. By monitoring this current and then taking appropriate action, the converter can remain operational during a temporary fault or overload condition.

The resonant controller of the SSL4120 has two functions when in an overcurrent condition:

- Half-Bridge OverCurrent Regulation (HB OCR) slowly increases $f_{sw(HBC)}$ and the protection timer is started
- Half-Bridge OverCurrent Protection (HB OCP) steps to $f_{max(soft\text{-}start)HBC}$

A V_{boost} compensation function is included to reduce the variation in the preset protection level of the resonant current.

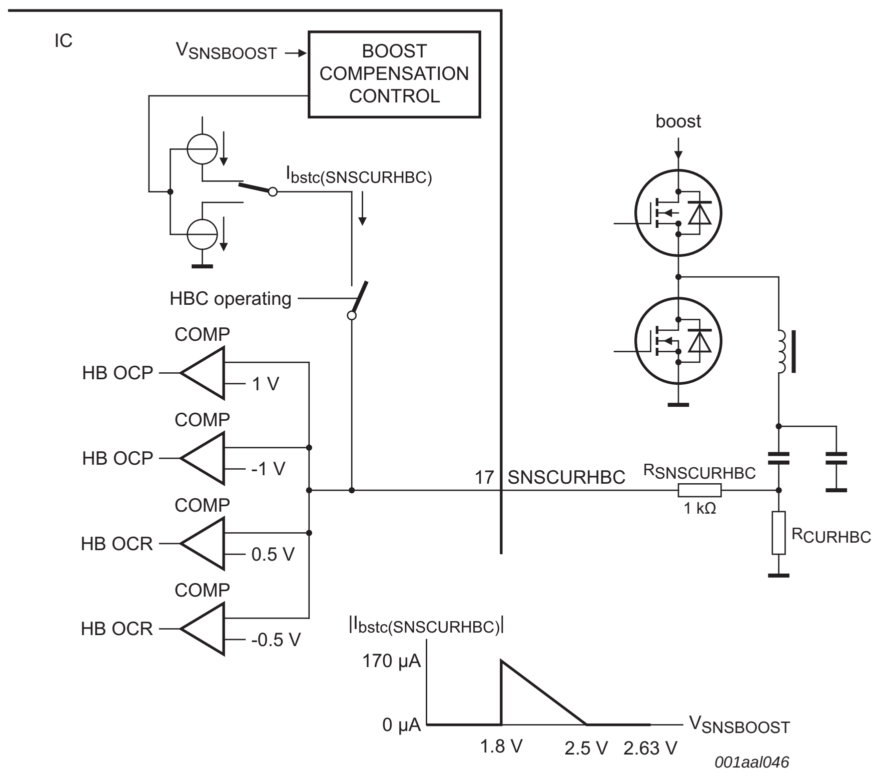


Fig 36. SNSCURHBC functions

8.7.1 HBC overcurrent regulation

The lowest comparator levels of ±0.5 V at the SNSCURHBC pin belong to the OverCurrent Regulation (OCR) level. There is a comparator for both the positive and negative polarity. If either level is exceeded, discharging the soft-start capacitor slowly increases the frequency. Every time the OCR level is exceeded, this state is latched until the next stroke and the soft-start discharge current is enabled. When both the positive and negative OCR levels are exceeded, the soft-start discharge current flows continuously. The operating frequency is slowly increased until the resonant current value just reaches the preset value.

The behavior during OCR can be observed on $V_{SSHBC/EN}$ as a resultant regulation voltage.

When an OCR situation is present for a long time, a serious fault condition is assumed. During OCR, the protection timer is activated. The charging of the protection timer is active approximately a half period cycle after the ±0.5 V level is exceeded. If the detection levels are continuously exceeded, the timer is charged continuously. However, if the detection levels are only exceeded occasionally, the timer is charged as required. Refer to Section 10.3.3.4 for details on charging and discharging of the protection timer. The restart state is activated when V_{RCPROT} reaches the protection level of 4 V.

8.7.1.1 Start-up

The overcurrent regulation is effective for limiting the output current during start-up. A smaller soft-start capacitor can be chosen which allows faster start-up. The small soft-start capacitor can result in an excessive output current but the OCR function can slow down the frequency sweep to keep the output current within the limits.

8.7.2 HBC overcurrent protection

In most cases, the HB OCR is able to keep the current under the set maximum values. However, HB OCR cannot be fast enough to limit the current for certain error conditions. Half-Bridge OverCurrent Protection (HB OCP) is implemented to protect against those error conditions.

The internal HB OCP level is set at ±1 V for $V_{SNSCURHBC}$. This level is higher than the HB OCR level of ±0.5 V. When the HB OCP level is reached, $f_{sw(HBC)}$ immediately jumps to $f_{max(soft\text{-}start)HBC}$ using a soft-start reset procedure. The frequency jump is followed by a normal sweep down. The selected $f_{max(soft\text{-}start)HBC}$ value must limit the output power under these conditions.

The operation during HB OCP can be observed on $V_{SSHBC/EN}$ as a new soft-start. Depending on the load, overload or fault condition during this new soft-start, OCR or OCP can be reactivated.

8.7.3 SNSCURHBC and V_{boost} compensation

The primary current, also called resonant current, is sensed via pin SNSCURHBC. It senses the momentary voltage across an external current sense resistor R_{CURHBC}. The use of the momentary current signal allows a fast OCP and simplifies the stability of the OCR. The OCR and OCP comparators compare $V_{SNSCURHBC}$ to the maximum positive and negative values.

The primary current is higher for the same output power when V_{boost} is low. A boost compensation function is included to reduce the dependency of the protected output current level for V_{boost}. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage across the series resistor $R_{SNSCURHBC}$. A typical value for $R_{SNSCURHBC}$ is 1 kΩ.

The amplitude of the current is linearly dependent on V_{boost}. At $V_{boost(nom)}$, the current is zero and the voltage across is also present on the SNSCURHBC pin. At the V_{boost} start level $V_{SNSBOOST}$ = 1.8 V and the current is maximum 170 μA. The direction of the current, sink or source, depends on the active gate signal. The voltage across $R_{SNSCURHBC}$ reduces the amplitude of $V_{SNSCURHBC}$, resulting in a higher effective current protection level. The value of $R_{SNSCURHBC}$ sets the amount of compensation.

8.7.4 Current measurement circuits

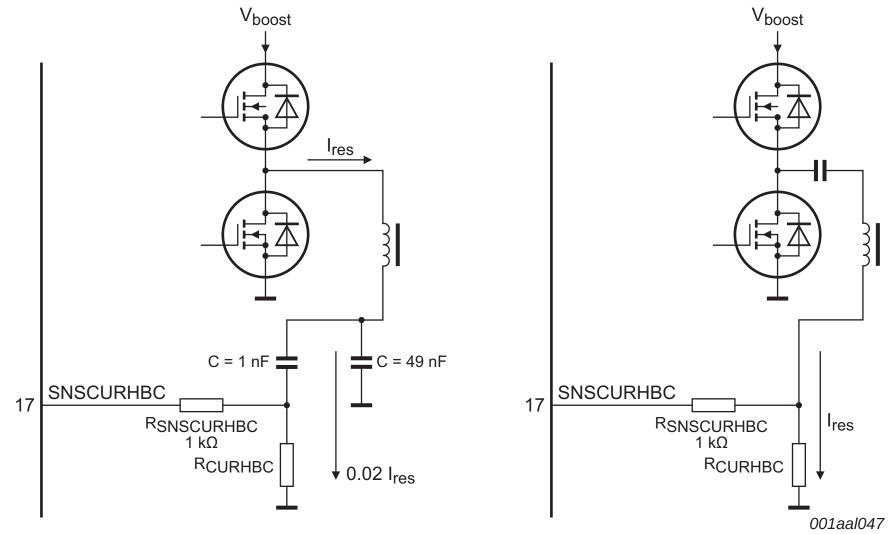


Fig 37. SNSCURHBC: half-bridge current measurement configurations

8.7.5 SNSCURHBC layout

As SNSCURHBC must be able to cycle-by-cycle sense the measurement signal at higher frequencies, it is easily influenced by disturbances. Place $R_{SNSCURHBC}$ close to the IC to reduce the length of the PCB track that can pick up interfering signals. This placement prevents interference on this input. As the impedance of R_{CURHBC} is normally low, the PCB track between $R_{SNSCURHBC}$ and R_{CURHBC} is not critical regarding disturbance.

9. Burst mode operation

In dimmable LED driver applications with current controlled output, the burst mode operation can be used to reach low output currents. Burst mode can also be used to improve efficiency at low output loads.

By temporarily interrupting the switching, losses during idle time are minimized. Because the average power needed at the output is low, it is easy for the converter to deliver it during a short conversion time (a burst).

The burst mode operation of the SSL4120 is based on interrupting the switching while maintaining regulation. With an external comparator, the regulation V_{SNSFB} can be monitored to determine when to stop and start switching. Stopping and starting again can be controlled via the SNSOUT pin. When starting again after interruption, no soft-start is applied as the system is still in regulation (close to the regular working point). The regulation-loop of the system (normally by the output voltage or current) determines the timing of burst switching on and off. In this way, a small ripple on the output voltage/current is deliberately created during burst mode.

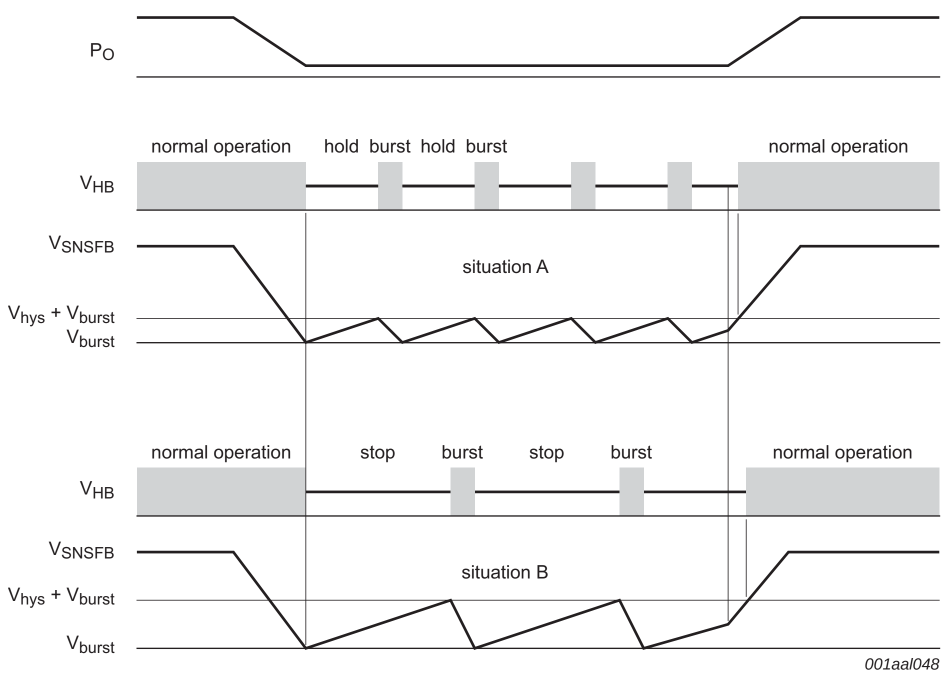


Fig 38. Principle of burst mode operation with V_{SNSFB} and comparator levels

9.1 SNSOUT controlled burst mode

The HBC (and the PFC) of the SSL4120 can be operated in burst mode. In burst mode, the converters operate for a limited time, followed by a period of non-operation. Burst mode operation increases the efficiency during low load conditions and can be used for current controlled outputs.

A simple external circuit that uses the information from the feedback loop can detect the low load condition. The detection circuit pulls down V_{SNSOUT} to pause the operation of the SSL4120 for a burst off-time.

V_{SNSOUT} has two levels for burst mode operation:

- burst-off level for HBC = 1.1 V

  Under this level, only the HBC pauses its operation. Both high-side and low-side power switches are off and the PFC continues operation. Above this level, the HBC resumes operation and it does not execute a soft-start sequence.
- burst-off level for PFC = 0.4 V

  Under this level, the PFC also pauses its operation using a soft-stop. The HBC is already paused. Above this level, the PFC resumes operation with a soft-start.

Keep the PFC always active for better THD and Power Factor for dimmable lighting applications. Diode D1 in Figure 39 ensures that the PFC is not using burst mode. A 100 μA current from the SNSOUT pin keeps the voltage at a 1.5 V internal clamp voltage which is above both burst mode levels. This function avoids burst mode activation when the output voltage is not yet present. The impedance between the SNSOUT pin and ground must therefore be larger than 20 kΩ.

9.2 External comparator for burst mode implementation

A comparator circuit between SNSFB and SNSOUT can do the implementation of the burst mode.

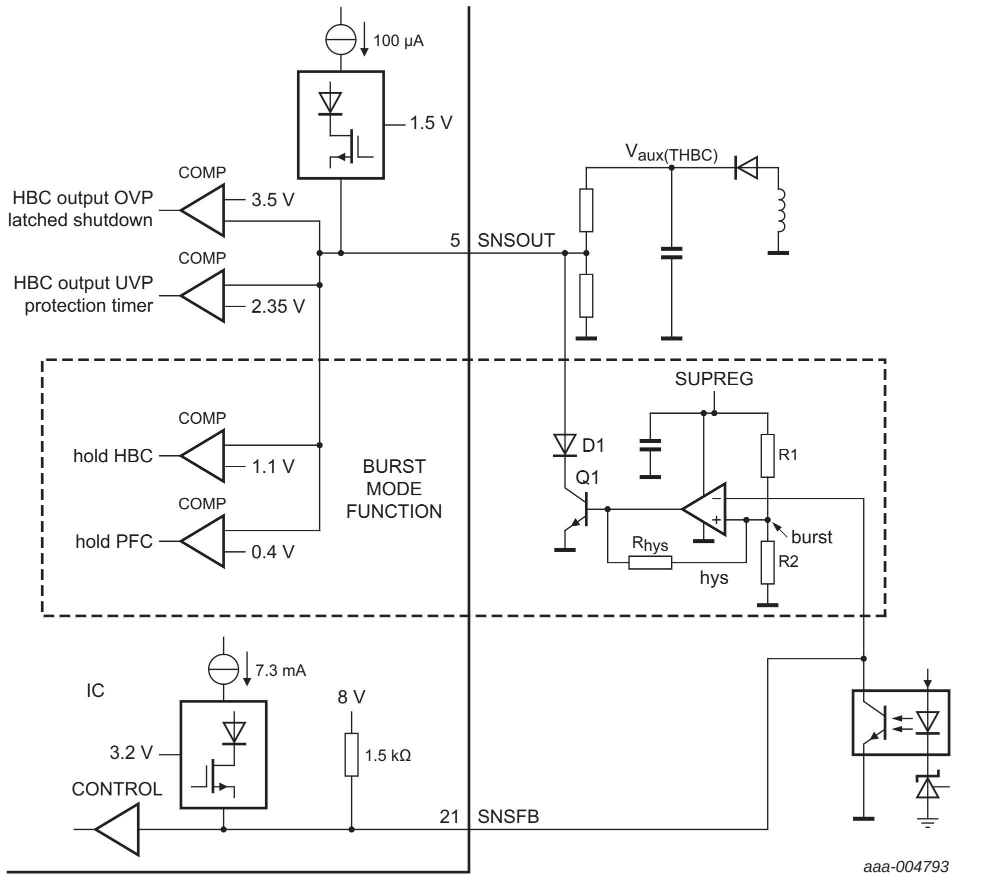


Fig 39. Principle of burst mode operation with SNSFB and comparator levels

The comparator input monitors the regulation voltage V_{SNSFB} to a preset burst voltage value by R1 and R2: V_{burst}. When the HBC power output power is low, V_{SNSFB} decreases and when it reaches V_{burst} the switching stops by pulling down V_{SNSOUT} to ground. When the switching stops, no energy is converted and V_O drops. V_{SNSFB} then increases again. When V_{SNSFB} reaches V_{burst} + V_{hys} (R_{hys} sets the voltage hysteresis) switching resumes.

When the power delivered during a burst is larger than needed for the output, V_{SNSFB} quickly decreases, stopping the switching at V_{burst}. The time needed for V_{SNSFB} to reach V_{burst} is dependent on V_O and its load.

When P_O increases to high levels, normal operation is resumed because V_{SNSFB} can no longer reach V_{burst}.

9.3 Advantages of burst mode for HBC

The main reasons for applying burst mode in a resonant converter are to:

- reduce the current output current of a current controlled output
- improve the efficiency at low output power by reducing the power losses

The graphs in Figure 40 and Figure 41 show the improvement principle in an example of a 250 W resonant converter including (non-bursting) PFC.

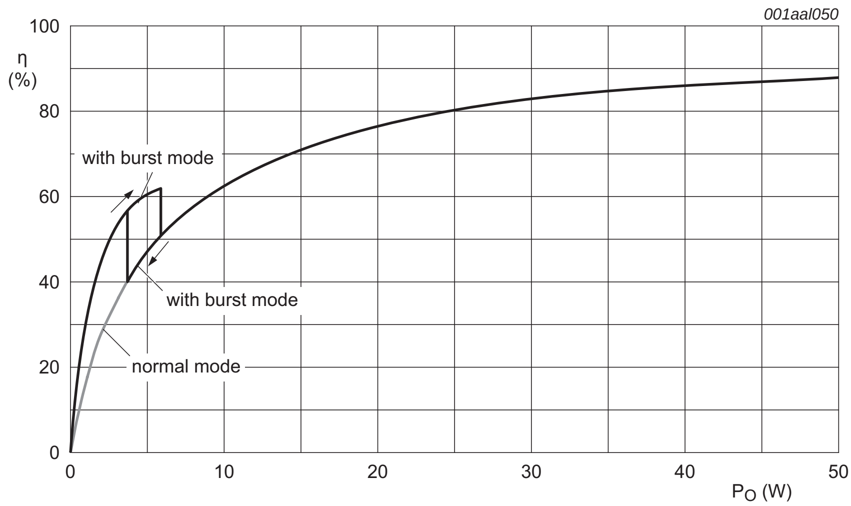


Fig 40. Improved efficiency by HBC burst mode in a 250 W converter

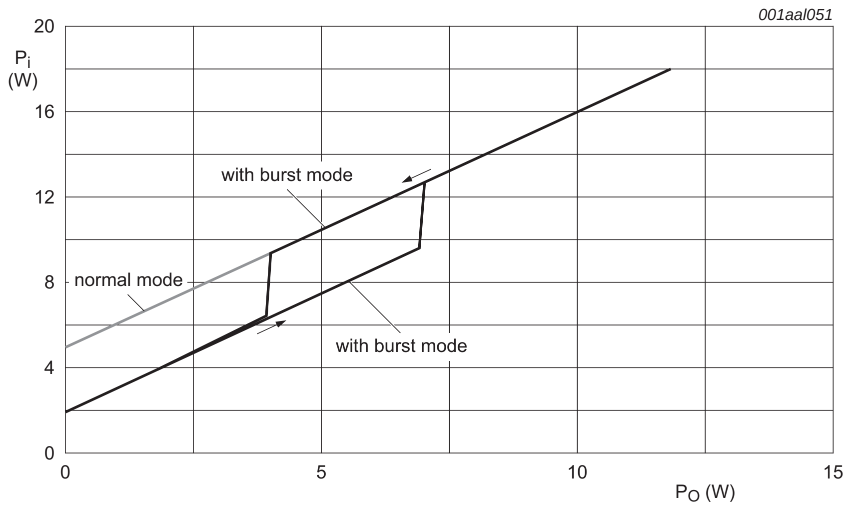


Fig 41. Reduced losses by HBC burst mode in a 250 W converter

9.4 Advantages of burst mode for HBC and PFC simultaneously

The SSL4120 provides a burst mode system that simultaneously switches the HBC and PFC. In this way, during the burst period, the power is transferred directly from the input to the output. The HBC determines the repetition time of the burst and the PFC follows. During the burst period, the PFC operates in normal regulation.

PFC bursting obtains extra reduction in power consumption. Figure 42 to Figure 44 show examples of the results.

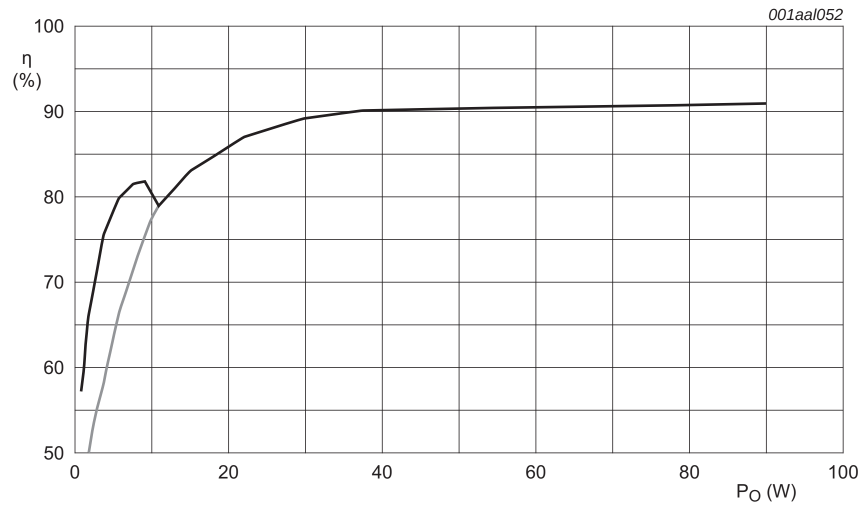


Fig 42. Increased efficiency at low output power in burst HBC and PFC (90 W converter)

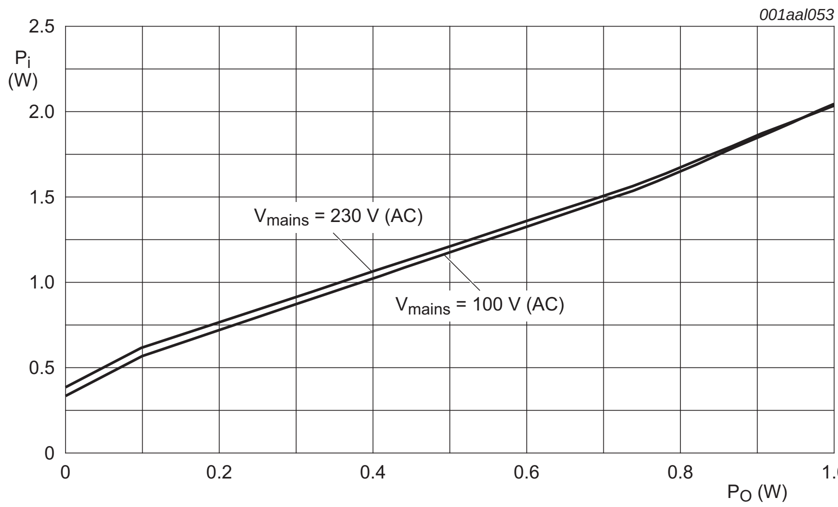


Fig 43. Remaining 90 W converter losses in burst mode

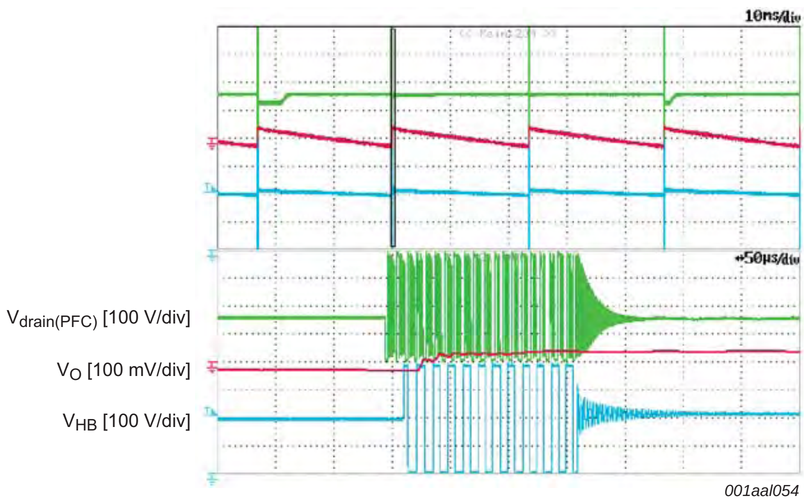


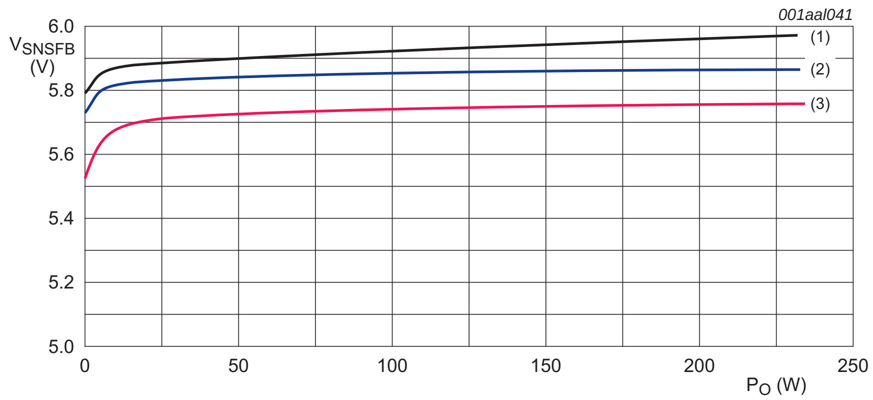
Fig 44. Simultaneous HBC and PFC burst mode operation (including output voltage ripple)

9.5 Choice of V_{burst} and V_{hys} levels

Set the power levels for bursting using an external comparator for dimensioning the burst mode. Figure 39 shows a typical comparator circuit with hysteresis.

The basic choice for the voltage level at which the comparator must be active (V_{burst}) can be made experimentally.

The input voltage of the resonant converter V_{boost} (see Figure 46) influences the relationship between V_O and V_{SNSFB}.



(1) V_{boost} = 310 V (DC)
(2) V_{boost} = 350 V (DC)
(3) V_{boost} = 390 V (DC)

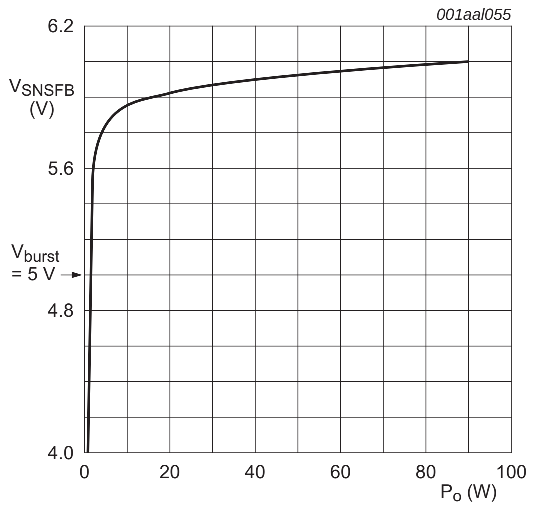
Fig 45. V_{SNSFB} to P_O characteristic examples

Aspects that influence the voltage levels (V_{burst} and V_{hys}) of burst mode:

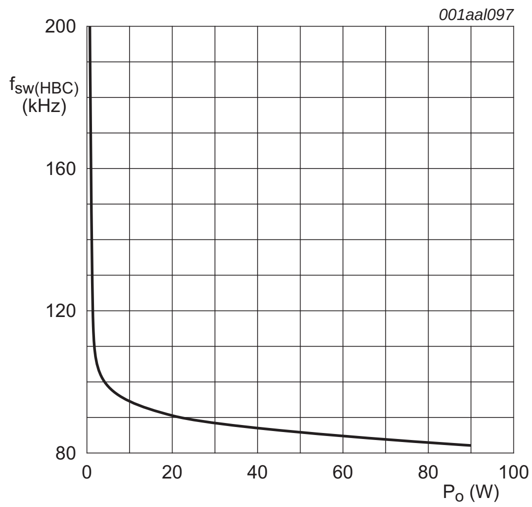
- HBC input voltage V_{boost}
- V_{SNSFB} regulation levels in combination with the preset frequency range determined using R_{RFMAX} and C_{CFMIN}
- Dynamic behavior of the regulation during burst mode and during normal operation (large load variations)

9.6 Output power - operating frequency characteristics

Figure 46 show that it is critical to make a design choice for a certain V_{SNSFB} to start bursting. This kind of characteristic has a risk, that because of the spread, that the system can remain in burst mode or never enter it at all. The dimensioning of the LLC can be made more suitable for burst mode. The standard approach is to design the system in such a way that it cannot regulate to no-load, even at the highest $f_{sw(HBC)}$. During the lowest loads, the $f_{sw(HBC)}$ required for regulation must become infinite. A voltage level for V_{burst} can then easily be chosen to ensure that burst mode is activated at the lowest load and that the remaining load conditions operate in normal mode. Burst mode now enables the system to operate at no-load.



V_{SNSFB} as a function of P_O



$f_{sw(HBC)}$ as a function of P_O

Fig 46. Normal mode output power characteristics (Adapted for easy implementation of burst mode comparator level detection)

9.7 Reduced V_{SUPHS} during burst

During the idle time C_{SUPHS} is not charged.

During normal operation, each time the half-bridge node HB is switched to ground level, the bootstrap function of the external diode between SUPHS and SUPREG charges C_{SUPHS}. In burst mode, there are periods of non-switching and therefore no charging of C_{SUPHS}. During this time, the circuit supplied using SUPHS slowly discharges C_{SUPHS}. When a new burst starts, V_{SUPHS} is lower than in normal operation. During the first switching cycles, C_{SUPHS} is recharged to its normal level. It is important that, during these first recharge cycles, V_{SUPREG} does not drop under the protection level of 10.3 V.

9.8 Audible noise

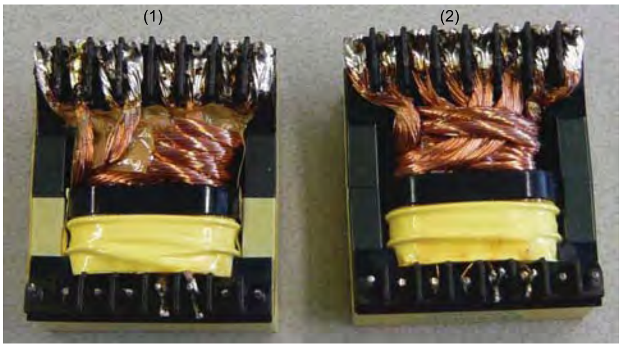
As the burst mode is normally used when the output power is low, the converted energy does not contribute much to generate audible noise. The magnetization current however is still present during low loads and is the dominant energy during burst mode. Switching the converter sequences on and off continuously at a certain speed and duration can lead to audible noise. The main mechanism for producing noise is the interruption of magnetization current sequences leading to a mechanical force. This interruption is especially the case on the core of the resonant transformer which starts acting as a loudspeaker.

When burst mode is applied during higher output power conditions, the converted energy also contributes and leads to an increased risk of audible noise.

9.8.1 Measurements in the resonant transformer construction

It is necessary to adapt the mechanical transformer construction to prevent problems with audible noise under specific conditions.

One measure is to adhere the core parts to each other using a material with damping (vibration absorbing) properties. A combination can be made with the air gap construction. Other vibration damping measures can also help when audible noise is a critical issue for a product.



(1) Left-hand transformer with glue to reduce audible noise

(2) Right-hand transformer has standard construction

Fig 47. Transformer construction

9.8.2 Burst power-dependent noise level

The amount of audible noise is related to the amount of energy in each burst.

At low output power, the magnetization current of the resonant converter determines the amount of energy. The amount of transferred energy is low. Use burst mode only at low power (a few watts output power) to avoid problems with audible noise. When the transition level between Normal mode and burst mode is chosen at a higher output power, the level of audible noise is larger.

Overshoot on feedback voltage

When the output load is increased, the system reverts to normal operation. The transition from burst mode to Normal mode is based on the feedback voltage. In certain burst conditions, the feedback voltage can overshoot. This feature keeps the system in burst mode at higher output power levels than intended. As the power level in this situation is larger, the amount of noise is also larger.

9.9 PFC converter and resonant converter simultaneous bursting

When in the burst mode, PFC operation stops while the resonant converter is not switching. In most cases, this saves extra energy consumption by reduced switching losses from the PFC converter.

The total system (PFC and resonant) behavior in burst mode can differ from the situation when only the resonant converter would operate in burst mode. Although this results in good performance, there are a number of interactions.

9.9.1 PFC output voltage variations

When bursting the PFC converter, the resonant control system determines the timing. This feature results in a situation where the PFC cannot maintain a constant V_{boost}. The burst operation limits the time during which the PFC can convert power. This time can be too short. The result is either a lower or a varying V_{boost}. This voltage also has consequences for the resonant converter as its input voltage is not the same. The working conditions change towards a new balance.

The resonant converter must be able to remain operational during these conditions.

It is important to check that the resonant controller has not been stopped because $V_{SNSBOOST}$ is too low. Triggering the boost UVP level on SNSBOOST causes an unacceptable voltage decrease in the output of the resonant converter.

9.9.2 PFC burst duration

Normally a square V_{SNSOUT} pulse leads to equal operation time for PFC and HBC (see Figure 44). If a longer PFC operating time is needed for correct balance, it can be achieved by adding a capacitor on SNSOUT to create a ramp signal. The PFC starts at a voltage of 0.4 V, allowing a longer PFC operating time.

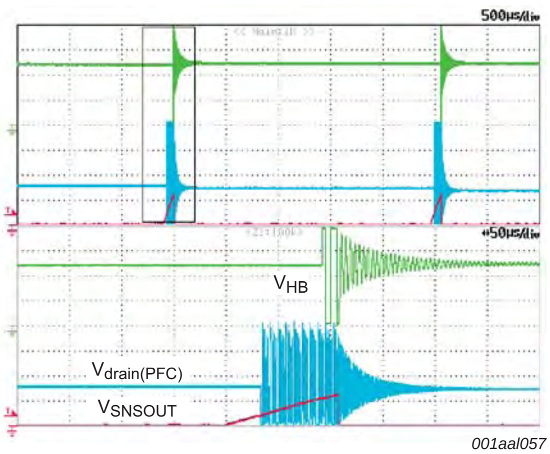


Fig 48. Example of longer burst time for PFC using ramp on SNSOUT

9.9.3 Switching between burst and normal operation

Interaction between the PFC and resonant converters in burst mode can lead to a situation where the system alternates between burst and normal mode for certain output power conditions.

9.9.4 Audible noise during mode transition

As a result of the previously mentioned interactions, a stable situation can occur during the following operating modes, alternating in time:

- Resonant burst with short burst time without PFC burst (time too short to start).
- Resonant burst with long burst time and PFC burst.
- Normal operation for resonant and PFC bursts.

Transitions between modes and variations within a certain mode have a corresponding effect on audible noise.

9.10 Design guidelines for burst mode operation

Design for a stable PFC (nominal) output voltage V_{boost} during burst mode.

Best efficiency is achieved when the number of cycles for each burst is as small as possible (only a few cycles).

Best efficiency is achieved by resistively tuning the comparator circuit to preset the V_{burst} and V_{hys}.

System and component tolerances play a significant role in variations of performance in production.

The HBC regulation feedback loop can be optimized for Normal mode. Any additional filtering can be done in the comparator circuit. However, use it moderately so control of the situation can be maintained during the burst mode operation.

9.11 Enable/disable burst mode

In microcontroller operated applications such as DALI controlled systems, a clear separation is made between normal operation and standby operation. An enable/disable function can be added to avoid the resonant converter entering burst mode when short periods of low load occur during normal operation. An extra enable/disable switch function in the comparator circuit implements the enable/disable function.

9.12 Unused burst mode

When the burst mode is not required, not applying a circuit to switch SNSOUT leaves the burst mode function inactive. This can be done by removing D1 and/or Q1 from Figure 39.

10. Protective functions

Most protection functions are discussed in the chapters of the systems of which they are a part. Table 4 contains an overview of links to the corresponding places in this document. In the following paragraphs the remaining, more independent, protection functions are discussed.

10.1 Protection overview

Table 4. Overview of protection functions with links

Part	Symbol	Protection	Action	Link
IC	SUPIC UVP	SUPIC undervoltage protection	SUPIC IC disable	Section 5.2.2
IC	SUPREG UVP	SUPREG undervoltage protection	IC disable	Section 5.5
IC	UVP supplies	undervoltage protection supplies	IC disable and reset	-
IC	SUPIC SCP	SUPIC short circuit protection	low HV start-up current	Section 5.2.2
IC	HBC output OVP	HBC overvoltage protection output	IC shutdown	Section 10.3.1
IC	HBC output UVP	HBC output undervoltage protection	IC restart after protection time	Section 10.3.2
IC	IC OTP	IC overtemperature protection	IC disable	Section 10.2.1
PFC	PFC OCR	PFC overcurrent regulation	PFC switch-off cycle-by-cycle	Section 7.4
PFC	mains UVP	mains undervoltage protection	PFC hold switching	Section 7.6.1
PFC	PFC boost OVP	PFC boost overvoltage protection	PFC hold switching	Section 7.5
PFC	PFC boost SCP	PFC boost short circuit protection	IC restart	Section 7.2.2
HBC	HBC boost UVP	HBC boost undervoltage protection	HBC disable	Section 8.1
HBC	HBC OLP	HBC open-loop protection	IC restart after protection time	Section 8.5.1
HBC	HBC HFP	HBC high frequency protection	IC restart after protection time	Section 8.4.4
HBC	HBC OCR	HBC overcurrent regulation	HBC frequency increase IC restart after protection time	Section 8.7.1
HBC	HBC OCP	HBC overcurrent protection	HBC step to maximum frequency	Section 8.7.2
HBC	HBC CMR	HBC capacitive mode regulation	HBC increase frequency	Section 8.3.2
HBC	HBC ANO	HBC adaptive non-overlap	HBC prevent hazardous switching	Section 8.3.1

10.2 IC protection

10.2.1 OverTemperature Protection (IC OTP)

The SSL4120 contains an accurate internal overtemperature protection. When the junction temperature exceeds the overtemperature level of 140 °C, the IC enters the Thermal hold state. The Thermal hold state is left when the temperature has dropped by 10 °C.

The circuit resumes operation with a complete restart including a soft-start of PFC and HBC.

10.2.2 Latched protection

Only an overvoltage detection on SNSOUT leads to a latched shutdown protection state. V_{SNSOUT} must exceed 3.5 V to enter a latched shutdown state.

10.2.2.1 Resetting a latched protection shutdown state

When a latched protection shutdown state has occurred, it is reset by one of the following actions:

- V_{SUPIC} drops under 7 V and V_{SUPHV} is lower than 7 V
- $V_{SNSMAINS}$ drops under 0.8 V and then rises above 0.85 V
- $V_{SSHBC/EN}$ is pulled down under 1.2 V ($V_{en(PFC)SSHBC/EN}$)

In most cases, a reset using $V_{SNSMAINS}$ is activated before a reset by SUPIC/SUPHV. This enables a restart before V_{boost} is discharged (fast shutdown reset).

When resetting by interrupting the mains input, some time is still required to lower $V_{SNSMAINS}$ under 0.8 V. The time depends on the component values used on the SNSMAINS circuit and the value V_{mains}. An additional aspect is a possible leakage of the bridge rectifiers that allows the charging of SNSMAINS by the rectified mains voltage capacitor (reverse current through the diodes). At moderate rectifier temperature, the charging of SNSMAINS can be neglected but at high temperature it is a significant parameter.

A reset possibility by external control (for example a microcontroller) is available using the SSHBC/EN function.

10.3 SNSOUT protection

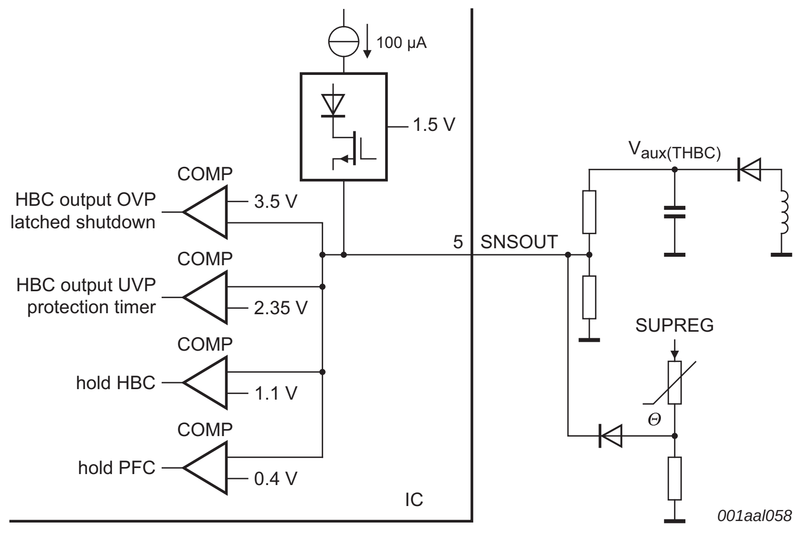


Fig 49. SNSOUT protection

10.3.1 OverVoltage Protection (HBC output OVP)

The SSL4120 has an OVP intended for monitoring the HBC V_O. HBC output OVP is one of the functions that is combined on the SNSOUT pin.

10.3.1.1 OVP using the T_{HBC} auxiliary winding

When dealing with a mains insulated converter, V_O can be measured via the T_{HBC} auxiliary winding. A special transformer construction is required to measure accurately the secondary voltage on the primary circuit side.

It is important that this winding has a good coupling with the secondary windings and a minimum coupling with the primary winding. In this way, a good representation of the output voltage situation is obtained (see Section 5.3.3.1 and Figure 6).

Triple insulated wire can be used to meet the mains insulation requirements.

10.3.1.2 Principle of operation

The voltage is sensed at the SNSOUT pin via an external rectifier and resistive divider. Overvoltage is detected when V_{SNSOUT} exceeds 3.5 V. After detecting HBC output OVP, the SSL4120 enters the latched protection shutdown state.

10.3.1.3 Connecting external measurement circuits

When latched protection is needed for other detection circuits, it can be added to SNSOUT with a series diode.

10.3.2 UnderVoltage Protection (HBC output UVP)

The SSL4120 has an undervoltage protection intended for monitoring the HBC output voltage. HBC output UVP is one of the functions that is combined on the SNSOUT pin.

10.3.2.1 UVP using the T_{HBC} auxiliary winding

When dealing with a mains insulated converter, V_O can be measured via the auxiliary winding of T_{HBC}. A special transformer construction is required to measure accurately the secondary voltage on the primary circuit side.

It is important that this winding has a good coupling with the secondary windings and a minimum coupling with the primary winding to obtain a good representation of the output voltage situation (see Section 5.3.3.1 and Figure 6).

Triple insulated wire can be used to meet the mains insulation requirements.

10.3.2.2 Principle of operation

The voltage is sensed at the SNSOUT pin via an external rectifier and resistive divider. Undervoltage is detected when V_{SNSOUT} drops under 2.35 V. When detecting HBC output UVP, the SSL4120 starts the protection timer by charging it with 100 μA.

When the undervoltage condition remains until the timer reaches the protection level, the controller stops and then the restart timer restarts it.

At start-up, V_{SNSOUT} normally starts at a level lower than 2.35 V. The timer setting must allow sufficient time for start-up to charge V_{SNSOUT} to a value above 2.35 V, preventing undesired protection during start-up.

In applications where the SSL4120 is supplied from an auxiliary winding (to SUPIC), V_{SUPIC} monitoring can also activate a protection when an error condition causes V_O to drop (see Section 5.2.2).

10.3.2.3 Severe voltage drop

When V_{SNSOUT} drops to a low voltage, the hold HBC and hold PFC functions on this input pin stop the HBC and PFC.

10.3.2.4 Connecting external measurement circuits

When restart protection is needed for other detection circuits, it can be added on SNSOUT with a series diode.

10.3.3 HBC output OVP and UVP combinations

10.3.3.1 Circuit configurations

The following list contains examples of configurations for which certain functionality on the SNSOUT pin is disabled.

- OVP enabled and UVP disabled (see Section 10.3.3.2)
- UVP enabled and OVP disabled (see Section 5.3.3.3)
- Both OVP and UVP disabled (see Section 10.3.3.4)

Remark: In the examples given, burst mode operation can still be implemented independent of the UVP and/or OVP functionality.

10.3.3.2 HBC output OVP enabled and UVP disabled

In some applications preventing the activation of UVP on SNSOUT by disabling UVP can be required (for example LED drivers with current controlled output). Disabling UVP can be realized by adding a circuit that prevents V_{SNSOUT} from dropping under 2.35 V.

As a practical example, V_{SNSOUT} can be prevented from dropping under a preset voltage by adding an external low impedance resistive divider, with a fixed voltage. The resistive divider is connected to SNSOUT using a diode. This simple circuit is not accurate but it does provide the basic capability to disable the UVP function of SNSOUT.

Remark: The diode is blocking for higher voltage values on SNSOUT so that the OVP is still enabled.

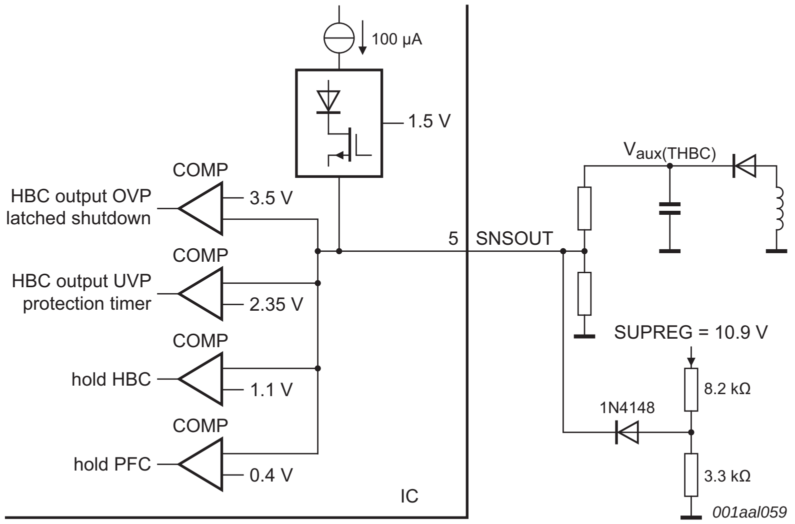


Fig 50. Example of disabling HBC output UVP function of SNSOUT

10.3.3.3 HBC output UVP enabled and OVP disabled

In some applications, disabling OVP can be required. Disabling OVP is realized by adding a circuit that prevents V_{SNSOUT} from exceeding 3.5 V.

As a practical example, V_{SNSOUT} can be prevented from exceeding the preset voltage by externally adding a low impedance resistive divider, with a fixed voltage. The resistive divider is connected to SNSOUT using a diode. This simple circuit is not accurate but it does provide the basic capability to disable the OVP function of SNSOUT.

Remark: The diode is blocking for lower values of V_{SNSOUT} so that the UVP is still enabled.

Another possibility is to add a Zener diode function on SNSOUT to limit the voltage on this pin.

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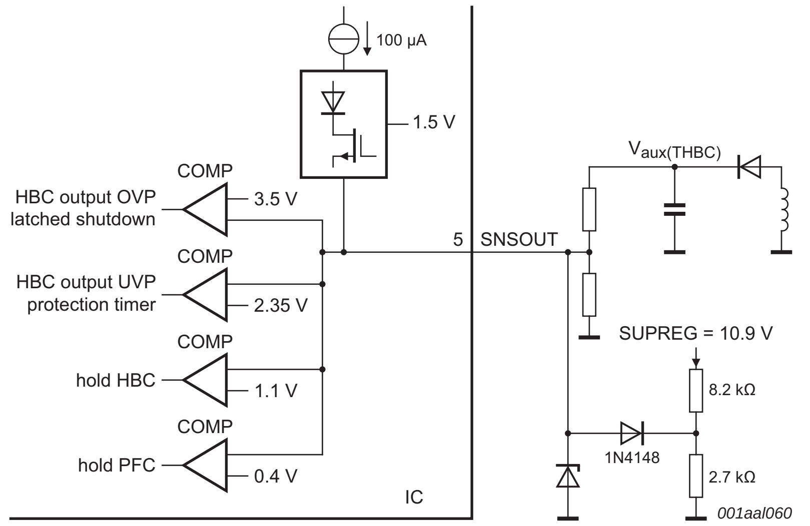


Fig 51. Example of disabling the SSL4120 OVP function of SNSOUT

10.3.3.4 Both HBC output OVP and UVP disabled

When OVP or UVP functionality is not required, a fixed voltage between 2.35 V and 3.5 V can be applied to SNSOUT. This fixed voltage is obtained from a resistive divider that is referenced to V_{SUPREG}.

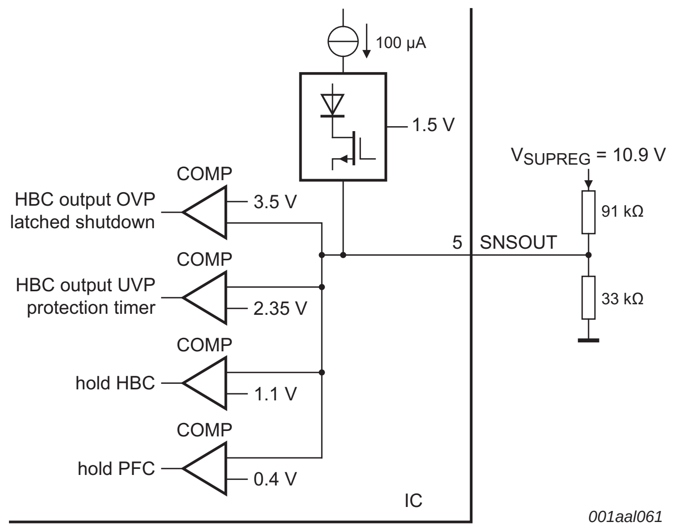


Fig 52. Example of disabling both HBC output UVP and OVP functions of SNSOUT

10.4 Protection timer

The SSL4120 has a programmable timer that is used for the timing of several forms of protection. The timer is used in two ways:

- As a protection timer
- As a restart timer

The values for both types of timer can be independently preset by an external resistor and capacitor connected to RCPROT.

10.4.1 Block diagram of the RCPROT function

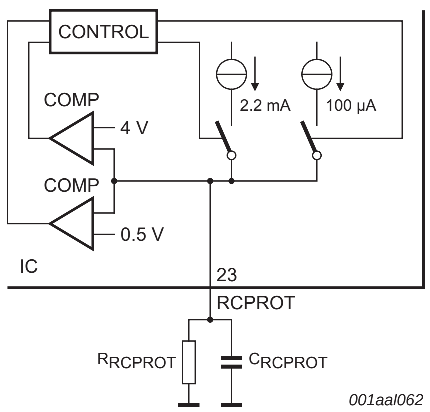


Fig 53. Block diagram of the RCPROT function

10.4.2 RCPROT working as protection timer

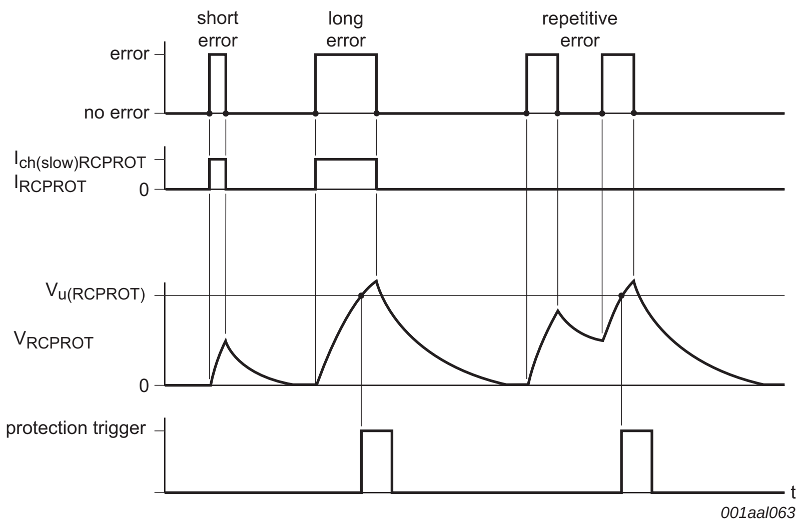


Fig 54. RCPROT protection timer operation

Figure 54 shows the operation of the protection timer. When an error condition occurs, a fixed current of 100 μA flows from the RCPROT pin and charges the C_{RCPROT}. The voltage rises inverse exponentially due to R_{RCPROT}. The protection time is passed when the upper switching level of 4 V has been reached. The appropriate protective action is then executed, the current source is stopped and R_{RCPROT} discharges C_{RCPROT}.

If error condition ends before 4 V has been reached, the current source is stopped, the pin discharges through R_{RCPROT}. No further actions are taken.

If the error condition is permanent, the system fluctuates between stop and restart.

The following events activate the protection timer:

- OCR using the SNSCURHBC pin
- HFP using the RFMAX pin
- OLP using the SNSFB pin
- UVP using the SNSOUT pin

The activation of protection (and restart) can be forced by increasing V_{RCPROT} above 4 V (but not higher than 12 V) using an external circuit.

10.4.3 RCPROT working as a restart timer

During certain error conditions, it can be required to disable the IC temporarily. This feature is especially useful when an error can overheat components. A temporary disable allows power supply components to cool down, after which the IC must automatically restart. The restart timer determines the time to restart.

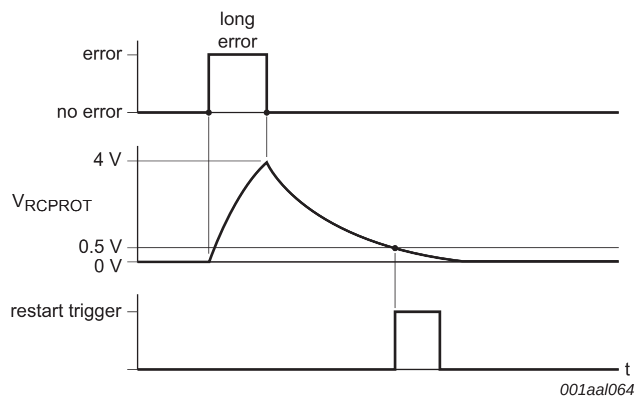


Fig 55. RCPROT operating as a restart timer

Normally, C_{RCPROT} is discharged to 0 V but when a restart is requested, a 2.2 mA current quickly charges C_{RCPROT} until it reaches the 4 V upper switching level. After this, the RCPROT pin current becomes zero and R_{RCPROT} discharges C_{RCPROT}. The restart time is triggered when the 0.5 V lower switching level has been reached. The IC is then restarted and C_{RCPROT} is further discharged. $I_{ch(fast)RCPROT}$ = 2.2 mA is only activated in the case of short circuit protection of the SNSBOOST.

10.4.4 Dimensioning the timer function

The required restart time $t_{restart}$ determines the time constant t_{RCPROT} made by the values of R_{RCPROT} and C_{RCPROT}.

$$t_{RCPROT} = \frac{-t_{restart}}{1n\langle\frac{V_{l(RCPROT)}}{V_{u(RCPROT)}}\rangle} = \frac{-t_{restart}}{1n\langle\frac{0.5}{4}\rangle} = 0.48 \times t_{restart} \tag{40}$$

With this time constant and the required protection time $t_{protection}$, the value of R_{RCPROT} and C_{RCPROT} can be calculated as follows:

$$R_{RCPROT} = \frac{V_{u(RCPROT)}}{I_{ch(slow)RCPROT} \times \langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}}\rangle} = \frac{4}{100\ \mu A \times \langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}}\rangle} \tag{41}$$

$$C_{RCPROT} = \frac{t_{RCPROT}}{R_{RCPROT}} \tag{42}$$

Example:

- $t_{restart}$ = 500 ms
- $t_{protection}$ = 30 ms
- t_{RCPROT} = 240 ms
- R_{RCPROT} = 341 kΩ
- C_{RCPROT} = 705 nF

11. Miscellaneous advice and tips

11.1 PCB layout

11.1.1 General setup

The SSL4120 contains two largely independent converter controllers in one package. General advice is to separate the PFC and HBC circuits physically on the PCB to avoid mutual interference.

11.1.2 Grounding

Connect SGND and PGND directly under the IC (on the ground plane if possible) to avoid false signal detection by driver current disturbance (see Figure 58).

A star grounding construction provides the lowest risk of mutual converter disturbance or signal detection disturbance. In this system, the central star point can be chosen at the boost capacitor ground.

Avoid large currents on grounding tracks that are meant for signal measurement. Also connect the heatsinks to the PGND to lower the HF emission.

11.1.3 Current loops

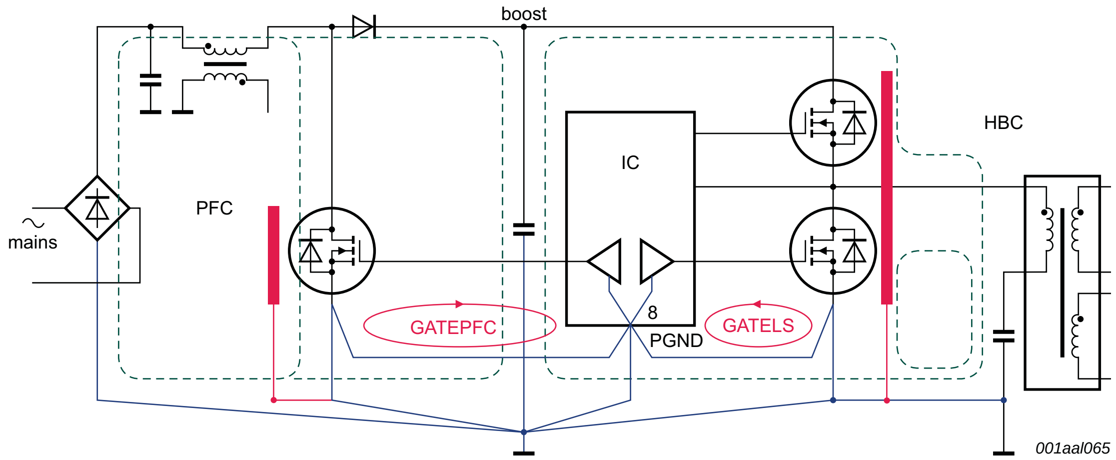


Fig 56. Gounding structure and current loops GATEPFC and GATELS

11.1.4 Grounding layout example

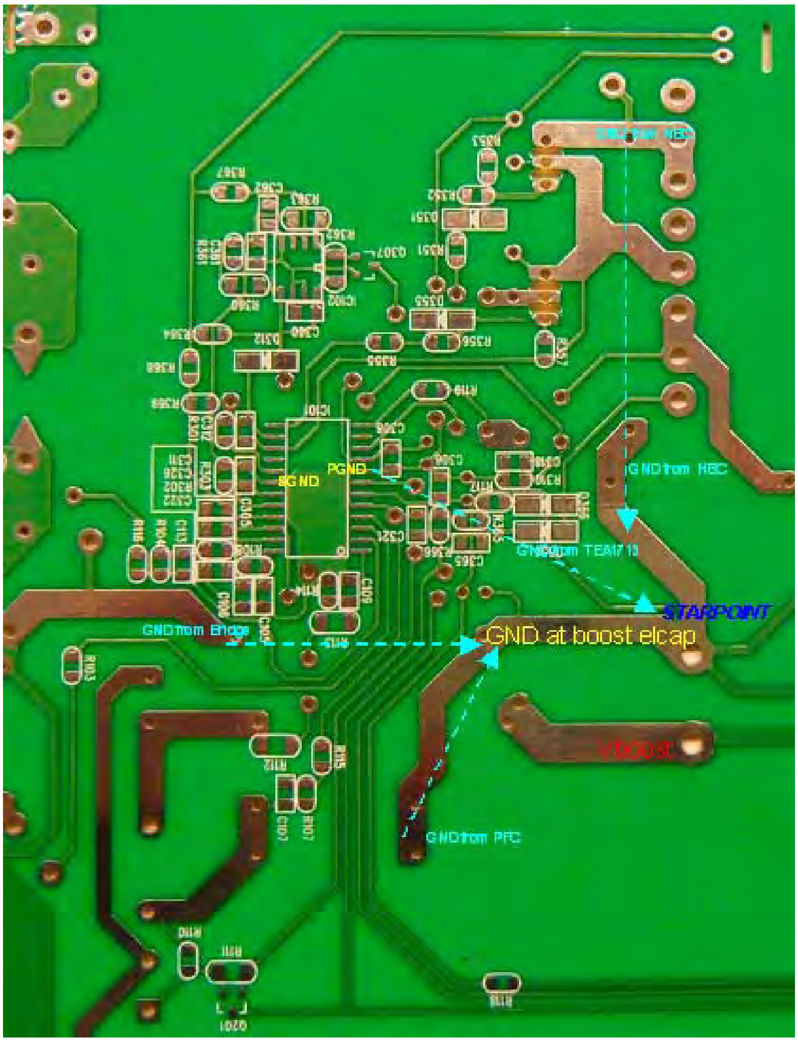


Fig 57. Grounding layout example with star point at the boost capacitor

11.1.5 Miscellaneous

11.1.5.1 Connecting SNSCURHBC (pin 17)

Place a series resistor $R_{SNSCURHBC}$ in the SNSCURHBC connection as close as possible to pin 17. The resistor is important for avoiding disturbance pick-up. Also avoid capacitive coupling between the connection to pin 17 and the HB track (to pin 15) that contains high dV/dt signals.

11.1.5.2 CFMIN (pin 19) and RFMAX (pin 20)

Connect the oscillator capacitor on C_{CFMIN} from pin 19 to SGND pin 18 with short tracks to prevent pickup of disturbances by an external field. Although less critical, a similar construction can be used for R_{RFMAX}.

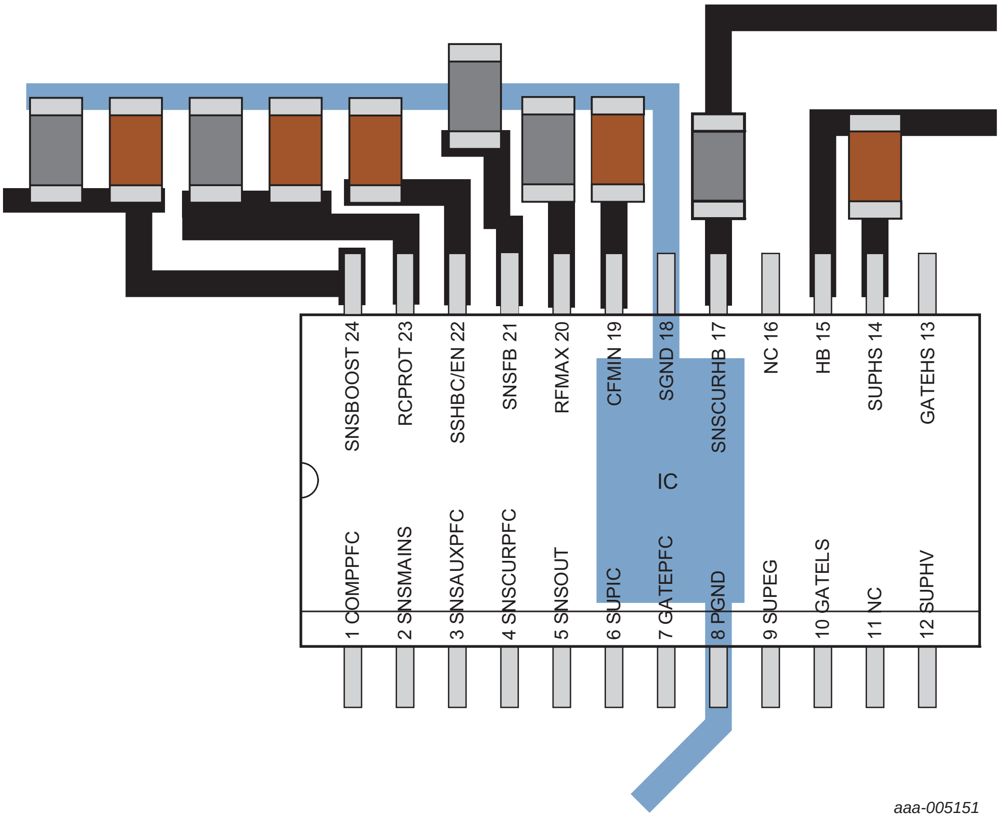


Fig 58. PCB layout of the SGND, PGND, CFMIN, RFMAX and SNSCURHBC pins

11.1.5.3 SNSBOOST pin

Connect the resistor and capacitor on SNSBOOST pin to the SGND pin with short tracks to prevent pickup of disturbances by an external field.

11.2 Starting/debugging partial circuits

When starting a newly built application for the first time or when an error is observed during operation, it is possible to activate circuit parts step-by-step. This function enables errors to be located more easily and an evaluation can be performed under conditions that restrict the influences from other circuit parts.

The following provides a step-by-step sequence for debugging:

1. HBC only, with protection disabled
2. HBC only, with protection disabled and variable DC input voltage
3. HBC only, with protection enabled
4. PFC only
5. PFC + HBC complete application

The best approach is to check the HBC converter first and then the PFC converter.

11.2.1 HBC only

Figure 59 shows a suggestion for the setup (temporary additions to the existing application to force operation) and the sequence for disabling/enabling the different functions. A moderate (current) load can be applied to the converters output to ascertain the correct functioning.

Remark: A latching, overvoltage detection on SNSOUT (> 3.5 V), can still prevent operation.

V_{CFMIN}, V_{GATELS}, V_{GATEHS} and V_{HB} can be monitored to assess continuously the functioning of the converter/controller.

When the PFC function is disabled, V_{boost} is often applied by using a DC or AC voltage to the mains input connections.

Check the regulation by increasing V_{boost} for the following situations in the sequence given:

1. Initially at V_{boost} = 0 V: $f_{sw(HBC)}$ is low with a short on-time and a long off-time. This is due to the HB detection not working properly at low voltage and the internal slope detection (HB) not detecting a fast slope. In this situation, a quick check of the PFC operation can be done by lowering the external supply voltage of 2.7 V on SNSMAINS and SNSBOOST to a value under 2.5 V. This function allows the gate-drive pulses on GATEPFC to be seen. Varying the voltage changes the on-time. After this check, revert the voltage to 2.7 V to continue the HBC-only start-up (see Section 11.2.2.1).
2. Increasing the value of V_{boost}: at a certain V_{boost}, the HB detection works correctly and $f_{sw(HBC)}$ to drive maximum power is minimal. If the HB slope remains slow, the output current is probably low. Increasing the output current probably results in proper HB switching.
3. When V_{boost} reaches a level closer to the nominal working voltage, the depending on the output load correct output voltage is reached. Then regulation starts working. This results in increasing $f_{sw(HBC)}$ with increasing V_{boost} until the nominal working voltage of V_{boost} is set.
4. When the basic operation of the HBC with SNSFB regulation, is working well, protection features are added one-by-one. Proper operation or a need for change can be evaluated.
5. When a self-supplying application is used, the external supply voltage can be removed when the system works well at $V_{boost(nom)}$. The system can now start with the internal high voltage start-up supply and an auxiliary winding can take over the SUPIC supply.

Remark: If, during debugging or starting, a protection has been activated, switching the SUPIC supply off and on to reset a latched protection state can be required.

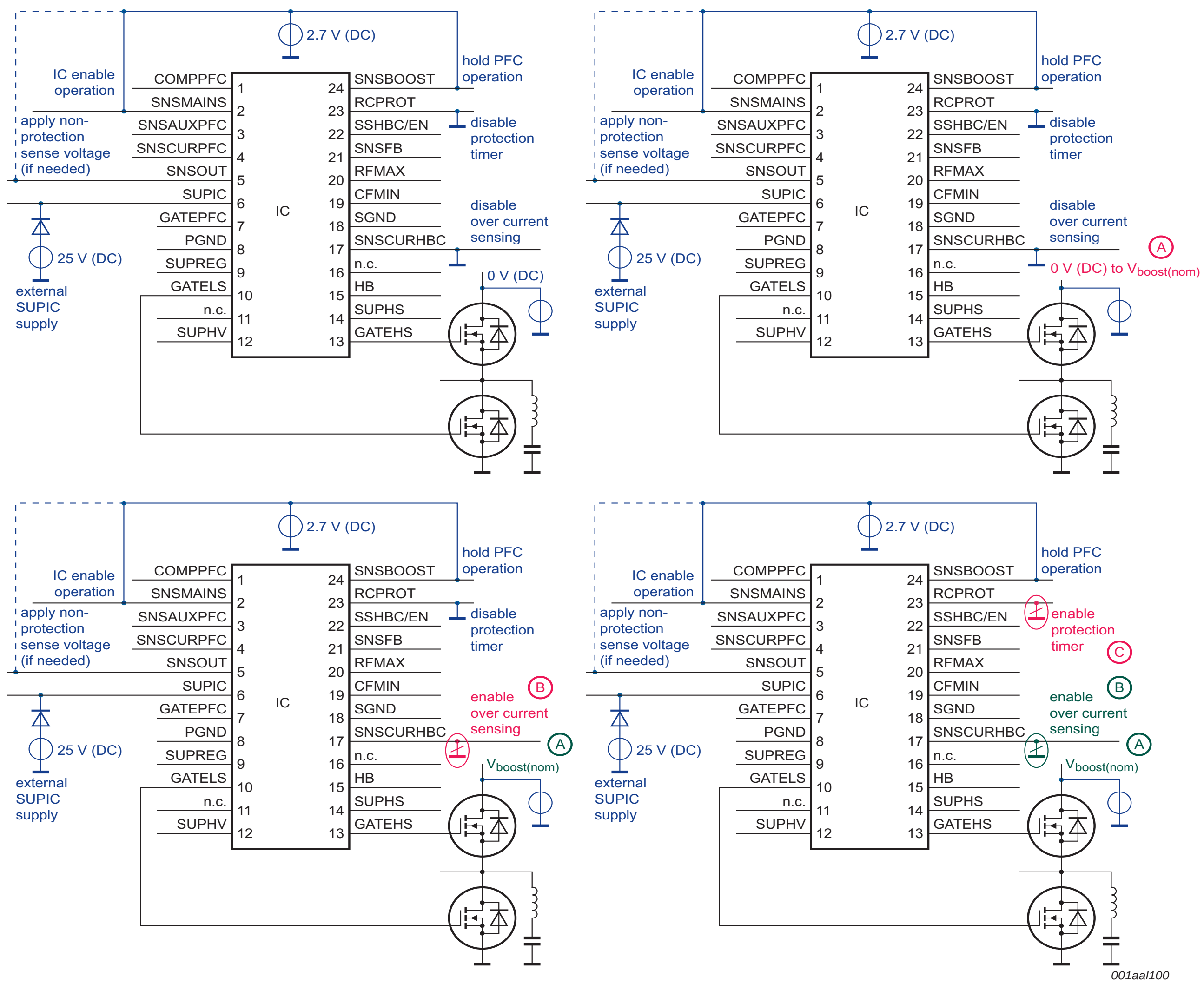


Fig 59. HBC only: start-up and debugging step-by-step

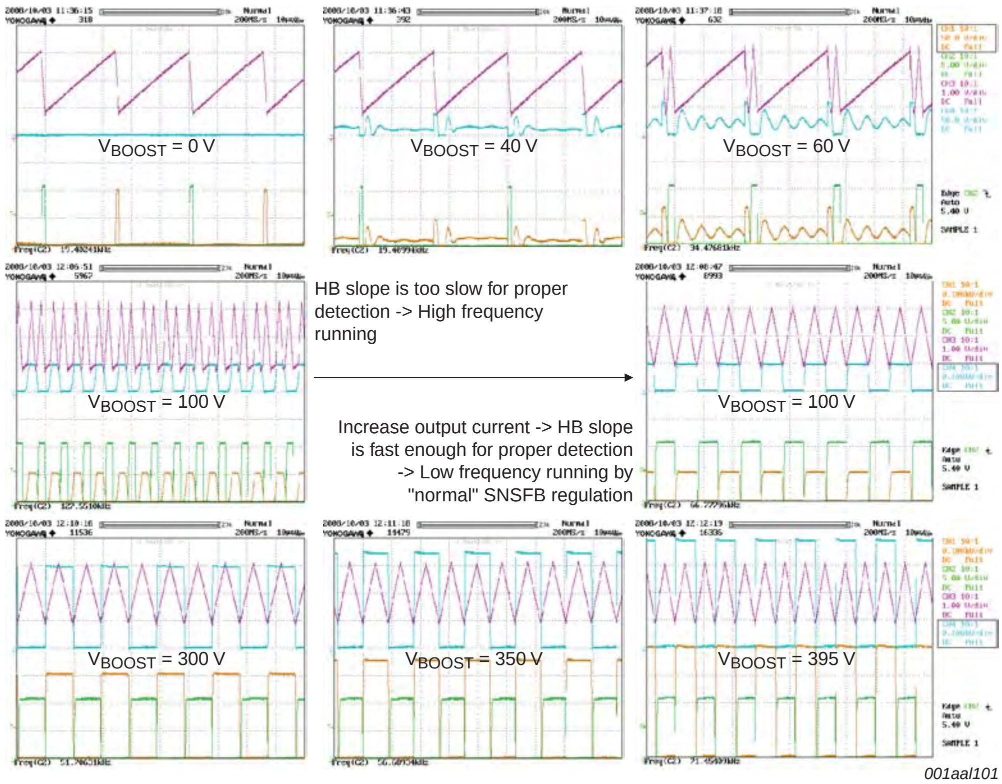


Fig 60. Typical signals during a separate HBC start-up for an increase in V_{boost}

The following list provides an association between pins and the protection states for which they are being monitored:

- SSHBC/EN:

  When the IC lowers $V_{SSHBC/EN}$, it indicates a protection with correction to high HBC frequency.
- RFMAX:

  V_{RFMAX} indicates the HBC oscillator frequency, which can cause a high frequency protection.
- CFMIN:

  A (partially) slow oscillator signal cannot observe proper detection of HB slope or a possible Capacitive mode detection.
- PGND and SGND:

  If the IC detects HB operation while there is zero input voltage, it indicates that the connection between these pins at the IC is not present. Gate currents lead to false HB-slope detection.
- SNSCURHBC:

  Any disturbances on this pin (voltage spikes) can lead to an increase of $f_{sw(HBC)}$ while the measurement voltage/signal is clean.

- SNSOUT:

  V_{SNSOUT} must be between 2.35 V and 3.5 V for normal operation. A voltage can be forced on pin SNSOUT to avoid protection. But it is often related (by a resistive divider) to the SUPIC and is correct when SUPIC is supplied externally.
- RCPROT:

  Several protection functions charges the timer capacitor C_{RCPROT}.

11.2.2 PFC only

Keeping $V_{SSHBC/EN}$ under or forcing it to drop under 2.2 V can disable the HBC function. A voltage higher than 1.2 V can enable the PFC function. Applying an additional voltage (from an external supply) of approximately 1.5 V on SSHBC/EN enables PFC only operation.

The set-up is similar to the HBC only operation setup but for extra safety, the V_{boost} connection to the HBC high-side switch can be disconnected. In addition, a small load can be connected on V_{boost} to prevent voltage overshoot and control the output power capability.

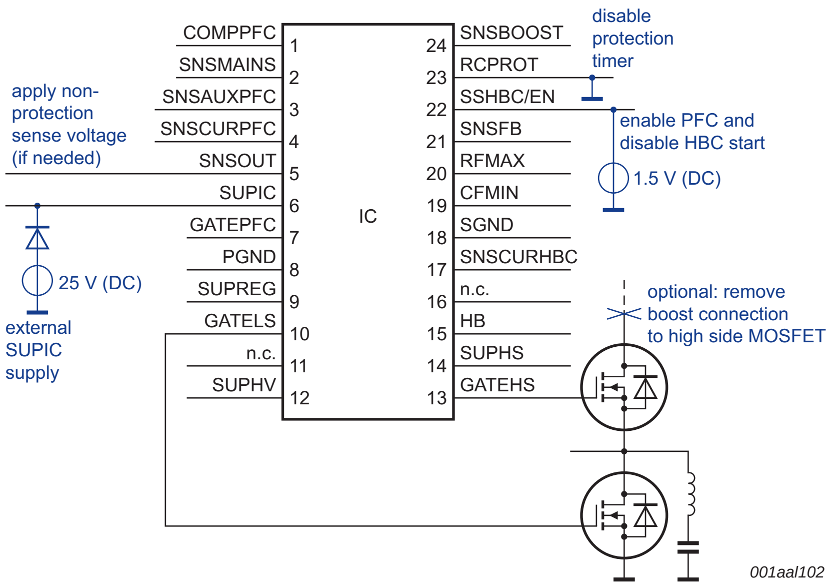


Fig 61. Start-up/debugging for PFC only

11.2.2.1 Operational check without mains voltage

Without mains input voltage, by lowering the (external) $V_{SNSMAINS}$ and $V_{SNSBOOST}$ to under 2.5 V, drive pulses can be observed on GATEPFC. Lower voltages lead to a longer on-time. Under 0.89 V, pulses stop because of SNSMAINS UVP and restarts when the level increases above 1.15 V.

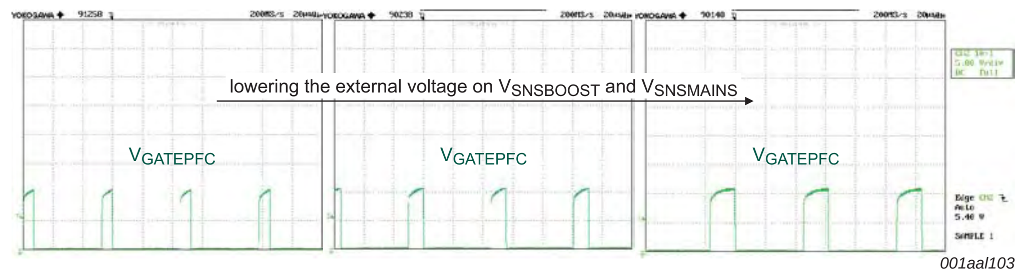


Fig 62. Typical GATEPFC signals without mains voltage

11.2.2.2 Operational check with mains voltage

There is no simple step-by-step method of gradually increasing V_{mains} to start PFC operation. $V_{mains(nom)}$ is applied to check PFC functionality. While doing this, remove any external voltage source on SNSMAINS and SNSBOOST.

If a problem is expected that V_O is too high, $R_{SNSBOOST}$ can be (temporarily) increased in value. This leads to a lower output voltage regulation setting.

Supply a DC voltage to the mains input instead of the usual AC voltage to be able to observe proper PFC operation more easily with an oscilloscope. This results in more stable signals with a fixed $f_{sw(PFC)}$ for evaluation.

11.2.3 HBC and PFC operation

When both converters work properly independently, they can be checked working simultaneously. Remove the additions used for start-up and debugging.

Remark: A (normal) ripple voltage on V_{boost} results in frequency variations in the HBC for compensation. At high output power, the voltage ripple on V_{boost} is larger.

12. Application examples and topologies

12.1 Examples of IC evaluation and test setup

Examples of a test/evaluation setup are provided in Figure 63 and Figure 64. This setup can be used to:

- Check if an IC is still functional (not defect).
- Evaluate specific IC functions or pin properties with limited interference from the total system.

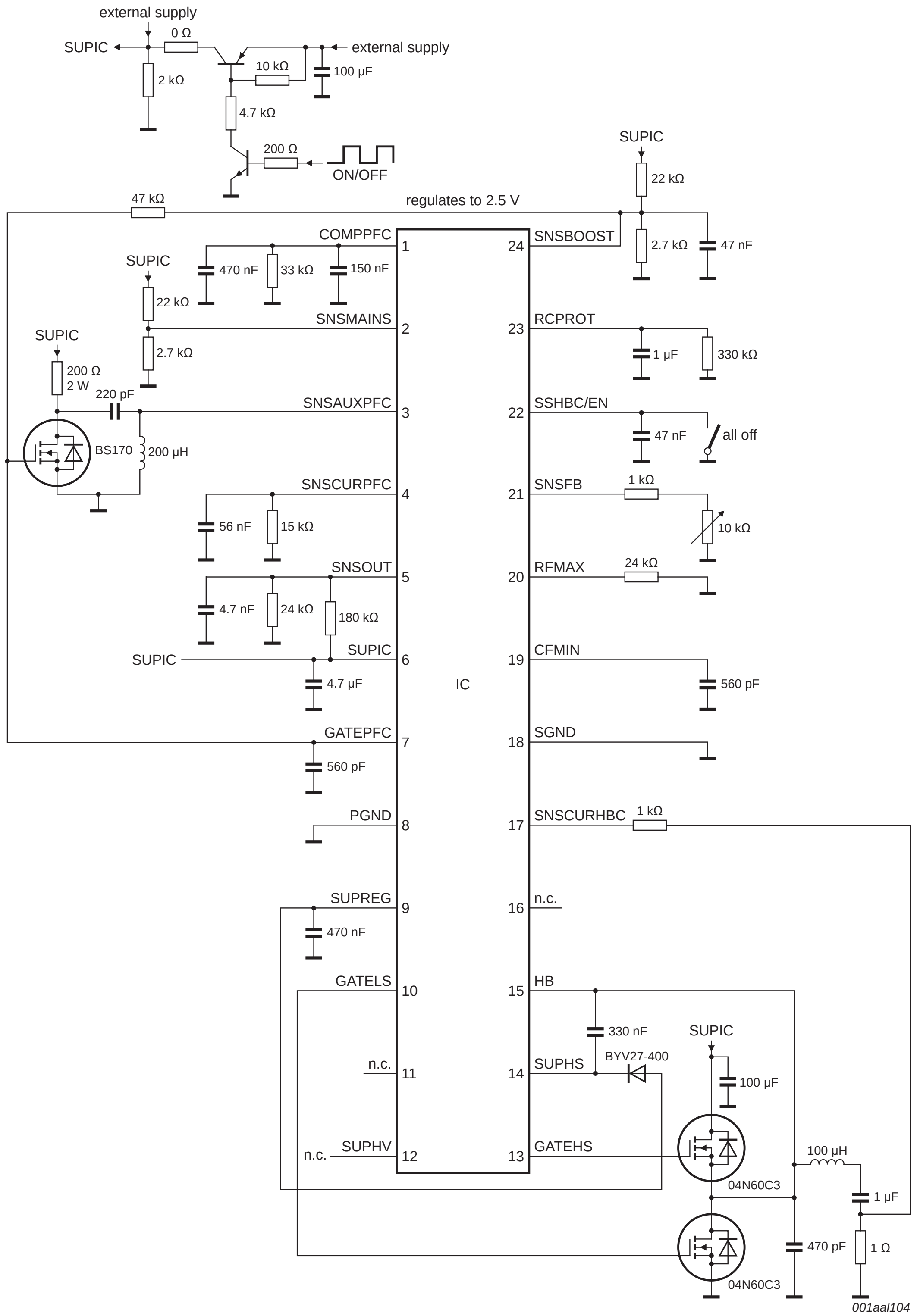


Fig 63. Example of a basic test setup on a single low voltage supply (24 V)

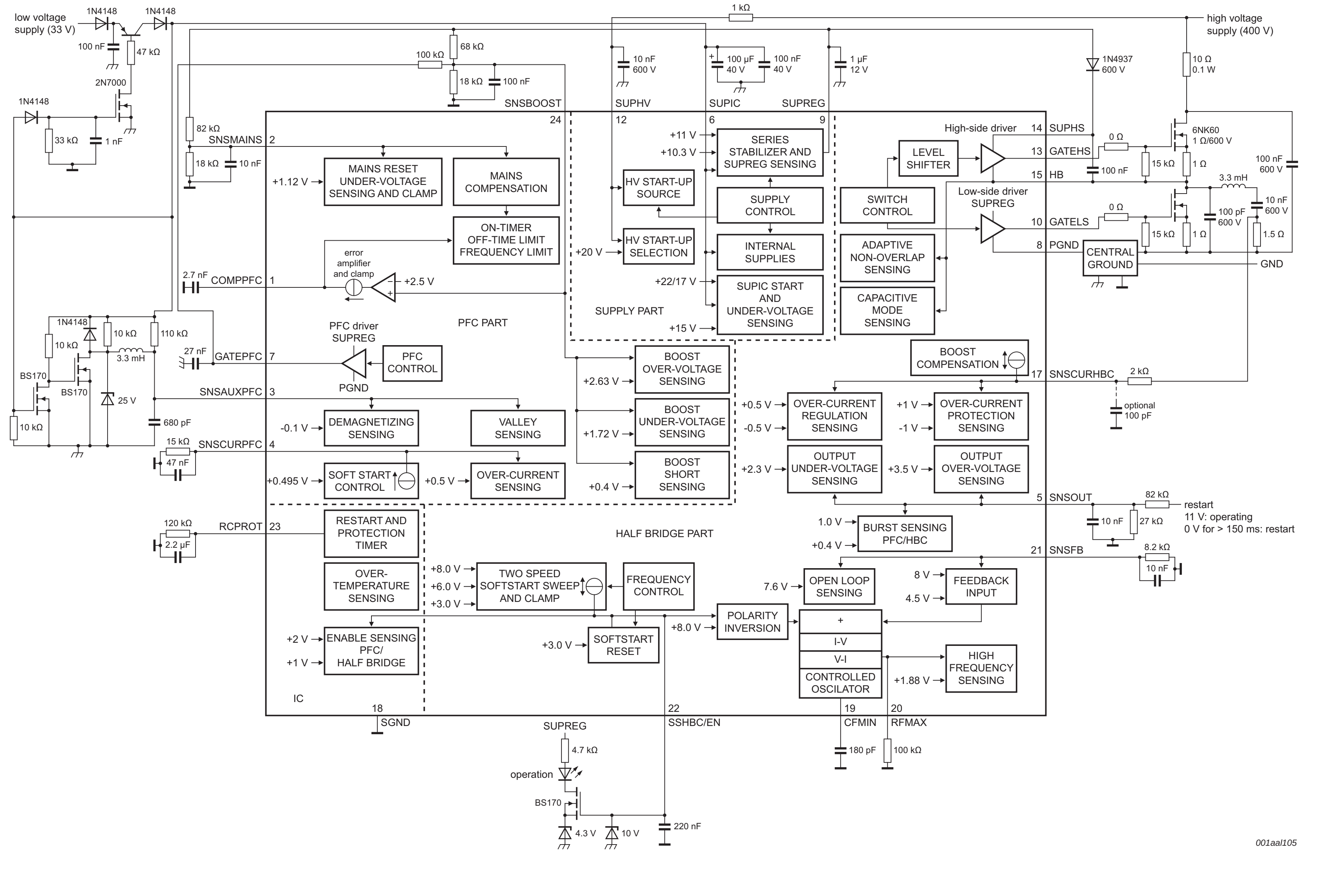


Fig 64. Example of a basic IC evaluation and test set-up with a high bus voltage

12.2 Example of a 250 W application with standby supply

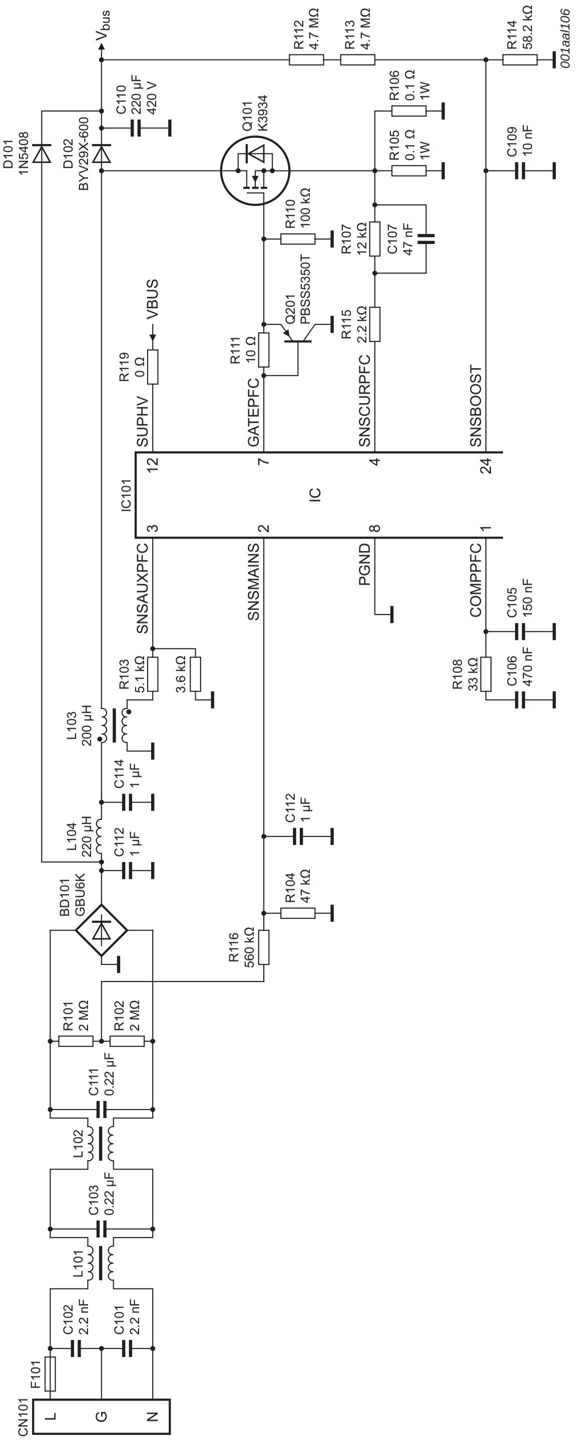
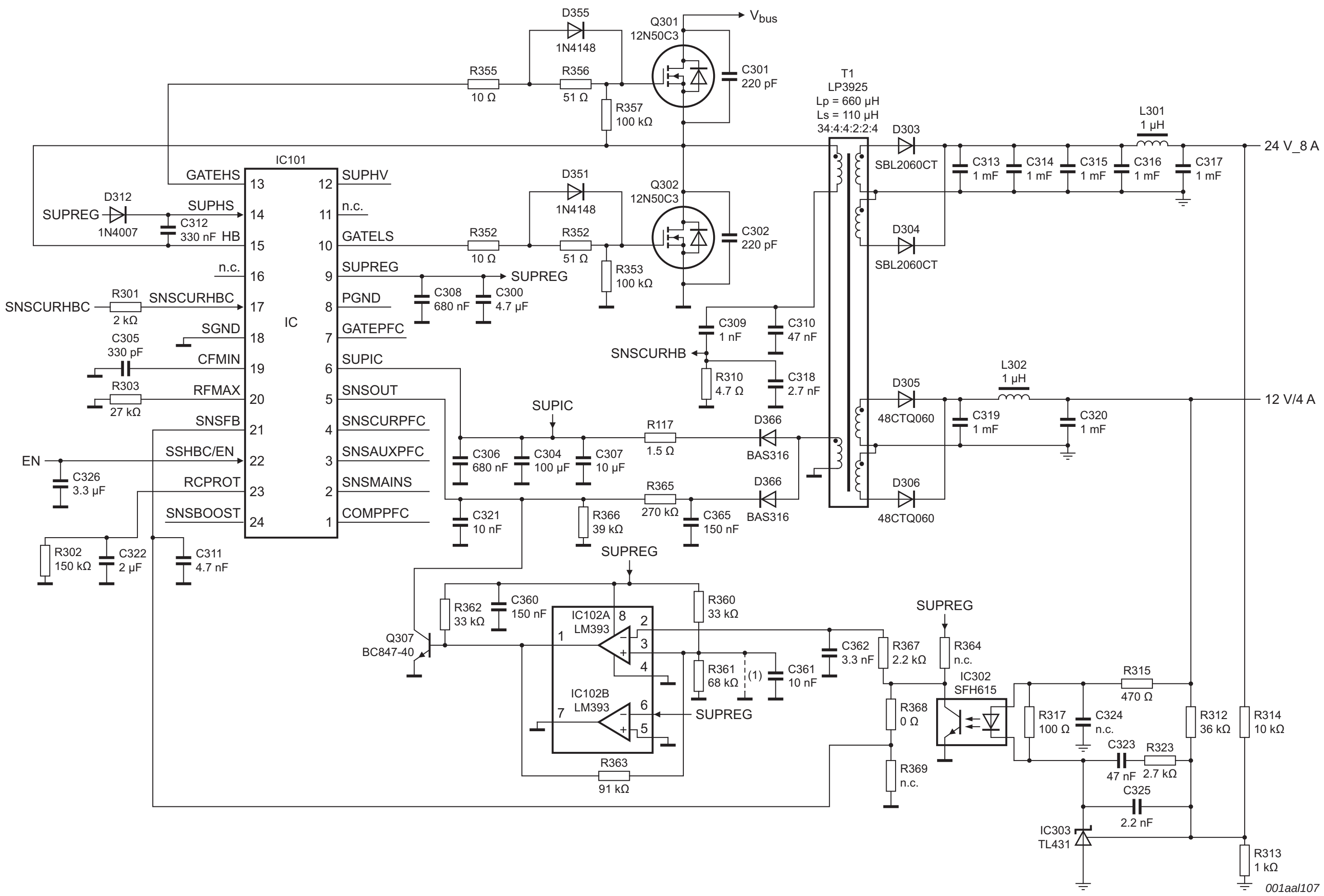


Fig 65. Example of a 250 W application with standby supply (part 1 of 3)



(1) Remove to enable burst mode operation

Fig 66. Example of a 250 W application with standby supply (part 2 of 3)

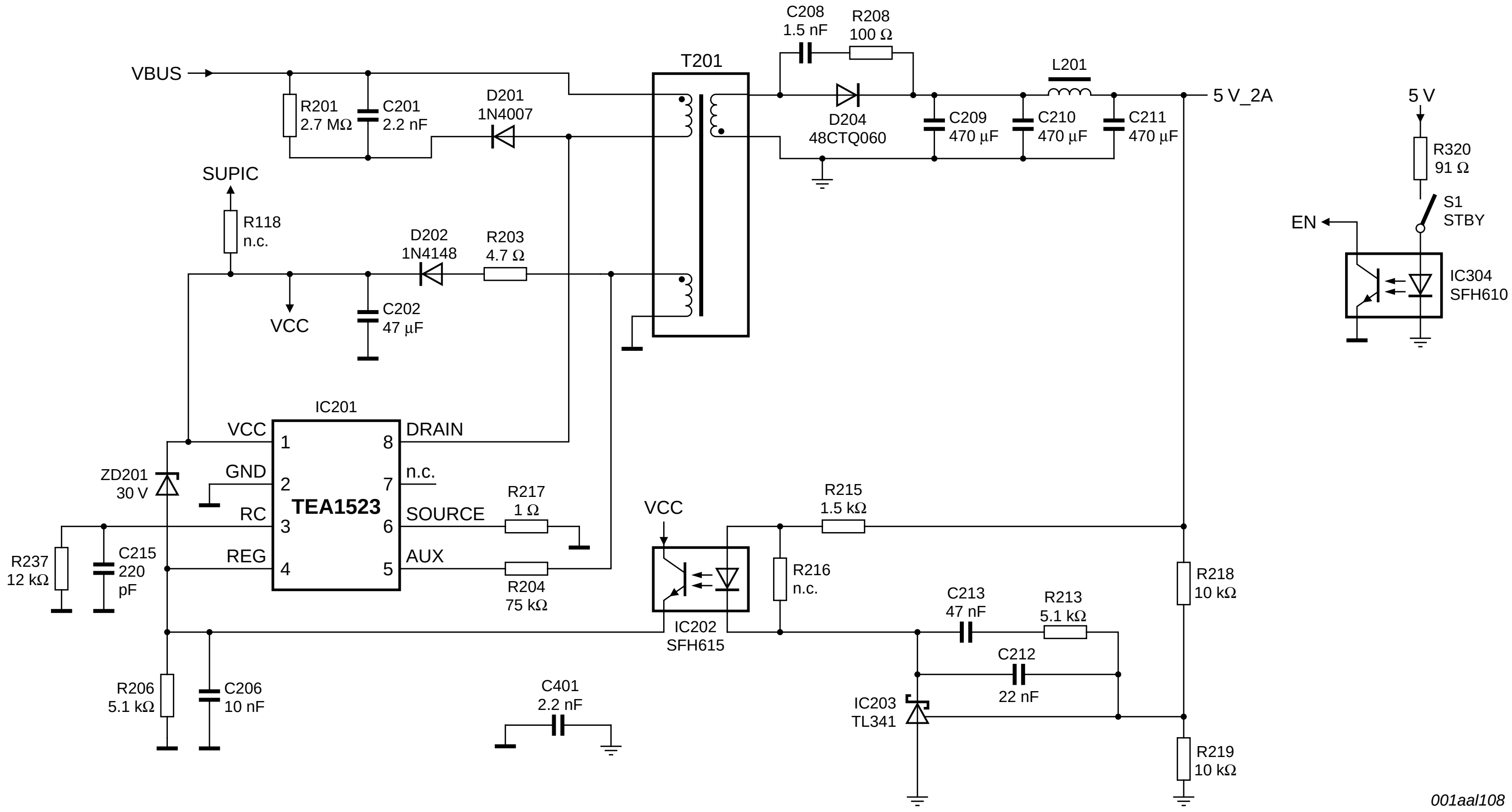


Fig 67. Example of a 250 W application with standby supply (part 3 of 3)

12.3 Example of a SSL4120 90 W LED driver with 1.5 A CC output

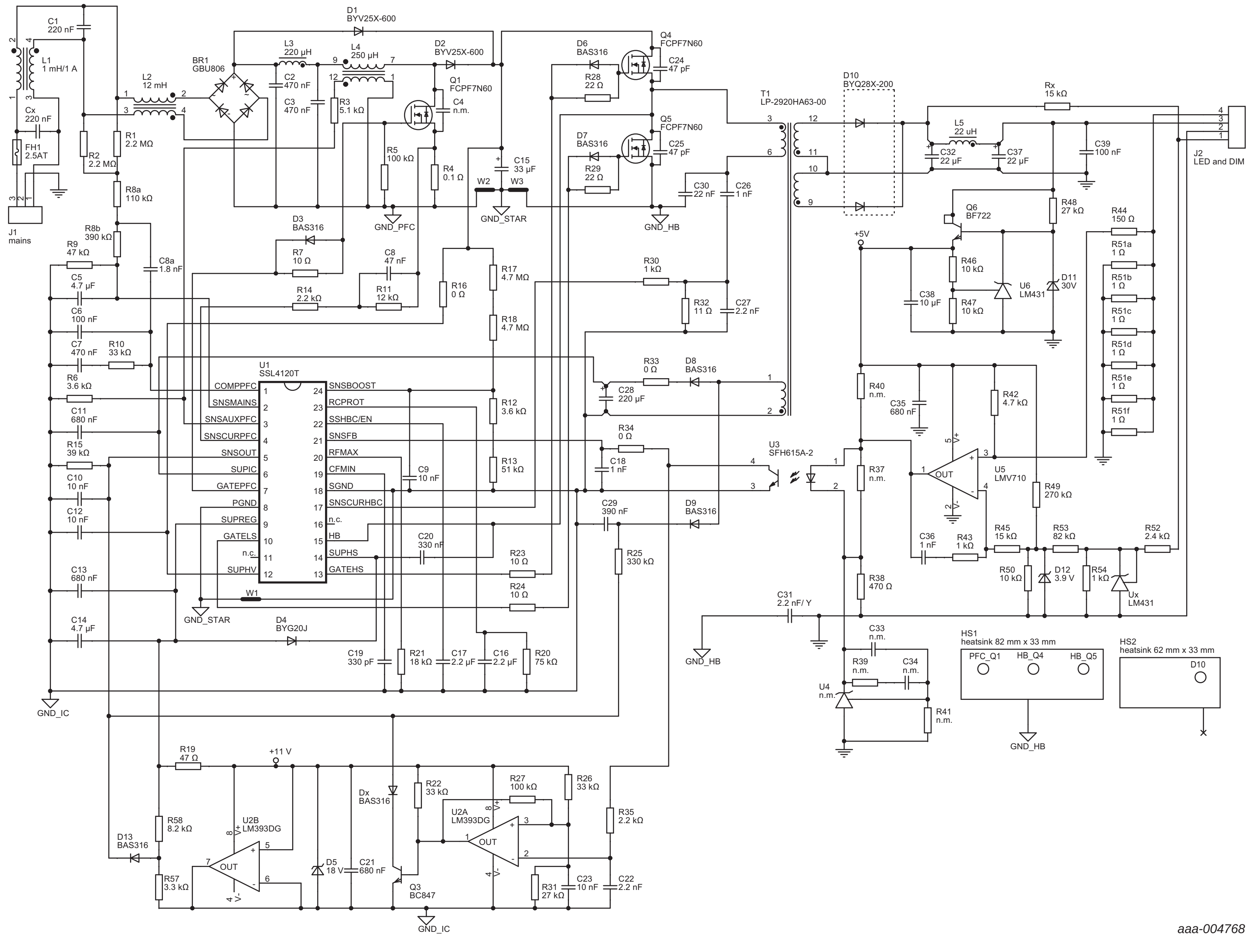


Fig 68. Example of a SSL4120 90 W LED driver with 1.5 A CC output

13. Abbreviations

Table 5. Abbreviations

Acronym	Description
ADT	Adaptive Dead Time
BCD	Bipolar CMOS DMOS
CMR	Common Mode Rejection
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference (or Immunity)
HB	Half-Bridge
HBC	Half-Bridge Converter (or Controller)
HFP	High-Frequency Protection
HV	High-Voltage
IC	Integrated Circuit
LCD	Liquid Crystal Display
LLC	Resonant tank or Converter (Lm + Lr + Cr in series)
OCP	OverCurrent Protection
OCR	OverCurrent Regulation
OLP	Open-Loop Protection
OPTO	Optocoupler
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PFC	Power Factor Converter/Controller/Correction
PWM	Pulse Width Modulation
SCP	Short Circuit Protection
SOI	Silicon-On-Insulator
UVP	UnderVoltage Protection

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