ARBITRATOR
T1 Compliance Monitor

$2,395.00

The ***Model 324A VALIDATOR*** is intended for use by service technicians to qualify and maintain a variety of DS1 transmission systems and equipment. It has all the essential features needed by the service technician to reliably perform his tasks, including testing the latest technology HDSL transmission systems. Like all T-COM products the VALIDATOR has a clear, intuitive user interface that requires minimum training for effective use.

Both instruments are the most cost and weight effective on the market today. They can withstand the rigors of outside plant use while performing sophisticated testing with the minimum of operator controls. Ask your T-COM sales representative for a demonstration. We are confident you will be delighted with these products.

Model 324A
VALIDATOR
T1/DS0 Analyzer
with HDSL Loop Codes

About the VALIDATOR

The T-COM Model 324A VALIDATOR is a low cost ($2,395 complete), light weight (only 1lb-10oz.), hand held test set designed to provide all the essential capabilities a test technician needs to reliably qualify and maintain and troubleshoot a variety of DS1 transmission systems and equipment, in the CO, the outside plant, or in customers' premises.

The VALIDATOR contains a DS1 receiver providing real-time impairment diagnostics, with dedicated LED's, on any DS1 signal observed when patched to DSX-1 access jacks (OUT or monitor) or bridged across a T1 line. The receiver provides level and frequency measurement of the T1 signal; it can also indicate bit slippage if a clock signal or another T1 signal is supplied to the reference receiver. At the press of a key the reciever provides comprehensive impairment statistics. The receiver automatically recognizes the framing format (NONE, D4, ESF, SLC-96) of the monitored signal. It also automatically identifies the test pattern presented. These features, not only contribute in simplifying the operation of the set, they also make it foolproof.

The Validator receiver displays the frequency and level of selected DS0 channels. Signaling Types, ROBBED BIT and CCIS, are operator selectable. Signaling Bits A, B, C, and D are displayed for a selected DS0 channel and selected Signaling Type.

The VALIDATOR transmitter can deliver a variety of standard test patterns to stress and qualify a T1 transmission system. The transmitter can also be used for sending various loop codes (CSU, NIU4, NIU5, PYLD, NTWK LINE, T.4/92, and PairGain HiGain).

The receiver and the transmitter can be used completely independently or in combination. When used independently, the receiver can monitor, for example, an ESF 3/24 pattern, while the transmitter delivers an ESF QRSS pattern.

The VALIDATOR transmitters can inject single logic bit errors or a 1^{-4} logic bit error rate.

The VALIDATOR can transmit and obtain pattern sync on a variety of BERT PATTERNS including QRSS, 1 IN 8, 2 IN 8, 3 IN 24, ALL ZEROS, ALL ONES, 1:1, NET55, OCT55, and DALY55. A user can select any of these patterns for transmission. Selecting a transmission pattern has no effect on the receiver, which continuously attempts to obtain Frame and Pattern signatures.

The VALIDATOR illuminates LED's indicating received signal status and history. These LED's include SIGNAL PRESENT, SIGNAL PRESENT HISTORY, FRAMING (NONE, D4, ESF, SLC-96), AMI and B8ZS LINE CODING, B8ZS HISTORY, PATTERN SYNC (QRSS, 1 IN 8, 2 IN 8, 3 IN 24, ALL ZEROS, ALL ONES, 1:1, NET55, OCT55, and DALY55) , OUT OF FRAME, OUT OF FRAME HISTORY, BLUE ALARM (AIS), BLUE ALARM (AIS) HISTORY, ONES DENSITY, ONES DENSITY HISTORY, EXCESS ZEROS, EXCESS ZEROS HISTORY, YELLOW ALARM, YELLOW ALARM HISTORY, PATTERN SYNC LOSS HISTORY and DS1 IDLE, DS1 IDLE HISTORY.

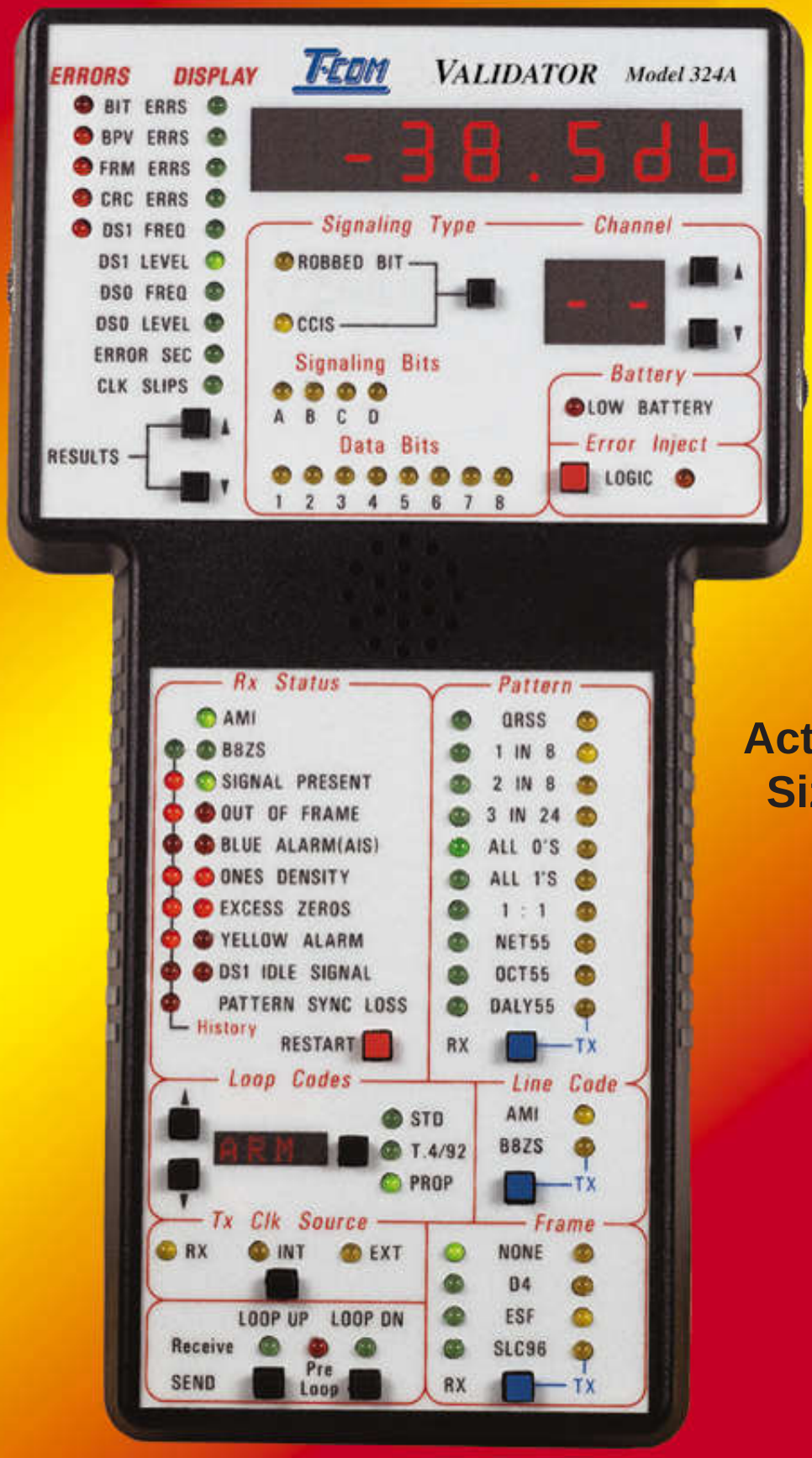
The VALIDATOR displays test results on eight, seven segment LED displays. Results displayed include CLOCK SLIPS, BIT, BPV, FRAME, CRC, DS1 FREQ and LEVEL, DS0 FREQ and LEVEL, and ERRORED SECONDS errors.

The VALIDATOR is powered by (3) 1.2V, 3.8A hr NiMH batteries providing approximately 6 hours of continuous operation. An AC-DC Power Adapter is provided for simultaneous operation and battery recharge.

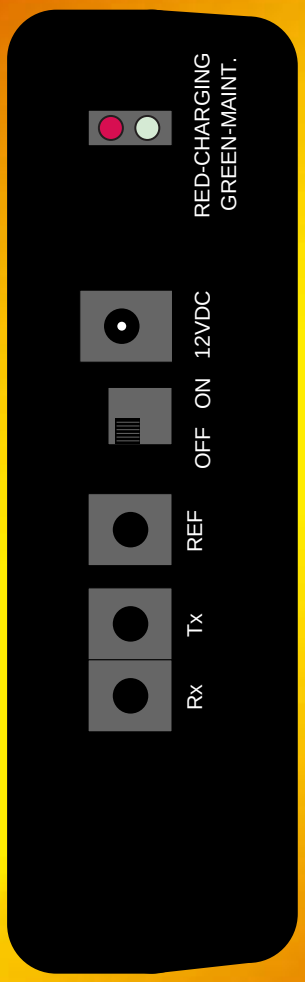
The VALIDATOR is supplied with the following items:

- A/C Power Adapter
- Two bantam-to-bantam cables
- User's Manual
- Carrying/storage case

Model 324A

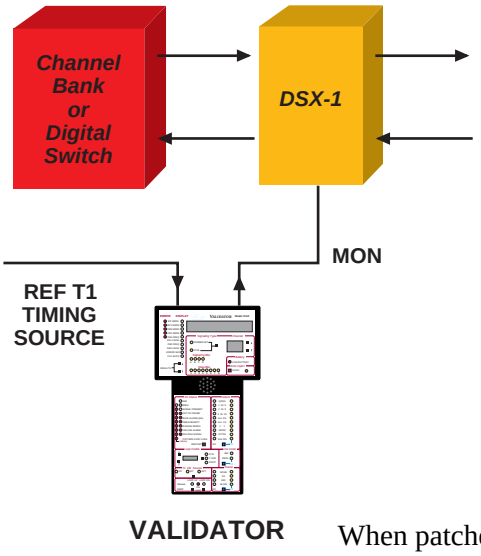


Top (detail)



Actual Size

Applications



DSI Bit Slippage and Jitter Checking

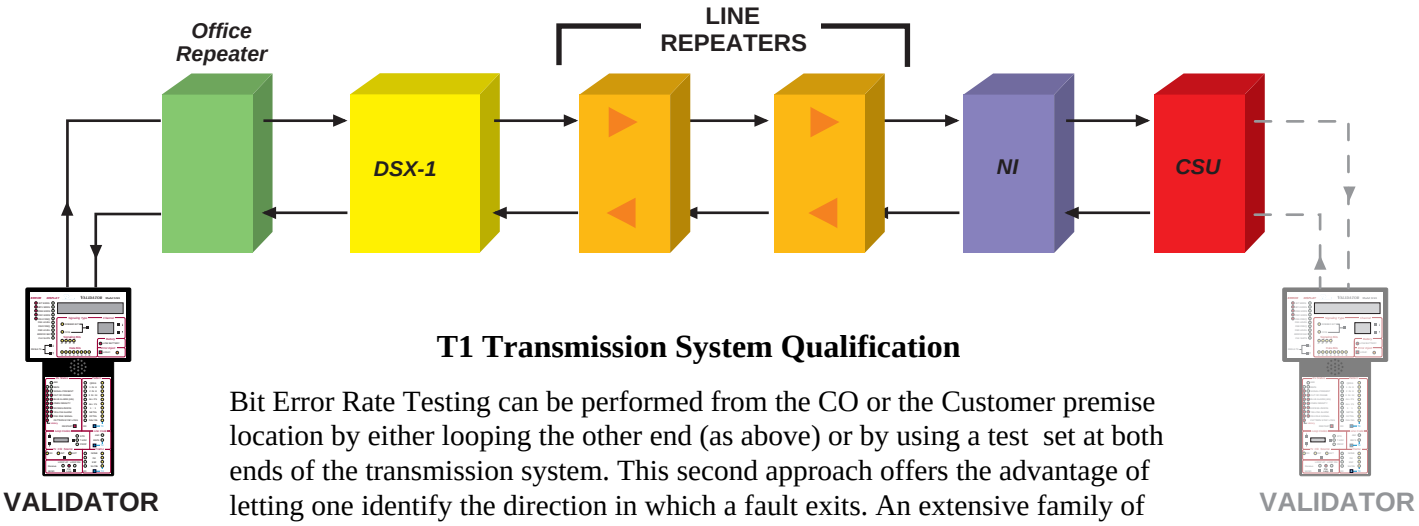
When patching the VALIDATOR REF T1 receiver to a T1 timing source, or utilizing the internal 1.544 MHz oscillator, while the RX T1 receiver is patched to a MONITOR jack or bridged across a T1 line, the VALIDATOR can display CLOCK SLIPS. CLOCK SLIPS are calculated as:

CLOCK SLIPS = REF clock pulses - RX clock pulses counted.

By observing the slippage one can readily access whether timing is lost or jitter is present on the system. This test can be carried-out on any live circuit without causing any interference.

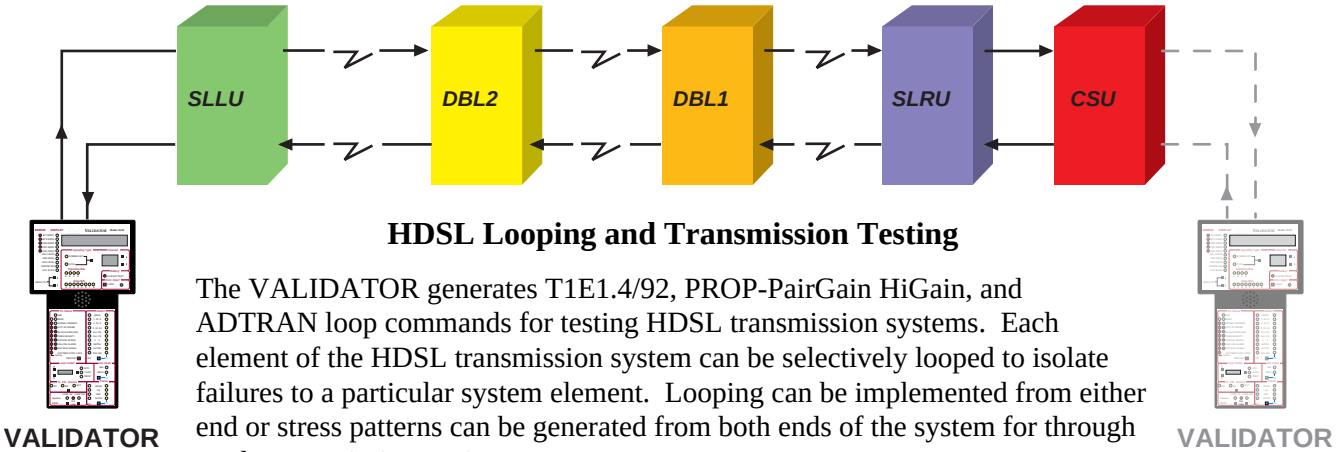
Looping CSU's and NI's

When patched to a T1 office repeater, the VALIDATOR can send and detect loop commands to selectively loop NIU's (NIU4, NIU5, NTWK (ESF)), and CSU's (LINE (D4, ESF) and PYLD (ESF)).



T1 Transmission System Qualification

Bit Error Rate Testing can be performed from the CO or the Customer premise location by either looping the other end (as above) or by using a test set at both ends of the transmission system. This second approach offers the advantage of letting one identify the direction in which a fault exits. An extensive family of test patterns is provided to stress the transmission system.



HDSL Looping and Transmission Testing

The VALIDATOR generates T1E1.4/92, PROP-PairGain HiGain, and ADTRAN loop commands for testing HDSL transmission systems. Each element of the HDSL transmission system can be selectively looped to isolate failures to a particular system element. Looping can be implemented from either end or stress patterns can be generated from both ends of the system for through mode transmission testing.

Specifications

314A

Input

Range: 6-36dB

Line Code: AMI and B8ZS

Impedance >1000 , Bridge
100 , Terminate
100 , Monitor

Indicators

Display LED's
BPV, Frame, CRC6, DS1 Frequency, DS1 Level (dBSX and volts)

Frame Format
NONE, D4, ESF, SLC96

Alarms
BPV, FRAME, CRC6, DS1 Frequency, Low Battery

ALARMS with History
Signal Present, Out of Frame, Blue Alarm (AIS), Ones Density (T1.403.1 1992) Excess Zeros (>15 Zeros) Yellow Alarm

Results

Errors BIT, BPV, Frame, CRC
DS1 FREQ Accuracy: ± 5ppm 0º C to 40º C
DS1 FREQ Resolution: 1 Hz
DS1 FREQ Range: 1544000 ± 10000
Line Level + 6 to -16dB ± 1dB
-16 to -40dB, ± 3dB
DS1 Level Range: + 6dB D to -40 DSX

SelfTest (*On Power-Up*)
"ErrCod 1" for an EPROM test failure
"ErrCod 2" for an SRAM test failure
"ErrCod 3" for an EPROM & SRAM test failure

Physical
1.75" h, 5" w, 9" l 14 oz

Power
Batteries three 1.2V NiMH, 1.5Ahr
approx. 6 hours continuous operation
red LED = apprx. 30 min. remaining
Auxiliary Power 12 VDC, 400 mA

Environmental
32º to 122º F Operating
5º to 158º F Storage
95% max., non-condensing, Humidity

324A

Compatibility
ANSI T1.403, AT&T PUB62411

Primary T1 Receiver

Input Impedance Bridge >1000
Term = 100 ± 5%
Monitor =100 ± 5%

Range Bridge = + 6 to -36dB
Term = + 6 to -36dB
Monitor = 100 ± 5%

Tx and Rx Framing
NONE, D4, ESF, SLC 96

Tx and Rx Line Coding
AMI, B8ZS

Tx and Rx Patterns
QRSS, 1 IN 8, 2 IN 8, 3 IN 24, ALL ZEROS, ALL ONES, 1:1, NET55, OCT55, DALY55
(all Tx Patterns are frame aligned)

Status/History
B8ZS, Signal Present, Out-of-Frame, Blue Alarm (AIS), Ones Density, Excess Zeros, Yellow Alarm, DS1 Idle, Pattern Sync Loss

DS0 Drop
Selected DSO channel to 8 data bit LED's and speaker

DS0 Signaling Types
Robbed Bit, CCIS (Selectable)

DS0 Signaling Bits A, B, C, D

Reference T1 Receiver

Input Impedance 100 ± 5%
Range 0 to -36dB
Compatibility AT&T TA24/CB113

Transmitter Output

LBO Fixed at 0 dBDSX
Tx Clock Source Internal, derived from received data, or external

Loop Codes
CSU, NIU4, NIU5, PAYLOAD (ESF), NETWORK (ESF), LINE (D4), LINE (ESF), T1E1.4/92 HDSL Maintenance, Pairgain HIGAIN proprietary and ADTRAN

Results

Errors BIT, BPV, FRAME, CRC, ERR SEC
Signal DS1 FREQ, DS1 LEVEL, DS0 FREQ, DS0 LEVEL, CLOCK SLIPS
DS1 FREQ Accuracy ± 5ppm 0º to 40º C
DS1 FREQ Resolution 1Hz
DS1 FREQ Range 1544000 ± 10,000 Hz
DS1 LEVEL Accuracy (DSX)
+ 6 to -16dB, ± 1dB
-16 to -40dB ± 3dB
DS1 LEVEL Range + 6 to -40dB DSX

DS0 FREQ Accuracy ± 1.5Hz
DS0 LEVEL Accuracy ± 0.2dBm

SelfTest (*On Power-Up*)
"ErrCod 1" for an EPROM test failure
"ErrCod 2" for an SRAM test failure
"ErrCod 3" for an EPROM & SRAM test failure

Physical
1.75" h, 5" w, 9" l 1 lb 10oz.

Power
Batteries three 1.2V NiMH, 3.8Ahr
approx. 6 hours continuous operation
red LED = approx. 30 min. remaining
Auxiliary Power 12 VDC, 1000 mA

Environmental
32º to 122º F Operating
5º to 158º F Storage
95% max., non-condensing, Humidity

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