IFX80471SKV

Demo Board User's Manual

Demoboard

Rev.1.0, 2012-05-15

1 Abstract

Note: The following information is given as a guideline for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide support for using the demo board of the Step-Down DC to DC Controller IFX80471SKV. This document is written in order to help the reader understand the dimensioning of the external components needed for the proper functioning of the DC/DC controller. It will also enable the reader to change the external components to adapt the function of the controller to his/her application needs.

2 Introduction

Selection of appropriate external components and the layout of the PCB are key factors when designing DC/DC applications for various industrial environments. The goal is to achieve optimum functionality with minimum output voltage ripple and good EMC performance. This application note provides, as an example,

1) proposal for the components selection
2) recommendation for layout

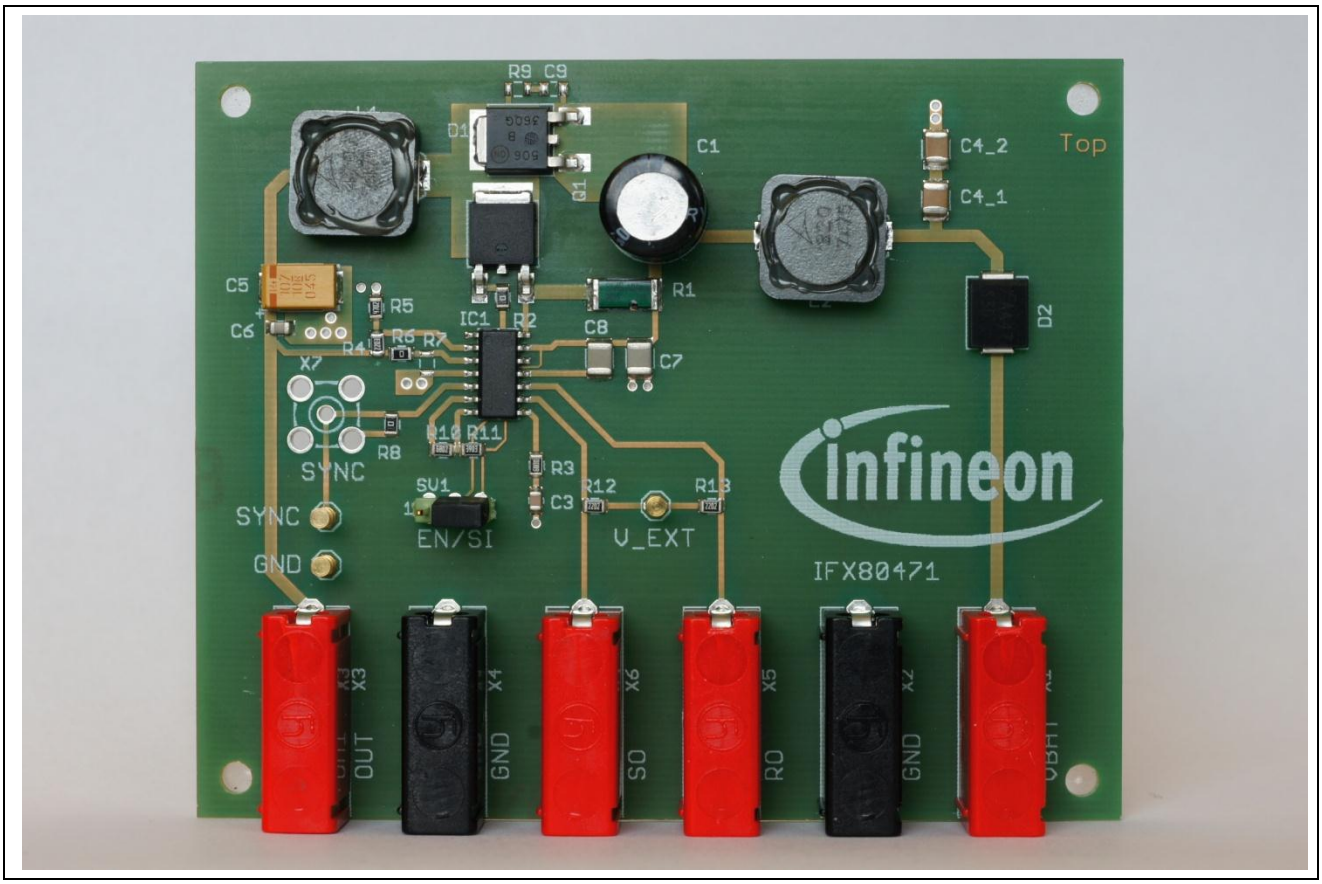


Figure 1 Photo of the demo board assembled with the IFX80471SKV DC/DC Controller.

3 Application schematic for Adjustable version

Figure 2 shows the minimum application circuit as proposed in the IFX80471 Datasheet which applies for the adjustable output voltage version IFX80471SKV.

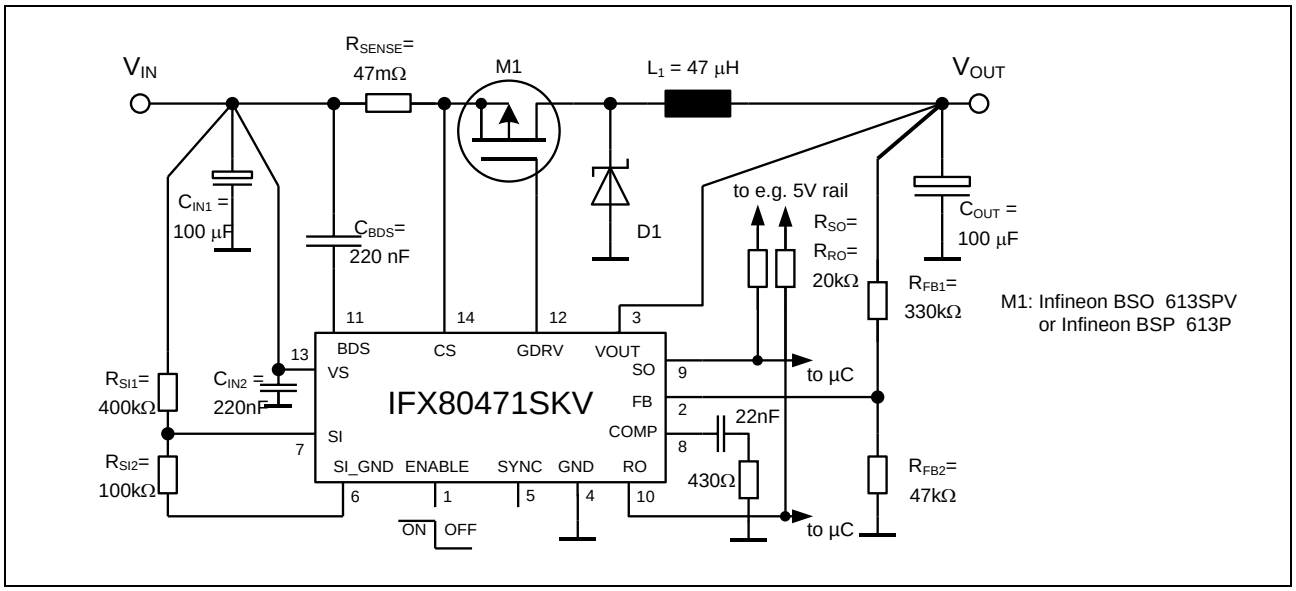


Figure 2 Minimum application circuit for IFX80471SKV.

The complete circuitry used for the demo board is shown in Figure 3. Compared to the minimum circuitry it:

- covers a wider load current range
- improves EMC performance
- enables to use only one PCB to evaluate other voltage variants of the device

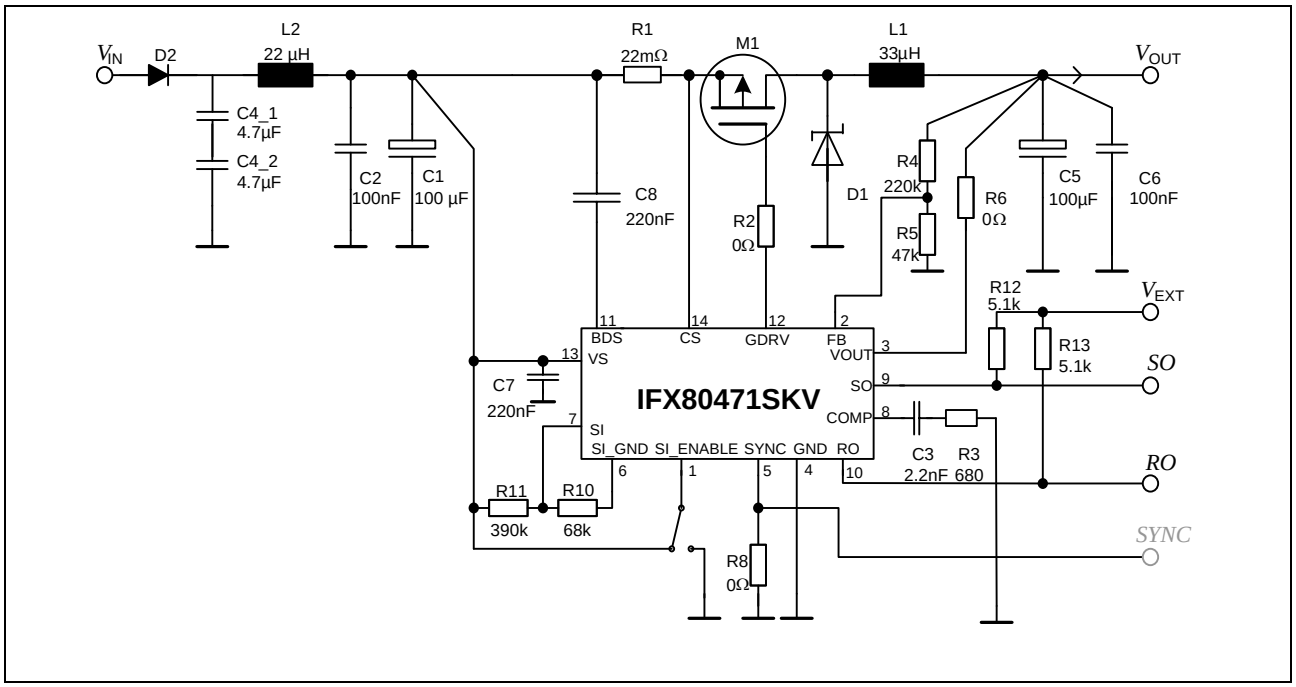


Figure 3 Schematic of the demo board for IFX80471SKV.

Table 1 Components recommendation – BOM for IFX80471SKV

Device	Supplier	Type	Value & Remark
L1	Coilcraft	DO-3340P-333	33µH, 2.0A, 80mΩ
L2	Coilcraft	DO-3340P-223	22µH, 2.5A, 66mΩ
C1	Various	Al-Electrolytic capacitor	100µF, 63V
C2		Ceramic capacitor	X7R, 100nF, >60V[1]
C3		Ceramic capacitor	X7R, 2.2nF, 16V
C4_1, C4_2	TDK	Ceramic capacitor C4532X7R1H475M	X7R, 4.7µF, 50Vq
C5	EPCOS	Tantalum electrolytic capacitor B45010D1076M506	Low ESR, 'Speed Power'
C6		Ceramic capacitor	X7R, 100nF, 16V
C7	TDK	Ceramic capacitor C3216X7R2A224	X7R, 220nF, 100V
C8	Various	Ceramic capacitor	X7R, 220nF, 16V
C9	not assembled		
R1		Resistor	22mΩ, ±1%
R2,R6,R8			0Ω
R3		Resistor	680Ω
R4		Resistor	220kΩ
R5		Resistor	47kΩ
R7,R9	not assembled		
R10		Resistor	68kΩ
R11		Resistor	390kΩ
R12,R13		Resistor	5.1kΩ
D1	ON	Schottky Diode	MBRD 360, 3A, 60V
D2	Various	Diode, S3D	3A
M1		P-channel MOSFET	BSP 613P [2]

3.1 About the IFX80471SKV demo board

The IFX80471SKV has open drain outputs at the pins RO and SO. The pull up resistors R12 and R13 on the demo board are connected to the V_EXT pad. V_EXT should be connected to an appropriate pull up voltage source (usually the microcontroller I/O voltage source). The pull up resistors have been assembled with a value of R12=R13=5.1kΩ. This resistor value should be checked with respect to the actual I/O voltage and microcontroller requirements. The driving capability of the reset output and sense output are described in the datasheet (under "Electrical Characteristics", item 5.1.40 and 5.1.55).

The synchronizing function is disabled by the 0Ω resistor R8 connecting pin 5 directly to GND. In case the synchronizing function is needed **make sure R8 is removed before connecting a TTL-Level frequency source to the SYNC connector of the demo board**.

[1] Mounted on PCB back side

[2] Pin 2 (GND) to be cut before assembly on demo board

4 Dimensioning of the external components

The equations for the dimensioning of the external components L1, R1 are given in the datasheet in chapter 7, where the dimensioning of the feedback divider resistors R4 and R5 is discussed.

In this application note a practical approach how to apply these equations for given application requirements is shown.

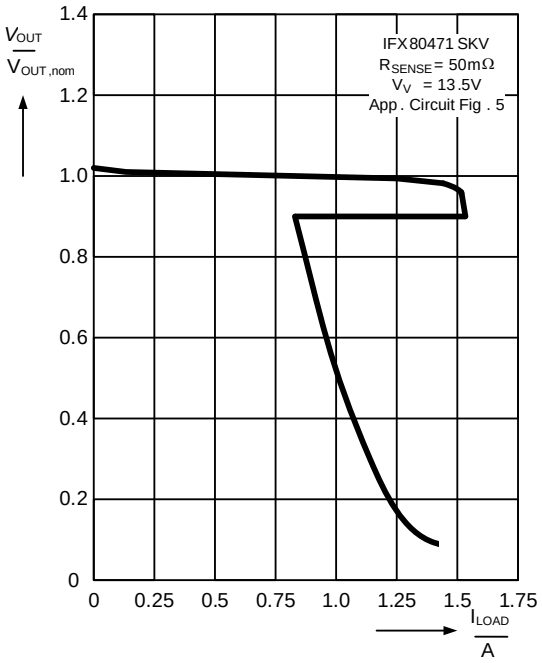


Figure 4 Example of typ. characteristic of the output current limit (foldback).

4.1 Variable output voltage

For the IFX80471SKV variable device demo board we use the same output current target as for the fixed voltage version: 2.0A, with permission to be in the foldback current limit range (see Fig. 4). The desired output voltage should be typ. 7.10V.

We should now fix the feedback output voltage divider. The datasheet (chapter 7.3) allows a range from 5kΩ to 500kΩ for R5 (corresponds to R_{FB2}). We have selected a value of R5= 47kΩ.

Using the feedback voltage value of 1.25V (item 5.1.12 of the electrical characteristics in the datasheet) we can calculate R4 as

$$R4= 47k\Omega\cdot(7.10V/1.25V -1) = 220k\Omega .$$

The following procedure is very similar to component dimentioning for the 5V versions. The shunt resistor is given by the current limitation target.

From the datasheet (Chapter 7.8.2) the equation for R1 is:

$$R1 = V_{LIM} / 2\cdot I_{PEAK;PWM} .$$

V_{LIM} is specified in the electrical characteristics as item 5.1.27 ‘peak current limit threshold voltage’, 50mV…90mV. To get the worst case (lowest) current we apply the equation above, but we leave out the factor 2 since we have accepted to enter the foldback part of the current characteristic. We get

$$R1\_max= 50mV/2.0A= 25m\Omega.$$

We have to take into account that we have not yet considered the ripple current which reduces the maximum available load current according to the equation

$$I_{Peak,PWM}=I_{Load}+0.5 \cdot \Delta I$$

To continue we select R1 as

R1=22mΩ .

Using this value we can calculate the maximum allowed ripple current, assuming still a load current of 2.0A:

$$\Delta I\_max = \frac{50mV/22m\Omega - 2.0A}{0.5} = 545mA.$$

In order to keep the output voltage ripple as low as possible we choose a ripple current of 300mA in the typical operation condition with 13.5V VBAT, corresponding to 15% of the 2.0A maximum load current. In the datasheet, chapter 7.8.1 we find the equation,

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{f_{SW} \cdot V_{IN} \cdot L1}$$

which we now use to define the buck inductance L1.

$$L1 = \frac{(13.5V - 5.0V) \cdot 5.0V}{370kHz \cdot 13.5V \cdot 300mA} = 30\mu H \ .$$

We select the next norm value:

L1=33µH.

Now it remains to check if the stability conditions arising from the slope compensation are fulfilled. The inequation from chapter 7.8.1 in the datasheet gives us

$$(2.0x10^{-4}) \bullet (V_{OUT}) \bullet (R_{SENSE}) < L1 < (4.0x10^{-4}) \bullet (V_{OUT}) \bullet (R_{SENSE})$$

$$(2.0x10^{-4}) \bullet (7.1V) \bullet (22m\Omega) < L1 < (4.0x10^{-4}) \bullet (7.1V) \bullet (22m\Omega)$$

$$31\mu H < L1 < 62\mu H \ ,$$

which confirms that our selected inductance is good to maintain stability.

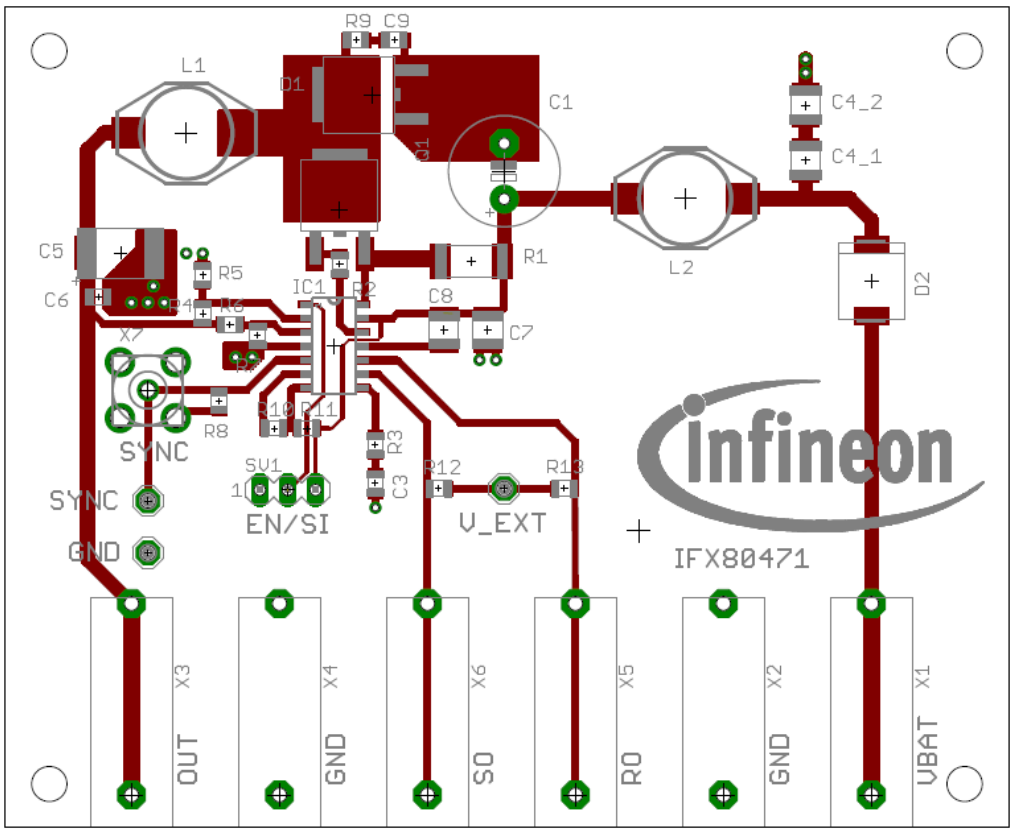
5 Components placement and PCB layout of the Demo Board

For EMC optimization the demo board comes with an input Π-Filter (C4, L2, and C1). Thus emission from the VBAT line is largely suppressed.

For proper operation and to avoid stray inductance paths the external catch diode, the Buck inductance and the input capacitor C_{IN1} have to be connected as close as possible to the PMOS device. Also the GDRV path from the controller to the switching transistor should be as short as possible. Best suitable for the connection of the cathode of the catch diode and one terminal of the inductance would be a small plain located next to the drain of the PMOS.

The GND connection of the catch diode must be also as short as possible. In general the GND level should be implemented as surface area over the whole PCB as second layer.

The most sensitive points for coupled switching noise are the feedback path to the pins FB and VOUT and the input path. Also switching noise coupled back to the SYNC input must be avoided. These paths should be kept away from the switching node. On the demo board also the ceramic capacitor C6 helps to suppress potential noise on the feedback line.



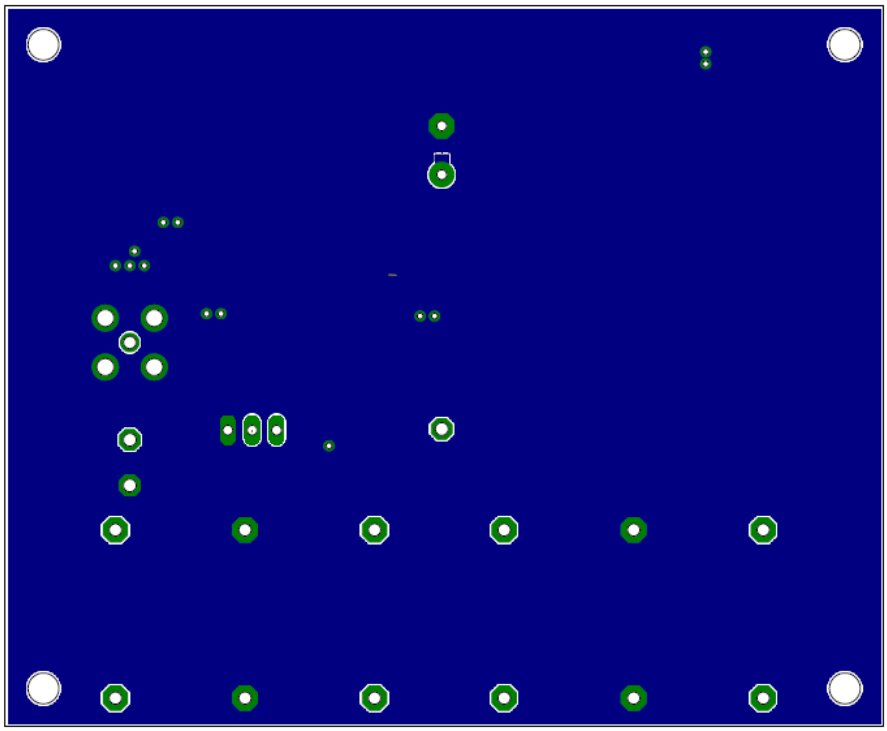
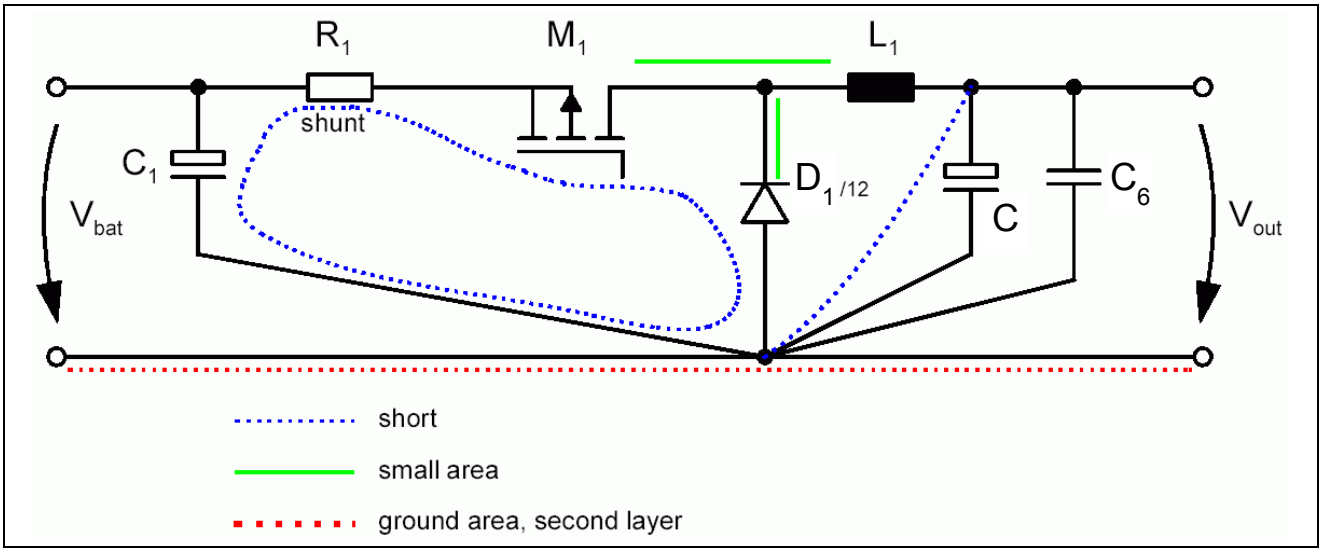


Figure 5 PCB Layout Front and Back

6 General Layout Recommendations

It is important to follow the layout recommendations given in this section. The commutation circuit input capacitor C1, the PMOS M1 and the free-wheeling diode D1 should be as compact as possible in order to have low inductance. The area of the connection M1-L1-D1 should be as small as possible. This can be seen in the Figure 7 as the green highlighted area and the blue trace respectively. The Input and Output capacitors should have a short low inductance link.



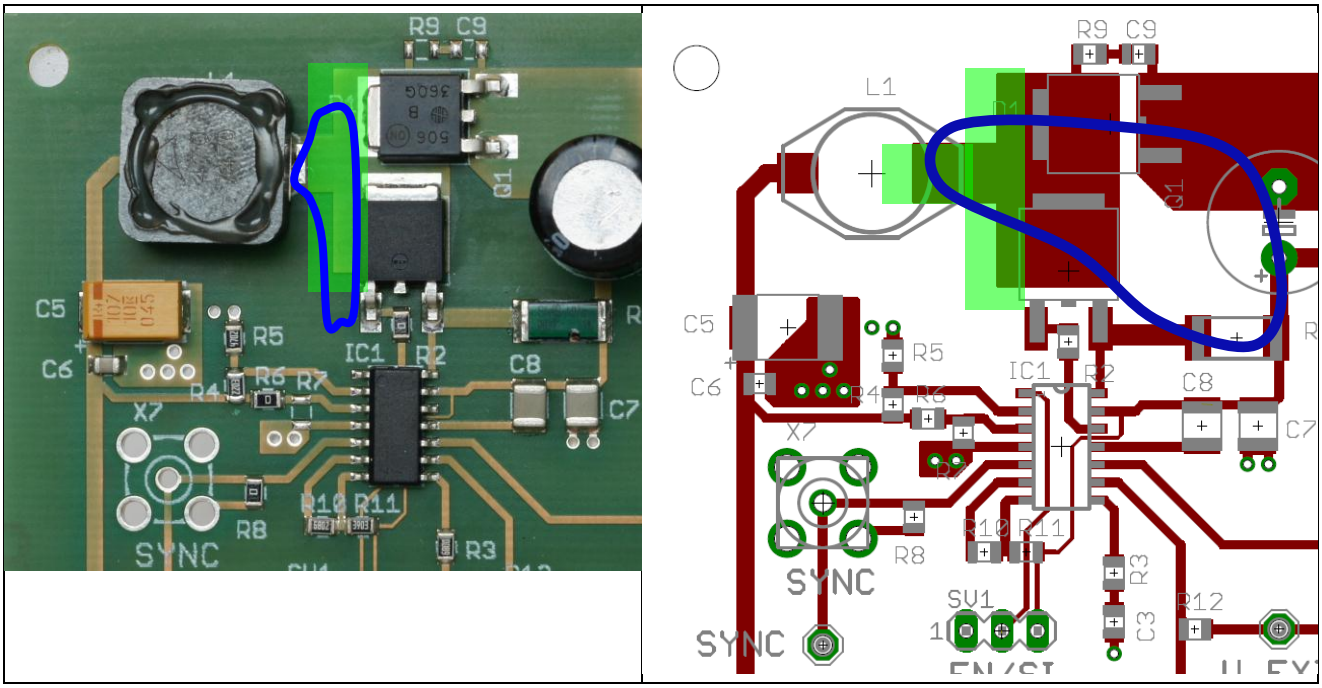


Figure 6 Layout Recommendations (Blue Line: Short Connection, Green: Small Area)

The supply voltage should be routed via the pins of the input capacitors. The output voltage should be routed via the pins of the output capacitors. It is recommended to design the ground as a ground area in a 2nd layer. There should be a direct connection of all GND terminals of input capacitors, free-wheeling diode D1, output capacitors, the IC, RC elements and filter capacitors. Use a star shaped ground link to avoid ground looping. Separate the ground system; connect to external wiring ground only via a single trace. Connect the current sensing IC terminals (pin 13 and 14) directly to the shunt R1 and design to be short.

Please also make sure the following pins are free from any switching noise:

- Pin 2: [FB], Feedback Input. Keep the PCB traces far from switching nodes to prevent from coupled switching noise. Use of low-ESR ceramic capacitors recommended.
- Pin 3: [VOUT], Buck Output Voltage Input. Use low-ESR ceramic capacitors.
- Pin 5: [SYNC], Input for external frequency synchronization.
- Pin 8: [COMP], Compesation Input.
- Pin 13: [VS], Device Supply Input. Spikes at VS may influence the Bandgap reference generating positive feedback that might cause instability. Usage of low-ESR ceramic capacitors in the range 220nF to 1µF is recommended.

For further details about the pin definitions and functions please refer to section 3.2 of the IFX80471 datasheet.

7 Additional Information

- For further information please refer to **www.infineon.com/industrial-standard**
- For technical support please write to support@infineon.com

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