Freescale Semiconductor
Application Note

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MPC8569E PowerQUICC III Design Checklist

This document provides recommendations for new designs based on the MPC8569E PowerQUICC III family of integrated host communications processors (collectively referred to throughout this document as MPC8569E):

- MPC8569E
- MPC8569

This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

For updates to this document, see the website listed on the last page.

Contents

1 Simplifying the First Phase of Design

This section outlines recommendations to simplify the first phase of design. Before designing a system with a MPC8569E device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

Figure 1 shows the major functional units within the device.

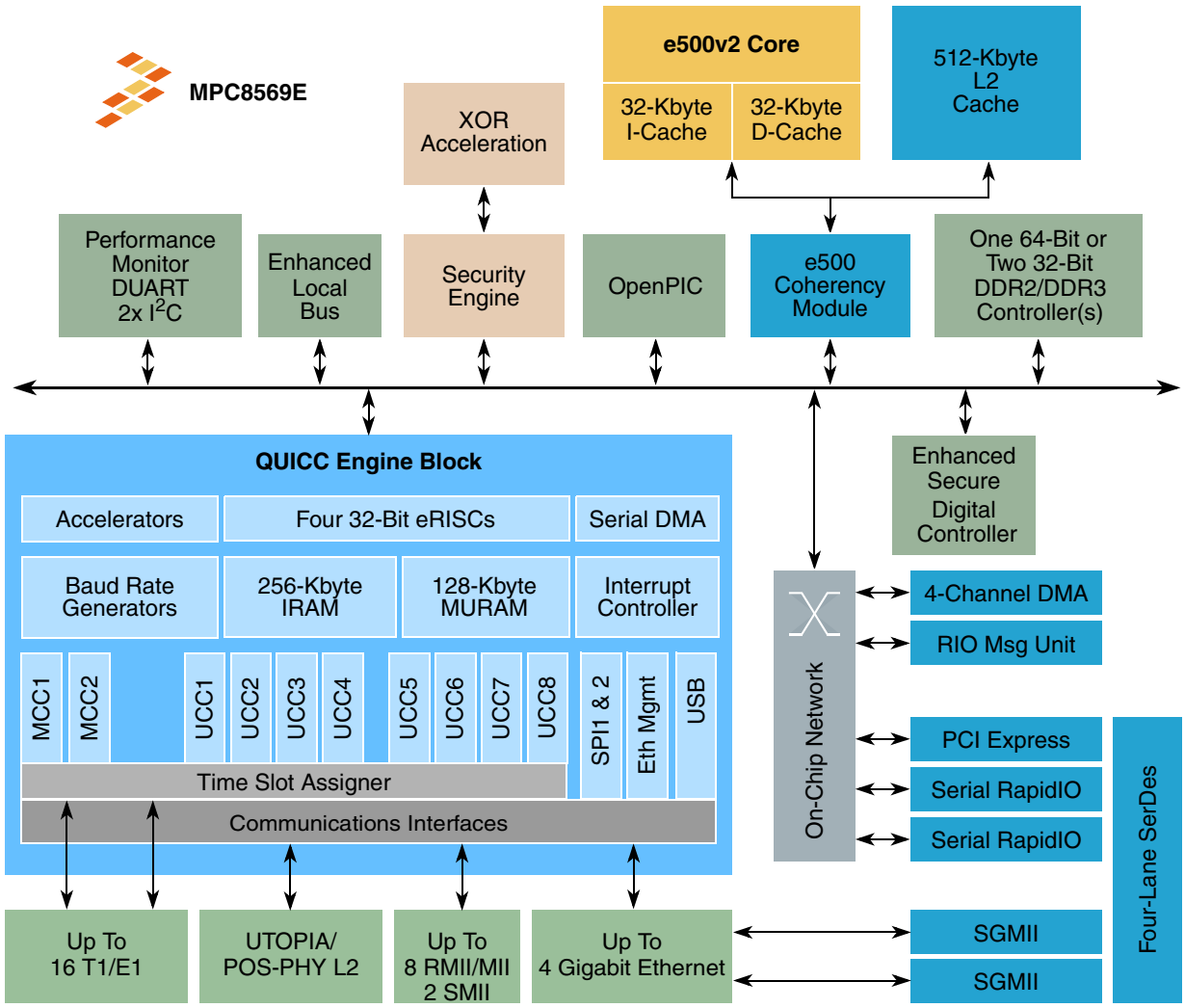


Figure 1. MPC8569E Block Diagram

1.1 Recommended References

Table 1 lists helpful tools, training resources, and references, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. MPC8569E Helpful Tools and References

ID	Name	Location
Related Documentation		
MPC8569EFS	*MPC8569 PowerQUICC III Fact Sheet*	www.freescale.com
MPC8569ERM	*MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual*	www.freescale.com
MPC8569ERMAD	*Errata to MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual*	Contact your Freescale representative
QEIWRM	*QUICC Engine Block Reference Manual with Protocol Interworking*	www.freescale.com
MPC8569ECE	*Device Errata for the MPC8569E PowerQUICC III*[1]	Contact your Freescale representative
MPC8569EEC	*MPC8569E PowerQUICC III Integrated Processor Hardware Specifications*	Contact your Freescale representative
AN4311	*SerDes Reference Clocking and HSSI Measurements Recommendations.*	Contact your Freescale representative
AN3369	*PowerQUICC DDR2 SDRAM Controller Register Setting Considerations*	www.freescale.com
AN2910	*Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces*	www.freescale.com
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.freescale.com
AN3939	*DDR Interleaving for PowerQUICC and QorIQ Processors*	www.freescale.com
AN3781	*Utilizing Extra FC Credits for PCI Express Inbound Posted Memory Write Transactions in PowerQUICC III Devices*	www.freescale.com
AN4039	*DDR3 SDRAM Controller Register Setting Considerations*	www.freescale.com
AN3830	*Hardware Debugging Using the CodeWarrior IDE*	www.freescale.com
AN3869	*Implementing SGMII Interfaces on the PowerQUICC III*	www.freescale.com
AN2919	*Determining the I2C Frequency Divider Ratio for SCL*	www.freescale.com
MPC8569E-MDS-PB	*MPC8569 Module Development System Processor Board User Guide*	www.freescale.com
MPC8569E-MDS-PB_HGS	*MPC8569MDS Hardware Getting Started Guide*	www.freescale.com
PQMDSPIBUM	*PowerQUICC Modular Development System Platform I/O Board User's Manual*	www.freescale.com
PQMDSPIBUMAD	*PowerQUICC Modular Development System Platform I/O Board Hardware Getting Started Guide*	www.freescale.com

Table 1. MPC8569E Helpful Tools and References (continued)

ID	Name	Location
Software Tools		
I2CBOOTSEQ	The boot sequencer tool configures any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I^2C EEPROM. The MPC8569E requires a particular data format for register changes as outlined in the MPC8569ERM. The I2CBOOTSEQ is a C-code file. When compiled and given a sample data file, it generates the appropriate raw data format as outlined in the MPC8569ERM. The file that is generated is an S-record file that can be used to program the EEPROM.	Contact your Freescale representative
LBCUPMIBCG	The UPM programming tool allows programming of all three of the MPC8569E's UPM machines. The LBCUPMIBCG features a GUI, which consists of a wave editor, a table editor, and a report generator. The user can edit the waveform or the RAM array directly. At the end of programming, the report generator prints out the UPM RAM array that can be used in a C-program.	Contact your Freescale representative
CommExpert Tool	The CommExpert tool is part of the NetComm device driver software package available for download. It includes the following: • Pin muxing tool • Complete QUICC Engine block and processor API configuration support	www.freescale.com/netcommsw
Hardware Tools[2]		
MPC8569MDS	Modular development system, including schematics, bill of materials, and board errata list	Contact your Freescale representative
PQMDSPIB	PowerQUICC Modular Development System Platform I/O Board	www.freescale.com
Models		
IBIS	To ensure first path success, Freescale strongly recommends using the IBIS models for board level simulations, especially for SerDes and DDR characteristics.	www.freescale.com
BSDL	Use the BSDL files in board verification.	www.freescale.com
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	www.freescale.com
Available Training		
—	Our third-party partners are part of an extensive alliance network. More information can be found at www.freescale.com/alliances.	www.freescale.com/alliances
—	Training materials from past Smart Network Developer's Forums and Freescale Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the MPC8569E.	www.freescale.com/alliances

1 The MPC8569ECE describes the device errata, fixes, and workarounds for the MPC8569E. This errata document must be researched thoroughly prior to starting a design with the MPC8569E device.

2 Design requirements in the device hardware specification and design checklist supersede the design/implementation of the MDS system.

1.2 Product Revisions

Table 2 lists the processor version register (PVR) and system version register (SVR) values for the various MPC8569E derivatives of silicon.

Table 2. Revision Level to Part Marking Cross-Reference

MPC8569E Revision	e500 V2 Core Revision	Processor Version Register	Mask Number	System Version Register
1.0	4.0	0x8021_1040	M38P	0x8088_0010 (with Security Engine)
2.0	5.0	0x8021_1050	M63X	0x8088_0020 (with Security Engine)
			M63X	0x8080_0020 (without Security Engine)
2.1	5.1	0x8021_1051	M63X	0x8088_0021 (with Security Engine)
			M63X	0x8080_0021 (without Security Engine)

2 Power Design Considerations

This section provides design considerations for the MPC8569E power supplies and power sequencing. For information about AC and DC electrical specifications and thermal characteristics for the MPC8569E, see the *MPC8569E PowerQUICC III Integrated Processor Hardware Specifications* (MPC8569EEC).

2.1 I/O DC Power Supply Recommendation

Operating-mode power dissipation numbers (typical, thermal, and maximum) are provided in the *MPC8569E PowerQUICC III Integrated Processor Hardware Specifications* (MPC8569EEC). Table 3 shows the estimated typical I/O power dissipation for the I/O power supplies for this device.

Table 3. MPC8569E I/O Power Supply Estimated Values

Interface	Parameters	1.0 V (XV_{DD})	1.1 V (XV_{DD})	1.5 V (GV_{DD})	1.8 V (B/GV_{DD})	2.5 V (B/LV_{DD})	3.3 V (B/LV_{DD})	Unit
DDR	400 MHz, v1x32 bits	—		—	0.53	—	—	W
	400 MHz, 2x32 bits	—		—	0.88	—	—	W
	400 MHz, 1x64 bits	—		—	0.69	—	—	W
	533 MHz, 1x32 bits	—		—	0.59	—	—	W
	533 MHz, 2x32 bits	—		—	0.97	—	—	W
	533 MHz, 1x64 bits	—		—	0.77	—	—	W
	667 MHz, 1x32 bits	—		0.40	0.64	—	—	W
	667 MHz, 2x32 bits	—		0.70	1.10	—	—	W
	667 MHz, 1x64 bits	—		0.53	0.85	—	—	W
	800 MHz, 1x32 bits	—		0.43	0.70	—	—	W
	800 MHz, 2x32 bits	—		0.76	1.21	—	—	W
	800 MHz, 1x64 bits	—		0.58	0.93	—	—	W
eLBC	33 MHz, 16b	—		—	0.047	0.089	0.132	W
	66 MHz, 16b	—		—	0.057	0.107	0.162	W
	133 MHz, 16b	—		—	0.078	0.143	0.222	W
	150 MHz, 16b	—		—	0.083	0.152	0.237	W
sRIO	4x, 3.125 Gbps	0.063	0.076	—	—	—	—	W
PCI Express	4x, 2.5 Gbps	0.056	0.068	—	—	—	—	W
QUICC Engine UCC	MII/RMII	—		—	—	—	0.036/0.020[1]	W
	GMII/TBI	—		—	—	—	0.083[1]	W
	RGMII/RTBI	—		—	—	0.042[1]	—	W

Note:
1. LV_{DD} power numbers are applicable to a single QE UCC port

2.2 PLL Power Supply Filtering

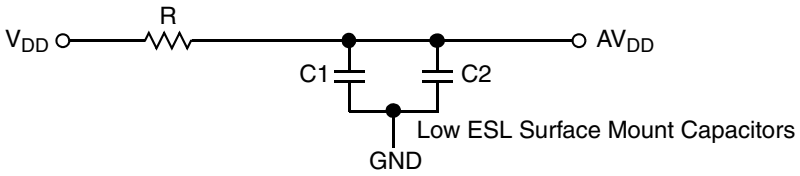
Each of the PLLs is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_QE, AV_{DD}_LBIU, and AV_{DD}_SRDS, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution (and the solution to which the device is guaranteed) is to provide independent filter circuits per PLL power supply,

as illustrated in Figure 2, one to each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

The PLL power supply filter circuit filters noise in the PLLs' resonant frequency range from 500 kHz–10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.



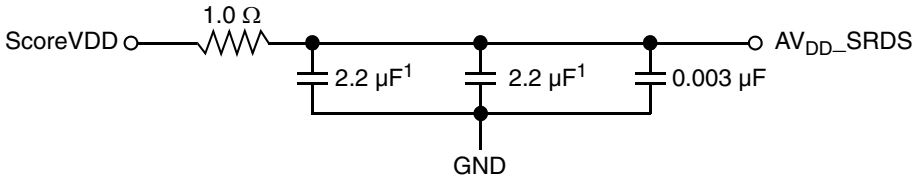
Notes:
1. R = 5.1 Ω ±5%.
2. C1 = 10 μF ± 10%, 0603, X5R with ESL ≤ 0.5 nH.
3. C2 = 1.0 μF ± 10%, 0402 X5R with ESL ≤ 0.5 nH.

Figure 2. PLL Power Supply Filter Circuit

NOTE

A higher capacitance value for C2 can be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 3. For maximum effectiveness, the filter circuit is placed as close as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS ball. The 0.003-μF capacitor is closest to the ball, followed by the two 2.2-μF capacitors, and finally the 1.0-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



1. An 0805 sized capacitor is recommended

Figure 3. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS should be a filtered version of ScoreVDD.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

CAUTION

These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.

2.3 Power Supply Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8569E system, and the device itself requires a clean, tightly regulated source of power.

The recommendations for ensuring a reliable power supply are as follows:

- Provide large power planes because immediate charge requirements by the device are always serviced from the power planes first.
- Place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and $LV_{DD}n$ pins of the device.
  - These decoupling capacitors should receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and $LV_{DD}n$, and GND planes in the PCB, utilizing short traces to minimize inductance.
  - Capacitors may be placed directly under the device using a standard escape pattern, and others may surround the part.
  - These capacitors should have a value of 0.1 µF. Only use ceramic surface mount technology (SMT) capacitors to minimize lead inductance, preferably 0402 or smaller.
- Distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and $LV_{DD}n$ planes to enable quick recharging of the smaller chip capacitors.
  - These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary.
  - They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).
  - The capacitors need to be selected to work well with the power-supply so as to be able to handle the MPC8569E's dynamic load requirements. Customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

2.4 SerDes Block Power Supply Decoupling Recommendations

If the SerDes module is used, it requires a clean, tightly regulated source of power (ScoreVDD and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined, as follows:

- Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.
- The board should have at least one 0.1-µF SMT ceramic chip capacitors as close as possible for each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias,

these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.

- There should be a 10-µF ceramic chip capacitor on the power plane of the ScoreVDD and/or XVDD planes, on the sides of the device where those planes are present. This should be done for all SerDes supplies.

2.5 Power Supplies Checklist

Table 4. Power Supplies Checklist for Designer

Description	Customer Comments	Completed
V_{DD}, AV_{DD}_n, ScoreVDD, XV_{DD} power supplies have a voltage tolerance no greater than 3% from the nominal value. Refer to the hardware specification for more details.		
All other power supplies have a voltage tolerance no greater than 5% from the nominal value. Refer to the hardware specification for more details.		
Choose UCC Ethernet supplies according to the mode of operation used. Refer to the hardware specification for more details.		
Power supply selected is based on MAXIMUM power dissipation. Refer to the hardware specification for more details.		
Thermal design is based on THERMAL power dissipation. Refer to the hardware specification for more details.		
Power-up sequence is within 50 ms. Refer to the hardware specification for more details.		
Recommend using large power planes to the extent possible		
Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_QE, and AV_{DD}_LBIU.		
If SerDes is enabled, the recommended PLL filter circuit is applied to AV_{DD}_SRDS, respectively. Otherwise, a filter is not required.		
PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.		
Decoupling capacitors of 0.1 µF are placed at each V_{DD}, B/G/L/OV_{DD} pin.		
Bulk capacitors are placed on each V_{DD}, B/G/L/OV_{DD} plane.		
If SerDes is enabled, the recommended decoupling for SCORE/XV_{DD} is used.		

3 Power-On Reset and Reset Configurations

3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These power-on reset (POR) inputs are either pulled high or low during this period. While these pins may be output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum of 10 SYSCLK. When $\overline{\text{HRESET}}$ de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal input/output circuit characteristics.

All of the configuration pins have an internally gated 20 kΩ nominal pull-up or pull-down resistor, enabled only during HRESET. For those configurations in which the default state is desired, no external resistor is required. Otherwise, a 4.7 kΩ pull-down (or pull-up) resistor is recommended to pull the configuration pin to a valid logic low (or high) level. If the default setting is not a valid setting, 4.7 kΩ pull-up or pull-down resistors are required for proper configuration.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals to the MPC8569E when HRESET is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 2 SYSCLK set-up time to HRESET), hold their values for at least 8 SYSCLK cycles after the de-assertion of HRESET, and then release the pins to high impedance afterward for normal device operation.

3.2 Configuration Settings

See the MPC8569ERM for a more detailed description of each configuration option shown in Table 5.

Table 5. MPC8569E User Configuration Options

Configuration Type	Functional Pins	Comments
System PLL Ratio	LA[24:27]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. See Section 6.2.3, “Platform to SYSCLK PLL Ratio.”
DDR PLL Ratio	QE_PE[27:29]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. See Section 6.2.6, “DDR to SYSCLK PLL Ratio.”
e500 core PLL Ratio	LBCTL, LALE, LGPL2/LOE/LFRE	There is no default value for this PLL ratio; these signals must be pulled to the desired value. See Section 6.2.4, “e500 Core to Platform Clock PLL Ratio.”
QE Block PLL Ratio	LCS3, LCS[4:7]/IRQ[8:11]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. See Section 6.2.5, “QUICC Engine Block to SYSCLK PLL Ratio
Boot ROM Location	QE_PB[27:28], QE_PC4, QE_PD4	There is no default value for this PLL ratio; these signals must be pulled to the desired value.
Host/Agent	LCS[0:2]	Default: 111. MPC8569E acts as the host processor/root complex on all interfaces
I/O Port Selection	LA[18:21]	Default: 1111. PCI Express® port active (×4) (2.5 Gbps)
CPU Boot	LA[23]	Default: 1. e500 core is allowed to boot without waiting for configuration by an external master
Boot Sequencer	LGPL3/LFWP, LGPL5	Default: 11. Boot sequencer is disabled. No I^2C ROM is accessed
DDR SDRAM Type	QE_PF11	Default: 1. DDR controller is configured for DDR2
DRAM Mode	LGPL1/LFALE	Default: 1. Primary DDR controller is enabled (64-bit width data bus). Secondary DDR is disabled
SerDes Reference Clock Configuration	LA16	Default: 1. SerDes expects a 100 MHz reference clock frequency

Table 5. MPC8569E User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
RapidIO Device ID	QE_PF9, LA17, $\overline{\text{DMA\_DACK0}}$	Default: The three lower-order bits of the RapidIO device ID are set to all 1s.
RapidIO System Size	LGPL0/LFCLE	Default: 1. Small system size (up to 256 devices).
DDR1 Debug	UART_SOUT0/$\overline{\text{DMA\_DREQ3}}$/SD_DAT1	Default: 1. Debug information is not driven on ECC pins. ECC pins function in their normal mode.
DDR2 Debug	$\overline{\text{DMA\_DONE0}}$	Default: 1. Debug information is not driven on ECC pins. ECC pins function in their normal mode.
General Purpose POR	LAD[0:15]	There is no default value for this general purpose POR.
eLBC ECC Enable	QE_PF14	Default: 1. eLBC ECC enabled after POR.
e500 core speed	QE_PF10	Default: 1. Core clock frequency is less than or equal to 1000MHz.
DDR speed	$\overline{\text{DMA\_DDONE1}}$/MSRCID2	Default: 1. DDR data rate is less than 500MHz.

3.3 Supply Power Default Setting

The MPC8569E is capable of supporting multiple power supply levels on its I/O supply. The signals used for these voltage selections are not POR configurations. This section describes the encoding used to select the voltage level for each I/O supply.

CAUTION

Incorrect voltage select settings can lead to irreversible device damage. Follow this section carefully.

Table 6. I/O Supply Voltage Select Settings

Voltage Select Input	Voltage Select Setting[1]	Supply Voltage (V)	Interfaces Effected
LVDD_VSEL0	0	$LV_{DD}1 = 3.3$	QUICC Engine block UCC1, UCC3
	1	$LV_{DD}1 = 2.5$	
LVDD_VSEL1	0	$LV_{DD}2 = 3.3$	QUICC Engine block UCC2, UCC4
	1	$LV_{DD}2 = 2.5$	
BVDD_VSEL[0:1]	00	$BV_{DD} = 3.3$	Enhanced local bus
	01	$BV_{DD} = 2.5$	
	10	$BV_{DD} = 1.8$	
	11	$BV_{DD} = 3.3$	

Note:
1. Logic 0 corresponds with a static tie to GND, while a logic 1 corresponds with a static tie to OV_{DD} (3.3 V).

For proper use, the voltage select device input signals LVDD_VSEL0, LVDD_VSEL1, and BVDD_VSEL[0:1] must be statically tied to reflect the voltage applied on the $LV_{DD}1$, $LV_{DD}2$, and BV_{DD} I/O supplies, respectively, as shown in Table 6. For example, for enhanced local bus operation at 2.5 V, the BVDD_VSEL[0] and BVDD_VSEL[1] device inputs must be configured to 01, and thus be tied on the

board to GND and OV_{DD}, respectively. For a 2.5-V operation, tying BVDD_VSEL[0] and BVDD_VSEL[1] to anything except GND and OV_{DD}, respectively can lead to irreversible device damage.

3.4 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only; if enabled during reset, they may result in the MPC8569E not coming out of reset. Table 7 lists these pins and explains how they should be addressed during the reset sequence.

Table 7. Internal Test Mode Pins

Pin Group	Pins	Guideline for Reset
Debug	TRIG_OUT/READY/QUIESCE	Because these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release these pins to high impedance during reset.
	DMA_DACK1/MSRCID1	
Design For Test	LSSD_MODE	These pins must be pulled to OV_{DD} via a 100 Ω–1 kΩ resistor.
Thermal Management	Reserved[0:2]	Recommend that a weak pull-down resistor (2–10 kΩ) resistor be placed on this pin to GND.
Power Management	ASLEEP	Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release these pins to high impedance during reset.
System Control	HRESET_REQ	

3.5 POR and Reset Configurations Checklist

Table 8. Checklist for POR and Reset Configurations for Designer

Description	Customer Comments	Completed
HRESET is asserted for a minimum of 10 SYSCLKs.		
The following signals are NOT pulled low during POR sequence: • HRESET_REQ • TRIG_OUT/READY/QUIESCE • DMA_DACK1/MSRCID1 • ASLEEP, LA22 • LCLK[0:1] • LWE0/LBS0/LFWE • IRQ_OUT • QE_PB[7,26,31] • QE_PD0 • QE_PE[24:26] • QE_PF13 • CKSTP_OUT		
The following signals are NOT pulled high during POR sequence: LWE1/LBS1		
Configuration pins are either appropriately tied-off with a 4.7 kΩ resistor, or driven by an external device (meeting their required setup and hold times). Otherwise, default configurations are used.		
PLL configurations are defined and meet the required set-up and hold times.		

Table 8. Checklist for POR and Reset Configurations for Designer (continued)

Description	Customer Comments	Completed
Voltage select input pins must be statically tied to reflect the voltage applied on the $LV_{DD}1$, $LV_{DD}2$, and BV_{DD} I/O supplies.		
Internal test mode pins, except for thermal management pins, are guaranteed to not be low during reset.		

4 Debug and Test Pin Recommendations

Table 9 shows how the debug and test pins should be connected.

Table 9. Debug and Test Pin Recommendations

Pin Name	Pin Used	Pin Not Used
ASLEEP	This pin must NOT be pulled down during power-on reset.	This pin must be left unconnected.
CLK_OUT	NOTE: This output is actively driven during reset rather than being tri-stated during reset.	This pin may be left unconnected.
MDVAL/IRQ6	—	If IRQ function of this pin is not used, tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{LSSD\_MODE}}$	These signals must be pulled up via a 100–1000 Ω resistor to OV_{DD} for normal machine operation.	
MSRCID0/$\overline{\text{DMA\_DREQ1}}$	—	If DMA function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
MSRCID1/$\overline{\text{DMA\_DACK1}}$	This pin must NOT be pulled down during power-on reset	This pin must be left unconnected.
MSRCID2/$\overline{\text{DMA\_DDONE1}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left unconnected.
MSRCID3/IRQ4	—	If IRQ function of this pin is not used, tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
MSRCID4/IRQ5	—	If IRQ function of this pin is not used, tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
SD_IMP_CAL_RX	This pin must be pulled down through a 200 Ω (±1%) resistor.	
SD_IMP_CAL_TX	This pin must be pulled down through a 100 Ω (±1%) resistor.	
SD_PLL_TPA	Do not connect.	
SD_PLL_TPD	Do not connect.	
THERM[0:2]	Recommend that a weak pull-down resistor (2–10 kΩ) be placed on this pin to GND.	

Table 9. Debug and Test Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
TRIG_IN	—	Tie low through a 2–10 kΩ resistor to GND.
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	This pin must NOT be pulled down during power-on reset.	This pin must be left unconnected.

5 Device Pins and Recommended Test Points

For easier debug, include the pins listed in Table 10 on the board.

Table 10. Recommended Pins for Easier Debug

Test Point Pin	Helps Verify:
CLK_OUT	The various internal clocks, as selected by the CLKOCR register
SYSCLK	Input clock at the device pin
MDVAL and MSRCID[0:4]	Memory debug signals
TRIG_OUT	The end of the reset sequence
ASLEEP	The end of the reset sequence
SENSEVDD	Power plane VDD
SENSEVSS	Ground plane VSS
$\overline{\text{CKSTP\_OUT}}$	Core checkstop indication
HRESET_REQ	Proper boot sequencer functions and reset requests

6 Clocks

Table 11 shows how the input clock pin functions and explains how they should be connected.

Table 11. Clock Pin Functions and Recommendations

Clock Pin Name	Function	Pin Used	Pin Not Used
TX_CLK	Used by the UCC Ethernet controller as a reference clock for gigabit Ethernet modes	If any of the UECs are used in gigabit mode, connect to a 125 MHz reference clock.	Program as GPO or use alternate function of pin
RTC	Optionally used to clock the e500 core timer and the PIC global timer facilities	The default source of the time base is the CCB clock divided by eight. For more details, see the *PowerPC e500 Core Complex Reference Manual*.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$	Reference clock for the PCI Express®, RapidIO and SGMII interfaces	If SerDes is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection.[1]	These pins must be connected to GND.
SYSCLK	Primary clock input to the device	Must always be connected to an input clock of 66–133 MHz	

Note:

[1] If SerDes is enabled, corresponding SerDes Reference Clock must be provided to successfully complete POR.

6.1 System Clocking

This section describes the PLL configuration of the MPC8569E. Note that the platform clock is identical to the internal Core Complex Bus clock (CCB_clk).

This device includes six PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 6.2.3, “Platform to SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock using the platform clock as the input. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 6.2.4, “e500 Core to Platform Clock PLL Ratio.”
- The enhanced local bus PLL generates the clock for the enhanced local bus.
- There is a PLL for the SerDes block.
- The QUICC Engine block PLL generates the QUICC Engine clock from the externally supplied SYSCLK.
- The DDR complex PLL generates clocking for the DDR controllers.

6.2 Clock Ranges

Table 12 provides the clocking specifications for the processor core, platform, memory, and enhanced local bus.

Table 12. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1067 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	500	800	500	1067	500	1333	MHz	1, 2
Platform/CCB clock frequency	333	400	333	533	333	533	MHz	1
Memory bus clock frequency	200	300	200	333	200	400	MHz	1, 3
Enhanced local bus clock frequency	20.81	100	20.81	133	20.81	133	MHz	4
Security Engine (SEC) clock frequency	166.5	200	166.5	267	166.5	533	MHz	5

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 6.2.3, "Platform to SYSCLK PLL Ratio," and Section 6.2.4, "e500 Core to Platform Clock PLL Ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.
3. The memory bus speed is half of the DDR2/DDR3 data rate.
4. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the *MPC8569E PowerQUICC III Integrated Processor Family Reference Manual* for more information.
5. SEC 1:1 mode is valid for Bin 1 devices only.

6.2.1 DDR Clock Ranges

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is sourced from a separate PLL than the rest of the platform.

Table 13 provides the clocking specifications for the memory bus.

Table 13. Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	200	400	MHz	1, 2, 3, 4

Notes:
1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 6.2.3, "Platform to SYSCLK PLL Ratio," and Section 6.2.4, "e500 Core to Platform Clock PLL Ratio," for ratio settings.
2. The memory bus clock refers to the MPC8569E memory controllers' Dn_MCK[0:2] and $\overline{\text{Dn\_MCK}}$[0:2] output clocks, running at clock frequencies that are half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 6.2.6, "DDR to SYSCLK PLL Ratio." The memory bus clock frequency must be less than or equal to the platform clock rate, which in turn must be less than the DDR data rate.

6.2.2 Selecting the DDR Data Rate or Platform Frequency

As a general guideline, use the following procedure for selecting the DDR data rate or platform frequency:

1. Start with the processor core frequency selection.
2. After the processor core frequency is determined, select the platform frequency from the options listed in Table 15.
3. Check the platform to SYSCLK ratio to verify a valid ratio can be chosen from Table 14.
4. If the desired DDR data rate can be the same as the platform frequency, use the synchronous DDR mode. Otherwise, if a higher DDR data rate is desired, use asynchronous mode by selecting a valid DDR data rate to DDRCLK ratio from Table 17. Note that in asynchronous mode, the DDR data rate must be greater than the platform frequency. In other words, running a DDR data rate lower than the platform frequency in asynchronous mode is not supported by the MPC8569E.
5. Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

6.2.3 Platform to SYSCLK PLL Ratio

The clock that drives the internal CCB bus is called the platform clock. The frequency of the CCB is set using the following signals, as shown in Table 14:

- SYSCLK input signal
- Binary value on LA[24:27] at power up

Note that there is no default for this PLL ratio; These signals must be pulled to the desired values.

Also note that in synchronous mode, the DDR data rate is the determining factor for selecting the platform bus frequency because the platform frequency must equal the DDR data rate. In asynchronous mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 14. Platform Clock Ratio

Binary Value of LA[24:27] Signals	Platform: SYSCLK Ratio	Binary Value of LA[24:27] Signals	Platform: SYSCLK Ratio
0000	Reserved	1000	8:1
0001	Reserved	1001	Reserved
0010	2:1	1010	Reserved
0011	3:1	1011	Reserved
0100	4:1	1100	Reserved
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	7:1	1111	Reserved

6.2.4 e500 Core to Platform Clock PLL Ratio

The clock ratio between the e500 core and the platform clock is determined by the binary value of LBCTL, LALE, and LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ signals at power up. Table 15 describes the clock ratio between the e500 core clock and the platform clock.

Table 15. e500 Core to Platform Clock Ratios

Binary Value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ Signals	e500 Core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ Signals	e500 Core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2 (4.5:1)	101	5:2 (2.5:1)
010	1:1	110	3:1
011	3:2 (1.5:1)	111	7:2 (3.5:1)

6.2.5 QUICC Engine Block to SYSCLK PLL Ratio

The QUICC Engine clock is defined by a multiplier applied to the SYSCLK input signal, as shown in the following equation:

$$\textit{QUICC Engine clock} = \textit{SYSCLK} \times \textit{cfg\_qe\_pll[0:4]} \qquad \textit{Eqn. 1}$$

The multiplier is determined by the binary value of $\overline{\text{LCS}}$[3:7] at power-up.

Table 16 shows the QUICC Engine clock multiplier.

Table 16. QUICC Engine Clock Multiplier

Binary Value of $\overline{\text{LCS}}$[3:7] Signals	Multiplier
0_0000	Reserved
0_0001	Reserved
0_0010	2
0_0011	3
0_0100	4
0_0101	5
0_0110	6
0_0111	7
0_1000	8
0_1001	9
0_1010	10
0_1011	Reserved
0_1100	Reserved
0_1101	Reserved
0_1110	Reserved
0_1111	Reserved

6.2.6 DDR to SYSCLK PLL Ratio

The dual DDR memory controller complexes can either be synchronous with or asynchronous to the platform, depending on their configuration.

Table 17 describes the clock ratio between the DDR memory controller complexes and SYSCLK. The DDR memory controller complexes' clock frequency is equal to the DDR data rate.

When synchronous mode is selected, the memory buses are clocked at half the platform clock rate. The mode of operation is for the DDR data rate for both DDR controllers to be equal to the platform clock rate (in synchronous mode) or the resulting DDR Complex Clock PLL to SYSCLK ratio as shown in Table 17 (in asynchronous mode).

The DDR clock is defined by a multiplier applied to the SYSCLK input signal, as shown in the following equation:

$$\textit{DDR clock} = \textit{SYSCLK} \times \textit{cfg\_ddr\_pll[0:2]} \qquad \textit{Eqn. 2}$$

The multiplier is determined by the binary value of QE_PE[27:29] at power-up, as shown in Table 17.

Table 17. DDR Complex Clock PLL Ratio

Binary Value of QE_PE[27:29] Signals	DDR Complex Clock: SYSCLK Ratio
000	3:1
001	4:1
010	5:1
011	6:1
100	8:1
101	10:1
110	12:1
111	Synchronous mode (DDR data rate = CCB clock)

NOTE

Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, by disabling the unused clocks, it lowers the power consumption and lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section.

6.2.7 SYSCLK and Platform Frequency Options

Table 18 shows the expected frequency options for SYSCLK and platform frequencies.

Table 18. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Clock Frequency (MHz)[1]				
2:1				—	—
3:1				333	400
4:1		333	400	445	533
5:1	333	415	500		
6:1	400	500	—		
7:1	467	—			
8:1	533				

Note:
1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).

6.2.8 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64} \qquad \text{Eqn. 3}$$

7 DDR Pin Recommendations

NOTE

When using DDR3 at the 800 MHz data rate, it is recommended that DDR3 DIMM or Discrete DRAM rated at 1066 MHz data rate or more be used.

Table 19. DDR Pin Recommendations

Pin Name	Pin Used	Pin Not Used
Dn_MA[0:15]	Auto-precharge for DDR signaled on A10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on A8 when DDR_SDRAM_CFG[PCHB8] = 1.	These pins may be left unconnected.
Dn_MBA[0:2]	Connect to memory module or discrete memory.	
$\overline{\text{Dn\_MCAS}}$	Connect to memory module or discrete memory.	
MCK/$\overline{\text{MCK}}$[0:2]	—	Unused MCK pins must be disabled via DDRCLKDR.
Dn_MCKE[0:3]	These pins are actively driven instead of being tri-stated during reset.	These pins may be left unconnected.
$\overline{\text{Dn\_MCS}}$[0:3]	—	
Dn_MDIC[0:1]	When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GVDD through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.	These pins may be left unconnected.
$\overline{\text{Dn\_MAPAR\_ERR}}$	—	This pin should be connected to GVDD via a 2-10 kΩ resistor.
Dn_MAPAR_OUT	—	These pins may be left unconnected.
D1_MDM[0:8], D2_MDM[0:3], D2_MDM[8]	—	These pins may be left unconnected.
Dn_MDQ[0:31]	—	These pins may be left unconnected.
D1_MDQS[0:8], D2_MDQS[0:3], D2_MDQS[8]	—	These pins may be left unconnected.
$\overline{\text{D1\_MDQS}}$[0:8], $\overline{\text{D2\_MDQS}}$[0:3], $\overline{\text{D2\_MDQS}}$[8]	—	These pins may be left unconnected.
Dn_MECC[0:7]	—	These pins may be left unconnected.

Table 19. DDR Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
Dn_MODT[0:3]	—	These pins may be left unconnected.
$\overline{\text{Dn\_MRAS}}$	—	
$\overline{\text{Dn\_MWE}}$	—	
Dn_MVREF	MVREF can be generated using a divider from GVDD as MVREF. This value is expected to be equal to 0.5 × GVDD. Another option is to use supplies that generate GVDD, VTT, and MVREF voltage. These methods help reduce differences between GVDD and MVREF. MVREF generated from a separate regulator is not recommended as MVREF will not track GVDD as closely.	These pins may be left unconnected when not used.

8 DMA Pin Recommendations

Table 20 shows how the DMA pins should be connected.

Table 20. DMA Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{DMA\_DREQ}}$[0]	—	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ}}$[1]/MSRCID0	—	If the debug function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ}}$[2]/SD_DAT0	—	If the SD function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ}}$[3]/UART_SOUT0/SD_DAT1	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
$\overline{\text{DMA\_DACK}}$[0]	These pins are reset configuration pins and may require 4.7 kΩ pull-up or pull-down resistors.	
$\overline{\text{DMA\_DACK}}$[1]/MSRCID1	This pin must NOT be pulled down during power-on reset.	This pin must be left unconnected.
$\overline{\text{DMA\_DACK}}$[2]/SD_CMD	—	If the SD function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DACK}}$[3]/UART_SIN0/SD_DAT2	—	If the DUART and SD functions of this pin are not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DDONE}}$[0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
$\overline{\text{DMA\_DDONE}}$[1]/MSRCID2	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.

Table 20. DMA Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
DMA_DDONE[2]/SD_WP	—	If the SD function of this pin is not used, this output pin may be left floating.
DMA_DDONE[3]/UART_CTS0/SD_DAT3	—	If the DUART and SD functions of this pin are not used, pull high through a 2–10 kΩ resistor to OV_{DD}.

9 DUART Pin Recommendations

Table 21 shows how the DUART pins should be connected.

Table 21. DUART Pin Recommendations

Pin Name	Pin Used	Pin Not Used
UART_CTS0	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
UART_RTS0	—	This output pin may be left floating.
UART_SIN0	—	Tie low through a 2–10 kΩ resistor to GND.
UART_SOUT0/ DMA_DREQ3/ SD_DAT1	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.

10 QUICC Engine Block Communication Interfaces

The QUICC Engine block communication interfaces include the following:

- Ethernet controller
  - Media independent interface (MII)
  - Gigabit media independent interface (GMII)
  - Serial media independent interface (SMII)
  - Serial gigabit media independent interface (SGMII)
  - Ten-bit interface (TBI)
  - Reduced media independent interface (RMII)
  - Reduced gigabit media independent interface (RGMII)
  - Reduced ten-bit interface (RTBI)
- ATM
- UTOPIA/POS
- IEEE 1588™v2 support
- Ethernet PHY management
- GPIO
- Universal asynchronous receiver/transmitter (UART)
- Universal serial bus controller (USB)

- Serial peripheral interface (SPI)

NOTE

The Pin Muxing tool within CommExpert is recommended for simplifying design; see Table 1.

10.1 UCC Ethernet Interface

Table 22. UCC Ethernet Checklist

Description	Customer Comments	Completed
UCC1 and UCC3 share the same power supply $LV_{DD}1$; UCC2 and UCC4 share the same power supply $LV_{DD}2$. This puts the limitation on the interface choices. For example, UCC1 GMII and UCC3 RGMII is not supported because GMII requires 3.3 V while RGMII requires 2.5 V.		
The MII and RMII interfaces are supported on all UCCs. The RGMII and RTBI are supported on UCC1 through UCC4. The TBI and GMII are supported on UCC1 and UCC2. The SMII and SGMII are supported on UCC6 and UCC8. Refer to the UCC Ethernet Controller chapter of the QEIWRM for more details.		
The I/O supply voltage select pins, LVDD_VSEL0 and LVDD_VSEL1, must match selected UCC1/UCC3 and UCC2/UCC4 operations.		
Program GUMR[MODE] to Ethernet mode. Then configure the QUICC Engine block port pin.		
For 1000Mbps operation, a 125 MHz reference clock, which is typically from PHY device, must be provided to the corresponding UCC TX_CLK. For GMII and TBI modes, TX_CLK is provided to UCC1 through QE_PC[8:11,14,15] (CLK9:12,15,16) and to UCC2 through QE_PC[2,3,6,7,15:17](CLK3,4,7,8,16:18). For RGMII and RTBI modes, TX_CLK is provided to UCC1 and UCC3 through QE_PC[11](CLK12) and to UCC2 and UCC4 through QE_PC[16] (CLK17). For example, for UCC1, a 125 MHz clock can be connected to PB[11]. Configure PB[11] to function as CLK12, and in CMXUCR1 register, configure transmit clock as CLK12.		

10.2 Ethernet Management Interface

The Ethernet management interface can be controlled by a UCC or the SPI2 interface (see Section 10.6, “Serial Peripheral Interface (SPI)”). To use the UCC management interface, program PC30 and PC31 to CE MUX:MDIO and CE MUX:MDC, respectively.

Each UCC has its own built-in Ethernet management logic. CMXGCR[MEM] determines which UCC masters the serial management interface (SMI).

NOTE

The UCC selected by CMXGCR[MEM] must run in Ethernet mode to use its SMI registers, so the management registers of other UCCs cannot be used. For example, if the UCC1 management interface is used, the UCC2 management interface cannot be used.

10.3 UTOPIA/POS

If you are familiar with the UTOPIA interface of the CPM in MPC82xx and MPC85xx, note that the external signal naming convention of the QUICC Engine block follows the UTOPIA standard. Therefore, there is different naming in master and slave modes. The naming conventions in the CPM retain the master mode signal naming for slave mode. For example, the QUICC Engine block transmit TXSOC in slave mode is named RXSOC, but the CPM transmit SOC in slave mode is named TXSOC. In the QUICC Engine block, you should connect signals between master and slave by name. In the example here, we connect the external master TXSOC with the QUICC Engine TXSOC.

10.4 QUICC Engine UART

Any UCC can be programmed to function as a UART. Use the QUICC Engine UART if software backward-compatibility is important. The QUICC Engine UART programming model is compatible with that of the CPM SCC UART. See Section 9, "DUART Pin Recommendations," for more information.

10.4.1 UART Configuration

The pins of the QUICC Engine UART are on each UCC NMSI interface. They are programmed through the following registers:

- CPODRx: Determines the open-drain configuration. 1 bit per pin
- CPDIR1x, CPDIR2x: Determines the in/out characteristics of the pins. 2 bits per pin
- CPPAR1x, CPPAR2x: Determines the functionality of each pin. 2 bits per pin

Table 23 shows the QUICC Engine UART pin listings.

Table 23. QUICC Engine UART Pin Listing

UCC No.	Signal	QUICC Engine Port	Termination
UCC1	UART1_SOUT	PA0/UCC1_TXD[0]	If UART1 is not used, all the pins can be programmed for other functions.
	UART1_SIN	PA6/UCC1_RXD[0]	
	UART1_CTS	PA12/$\overline{\text{UCC1\_CTS}}$	
	UART1_RTS	PA4/$\overline{\text{UCC1\_RTS}}$	
UCC2	UART2_SOUT	PA14/UCC2_TXD[0]	Same as UCC1
	UART2_SIN	PA20/UCC2_RXD[0]	
	UART2_CTS	PA26/$\overline{\text{UCC2\_CTS}}$	
	UART2_RTS	PA18/$\overline{\text{UCC2\_RTS}}$	
UCC3	UART3_SOUT	PA29/UCC3_TXD[0]	Same as UCC1
	UART3_SIN	PB3/UCC3_RXD[0]	
	UART3_CTS	PB9/$\overline{\text{UCC3\_CTS}}$	
	UART3_RTS	PB1/$\overline{\text{UCC3\_RTS}}$	

Table 23. QUICC Engine UART Pin Listing (continued)

UCC No.	Signal	QUICC Engine Port	Termination
UCC4	UART4_SOUT	PB12/UCC4_TXD[0]	Same as UCC1
	UART4_SIN	PB18/UCC4_RXD[0]	
	UART4_CTS	PB24/$\overline{\text{UCC4\_CTS}}$	
	UART4_RTS	PB16/$\overline{\text{UCC4\_RTS}}$	
UCC5	UART5_SOUT	PD0/UCC5_TXD[0]	Same as UCC1
	UART5_SIN	PD6/UCC5_RXD[0]	
	UART5_CTS	PD12/$\overline{\text{UCC5\_CTS}}$	
	UART5_RTS	PD4/$\overline{\text{UCC5\_RTS}}$	
UCC6	UART6_SOUT	PD14/UCC6_TXD[0]	Same as UCC1
	UART6_SIN	PD20/UCC6_RXD[0]	
	UART6_CTS	PD26/$\overline{\text{UCC6\_CTS}}$	
	UART6_RTS	PD18/$\overline{\text{UCC6\_RTS}}$	
UCC7	UART7_SOUT	PD28/UCC7_TXD[0]	Same as UCC1
	UART7_SIN	PE2/UCC7_RXD[0]	
	UART7_CTS	PE8/$\overline{\text{UCC7\_CTS}}$	
	UART7_RTS	PE0/$\overline{\text{UCC7\_RTS}}$	
UCC8	UART8_SOUT	PE10/UCC8_TXD[0]	Same as UCC1
	UART8_SIN	PE16/UCC8_RXD[0]	
	UART8_CTS	PE22/$\overline{\text{UCC8\_CTS}}$	
	UART8_RTS	PE14/$\overline{\text{UCC8\_RTS}}$	

10.5 USB Controller

The USB controller interfaces to the bus through a differential line driver and differential line receiver. The output enable signal, $\overline{OE}$, enables the line driver when the USB controller transmits on the bus.

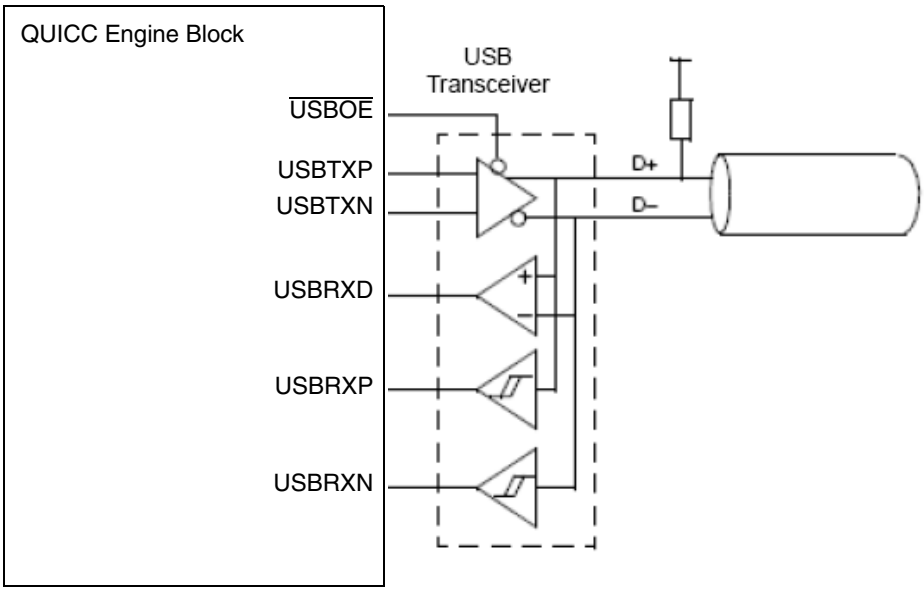


Figure 4. USB Interface

In addition, a reference clock must be provided. CMXGCR[USBCS] determines the source of the USB clock. The USB reference clock must be four times the USB bit rate (48 MHz for a 12-Mbps full-speed transfer or 6 MHz for a 1.5-Mbps low-speed transfer).

Table 24. USB Pins and Connections

Signal	QUICC Engine Port	Termination
$\overline{USB\_OE}$	PF3	If USB is not used, program these signals for general-purpose IO or other QUICC Engine functions.
USB_TP	PF4	
USB_TN	PF5	
USB_RP	PF6	
USB_RN	PF8	
USB_RXD	PF7	
USBCLK	CLK3, CLK5, CLK7, CLK9, CLK13, CLK17, CLK19, CLK21, BRG9, BRG10	

10.6 Serial Peripheral Interface (SPI)

The MPC8569E supports two serial peripheral interfaces (SPI1 and SP2). SPI2 also supports Ethernet PHY management.

Table 25. SPI Pin Listing

SPI No.	Signal	Pin Type	QUICC Engine Port	Termination
SPI1	SPIMOSI	I/O	PE27	• Configure for another function if not used for SPI1. • For systems supporting SPI multi-master mode, configure to open drain and pull up to OV_{DD}.
	SPIMISO	I/O	PE28	• Configure for another function if not used for SPI1 • For systems supporting SPI master and slave modes, configure to open drain and pull up to OV_{DD}.
	SPICLK	I/O	PE29	• Configure for another function if not used for SPI1 • For systems supporting SPI master and slave modes, configure to open drain and pull up to OV_{DD}.
	SPISEL	I	PE30	Master mode: Pullup to OV_{DD} Slave mode: Pulldown to GND
SPI2	SPIMOSI	I/O	PB28/PC30	• Configure for another function if not used for SPI2. • For systems supporting SPI multi-master mode, configure to open drain and pull up to OV_{DD}.
	SPIMISO	I/O	PB29	• Configure for another function if not used for SPI2 • For systems supporting SPI master and slave modes, configure to open drain and pull up to OV_{DD}.
	SPICLK	I/O	PB30/PC31	• Configure for another function if not used for SPI2 • For systems supporting SPI master and slave modes, configure to open drain and pull up to OV_{DD}.
	SPISEL	I	PB31	Master mode: Pullup to OV_{DD} Slave mode: Pulldown to GND
SPI2	MDIO	I/O	PB28/PC30	Configure for other function if not used for SPI2
	MDC	O	PB30/PC31	Configure for other function if not used for SPI2

11 I^2C Pin Recommendations

Table 26. I^2C Pin Recommendations

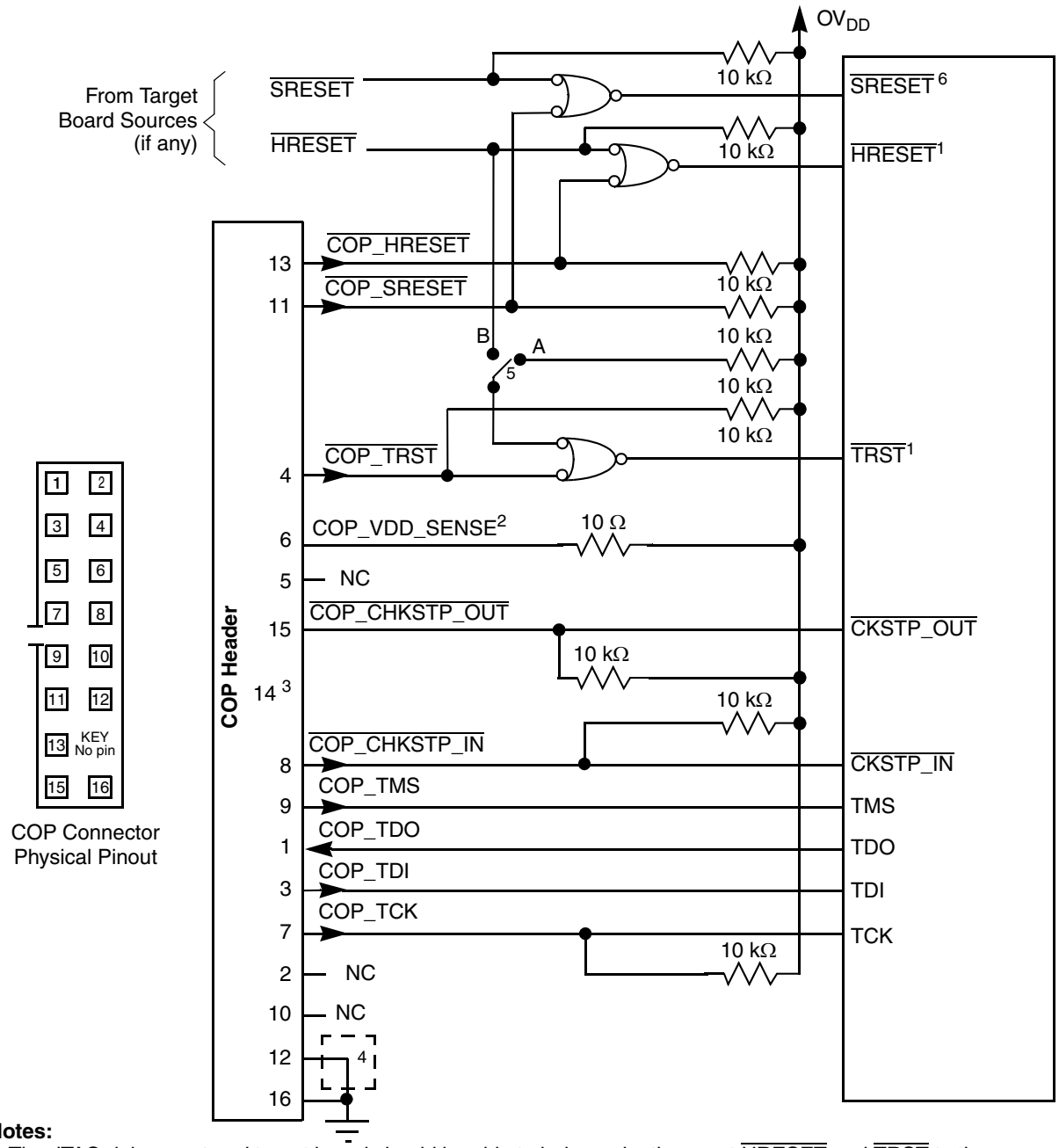
Pin Name	Pin Used	Pin Not Used
IIC1_SCL	Tie these open-drain signals high through a 1 kΩ resistor to OV_{DD}.	Tie high through a 2–10 kΩ resistor to OV_{DD}.
IIC2_SCL		
IIC2_SDA/SD_CLK		
IIC2_SCL/$\overline{\text{SD\_CD}}$		

12 JTAG Interface

12.1 Required Configuration for JTAG Operation

To correctly operate the JTAG interface, configure the group of system control pins as shown in Figure 5.

These pins must be maintained at a valid de-asserted state under normal operating conditions because most have asynchronous behavior, and spurious assertion gives unpredictable results.



Notes:

1. The JTAG debug port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10-Ω (1/6W rating; 0402 or larger) resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the JTAG debug header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 5. JTAG Interface Connection

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors built on Power Architecture® technology.

The MPC8569E requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the JTAG state machine can be forced into the Test Logic Reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The common on-chip processor (COP) function of these processors allows a remote computer system, typically a PC with dedicated hardware and debugging software, to access and control the internal operations of the processor. The COP interfaces primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged along with these signals with logic.

Follow the arrangement shown in Figure 5 to allow the COP port to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 6, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an

IC). Regardless of the numbering scheme, the signal placement recommended in Figure 6 is common to all known emulators.

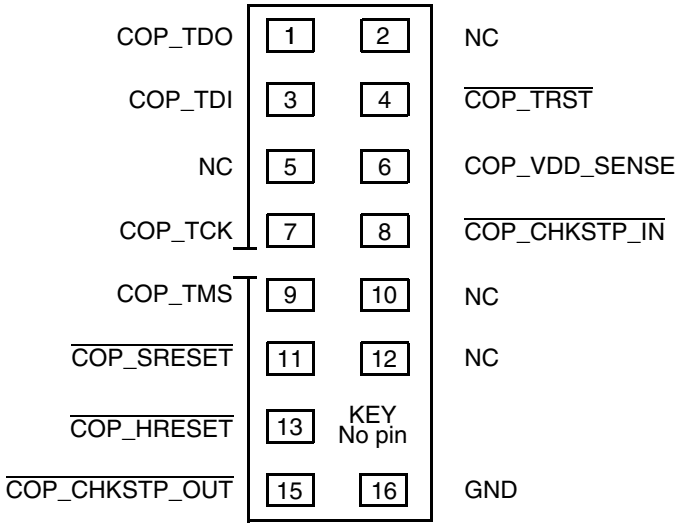


Figure 6. COP Connector Physical Pinout (Top View)

12.2 JTAG Pin Recommendations

If the JTAG interface and COP header are not used, connect the unused pins as follows:

- Tie $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 5. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Table 27. JTAG Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TCK	If COP is used, connect as needed plus strap to OVDD via 10 kΩ pull up. Connect to Pin7 of the COP connector.	If COP is unused, tie TCK to OV_{DD} through a 10-kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
TDI	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin3 of the COP connector	This pin may be left unconnected.
TDO	Connect to Pin1 of the COP connector	This pin may be left unconnected.
TMS	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin9 of the COP connector	This pin may be left unconnected.
$\overline{\text{TRST}}$	Connect as shown in Figure 5.	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 Ω resistor.

Table 27. JTAG Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
VDD_SENSE	Connect to Pin6 of the COP connector. Tie 10-Ω resistor to OV_{DD}.	This pin may be left unconnected.
$\overline{\text{COP\_CHKSTP\_IN}}$	Connect to Pin8 of the COP connector. Strap to OV_{DD} via 10 kΩ resistor.	This pin may be left unconnected.
$\overline{\text{COP\_SRESET}}$	Connect to Pin11 of the COP connector and $\overline{\text{SRESET}}$ (see Figure 5). Strap to OV_{DD} via 10 kΩ resistor.	This pin may be left unconnected.
$\overline{\text{COP\_HRESET}}$	Connect to Pin13 of the COP connector and $\overline{\text{HRESET}}$ (see Figure 5). Strap to OV_{DD} via 10 kΩ resistor.	This pin may be left unconnected.
$\overline{\text{COP\_CHKSTP\_OUT}}$	Connect to Pin15 of the COP connector. Strap to OV_{DD} via 10 kΩ resistor.	This pin may be left unconnected.

13 eLBC Pin Recommendations

Table 28. Local Bus Pin Recommendations

Pin Name	Pin Used	Pin Not Used
LA[16]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[18:21]		
LA[23]		
LA[17]	This pin is a reset configuration pin and may require a 4.7 kΩ pull-up or pull-down resistors.	
LA[22]	This pin must NOT be pulled down during power-on reset	This pin must be left unconnected.
LA[24:27]	This pin is a reset configuration pin that sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LAD[0:15]	Note that the LSB for the address = LAD[8:15]; however, the MSB for the data is on LAD[0:7].	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND, respectively, if the general purpose POR configuration is not used.
LALE	These pins are a reset configuration pins that set the core clock to CCB clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LBCTL		
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$		
LCLK[0]	This pin must NOT be pulled down during power-on reset	This pin must be left unconnected.
LCK[1]		
$\overline{\text{LCS}}$[0:2]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
$\overline{\text{LCS}}$[3]	These pins are reset configuration pins that set the QUICC Engine clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
$\overline{\text{LCS}}$[4:7]		

Table 28. Local Bus Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
LDP[0:1]	—	Tie high or low to the inactive state through a 4.7 kΩ resistor to BV_{DD} or GND, respectively.
LGPL0/LFCLE	These pins are reset configuration pins. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LGPL1/LFALE		
LGPL3/$\overline{\text{LFWP}}$		
LGPL5		
LGPL4/LUPWAIT/ LPBSE/$\overline{\text{LFRB}}$	For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a 2–10 kΩ pull up is required on this pin.	This pin either needs to be pulled-up via a 2–10 kΩ resistor to BV_{DD} or needs to be reconfigured as LPBSE prior to boot-up
LSYNC_IN	LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used.	LSYNC_IN needs to be directly connected to LSYNC_OUT.
LSYNC_OUT		
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$	This pin must NOT be pulled down during power-on reset	This pin must be left unconnected.
$\overline{\text{LWE}}$1/$\overline{\text{LBS}}$1	This pin must NOT be pulled up during power-on reset	This pin must be left unconnected.

14 PIC Pin Recommendations

Table 29. PIC Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IRQ[0:3]	A weak pull-up or pull-down may be needed to the inactive state.	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
IRQ4/ MSCRID3		
IRQ5/ MSCRID4		
IRQ6/ MDVAL		
IRQ8/ $\overline{\text{LCS4}}$		If IRQ[8:11] are not used, they may be programmed as LCS[4:7] pins. If these LCS pins are also not used, tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
IRQ9/ $\overline{\text{LCS5}}$		
IRQ10/ $\overline{\text{LCS6}}$		
IRQ11/ $\overline{\text{LCS7}}$		
$\overline{\text{IRQ\_OUT}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}.	This output pin may be left floating.

Table 29. PIC Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{MCP}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}.	
$\overline{\text{UDE}}$		

15 eSDHC Pin Recommendations

Table 30. eSDHC Pin Listing

Pin Name	Pin Used	Pin Not Used
SD_CLK/IIC2_SDA	A 33 Ω serial resistor must be provided for SD_CLK and placed close to the MPC8569 device.	If the I^2C function of this pin is not used, this pin may be left floating
SD_CMD/ $\overline{\text{DMA\_DACK2}}$	This pin requires a 10k–20 kΩ pull-up to OV_{DD}.	If the DMA function of this pin is not used, pull high through 2 k–10 kΩ resistor to OV_{DD}
SD_DAT[0]/ $\overline{\text{DMA\_DREQ2}}$	This pin requires a 10k–20 kΩ pull-up to OV_{DD}.	If the DMA function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
SD_DAT[1]/ UART_SOUT0/ $\overline{\text{DMA\_DREQ3}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pin requires a 10k–20 kΩpull-up to OV_{DD}.	If the POR default is acceptable, this pin may be left floating. If the DUART and DMA function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}
SD_DAT[2]/ UART_SIN0/ $\overline{\text{DMA\_DDACK3}}$	This pin requires a 10k–20 kΩ pull-up to OV_{DD}.	If the DUART and DMA function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}
SD_DAT[3]/ UART_CTS0/ $\overline{\text{DMA\_DDONE3}}$	When configured as SD, this pin requires a 10k–20 kΩ pull-up to OV_{DD}. Do not use DAT3 pin for SD card detection. See errata number A-004373 in the applicable chip errata document.	If the DUART and DMA function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}
$\overline{\text{SD\_CD}}$ / IIC2_SCL	This pin requires a 10k–20 kΩ pull-up to OV_{DD}.	If the I^2C function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
SD_WP/ $\overline{\text{DMA\_DDONE2}}$	This pin requires a 10k–20 kΩ pull-down to GND..	If the DMA function of this output pin is not used, pull low through a 2–10 kΩ resistor to GND.

16 SerDes Pin Recommendations

SerDes must always have power applied to its supply pins. Note that a valid clock input is required on SD_REF_CLK if SerDes is enabled.

NOTE

Failure to provide a reference clock for an enabled SerDes block prevents the device from completing POR sequence.

Table 31. SerDes Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD_PLL_TPD	Do not connect	
SD_PLL_TPA		
SD_RX[0:3]	—	These pins must be connected to GND.
$\overline{\text{SD\_RX}}$[0:3]		
SD_TX[0:3]	—	These pins must be left unconnected.
$\overline{\text{SD\_TX}}$[0:3]		
SD_IMP_CAL_RX	This pin must be pulled down through a 200 Ω (±1%) resistor.	
SD_IMP_CAL_TX	This pin must be pulled down through a 100 Ω (±1%) resistor.	
SD_REF_CLK	If SerDes is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection.[1]	These pins must be connected to SCOREGND.
$\overline{\text{SD\_REF\_CLK}}$		
SD_TX_CLK	Do not connect	
$\overline{\text{SD\_TX\_CLK}}$		

Note:

[1] If SerDes is enabled, the corresponding SerDes reference clock must be provided to successfully complete POR.

17 System Control Pin Recommendations

Table 32. System Control Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{CKSTP\_IN}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin8 of the COP connector (refer to Figure 5).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{CKSTP\_OUT}}$	Pull this open-drain signal high through a 2–10 kΩ resistor to OV_{DD}. This pin must NOT be pulled down during power-on reset. Connect to Pin15 of the COP connector (refer to Figure 5).	This pin must NOT be pulled down during power-on reset.
$\overline{\text{HRESET}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin13 of the COP connector (refer to Figure 5).	
$\overline{\text{HRESET\_REQ}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. This pin must NOT be pulled down during power-on reset.	This pin must NOT be pulled down during power-on reset.
$\overline{\text{SRESET}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin11 of the COP connector (refer to Figure 5).	Pull high through a 2–10 kΩ resistor to OV_{DD}.

18 Power and Ground Pin Recommendations

Table 33 describes each of the power supplies for the MPC8569.

Table 33. Power and Ground Pin Recommendations

Pin	Comment
AV_{DD}_CORE	Power supply for Core PLL (1.0/1.1 V through a filter)
AV_{DD}_DDR	Power supply for DDR (1.0/1.1 V through a filter)
AV_{DD}_LBIU	Power supply for Local Bus PLL (1.0/1.1 V through a filter)
AV_{DD}_QE	Power supply for QE PLL (1.0/1.1 V through a filter)
AV_{DD}_PLAT	Power supply for core complex bus PLL (1.0/1.1 V through a filter)
AV_{DD}_SRDS	Power supply for SerDes PLL (1.0/1.1 V through a filter)
BV_{DD}	Power supply for the Local Bus I/Os (1.8 V/2.5 V/3.3 V)
GND	Ground
GV_{DD}	Power supply for the DDR I/Os (1.5 V/1.8 V)
LV_{DD}1	Power supply for QUICC Engine Ethernet interface I/Os (2.5 V/3.3 V)
LV_{DD}2	Power supply for QUICC Engine Ethernet interface I/Os (2.5 V/3.3 V)
MVREF	DDR input reference voltage equal to approximately half of GV_{DD}
OV_{DD}	General I/O Supply (3.3 V)
SENSEVDD	This pin is connected to the V_{DD} plane internally and may be used by the core power supply to improve tracking and regulation.
SENSEVSS	This pin is connected to the GND plane internally and may be used by the core power supply to improve tracking and regulation.
ScoreVDD	Core power for SerDes transceivers (1.0/1.1 V)
XV_{DD}	Pad power for SerDes transceivers (1.0/1.1 V)
XGND	SerDes Transceiver Pad GND
SCOREGND	SerDes Core Logic GND
AGND_SRDS	SerDes PLL GND
V_{DD}	Power supply the core logic (1.0/1.1 V)

19 Thermal Recommendations

19.1 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

19.2 Thermal Management for FC-PBGA

This section provides thermal management information for the flip-chip plastic-ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design: the heat sink, airflow, and thermal interface material.

19.2.1 Attaching the Board to the Heat Sink

Figure 7 shows the recommended board attachment method to the heat sink. The heat sink should be attached to the printed-circuit board with the spring force centered over the package. This spring force should not exceed 10 pounds force (45 Newtons).

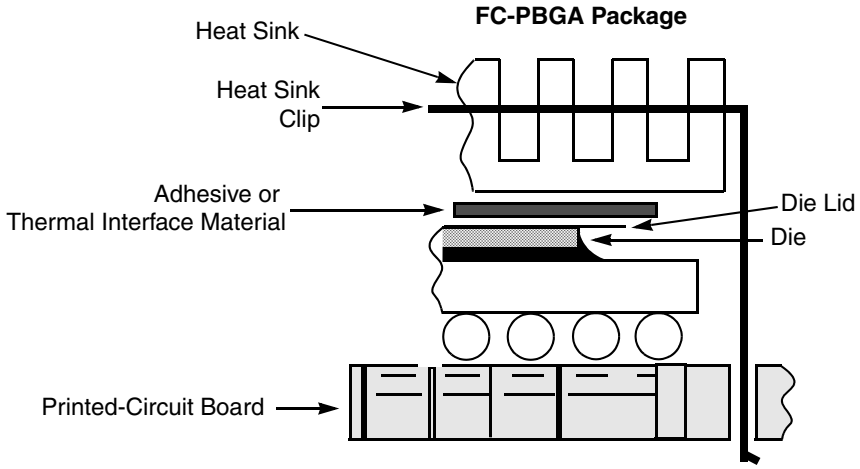


Figure 7. Recommended Board Attachment Exploded Cross-Sectional View

The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.2 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 8 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

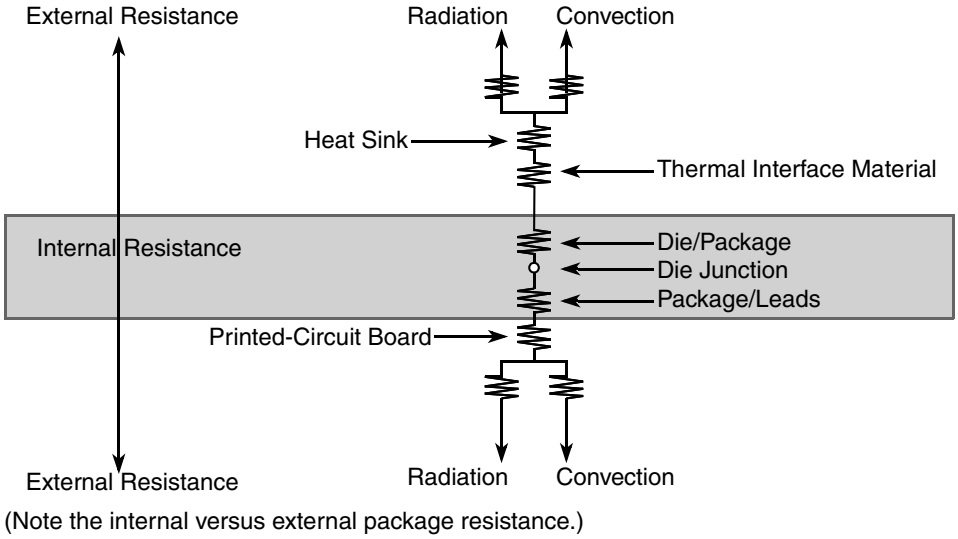


Figure 8. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted to the heat sink through the silicon and the heat sink attach material (or thermal interface material). The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

19.2.3 Minimizing Thermal Contact Resistance

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic chart to guide improved performance. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 7). The system board designer can choose among several types of commercially-available thermal interface materials.

20 Document Revision History

Table 34 provides a revision history for this application note.

Table 34. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	04/2014	• In Table 30, eSDHC Pin Listing: – Added resistor requirement for SD_CLK pin. – Updated pin usage for SD_DAT[3]/UART_CTS0/DMA_DDONE3. • In Table 7, removed DMA_DDONE1/MSRCID2 since it is not an internal test mode pin.
0	05/2011	• Initial public release

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Rev. 1
04/2014