PALMiCE FPGA Probing Function User's Manual

This manual describes the probing function and presents the basic usage patterns.

Chapter1 Introducing the Probing Function

The probing function makes it easy for the CSIDE debugging software to connect FPGA internal nodes (signals) to pins. This allows waveform monitoring based debugging to proceed smoothly.



The previously troublesome and time-consuming operation of modifying a source file, performing the logic synthesis/place and route operations, and finally performing a configuration operation can now be performed simply with just CSIDE operations, and execution only takes from under a minute to just a few minutes.



Note

- The signals that can be modified or added are the signals that have placement information (that is, the signals displayed in the CSIDE Node Location window). Signals that have been optimized in logic circuits cannot be routed. In this case, you must either use the CSIDE ISE linkage function (see Chapter4 ISE Linkage Function) or re-synthesize in the Xilinx FPGA development tool ISE.
- Since the actual routing operation uses the ISE FPGA editor, the ISE Web Pack is not supported.

The following section describes the probing function in detail.

Chapter2 Using the Probing Function



2.1.1 Linking by using the probing settings wizard

1. When registering and changing the monitored signals, click the **[Probing function]** button to enable the probing function. Then click **[Analyzer Pin Settings]**.

| Set Signal 🔀 |
|--|
| Signal Registration |
| Channel Color Close |
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| Probing function << |
| Chain number 1 - Analyzer pin settings |
| Node name |
| Channel: [BusSize = 0 / ?] |
| Channel Chain number Pin num. Node |
| Automatic channel allocation |
| |

2. The Probing Settings wizard is displayed. Register the FPGA pins according to the wizard procedure. Click **[Finish]** when done registering pins.



2.1.2 Linking by using commands

This section describes the procedure for linking using commands.

Commands are entered and executed in the Command window.

Use the "StateAnalyzerChannelPin" command. (See the Command Reference section in the PALMiCE FPGA Online Manual.)

Example1

To set the FPGA pin connected to channel 0 (CH0) to chain number 1 FPGA pin number M15. **StateAnalyzerChannelPin(0, 1, M15)**

It is also possible to set up multiple channels and FPGA pins easily by creating a macro file and executing it in the Command window.

| Мас | o file example: settings for channels 0 to 7 (CH0 to CH15) |
|-----|--|
| q} | bingset |
| | tateĀnalyzerChannelPin(0, 1, M15) |
| | tateAnalyzerChannelPin(1, 1, M16) |
| | tateAnalyzerChannelPin(2, 1, M13) |
| | tateAnalyzerChannelPin(3, 1, L14) |
| | tateAnalyzerChannelPin(4, 1, L15) |
| | (ateAnalyzerChannelPin(5, 1, L16)) |
| | (ateAnalyzerChannelPin(6, 1, L13) httoAnalyzerChannelPin(7, 1, K14) |
| | lateAnalyzerChamler m(7, 1, K14) |
| | lateAnalyzerChannelPin (9, 1, KT6) |
| | tateAnalyzerChannelPin (10, 1, L12) |
| | tateAnalyzerChannelPin(11, 1, K12) |
| | tateAnalyzerChannelPin(12, 1, K13) |
| | tateAnalyzerChannelPin(13, 1, J14) |
| | tateAnalyzerChannelPin(14, 1, J15) |
| | tateAnalyzerChannelPin(15, 1, J16) |

2.2 Registering Monitored Signals

The following methods can be used to register signals for waveform monitoring.

- Registration from the Editor window
- Registration from the Node Location window
- Registration from the analyzer settings

Editor - [1] c:\up380\up380. D × signal signal signal signal signal signal signal std_logic_vector(8 downto 0);4 std logic vector(7 downto 0);4 98 99 100 std logic; std_logic;4 101 102 103 104 105 106 107 108 109 Watch Ctrl + W er in the a GCK MEM signal signal signal signal signal Jump to bracket Ctrl + J Co T1MSEC0 nto 0):4 wnto 0);4 wnto 0);4 T500MSE F11 Next editor window T30MS TIM_U Previous editor wind 110 111 Key macro signal SWRST Print Cut Copy Paste Properties

| Node | IOB | CLB/SLICE | |
|-----------|--------------------------|---------------|--|
| buzon . | .YQ | CLB_R22C18.S1 | |
| clk_1ms | vn | B_R19C43.S0 | |
| count12_ | Watch | B_R21C18.S0 | |
| count12 | Watch all | B_R21C18.S0 | |
| count12 | Expand bus and watch | B_R20C18.S0 | |
| count12 | Register in the analyzer | B_R20C18.S0 | |
| count12 | | B_R19C18.S0 | |
| count12 | Update | B_R19C18.S0 | |
| count12 | Freeze | B_R18C18.S0 | |
| count12 | Always top | B_R18C18.S0 | |
| count12 | | B_R17C18.S0 | |
| count12 | Properties | | |
| gck_m 📜 | .xų | CEB_R25C37.S0 | |
| inc_enab] | .e .YQ | CLB_R27C20.S1 | |
| maddr[8:0 | 91 .O | | |

2.2.1 Registration from the Editor and Node Location windows

Registration from the Editor window

Registration from the Node Location window

Right click on the signal to be registered and select [Register in the Analyzer] from the pop-up menu.

2.2.2 Registration from the analyzer settings

Right click anywhere in the Analyzer window and select **[Analyzer settings]** from the pop-up menu. The Analyzer Settings dialog box will be displayed. Signals can be registered with the **[Set trigger and signal]** tab. See **Chapter3 Trying the Probing Function** for details.

The signals that can be registered as monitored signal are the signals that have placement information (that is, the signals displayed in the CSIDE Node Location window).

Signals that have been optimized in logic circuits cannot be routed.

The sequence of modifying the source file, performing the logic synthesis/place and route operations, and finally performing a configuration operation is required to monitor signals that have no placement information. However, these operations can also be performed in CSIDE using the ISE linkage function. (See Chapter4 ISE Linkage Function.)

This chapter describes the probing function using a sample program.

This sample program is written in the VHDL language. It is a simple circuit consisting of 8-bit counter and flip flop elements.

The sample program is shown here.



3.1 Linking Channels to FPGA Pins

First, we link the channels to the FPGA pins.

In this section we describe the procedure for using the Probing Settings wizard.

1. Select [Analyzer] from the [View] menu in the CSIDE main window. The Analyzer window will be displayed.



Right click anywhere in the Analyzer window and select **[Analyzer Settings]** from the pop-up menu. The Analyzer Settings window will be displayed.



Select the [Set trigger and signal] tab. The dialog box show here will be displayed. Click [Add] .



2. Click [Probing function] to enable the probing function. Next click [Analyzer Pin Settings].

| Set Signal | × | | | | | | |
|---------------------------------------|-----------------------|--|--|--|--|--|--|
| Signal | Registration | | | | | | |
| Channel | Color Close | | | | | | |
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | |
| Probing function << | | | | | | | |
| Chain number 1 | Analyzer pin settings | | | | | | |
| Node name | | | | | | | |
| Channel: [BusSize = 0 / ?] | | | | | | | |
| Channel Chain number Pin num Node | _ | | | | | | |
| 0 | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| 6 | _ | | | | | | |
| | | | | | | | |
| | | | | | | | |

3. <u>The Probing Settings wizard will be displayed. Register the FPGA pins according to the wizard procedure.</u>



4. Register the FPGA pin numbers in each channel. Select the channel for registration and click [Edit].

| 191.16/19/1 | Channel | Chain number | Pin number | Edit |
|-----------------------|--------------------------------|----------------------------------|--------------------|-------------|
| Probing k | 1 | | | Delete |
| Chain number 1 | 3 | | | Delete all |
| Node name Jok | 5 | | | |
| hannet (Bussize = 0 / | 8 | | | |
| harnel Chain rambe | 10 | | | |
| , | 12 | | | |
| 1 | 14 | | | Save macro |
| , L | 1.1 | | | |
| 1 (1 | | | | |
| 1 413 | After editing wizard, click | the appropriate ite [Cancel]. | em, click [Next>]. | To exit the |
| | | | | |
| | | | | - · · |

Note

[Save Macro] button This button saves the current settings in a macro file.

5. The Modify Analyzer Pin dialog box will be displayed. Set the pin number and click [OK].

| Analyzer Pin Edit 🔀 | | | | | | | |
|---------------------|------------------|------------------------------------|--|--|--|--|--|
| CH0 | Adv | anced settings | | | | | |
| 1 - | | | | | | | |
| A3 | | • | | | | | |
| | OK | Cancel | | | | | |
| | Edit CH0 1 | Edit CH0 Adv 1 X A3 OK | | | | | |

6. After registering the pins, click [Next].

| Tel cel rel 1 | Channel | Chain number | Pin number | ▲ Edit |
|---------------|---------------|---------------------|-----------------|------------------|
| | 0 | 1 | M15 | |
| Prohing 1 | 1 | 1 | M16 | Delete |
| r roung k | 2 | 1 | M13 | |
| - | 3 | 1 | L14 | Delete all |
| er /1 | 5 | 1 | 116 | |
| | 6 | 1 | 113 | |
| Jak_ | 7 | i | K14 | |
| WC | 8 | 1 | K15 | |
| 10366=01 | 9 | 1 | K16 | |
| Chain er al | 10 | 1 | L12 | |
| T ANDE | 11 | 1 | K12 | |
| | 12 | 1 | K13 | |
| | 13 | 1 | J14 115 | = |
| | 14 | 1 | 010 | Save macr |
| 1. | | | <u>r</u> | |
| 1 | | | | |
| 41 | | | | |
| LTI | | | | |
| /15 | After editing | the appropriate its | em, click [Next | :>]. To exit the |
| 4/3 | wizard, Click | (cancel). | | |
| | | | | |
| | | | | |
| | | | | |
| | | < Back | Nevt | Cance |

Note

[Advanced Settings] button

Sets the pin electrical characteristics. See the online manual for details.

7. Verify the set values and click [Finish].

| Channel | Chain number | Pin number | _ |
|-----------------|---|----------------------|----------|
| СНО | 1 | M15 | |
| ICH1 | 1 | M16 | |
| ICH2 | 1 | 114 | |
| CH4 | i | L15 | |
| CH5 | 1 | L16 | |
| ICH6 | 1 | L13 | |
| ICH7 | 1 | K14 K15 | |
| CH9 | i | K16 | |
| CH10 | 1 | L12 | |
| | | | Ē |
| | | | - |
| | | | |
| This is the end | of itoms to be act up. Cli | ok (Einish) if the r | ottine |
| made are corre | ct. If not. click [<back] o<="" td=""><td>or [Cancel] to set</td><td>up ite</td></back]> | or [Cancel] to set | up ite |
| n a nin | | | |

Y

8. This completes linking the channels to the FPGA pins.

| or orginal | | | | | | | | | |
|---------------------|--|-----------|------|-------|-----------------------|--|--|--|--|
| Signal Channel | | | 7 | Color | Registration Close | | | | |
| 15 14 1 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | |
| Probing function << | | | | | | | | | |
| Chain numb | Chain number 1 💌 Analyzer pin settings | | | | | | | | |
| Node name | | | | | • | | | | |
| Channel: | BusSize = 0 / ? | 1 | | | | | | | |
| Channel | Chain numbe | r Pin num | Node | | | | | | |
| | 1 | M15 | | | | | | | |
| □ 1 · · · | 1 | M16 | | | | | | | |
| 2 | 1 | M13 | | | | | | | |
| 3 | 1 | L14 | | | | | | | |
| 4 | 1 | L15 | | | | | | | |
| 5 | 1 | L16 | | | | | | | |
| 6 | 1 | L13 | | | | | | | |
| 7 | 1 | K14 | | | | | | | |
| | | | | | | | | | |
| C Autom | atic channel allo | cation | | | | | | | |

Once the channels and FPGA pins have been linked, next, register the bus signals count_dt[7:0] in channels 0 to 7. This section describes this operation from the standpoint of the Analyzer Settings dialog box. To register the signals using the Editor window and the Node Location window, proceed to step 4 immediately.

1. Right click anywhere in the Analyzer window and select **[Analyzer Settings]** from the pop-up menu. The Analyzer Settings dialog box will be displayed. Select the **[Set trigger and signal]** tab. Then click **[Add]**.

| Analyzer Function Set Trigger and Signal Register signal Signal name 157 Add Remove Ar Remove Ar Set capture condition Capture condition Capture condition Signal name Condition Signal name Condition Set/Change Citer ArI Trigger position Trigger position Capture Condition Set/Change Citer ArI Capture Condition Capture Condition Set/Change Citer ArI Capture Condition Capture Condit | et the analyzer. 🗙 |
|---|--|
| Register signal Signal name 15 Add Freet. Berrove Remove Berrove Remove Berrove Berrov | Analyzer Function Set Trigger and Signal |
| Signal name 157 Add | - Register signal |
| Signal name 15 Add Pressure Pressure Premove All Premove All Set capture condition Capture condition Capture condition Signal name Condition Set Capture condition | |
| Set capture condition Capture condition Capture condition Capture condition Signal name Condition Signal name Condition Capture Condition Signal name Condition Capture Condition Capture Capture Condition Capture Capture Condition Capture Capture Condition Capture Capture Condition Capture Capture Captur | Signal name 157 |
| Set capture condition Capture condition Capture condition Signal name Condition Co | |
| Set capture condition Capture condition Capture condition Trigger condition Signal name Condition Care Alt Trigger position Care Alt Trigger position Care Alt Care A | insert |
| Set capture condition Capture condition Trigger condition Signal name Condition Set/Chienge City Trigger position Image: Condition OK Cancel | Remove |
| Set capture condition Capture condition Trigger condition Signal name Condition Set/Change Capture Condition Capture Condition Capture Condition Capture Condition Capture | Remove All |
| Set capture condition Capture condition Trigger condition Signal name Condition Set/Charge Clear All Trigger position Capture Condition Capture Condition | |
| Capture condition Capture | |
| Lapute condition | Set capture condition |
| Trigger condition Signal name Condition Set/Change Gere Alt Trigger position OK Cancel Apply | Lapture condition |
| September Londion September GearAll Trigger position Londion Lon | Trigger condition |
| | Signal hame Condition Set Unange |
| | CleanAll |
| OK Cancel Apply | Trigger position |
| OK Cancel Apply | <u><u><u> </u></u></u> |
| OK Cancel Apply | |
| | OK Cancel Apply |

2. The Signal Settings dialog box will be displayed. Click [Probing function] to enable the probing function.

| Set Signal | | | | | × | | | |
|-------------------------------|--------------------|---------|-------|-----------|--|--|--|--|
| Signal Channel 15 14 13 | 3 12 11 10 | 3 8 | 7 6 5 | Color 4 3 | Registration Close 2 1 | | | |
| Probing function << | | | | | | | | |
| Chain numbe | я <mark>1 💌</mark> | | _ | Analyz | er pin settings | | | |
| Node name | Node name | | | | | | | |
| Channel: [E | BusSize = 0 / ?] | | | | | | | |
| Channel | Chain number | Pin num | Node | | | | | |
| | 1 | M15 | | | | | | |
| | 1 | M16 | | | | | | |
| 🗆 2 | 1 | M13 | | | | | | |
| 3 | 1 | L14 | | | | | | |
| 4 | 1 | L15 | | | | | | |
| 5 | 1 | L16 | | | | | | |
| 6 | 1 | L13 | | | | | | |
| 7 | 1 | K14 | | | | | | |
| 1 | | | | | • | | | |
| 🗖 Automa | tic channel alloca | ation | | | | | | |

3. Select the signal name to register from the [Node name] list. Select count_dt[7:0].



4. Select the channels to allocate. Check channels 0 to 7. Click [Registration] after the channels have been selected.



If **[Automatic Channel Allocation]** is checked, CSIDE will select the channels to use from the unused channels and allocate them automatically.



5. The Signal Settings dialog box will be displayed for the next signal registrations. Since we will not be registering them using this dialog box, click **[Close]** to close this dialog box.



6. The count_dt[7:0] signals are registered for channels 0 to 7. Set the trigger and other conditions and click **[OK]**.



7. A dialog box that verifies whether or not you want to have all the signal settings reflected in the window will open. Click **[Yes]**.

| ⚠ | Do you w | ant to reflect all the | set contents of l | the signal to the window? |
|---|--------------|------------------------|-------------------|---------------------------|
| | If reflectin | ig them, all bus exp | ansion and order | sorting are initialized. |
| | If not refle | acting them, add or i | remove the signa | al on the window. |
| | | Yes | No |] |

8. Start the FPGA editor and click **[Yes]** in the dialog box that opens to confirm whether or not you want to perform a configuration operation.



9. The FPGA editor runs and performs a configuration operation.



When the configuration completes normally, "Configuration of FPGA completed normally" will be displayed in the status bar.



10. The count_dt[7:0] signals will have been added.



3.3 Modifying the Monitored Signals

This section describes the procedure for modifying the count_dt[7:0] signals registered in section 3.2 Registering the Monitored Signals

1. Right click anywhere in the Analyzer window and select [Analyzer Settings] from the pop-up menu. The Analyzer Settings dialog box will be displayed. Select the **[Set Trigger and Signal]** tab. Select count_dt[7:0] as the signal name to be modified and click **[Change]**.

| Set the analyzer. 🔀 |
|--|
| Analyzer Function Set Trigger and Signal |
| Besiden intered |
| negistei signal |
| Signal name 157 |
| count_dt[7:8] **** + Change |
| |
| Remove |
| Remove All |
| |
| |
| Set capture condition |
| Capture condition One shot |
| Trigger condition |
| Signal name Condition Set/Change |
| count_dt[7:0] ?? |
| |
| Trigger position |
| |
| |
| OK Cancel Apply |

2. The Signal Settings dialog box will be displayed showing the current registration state.

| ecolynai | | | | ^ |
|-------------|-------------------|---------|-------------|-----------------------|
| Signal | count_dt[7:0] | | 7 | 0K |
| Channel | | | | Color Cancel |
| 15 14 13 | 8 12 11 10 | 9 8 | 765 | 4 3 2 1 0 |
| Pr | obing function << | | | |
| Chain numbe | er 1 💌 | | | Analyzer pin settings |
| Node name | count_dt[| /:0] | | • |
| Channet (B | BusSize = 8 / 8] | | | |
| Channel | Chain number | Pin num | Node | <u>^</u> |
| № 0 | 1 | M15 | count_dt[0] | |
| ⊻ 1 | 1 | M16 | count_dt[1] | |
| ≥ 2 | 1 | M13 | count_dt[2] | |
| ⊻ 3 | 1 | L14 | count_dt[3] | |
| ₩ 4 | 1 | L15 | count_dt[4] | |
| ⊻ 5 | 1 | L16 | count_dt[5] | |
| № 6 | 1 | L13 | count_dt[6] | _ |
| ⊻ 7 | 1 | K14 | count_dt[7] | |
| | | | | |
| C Automa | tic channel alloc | ation | | |

3. Select the signals to be modified from the **[Node name]** list. Select "ce". The unnecessary channels will be cleared.



To allocate the ce signal to another channel, check the channel to which it is to be allocated.

| et Signal | | | | | × |
|------------|--------------------|---------|------|-------|------------------|
| Signal | count_dt[7:0] | | Ŧ | | OK |
| Channel | | | | Color | Cancel |
| 15 14 1 | 3 12 11 10 | 9 8 | 7 6 | 5 4 | 3 2 1 0 |
| P | robing function << | | | | |
| Chain numb | er 1 💌 | | | Analy | zer pin settings |
| Node name | CB | | | | • |
| Channel [| BusSize = 1 / 1] | | | | |
| Channel | Chain number | Pin num | Node | | |
| | 1 | M15 | | | |
| 01 | 1 | M16 | | | |
| 2 | 1 | M13 | | | |
| ✓ 3 | 1 | L14 | ce | | |
| 4 | 1 | L15 | | | |
| 5 | 1 | L16 | | | |
| 6 | 1 | L13 | | | |
| 0.7 | 1 | K14 | | | - |
| 4 | | | | | • |
| - | | | | | |

4. When the signal modifications have been made, click **[OK]**.

| et signal | | | | X | | | | | |
|------------|---------------------------------------|---------|------|-----------------------|--|--|--|--|--|
| Signal | count_dt[7:0] | | 7 | ОК | | | | | |
| Channel | | | _ | Color | | | | | |
| 15 14 1: | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | |
| Pr | obing function << | : | | | | | | | |
| Chain numb | er 1 💌 | | | Analyzer pin settings | | | | | |
| Node name | Ce | _ | _ | • | | | | | |
| Channet [I | BusSize = 1 / 1] | | | | | | | | |
| Channel | Chain number | Pin num | Node | ^ | | | | | |
| ✓ 0 | 1 | M15 | ce | | | | | | |
| 1 | 1 | M16 | | | | | | | |
| 2 | 1 | M13 | | | | | | | |
| 3 | 1 | L14 | | | | | | | |
| 4 | 1 | L15 | | | | | | | |
| 5 | 1 | L16 | | | | | | | |
| 6 | 1 | L13 | | _ | | | | | |
| 7 | 1 | K14 | | | | | | | |
| | | | | | | | | | |
| C Automa | atic channel alloc | ation | | | | | | | |

5. This modifies the ce signal. Set the trigger and other conditions and click [OK].

| Set the analyzer. | ×. |
|--------------------------|----------------------------------|
| Analyzer Function Set T | rigger and Signal |
| - Register signal | |
| Signal name 1 ce - | 578 Ad |
| | inse |
| | Remove All |
| • | |
| - Set capture condition- | |
| Capture condition | ne shot 💌 |
| Trigger condition | |
| Signal name ce | Condition Set/Change ? Citer All |
| | Trigger position |
| | OK Cancel Apply |

6. A dialog box that verifies whether or not you want to have all the signal settings reflected in the window will open. Click **[Yes]**.



7. Start the FPGA editor and click **[Yes]** in the dialog box that opens to confirm whether or not you want to perform a configuration operation.



8. The FPGA editor runs and performs a configuration operation.



When the configuration completes normally, "Configuration of FPGA completed normally" will be displayed in the status bar.

| Analyzer | 25hJTAG Clock |
|-----------------------|-----------------------|
| Configuration of FPGA | 1 completed normally. |



The CSIDE ISE linkage function is used to register and modify signals that have no placement information. This function can perform the sequence of operations consisting of (1) modifying the source in CSIDE, (2) synthesis, and (3) configuration. The actual synthesis operation is performed by the Xilinx FPGA development tool ISE.

(Read the **"Synthesis**" and **"Synthesis following Place and Route**" in the online manual in conjunction with this section.) This section uses the example used in Chapter3 Trying the Probing Function.



The following describes the procedure for registering the bus signal count_dt[0..7].

1. For the signals that were registered (added), define pins in the UCF file so that the allocated pins are routed as analyzer pins during synthesis.

Select **[Source]** in the **[FPGA]** menu. The FPGA source window will be displayed. Open the sample.ucf file and define the FPGA pins.



2. Define the FPGA pins. Although any names can be used for the added pins, we will use CH_CTEX(0) to (7) in this section.

| E ditor - | - [2] c:\p | robing\sample.ucl * | | | | - 🗆 × |
|-----------|------------|---------------------|-------|------------|----|-------|
| | L., | | 20 | 30 | 40 | |
| | 8 NET | "OUT DT<3>" | LOC = | "H2": 🎝 | | |
| | 9 NET | "OUT_DT<4>" | L0C = | "H1" 💭 | | |
| | 18 NET | "OUT_DT<5>" | LOC = | "J4" 🛃 | | |
| | 11 NET | "OUT_DT<6>" | LOC = | ''J2''; 🎝 | | |
| | 12 NET | "OUT_DT<7>" | L0C = | ''J3'' 🚽 | | |
| | 13 🚽 | - | | | | |
| | 14 NET | "CE" | LOC = | ''L3'' ; 🎝 | | 100 |
| | 15 NET | "RESET" | L0C = | "M2" 🚽 | | |
| | 16 🚽 | | | | | |
| | 17 NET | "CK" | L0C = | ''B8''; 🚽 | | |
| | | | | | | 100 |
| | 19 NET | "CH CTEX<0>" | L0C = | ''M15''; 🚽 | | 100 |
| | 20 NET | "CH_CTEX<1>" | L0C = | ''M16'' 🛃 | | |
| | 21 NET | "CH_CTEX<2>" | L0C = | "M13" 🚽 | | |
| | 22 NET | "CH_CTEX<3>" | LOC = | "L14" | | |
| | 23 NET | "CH_CTEX<4>" | L0C = | "L15" 🚽 | | |
| | 24 NET | "CH_CTEX<5>" | L0C = | ''L16''; 🚽 | | 100 |
| | 25 NET | "CH_CTEX<6>" | L0C = | ''L13'' 🚽 | | 10 |
| | 26 NET | "CH_CTEX<7>" | L0C = | 'K14' 🎝 | | 100 |
| | 27 🚽 | - | | | | |
| | | LOON LINE | | | | |
| | 29 [E0 | F1 - | | | | |
| | | | | | | - |
| 4 | | | | | | |

Note

The FPGA pins defined here are pins that are actually connected to the user system.

After defining the FPGA pins, select [Save] - [File] from the File menu to save the ucf file.

3. Select the sample.vhd file in the FPGA Source Management window, and open the file. Edit the file as necessary.



4. After the sample.vhd file has been edited as required, execute **[Synthesize]** from the FPGA menu. The message shown here will be displayed. If this is acceptable, click **[Yes]**.

| CSIDE for I | Palmice FPGA-e | | | | × |
|-------------|---|--|-------------------------------------|---|------------------------------|
| | Perform a configuration op All the HDL files being ed OK? | eration after star ited will be saved | ting the synthe d. Also, certain | sis tools and synthesi intermediate files will l | zing an FPGA. be deleted. |
| | | Yes | No | | |

5. ISE will run, and after synthesis, a configuration operation will be performed.



When the configuration completes normally, "Configuration of FPGA completed normally" will be displayed in the status bar.



6. Register the signals in the Analyzer window.

Select [Analyzer] in the [View] menu. The Analyzer window will open.

Either double click or right click anywhere in the Analyzer window and select [Analyzer Settings] from the pop-up menu. The Analyzer Settings dialog box will be displayed. Select the **[Set Trigger and Signal]** tab. Click **[Add]**.

| at the analyzer. | × |
|--|---------------------|
| Analyzer Function Set Trigger and Signal | 1 |
| Register signal | |
| Signal name 15 7 | Add |
| • | |
| | Insert |
| | Hemove Remove AT |
| | FIGHEVE AL |
| 1 | |
| Set capture condition | _ |
| Capture condition One shot | · |
| Trigger condition | |
| Signal name Condition | Set/Change |
| | Clear All |
| | rigger position |
| | <u></u> |
| | |
| | |

7. The Signal Settings dialog box will be displayed. Disable the probing function.

| Registration |
|--------------|
| Close |
| 3 2 1 0 |
| |
| |
| |

8. Enter count_dt as the [Signal] and click channels 0 to 7. Next, click [Registration].

| Set Signal | | × |
|----------------------------------|-------|--------------|
| Signal cunt_dt | | Registration |
| Crignito | Color | Close |
| <u>15 14 13 12 11 10 9</u> 8 7 6 | 5 4 | 3 2 1 0 |
| Probing function >> | | |

9. The Signal Settings dialog box will be displayed for the next signal registration. Since there are no signals to register at this point, click **[Close]** to close this dialog box.



10. The count_dt[7:0] signals are now registered for channels 0 to 7. Set the trigger and other conditions and click [OK].



11. A dialog box that verifies whether or not you want to have all the signal settings reflected in the window will open. Click **[Yes]**.



12. The count_dt[7:0] signals have now been added.

| Sampling 5n5/Div C Env On Active mark Delay 5n5 I I Env On Env On mm Signal name State Image: Stat | Analyze | a winuu | w - [1] | | | | | | |
|---|-------------------|---------|--|------------|----------------------|-------------|--------|-----|--|
| Signal name State | Sampling Delay | 5nSz | ′Div <u>@</u> (5nS | | En 💌 🛛 Or En 💌 Or | Active mark | On Jmp | RUN | |
| cunt_att[7:0] 00 Image: start of the start o | Signal nar | me | State | | | | | | |
| Frame St., count Time stamp | cunt_dt[| [7:0] | 99 | | | | | | |
| | Frame | St 6 | count | Time stamp | | | | | |
| | 1 | | | | | | | | |



Computex Co., ltd. Head office

432-13, 4-chome, Gojyoubashi-higashi, Higashiyama-ku, Kyoto, 605-0846 TEL.075(551)0528 FAX.075(551)2585

Sales department 7F, DNK-building, 15-2, 2-chome, Uchikanda, Chiyoda-ku, Tokyo, 101-0047 TEL.03(3253)2901 FAX.03(3253)2902

PALMICE FPGA Probing Function User's Manual CM654(B)0411