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Interconnectivity

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ISP1122 USB Hub Demonstration Board

User's Manual

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ISP1122 USB Hub Demonstration Board - User's Manual

Table of Contents

ISP1122 USB Hub Demonstration Board - User's Manual

PREFACE

The Philips Semiconductors Hub ISP1122 is a state of the art, 3rd generation, stand-alone USB hub controller IC that complies with the latest USB Spec Rev 1.1. The major considerations for this board are:

1. Interoperability
2. Reduction in the overall system cost
3. Ease of use

We have relied on more than three years of our USB design and customer support experience to achieve these objectives. Today our USB products already provide an industry benchmark for the interoperability tests. Since interoperability problems result in the most expensive failures in the field, we have further tightened the design specifications to address many ambiguities. The IC has integrated many functions and offers features that reduce the major components of the total system cost. We have employed many design techniques to reduce the EMI emissions, increase the ESD resiliency and improve the manufacturing test criteria to insure a high quality product.

Our ultimate aim is to provide you with peace of mind when using our products in the total system solution. We welcome your comments and suggestions to help us improve. For more information about the ISP1122 and the latest updates to the design support document, please visit the web site http://www.flexiusb.com/

With Best Regards,

Team Members of the Asia Product Innovation Center

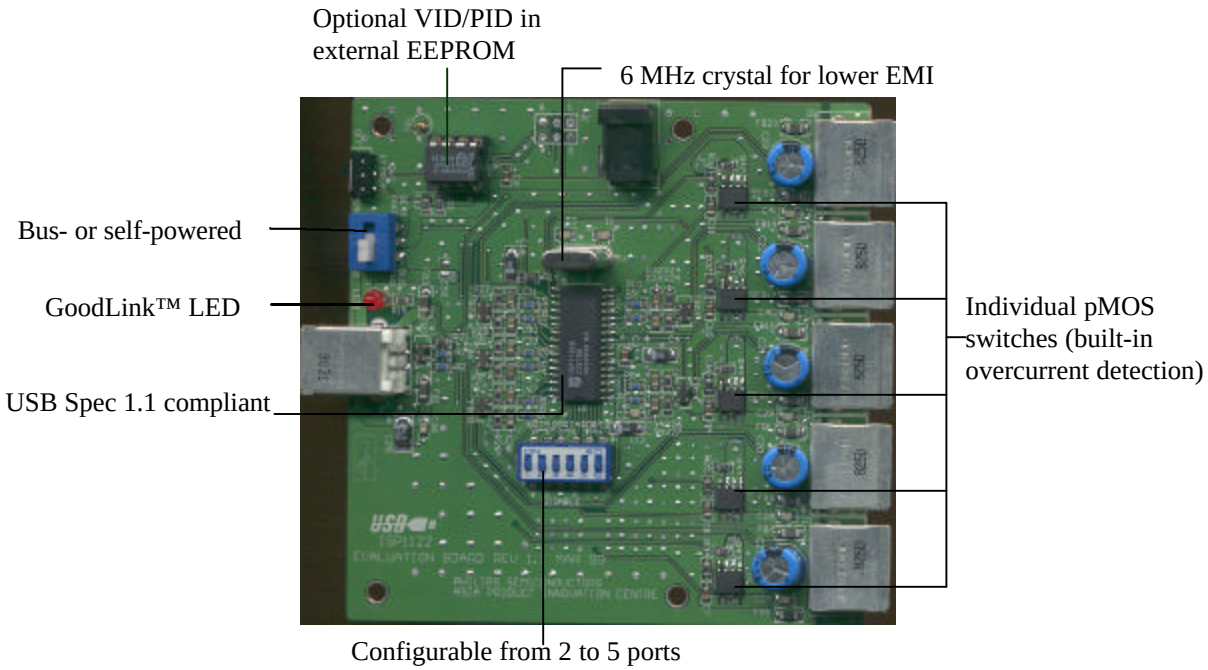
ISP1122 USB Hub Demonstration Board - User's Manual

1 INTRODUCTION

The ISP1122 demonstration board (henceforth referred to as *demo board*) is designed for evaluating the features and functionality of the ISP1122 integrated circuit (IC). This manual explains the schematic of the ISP1122 demo board, demonstrates the PCB layout, shows the Bill of Material (BOM) and describes the switches on the board.

1.1 Demo Board Features

- USB Spec Rev 1.1 compliant
- Selectable bus or self/hybrid-powered operation
- Configurable number of downstream ports from 2 to 5
- Customizable Vendor ID and Product ID through EEPROM
- Individual power switching and individual overcurrent protection
- Hub health indicator through GoodLink™ LED
- Verified interoperability with many systems and peripherals
  (Check the continuously updated Interoperability report on the web site)
- FCC Part 15 , Subpart J, Class B compliant
- 8 kV in-circuit ESD protection



ISP1122 USB Hub Demonstration Board - User's Manual

2 BOARD DESCRIPTION

2.1 Configuration Modes

The INDV, OPTION and SP/BP_N pins determine the hub configuration modes. Users can set these signals to logic high or low. The INDV and OPTION pins can also be used for connections to external EEPROM. This allows for customized Vendor ID and Product ID among other configuration modes. The contents of the EEPROM will be described later.
The three configuration pins are described in Table 1.

Table 1 Mode Configuration Pins

Name	Value	Description	Other Usage
INDV	0	Gang power switching and global overcurrent protection mode	SCL
	1*	Individual power switching and individual overcurrent protection mode	
OPTION	0	Both power switch and overcurrent protection functions are active	SDA
	1*	Only one function is active: in self-powered mode, the power switch control is inactive; in bus-powered operation, the overcurrent protection is inactive	
SP/BP_N	0	Bus-powered mode	
	1	Self-powered or hybrid powered mode	Local Power Lost Indication

1 signifies a pull-up high.*

Note: The ISP1122 also supports hybrid self-powered mode. In this mode, the hub controller draws power from upstream Vbus and local power is used for downstream ports. Hybrid powered mode is advantageous to differentiate between a disconnected and an unpowered device. This makes it possible to keep communicating between the host and the device/hub even if local power is lost.

Each composite setting of the three pins determines one configuration mode of the hub. Therefore, ISP1122 can be configured into eight modes. Table 2 shows these configuration modes. For a detailed description of these power management modes, refer to the "ISP1122 Power Management Design Guide" document.

Table 2a Mode Selection Table

Mode	INDV	OPTION	SP/BP_N	PSW1,2,3,4_N	PSW5_N	OC1,2,3,4_N	OC5_N
0	0	0	0	GL1,2,3,4_N	GPSW_N	Inactive	GOC_N
1	0	0	1	GL1,2,3,4_N	GPSW_N	Inactive	GOC_N
2	0	1	0	GL1,2,3,4_N	GPSW_N	Inactive	Inactive
3	0	1	1	GL1,2,3,4_N	GL5_N	Inactive	GOC_N
4	1	0	0	PSW1,2,3,4_N	Inactive	OC1,2,3,4_N	Inactive
5	1	0	1	PSW1,2,3,4_N	PSW5_N	OC1,2,3,4_N	OC5_N
6	1	1	0	PSW1,2,3,4_N	Inactive	Inactive	Inactive
7	1	1	1	GL1,2,3,4_N	GL5_N	OC1,2,3,4_N	OC5_N

Inactive OCX_N pins must be tied to Vcc.

ISP1122 USB Hub Demonstration Board - User's Manual

Table 2b Mode Selection Table (Continued)

Mode	Self-/Bus-Powered	Power Switch control	GoodLink	Overcurrent Protection	Remarks
0	Bus-powered	Ganged	Yes*	Global	Ganged and bus powered
1	Self-powered	Ganged	Yes*	Global	Ganged and self powered
2	Bus-powered	Ganged	Yes*	Inactive	No overcurrent
3	Self-powered	Inactive	Yes	Global	No power switch control
4	Bus-powered	Individual*	No	Individual*	Individual and bus powered
5	Self-powered	Individual	No	Individual	Individual and self powered
6	Bus-powered	Individual*	No	Inactive	No overcurrent
7	Self-powered	Inactive	Yes	Individual	No Power switch control

** Without Port 5*

The demo board implements modes 4 and 5 using switch SW1 (see Table 3). In these two modes, the hub supports individual power control and individual overcurrent protection for downstream ports.

Table 3 Bus/Self-Powered Selection Switch

SW1	Selection
1-3	Bus powered
1-2	Self/Hybrid powered

WARNING:
When supplying power through the DC jack, make sure that SW1 is at position 1-2 indicating a self-powered mode. If SW1 is at position 1-3 (bus-powered mode), the upstream supply and the local supply will be shorted!

2.2 EEPROM Support

INDV and OPTION pins can also be connected to an external serial EEPROM for Vendor ID, Product ID customization and configuration setting. The interfacing protocol is I^2C. The ISP1122 acts as the master and the EEPROM as the slave. The I^2C clock frequency generated by the ISP1122 is slightly less than 100 kbits/s to support low end EEPROM. The following EEPROM models have been proven suitable: PCA8581, PCF8582C-2, 24C00, 24C01. Both the SCL (OPTION) and SDA (INDV) pins must be pulled up to Vcc; a 3.3 kilo-ohm value is recommended.

On power on, ISP1122 detects the presence of the EEPROM through the Signature byte (=AAh). If the signature is correct, the content of the EEPROM will overwrite the default setting. Table 4 lists the EEPROM's contents and Table 5 describes the configuration bits.

ISP1122 USB Hub Demonstration Board - User's Manual

Table 4 EEPROM Content

Address	Content							
0	*idVendor* lower byte (default = CCh)							
1	*idVendor* higher byte (default = 04h)							
2	*idProduct* lower byte (default = 22h)							
3	*idProduct* higher byte (default = 11h)							
4	C7	C6	C5	C4	C3	C2	C1	C0
5	Signature = AAh							

Table 5 Configuration Bits

Bit	Name	Value	Meaning
C0	OPTION		Refer to mode selection table
C1	INDV		Refer to mode selection table
C2	RESERVED	0*	Should always be programmed to '0'
C3	PwrOn2PwrGood	0* 1	Modifies the Hub Descriptor Field *PwrOn2PwrGood* 100 ms (32h) 500 ms (FAh)
C4	String Descriptor Enable	0* 1	Disable String Descriptor Enable String Descriptor (String is "Philips Semiconductors" and "ISP1122")
C5	Internal Analog Overcurrent Detection Enable	0 1*	Disable internal analog overcurrent detection circuit. When disabled, the overcurrent pins OCX_N convert to digital (TTL) level. Enable internal analog overcurrent detection circuit
C7:6	MaxPower	00* 01 1X	Modifies the Configuration Descriptor Field *MaxPower* 100 mA (32h) 500 mA (FAh) 0 mA (00h)

*Note: * denotes the internal default value when the EEPROM is not present.*

Although the C0 (OPTION) and C1 (INDV) bits can be programmed to any value, the demo board hardware only supports Modes 4 and 5. That means these two bits must be programmed with

C0 (OPTION) = 0
C1 (INDV) = 1

for this demo board to work.

The EEPROM can be disabled through switch SW2 as shown in Table 6. When the EEPROM is not present, switch SW2 has to be set to "EEPROM disabled" state to correctly configure the board in the right mode of operation (Modes 4 or 5).

Table 6 EEPROM Enable/Disable Switch

SW2	EEPROM
1-3	EEPROM enabled
1-2	EEPROM disabled

ISP1122 USB Hub Demonstration Board - User's Manual

2.3 Number of Downstream Ports

The number of downstream ports for ISP1122 is configurable from 2 to 5. For bus-powered mode, the USB spec only allows for 4 downstream ports. Table 7 lists the port number configuration, which is set through switch SW3.

Table 7 Number of Downstream Ports Setting (SW3)

1-12 2-11	3-10 4-9	5-8 6-7	Number of Downstream Ports
OFF	OFF	OFF	5
ON	OFF	OFF	4
ON	ON	OFF	3
ON	ON	ON	2
Other combinations			Illegal

Note: Bus-powered mode can only have 4 downstream ports according to the USB spec.

2.4 Factory Default Setting

The factory default setting of the configuration switches are shown in Table 8.

Table 8 Factory Default Setting

Switch	Selection	Default
SW1	Self/Bus-powered	Bus-powered
SW2	EEPROM	No EEPROM (disabled)
SW3	Number of Downstream Ports	4

2.5 PCB Layout Considerations

The following PCB layout considerations are employed:

1. Route signal traces on the top layer as much as possible. The bottom layer is reserved for ground routing. This should minimize EMI issues.
2. Power traces must be thick to meet USB spec voltage drop requirement.
3. Put 150 µF capacitors as close as possible to the downstream ports. These capacitors, together with ferrite beads, minimize voltage droop upon downstream ports hot insertion.
4. Route each pair of the D+ and D- lines close and parallel to each other and their length should be equalized. This will ensure good symmetrical differential signal swing that enhances interoperability and also lower EMI.
5. Crystal oscillator should be placed close to ISP1122.
6. Decoupling capacitors for the ISP1122 Vcc and $V_{3.3}$ signals should be placed close to the pins.

ISP1122 USB Hub Demonstration Board - User's Manual

3 Appendix

For schematic diagram and PCB layout, refer to their respective .SCH and .PCB files.

3.1 ISP1122 Pin Diagram

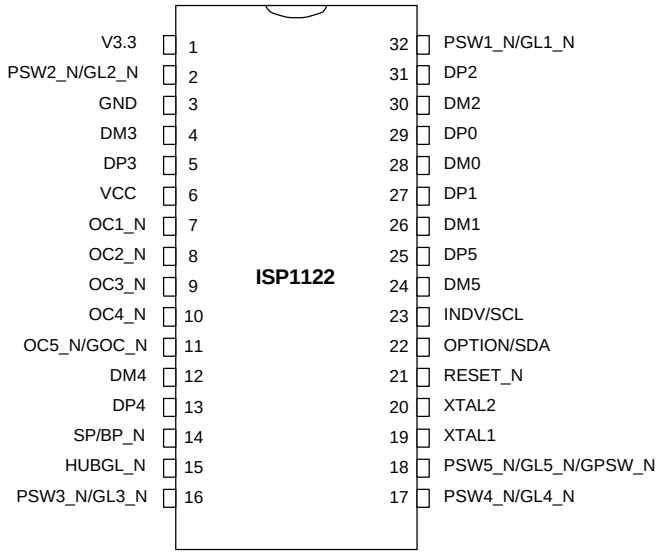


Figure 1 Pin Diagram of ISP1122

ISP1122 USB Hub Demonstration Board - User's Manual

3.2 Bill of Material (BOM)

Part #	Part Type	Designator	Qty
1	0.01µF ceramic capacitors	C26,C27,C28,C29,C40,C41	6
2	0.1µF ceramic capacitor	C3, C6, C7,C8,C9,C10,C11	7
3	1µF TANT capacitors	C4, C13,C16	3
4	4.7µF TANT capacitor	C25	1
5	150µF Electrolytic capacitor	C20, C21, C22, C23, C24	5
6	22pF ceramic capacitor	C1, C2	2
7	47pF ceramic capacitor	C30, C31, C32, C33, C34, C35, C36, C37, C38, C39	10
8	100 kilo-ohm 0805	R43, R44, R45, R46, R47	5
9	1.5 kilo-ohm 5% 0805	R21	1
10	10 kilo-ohm 5% 0805	R14	1
11	15 kilo-ohm 5% 0805	R22, R23, R24, R25, R26, R27, R28, R29,R30	10
12	18 ohm 1% 0805	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12	12
13	3.3 kilo-ohm 0805	R32, R33	2
14	330 ohm 0805	R15	1
15	47 kilo-ohm 0805	R34, R35, R36, R37, R38	5
16	Ferrite beads – Murata BLM31P221SG	FB1, FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17, FB19, FB21, FB23	12
17	Common mode choke filter- Murata PLP3216S551SL2	FB2, FB6, FB10, FB14, FB18	5
18	6 MHz Crystal oscillator	X1	1
19	5V/2.5A DC jack	P1	1
20	USB "A" Receptacle (Downstream port connectors)	J1, J2, J3, J4, J5	5
21	USB "B" Receptacle (Upstream port connector)	J0	1
22	ISP1122. Philips Semiconductors USB Hub controller (SO32 package)	U1	1
23	PCA8581C/PCF8582C-2/24C00/24C01. EEPROM with I^2C interface	U2	1
24	PHP109. PMOS power transistor	Q1, Q2, Q3, Q4, Q5	5
25	LED	LED1	1
26	Switch DIP-6	SW3	1
27	Switch SPDT	SW2	1
28	Switch DPDT	SW1	1
29	TEST POINT	TP1	1

ISP1122 USB Hub Demonstration Board - User's Manual

3.3 Component Placement

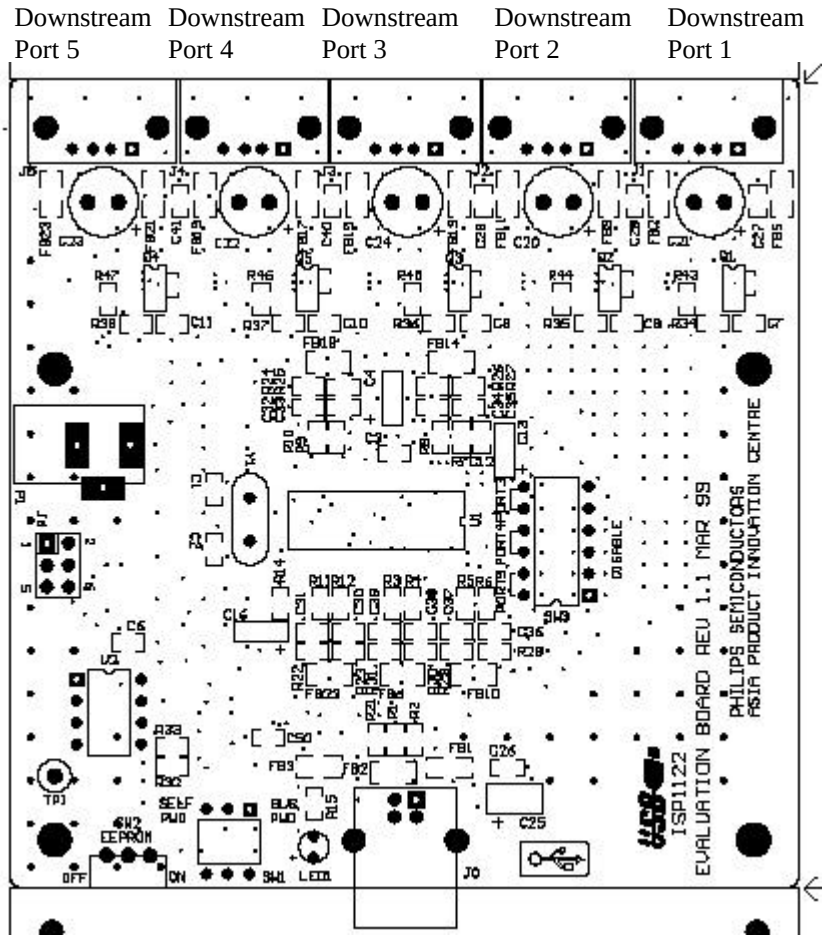


Figure 2 Component Placement of the ISP1122 Demo Board