Model DSA-2000/A Digital Spectrum Analyzer

User's Manual

9231280L

ISO 9001 SYSTEM CERTIFIED

CE

Canberra Industries, 800 Research Parkway, Meriden, CT 06450
Tel: 203-238-2351 FAX: 203-235-1347 http://www.canberra.com

Printed in the United States of America.

Table of Contents

1. Introduction

This manual is a comprehensive reference, covering the capabilities and operation of the DSA-2000 Digital Signal Analyzer.

1. Introduction

This chapter is an introduction to the manual's contents and an overview of the DSA's features.

2. Controls and Connectors

You'll find a brief description of the front and rear panels' indicators and connectors here.

3. Setup and Configuration

Read this chapter for instructions on unpacking and setting up your system, including how to connect it to an Ethernet.

4. User Interface and Controls

This chapter tells you how to easily configure your system using the MID Wizard, but also covers using the MID Editor for more complex configurations.

5. Using the Monitor Output

The DSA's Monitor Output presents an analog signal representing the sampled digital filtered signal. This chapter discusses how to use it in setting up the DSA-2000 and verifying system gain.

6. Setup and Operation

This is the heart of the manual, covering day-to-day basic spectroscopy operation, pole/zero matching your DSA-2000 to the detector for maximum resolution, and acquiring a spectrum.

7. PUR/LTC Operation

This chapter details how and why you use the DSA-2000's Pulse Pileup Rejector and Live Time Corrector (PUR/LTC) feature, which improves both measurement and analysis.

The Appendices

The appendices offer useful information not usually needed in day-to-day operation.

The DSA-2000 Digital Spectrum Analyzer is a fully integrated, high performance multichannel analyzer. All of the subsystems required for high quality spectrum acquisition are integral to the unit – digital signal processor (DSP), high voltage power supply (HVPS), digital stabilizer, MCA memory and Ethernet network interface. The instrument is suitable for applications involving virtually all gamma, and most X-ray, detector types.

The heart of the DSA-2000 is the Digital Signal Processor subsystem. Unlike conventional systems, which digitize the detector preamplifier signals at the end of the signal processing chain, the DSA-2000 digitizes the detector preamplifier signals at the front end of the signal processing chain. This approach eliminates significant amounts of analog circuitry at the front end of the instrument, resulting in increased stability, accuracy and reproducibility.

The signal processing subsystem in the DSA-2000 also includes automatic Ballistic Deficit Correction (Auto BDC). When an Auto BDC optimization is started, the system monitors the rise time of the incoming detector preamplifier pulses and automatically adjusts the flat top setting to accommodate the detector's collection time, virtually eliminating resolution degradation due to ballistic deficit. The information in Appendix B, *Performance Adjustments*, tells you how to "fine tune" your DSA's rise time and flat top settings.

For applications involving the study of radiation signals that may vary with time, the DSA-2000 provides a Multichannel Scaling (MCS) mode. MCS dwell times may be set from 2 µs to over 2000 seconds at input rates of up to 50 MHZ (TTL) or 500 kHz (Analog). The DSA-2000 allows MCS and Pulse Height Analysis (PHA) modes of operation to be executed simultaneously.

Electronics in the DSA-2000 are 100% computer controlled. The host computer controls the DSA-2000 via the integral Ethernet interface built directly into the unit. Software control is provided via Canberra's flagship Genie-ESP and Genie-2000 spectroscopy software platforms. Additionally, the host Genie software automatically stores a record of all the setup parameters – and the instrument serial number – with each spectrum file. This provides a secure authentication record with each sample, ensuring that the parameters and instrument have not been changed from the prior calibration or QA verification

The ability of the DSA-2000 to be connected directly to an Ethernet network adds considerably to the flexibility in operation and location of system components. A networked DSA-2000 need not be located near the host computer – either for convenience of adjustment or due to any electrical distance restrictions. The unit can be located as close as possible to the detector, minimizing the length of sensitive analog signal cables, without creating operating inconveniences.

In addition, network operation adds to the fault tolerance of larger systems. Multiple computers can be located on the network and the DSA-2000 operated from any computer. Thus, if a computer fails, any surviving computer can continue the operation and no counting capacity in the laboratory is lost.

DSA-2000's which include an "A" suffix in the model number (DSA-2000A) have the automatic pole/zero option installed. For the DSA-2000A the pole/zero adjustment can be performed automatically - the process is initiated by software command. The pole/zero may also be adjusted manually by the software. To verify the model please check the serial number tag located on the rear panel.

For the DSA-2000 without the automatic pole/zero option the pole/zero is adjusted manually from the software.

2. Controls and Connectors

Front Panel

This is a brief description of the DSA-2000's front panel LED indicators and power switch. For more detailed information, refer to Appendix A, Specifications.

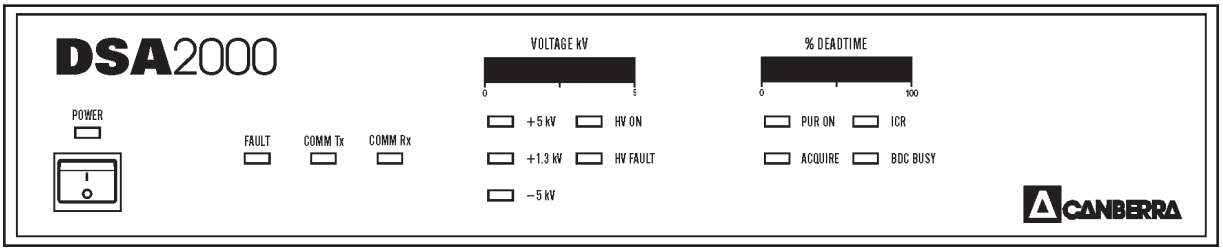


Figure 1 Front Panel Connectors

Power Switch

The DSA-2000's power switch (1/0), located on the lower left side of the front panel, controls power to the instrument. Power is enabled when the switch is in the 1" position and disabled when the switch is in the 0" position. The associated LED glows when the instrument is powered.

The Status Indicators

The DSA-2000's front panel indicators show the status of: power on, Ethernet communication activity with the host computer, detector high voltage power supply, acquisition and the automatic BDC function.

POWER	Green LED, indicates when the instrument is connected to the ac mains and the power switch is on.
FAULT	Yellow LED, indicates a Ethernet communication fault has occurred with the host computer.
COMM Tx	Green LED, indicates Ethernet transmit activity from the DSA-2000.

COMM Rx	Green LED, indicates Ethernet receive activity from the host computer.
VOLTAGE kV	Red 20-segment horizontal LED bar graph, indicates the current voltage setting of the detector high voltage power supply; 0 to 5000 volts full scale, with each segment representing approximately 250 volts.
+5 kV	Green LED, indicates the high voltage power supply polarity and range is set to the positive 5000 volt range.
+1.3 kV	Green LED, indicates the high voltage power supply polarity and range is set to the positive 1300 volt range.
–5 kV	Green LED, indicates the high voltage power supply polarity and range is set to the negative 5000 volt range.
HV ON	Green LED, indicates the detector high voltage power supply in on and high voltage could be present at the rear panel high voltage connector.
HV FAULT	Yellow LED, indicates a high voltage fault condition, such as HV inhibit or high voltage overload.
% DEADTIME	Red 20-segment horizontal LED bar graph, indicates the average system dead time in increments of 5%.
PUR ON	Green LED, indicates the PUR/LTC (Pileup Rejection/Live Time Correction) function is on or enabled.
ACQUIRE	Green LED, indicates when data acquisition is active.
	Green LED, indicates when data acquisition is active.
ICR	Green LED, indicates incoming count rate activity from the associated detector; also serves as a user aid when setting the Fast Discriminator Threshold manually.
BDC BUSY	Green LED, indicates an automatic BDC operation has been initiated and is in process.

Rear Panel

This is a brief description of the DSA-2000's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

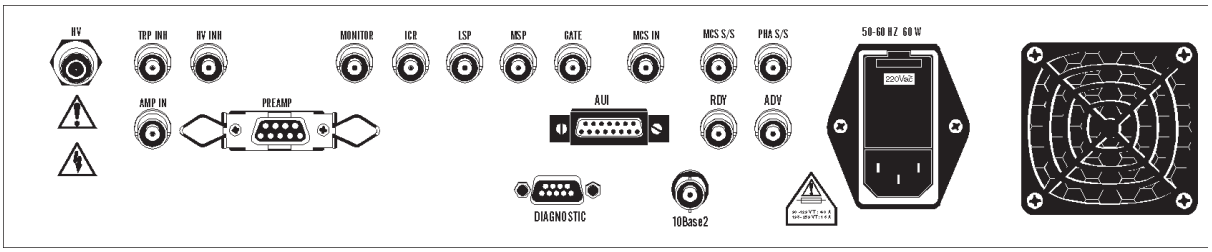


Figure 2 Rear Panel Connectors

Detector/Signal Processing Connectors

HV	High voltage output for detector bias; programmable range and polarity; SHV connector.
TRP INH	Reset preamp inhibit input; BNC connector.
HV INH	Logic low or ground inhibits the HV output.
AMP IN	Detector/Preamplifier signal input, BNC connector.
PREAMP	Provides power to standard detector preamplifier, output, 9 pin female D-connector.
MONITOR	Monitor output, allows examination of sampled data reconstructed in time, serves as a user aid to assist with setup; BNC connector.
ICR	Incoming count rate output, provides a standard TTL logic pulse, frequency corresponds to the input count rate; BNC connector.
GATE	Gate signal input, accepts logic pulse or dc level for coincidence and anti-coincidence gating; BNC connector.

Precision Pulser Connectors

LSP	Reserved for control of future precision pulser.
MSP	Reserved for control of future precision pulser.

MCS/PHA Start/Stop Connectors

MCS IN	MCS count input; BNC connector.
MCS S/S	External MCS start/stop input; BNC connector.
PHA S/S	External PHA start/stop input; BNC connector.

Sample Changer Connectors

RDY	Sample Changer Ready input; BNC connector.
ADV	Sample Changer Advance output; BNC connector.

Ethernet Connectors

AUI	Ethernet AUI output; 15 pin female D-connector.
10Base2	Thin wire Ethernet output; BNC connector.

Note The Ethernet station address for this unit is located near these connectors.

Diagnostic Connector

Bidirectional RS-232 diagnostic port; 9-pin male D-connector.

Power Entry Module

Power entry module with integral IEC 320 connector to accept detachable 3-wire line cord. The module must be configured to match the ac main supply voltage (refer to Appendix C, *Voltage Selection* for instructions).

Internal Controls

The DSA-2000 Digital Spectrum Analyzer is fully programmable by the host computer. There are no internal controls or jumpers that require adjustment or service by the user.

3. Setup and Configuration

This chapter serves as a guide to unpacking and connecting the system. Software installation is covered in Appendix , *Software Installation*, of the Genie-2000 Operations Manual.

Unpacking the DSA-2000 Digital Spectrum Analyzer

When you receive your DSA-2000 hardware, examine it carefully for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately.

Use the following checklist to verify that you have received all of the system components

Basic System

Your package should contain the following items:

- The DSA-2000 Digital Spectrum Analyzer Instrument.
- This Manual.
- One ac Line Cord.
- One 3m (10 ft) RG-58/U 50 ohm coaxial cable.
- One BNC Tee Connector
- One LB1500 Cable Transformer.
- A rack mount kit consisting of one set of rack mount ears and associated hardware.

System Options

Your package will include any optional DSA-2000 items ordered.

Complete System

A complete system consists of all of the items in the Basic System, plus a computer. All software will have been installed on the computer and the system will have been configured and tested at the factory.

Initial Setup

To properly install and apply power to the DSA-2000 Spectrum Analyzer, please verify the following:

Operating Environment

Be sure you are operating in the operating environment specified for the instrument. The temperature and humidity specifications can be found in Appendix A, *Specifications*.

Instrument Cooling

The DSA-2000 Spectrum Analyzer is fan cooled. The fan inlet is located at the right side of the rear panel and exhaust holes are located on the left and right side of the bottom cover near the front panel. For optimum cooling, be sure to leave space behind and below the instrument and keep the air intake and exhaust holes free of any obstructions.

Connecting to the AC Line Power

The DSA-2000 Spectrum Analyzer can operate over a voltage range of 90 to 259 volts ac at 47 to 63 Hz and may require up to 60 watts of power. Your DSA-2000 should have been configured at the factory for the line voltage specified in your order. Please verify that the Power Entry module voltage selection matches the ac line input power. The module's voltage selection is visible through the window in its cover.

If it is necessary to change the Module's voltage selection or fuses, detach the ac Line cord from the DSA-2000 and follow the steps in Appendix C, *Voltage Selection*.

WARNING Turn off the DSA-2000 and disconnect the input power cord before working on the unit. Leaving the ac input power connected while working on the power entry module can result in serious injury or death.

Connecting to the Ethernet

The following discussion will guide you in connecting your DSA-2000 Digital Spectrum Analyzer for communications over the Ethernet. Figures 3 and 4 show typical Ethernet connections.

- Locate the desired Ethernet port on the DSA-2000's rear panel. Both 10Base2 and AUI connectors are available.
- Connect the appropriate cable.

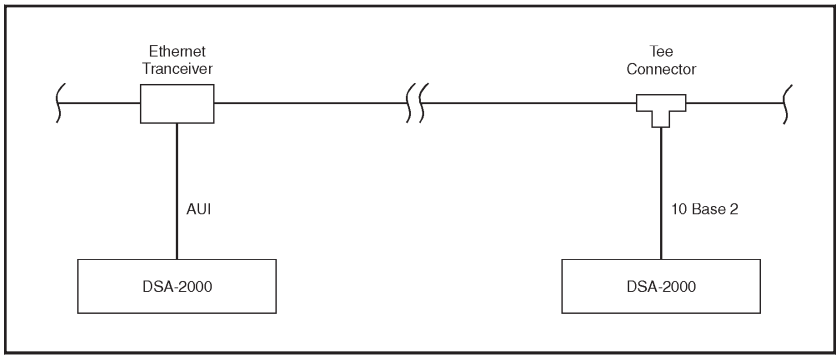


Figure 3 Multiple DSA-2000s in an Existing Network

- Identify the unique Ethernet station address assigned to the DSA-2000 (the four characters, such as 07C6, on the label next to the Ethernet port).

Connecting to the Ethernet

Each DSA-2000 is shipped with a 3 m (10 ft), RG-58/U coax cable and a Tee connector for connecting to the Thinwire (10 base 2) network. If the DSA-2000 is to be connected directly to its host computer, you need only the coax cable, your system 50 ohm terminators and the Tee connector. However, if the DSA-2000 is going to be connected in a network with other devices on the Ethernet, you may need additional cables and connectors.

Note A BNC Tee connector and 3 m (10 ft) RG-58/U coaxial cable are provided with the DSA-2000. The following hook-up examples assumes using your system 50 ohm terminators and additional BNC Tee connectors when required.

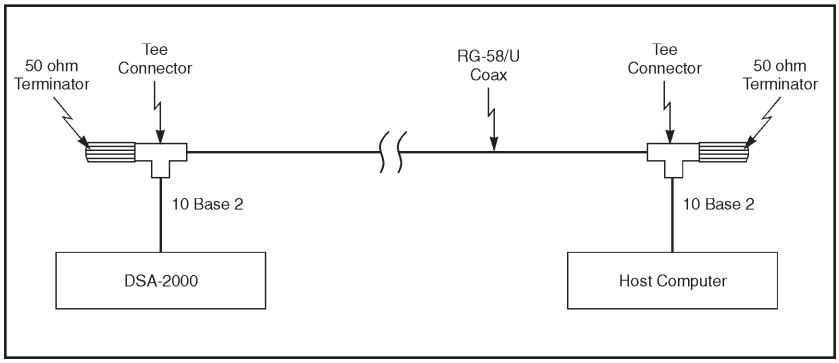


Figure 4 Local Ethernet Connection

The DSA-2000 can be connected to other types of Ethernet networks using external transceiver units, such as fiber optic or twisted pair. The AUI connector on the rear panel of the DSA-2000 provides power and signal connections for these external modules. At power on, the DSA-2000 automatically senses the type of network connection and configures itself for Thinwire or AUI operation. If no Ethernet connection is detected the Fault LED will be activated. At this point, both the Thinwire and AUI ports are enabled. After making either the Thinwire or AUI connection, the Fault LED will go out when packets are processed.

Note For proper operation, connect either Thinwire or AUI, not both.

Existing Thinwire Connection

1. Connect a BNC Tee connector to the existing Thinwire coax cable.

2. Attach the BNC Tee connector (with Thinwire coax cable attached to each end) to the 10 Base 2 connector on the DSA-2000's rear panel.

Local Thinwire Connection To Host Computer

1. Attach a 50 ohm terminator to one side of a BNC Tee connector and one end of the 50 ohm coax cable to the other side.

2. You can either completely uncoil the cable or only as much is needed to reach the host computer.

3. Attach the BNC Tee connector (with coax cable and terminator attached) to the 10 base 2 BNC connector on the DSA-2000's rear panel.

4. Make note of the four character label (example 07C6) next to the Ethernet port. This is the unique Ethernet station address for this DSA-2000. You will need to refer to it when you configure the instrument.

Connecting to the Host Computer

1. To the other end of the coax cable you just installed at the DSA-2000 attach a another BNC Tee connector and 50 ohm terminator.

2. Attach the BNC Tee connector (with coax cable and terminator attached) to the female BNC connector on the Ethernet adapter card in the host computer.

The DSA-2000 and host computer are now ready for direct communication.

Power On

When power is first applied to the DSA-2000, it will go through an initialization and self diagnostics process. During this initialization period, indicated by the Power On" LED blinking, the DSA-2000 is running internal diagnostic routines to verify correct operation of the hardware. These routines require 15 to 20 seconds to complete. The front panel hardware is tested next, with the front panel LEDs and bar graph displays turning on sequentially for approximately 2 to 5 seconds. As the bar graph displays sequence, they will pause briefly at half scale. The ICR LED may remain illuminated throughout the diagnostic check if an input signal is connected to the DSA-2000's AMP IN connector.

If the diagnostics were successful and communication with the host computer is established, the Power On LED and one of the High Voltage Range LEDs will remain on (unless otherwise programmed by the host computer, the DSA-2000 defaults to the +1.3 kV range). In addition, the Comm Tx and Comm Rx LEDs may flash indicating that communication with the host computer is taking place.

If the DSA-2000 detects a communications error with the host computer, the Fault LED will remain illuminated. This could result from a fault in the DSA-2000 hardware or a Ethernet communication problem with the network or host computer.

4. User Interface and Controls

This chapter provides basic information on the user interface and functional operation of the setup controls for the Model DSA-2000 Digital Spectrum Analyzer. Additional details and discussion can be found in Chapter 6 *Basic Spectroscopy Operation*, Chapter 7, *PUR/LTC Operation*, and Appendix B *Performance Adjustments.*

Unless noted otherwise, all controls are programmable through the host computer software. For specific details on using the host computer software, please refer to the appropriate software user's manual.

MID Wizard or MID Editor

The first step in using your DSA-2000 is to let it know the number and types of MCAs that are installed in or connected to your system, by way of an MCA Input Definition (MID).

For most Genie-2000-based systems, you'll want to use the MID Wizard to help you set up your DSA-2000's Input Definition quickly and easily.

If your Input Definition is more complex than the MID Wizard was designed to handle, you'll have to use the MID Editor to create your definition. It is covered in detail starting on page 16.

The MID Wizard

To use the MID Wizard, open the Genie-2000 folder and select the MID Wizard icon to start the definition process.

Step 1

The first screen (Figure 5) lets you select the MCA you want to create a definition for. Choose DSA-2000, then click the **Next** button.

Note: Figure 5 shows the MID Editor's Add MCA dialog for Genie 2000 V2.1 and later. Earlier versions of the MID Editor do not group MCAs by board type.

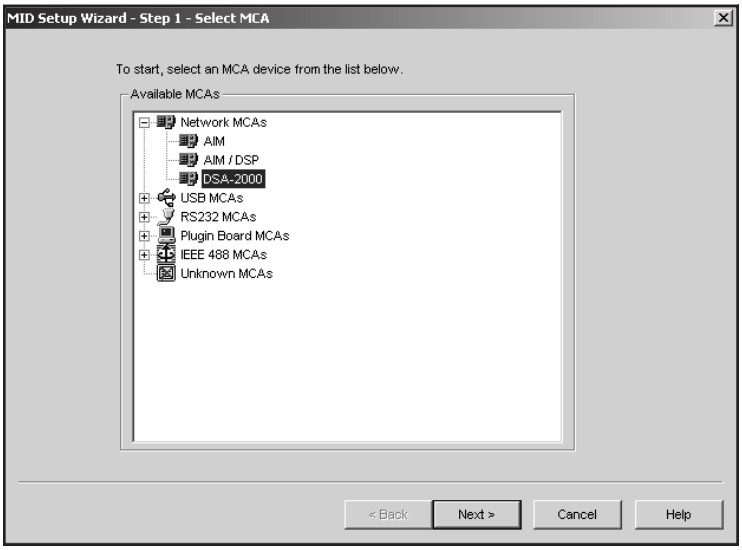


Figure 5 Selecting the MCA

Step 2

The Step 2 screen will ask you to define the MCA's Full Memory number of inputs and Ethernet address, as shown Figure 6. In addition, you can specify whether the input is PHA or MCS.

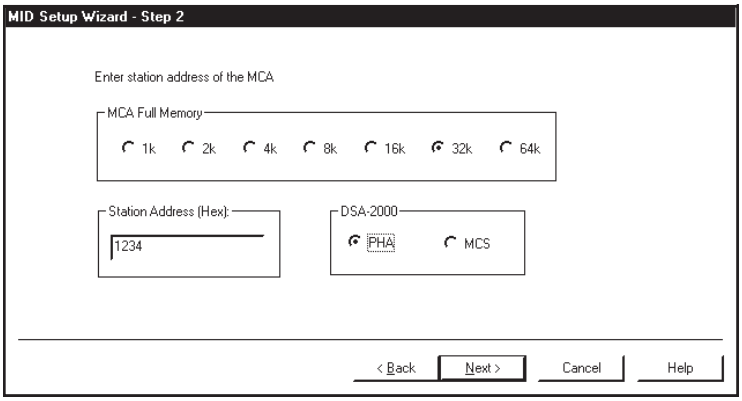


Figure 6 Defining the Full Memory and the Address

Steps 3 and 4

You won't see the screens for Steps 3 and 4; these steps are not used when setting up a DSA-2000.

Step 5

The screen in Figure 7 asks you to define the high voltage power supply's Range, Voltage Limit and Voltage.

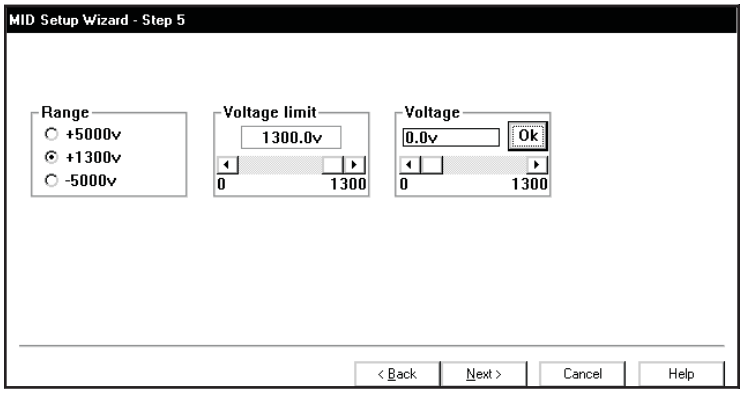


Figure 7 Defining the High Voltage Parameters

Step 6

The Step 6 screen in Figure 8 asks for a Detector Type and acquisition memory size in channels, and requires that an Input Name be entered.

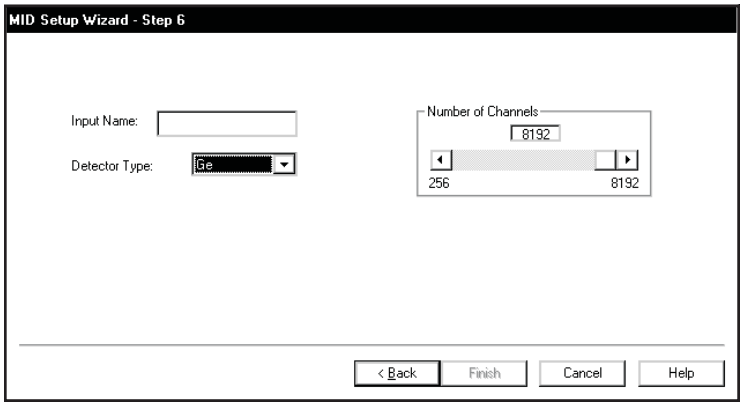


Figure 8 Assigning the Detector Type

Ending the Definition

To complete your Input Definition, select **Finish**. The input that you just defined will be stored as an MID file named inputname.MID and automatically loaded into the MCA Runtime Configuration Database (described on page 36). When you select **Finish**, you will be asked if you would like to define another input. Answering No will close the Wizard.

Note that if you didn't enter an Input Name, you won't be allowed to exit the Step 6 screen. If the name you entered is the same as the name of an existing MID file, the system will tell you so and go back to Step 6 to let you enter another name.

The MCA Input Definition Editor

You'll have to use the MID Editor only if you want to change default settings for any of the DSA-2000's programmable components. The following sections tell you how to use the MID Editor to make those changes.

Basic Concepts

We'll begin with some basic concepts that are important to understand before actually getting into the details of how you define your system's MCAs.

Multiple MCA Configurations

Since MCA definitions are saved in disk files, you can have as many definitions as you like. For example, you might have one MCA defined as an 1K Sodium Iodide Spectroscopy MCA in one file and another as a 2K Sodium Iodide Spectroscopy MCA in another file. Before you start an experiment you simply pick the configuration you want to use.

Because an MCA definition file can include any or all of the MCAs that are available to your system, you can use more than one MCA at a time. However, each MCA can be included only once in a given definition file and each MCA in that file must have a unique name.

Using the MCA Definition Files

To use an MCA Definition, you must first have saved the definition to disk as a file. Once you've done that, all you have to do is load that file into the VDM's internal MCA Runtime Configuration Database. From that point on, all MCA operations will use the configuration information that was stored in the Definition File. To change to a new configuration, all you have to do is replace the database's contents with a new file.

Starting the MCA Input Definition (MID) Editor

Start the MID Editor by double clicking on its icon in the Genie-2000 Program Group. The result will be the application window shown in Figure 9.

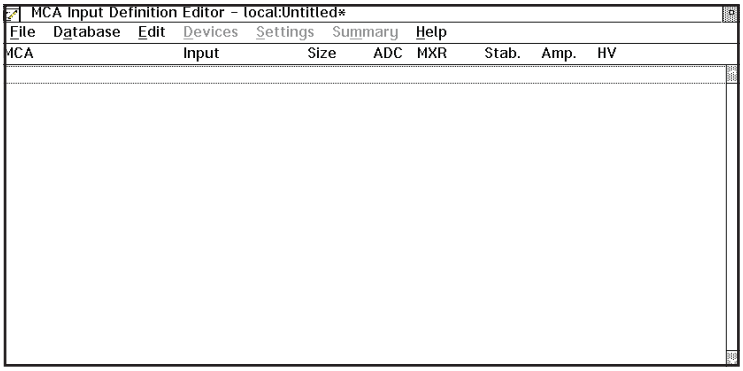


Figure 9 The MID Editor Window

Note that the phrase “local:Untitled” in the title bar, means that the MID Editor is connected to the local VDM and that no file is currently open; this is the default condition in a non-networked environment.

Building an MCA Definition

Building an MCA Definition means:

- Selecting the MCA and front end hardware to be used for each input through the Device Menu.
- Defining the operating characteristics and modes for each MCA and its front end hardware through the Settings Menu.

In this section we’ll explain how to add (and delete) the MID editor’s MCA entries and will explain what the definition entry consists of and the next section tells how to define the DSA-2000 MCAs.

The remainder of this chapter discusses how the definition is saved to a disk file, how a definition can be edited, and how to use a definition by loading the file into the MCA Runtime Configuration Database.

Adding an MCA

The Edit menu, shown in Figure 10, is used to add MCA hardware to or delete MCA hardware from an MCA Input Definition.

Figure 10 The Edit Menu

To add an MCA, select the **Add MCA** command in the **Edit** menu to see the "Add MCAs to Definition Table" Dialog Box (Figure).

Figure shows a typical Add MCA list box, allowing you to add an DSA-2000 MCA to the MCA Definition Table. You can add more DSA-2000 MCAs to the definition at any time with this command.

To add an MCA to your definition, you can:

1. Click on your choice, then click on the **Add** button, or

2. Double click on your choice.

Either way, you'll see an entry added to the MCA Definition Table for each such selection you make. When you've added your MCA to this definition, click on the DONE button to return to the main MID window.

Figure 11 shows the result of using this process to add a single DSA-2000 MCA to the Definition Table. Please remember that this display, as well as many others in this chapter, are examples of what you *might* see; your display may not be identical.

Interpreting the Definition Entry

As you can see in Figure 11, adding the entry put more than just the name of the MCA in the definition table. We'll take a brief look at the other items in the entry now. As we get further into the definition process we'll cover them in greater detail. Note the letter following the unit number in each Definition Table item: an M indicates a manually controlled unit, and a P indicates a programmable unit.

MCA

This is the type of MCA device being used for this particular entry in the table.

Input

This is the name that will be used to refer to this specific hardware entry in the table. The MID Editor automatically assigns these names sequentially as DET*nn*, starting with *nn*=01. As we'll see in "Input Name" on page 33, you can easily change these names to something you find more meaningful.

Size

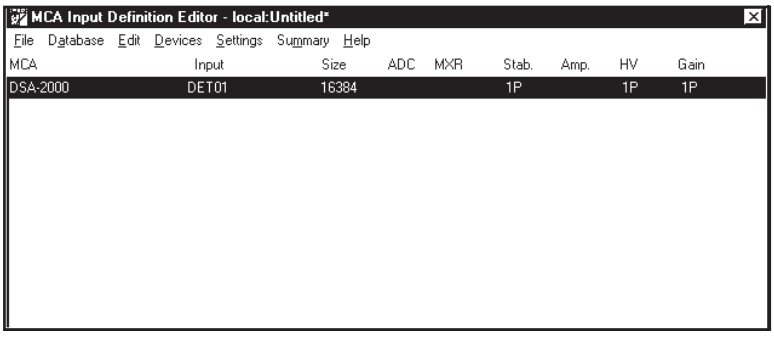


Figure 11 A DSA-2000 Has Been Added to the Table

This shows the number of data channels assigned to this input.

ADC

This column displays the type of ADC associated with the DSA-2000.

MXR

The MXR column isn't used by the DSA-2000.

Stab

This column describes the Stabilizer associated with the DSA-2000.

Amp

This column describes the amplifier associated with the DSA-2000.

HV

This column describes the High Voltage Power Supply associated with the DSA-2000.

Gain

This column describes the DSP Gain device associated with the DSA-2000.

Deleting an MCA

If you change your mind and want to remove an MCA that you have added to the definition, you can do it easily by:

1. Selecting the table entry you want to delete.

2. Clicking on the **Delete MCA** command in the **Edit** menu to see the Dialog Box in Figure 12. Click on **OK** to remove the entry.

Defining an MCA

This section discusses setting up a DSA-2000 MCA, which has a fully programmable front end. That is, its DSP Gain, DSP Filter, Digital Stabilizer, MCS and High Voltage Power Supply are all controlled from the host computer rather than manually with front panel knobs and switches. To begin, click on the MCA entry in the Definition Table that you want to set up.

Device Setup

The **Devices** menu, shown in Figure 13, sets the parameters for the DSA-2000's MCA and associated devices. Some Devices are disabled (grayed out) because they do not have any settable parameters. Of the enabled Devices, only the MCA and Sample Changer have user-selectable parameters. The remainder default to their only parameter: Internal.

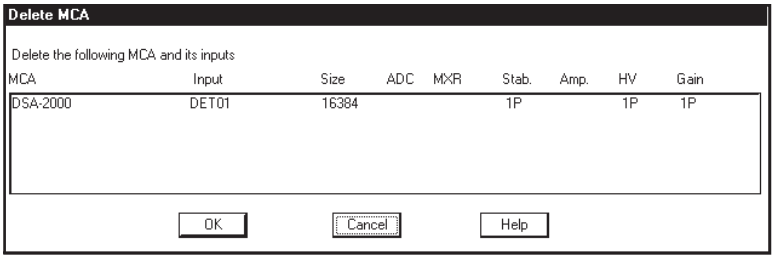


Figure 12 The Delete MCA Dialog

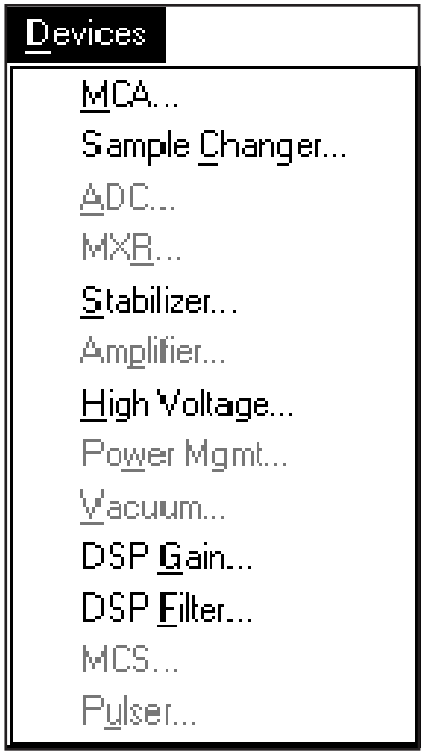


Figure 13 The Device Setup Menu

MCA

Selecting the **MCA** command in the **Devices** menu pops up the Dialog Box shown in Figure 14, which lets you set the Ethernet address for the DSA-2000 and select the type of input.

Full Memory Address

Select the DSA-2000's full memory size.

Station Address

Since the DSA-2000 is connected to the system through an Ethernet, you must specify the network address that will be used to communicate with the module. Enter the DSA-2000's four-digit address in the Station Address text box.

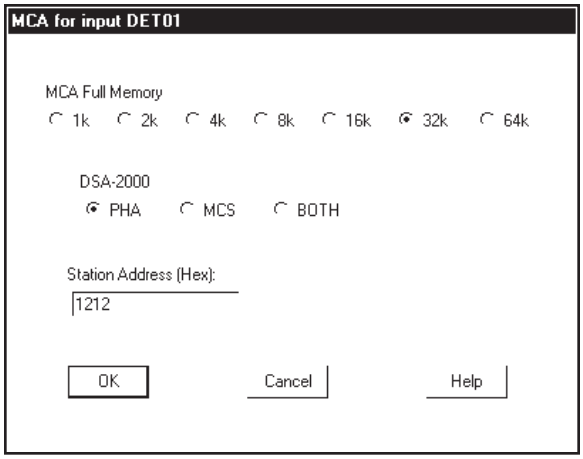


Figure 14 The MCA Device Setup Dialog

Type of Input

Select the DSA-2000's input type here: PHA, MCS or Both.

Sample Changer

This screen lets you set the polarity, Normal or Inverted, of the sample changer's Advance and Ready control signals.

The Settings

The following section describes those parameters for the DSA-2000 that can be accessed from the MID Editor via the Settings menu (Figure 15).

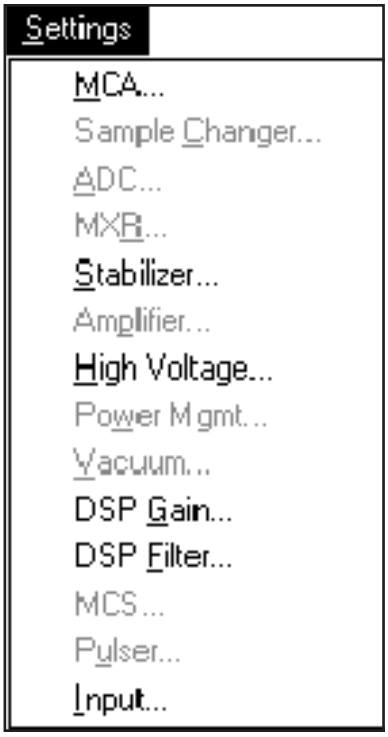


Figure 15 The Settings Menu

MCA Settings

The only setting you can change here is the Input Type: PHA, MCS or Both.

Stabilizer Settings

The Stabilizer maintains the stability of high resolution spectroscopy in applications involving long count times or high count rates. It accomplishes this by using reference peaks in the spectrum and correcting the ADC's conversion gain or its zero intercept, or both, to keep these peaks from drifting. The count rates in these reference peaks should be high enough to be significantly more than the background in their chosen stabilizer windows.

Selecting the **Stabilizer** command pops up the Dialog Box shown in Figure 16.

Note This window's initial focus is on the **Cancel** button; pressing the keyboard's ENTER key after making changes in this dialog box will cancel the changes. Be sure to click on the **OK** key to accept the changes.

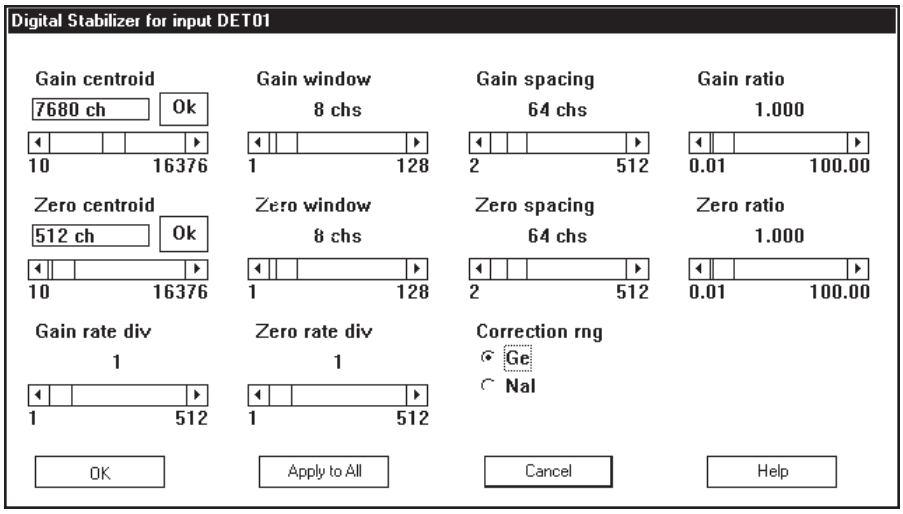


Figure 16 The Stabilizer Settings Dialog

Figure 17 shows the relationship between the Stabilizer's Centroid, Window and window Spacing on a typical peak.

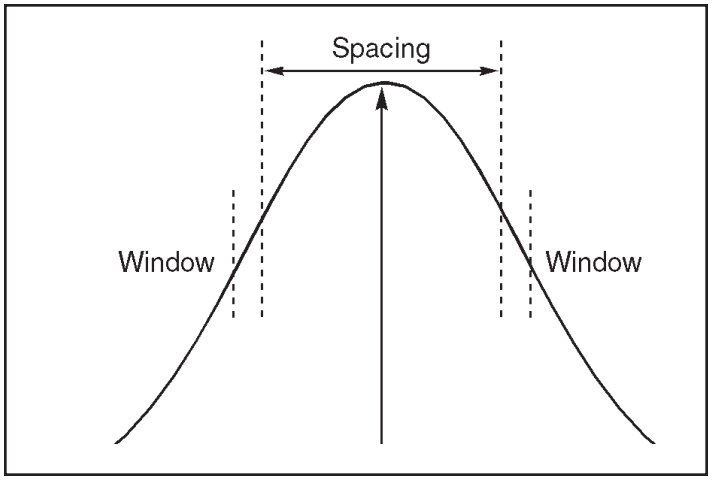


Figure 17 The Relationship Between Stabilizer Functions

Gain Centroid

Sets the centroid (in channels) of the reference peak at the high end of the spectrum for gain stabilization.

Gain Window

Sets the width (in channels) of the upper and lower sampling windows on either side of the gain reference peak.

Gain Spacing

Sets the spacing (in channels) between the upper and lower sampling windows. The windows should be placed so that a shift in the reference peak reflects a significant change in count rate through the window. For broad peaks, the spacing should be set so that the windows' edges are not on the flat part of the peak.

Gain Rate Div

The Gain Rate Divisor sets the count rate dividers at the input to the correction register for Gain. For high count rate reference peaks, increasing the Divider value will smooth out the correction applied to the system and minimize any peak broadening. This control can only be set via the MID Editor.

Gain Ratio

The Gain ratio value is interpreted by the stabilizer as the ratio to maintain between the two gain windows (ratio = upper window / lower window). For instance, a value of 1 would be appropriate for a pure Gaussian peak.

Zero Centroid

Sets the centroid (in channels) of the reference peak at the low end of the spectrum for zero intercept stabilization.

Zero Window

Sets the width (in channels) of the upper and lower sampling windows on either side of the zero reference peak.

Zero Spacing

Sets the spacing (in channels) between the upper and lower sampling windows. The windows should be placed so that a shift in the reference peak reflects a significant change in count rate through the window. For broad peaks, the spacing should be set so that the windows edges are not on the flat part of the peak.

Zero Rate Div

The Zero Rate Divisor sets the count rate dividers at the input to the correction register for Zero intercept. For high count rate reference peaks, increasing the Divider value will smooth out the correction applied to the system and minimize any peak broadening. This control can only be set via the MID Editor.

Zero Ratio

The Zero ratio value is interpreted by the stabilizer as the ratio to maintain between the two zero windows (ratio = upper window / lower window). For instance, a value of 1 would be appropriate for a pure Gaussian peak.

Correction Rng

Correction range: 1% (Ge) or 10% (NaI). This control selects the Gain Correction range that can be provided to correct for drift. Select ±1% for a germanium detector or ±10% for a sodium iodide detector. This control can only be set via the MID Editor.

High Voltage Settings

The **High Voltage** command, shown in Figure 18, adjusts the High Voltage Power Supply (HVPS).

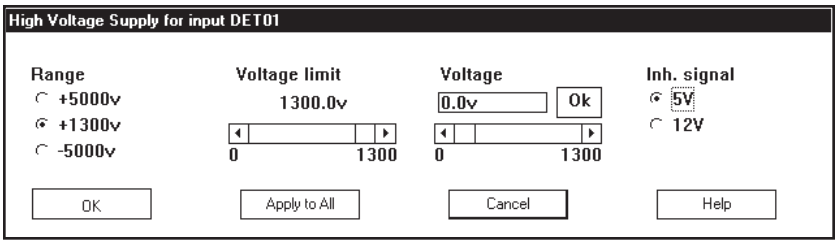


Figure 18 The High Voltage Settings

Note: This window's initial focus is on the **Cancel** button; pressing the keyboard's ENTER key after making changes in this dialog box will cancel the changes. Be sure to click on the **OK** button to accept the changes.

Range

The **Range** control, must be set *before* the Voltage Limit or Voltage Control is adjusted, sets HV Power Supply's absolute voltage limit to positive 1300 volts for a sodium iodide or cadmium telluride detector, or positive or negative 5000 volts for a detector requiring no more than 100 µA of bias current, such as a germanium detector. This automatically changes the upper value for the Voltage Limit and Voltage controls. This control can be set only in this Dialog Box; it cannot be changed in the Acquisition and Analysis application.

Voltage Limit

The **Voltage limit** control establishes the HVPS's maximum output voltage within the selected range. It must be set *before* the Voltage control is adjusted. This control can be set only in this Dialog Box; it cannot be changed in the Acquisition and Analysis application.

Voltage

After setting the Voltage Limit, the **Voltage** scroll bar sets the output of the HVPS between the Voltage Limit's minimum and maximum settings. The voltage can also be typed in from the keyboard, then accepted with the Ok button within the control. The Acquisition and Analysis application allows you to adjust the output voltage, as well as turn the HVPS on and off and reset it.

Inh. Signal

Sets the pull-up voltage of the HV INH connector to +5 or +12 V. All Canberra detectors and preamps use +5V.

DSP Gain Settings

The DSP Gain settings screen (Figure 19) for the DSA-2000 contains the following controls.

Coarse Gain

Sets the device's coarse gain. It's best to choose the highest Fine Gain which, combined with the Coarse and Super-Fine Gains, will produce the total desired gain.

Fine Gain

Sets the device's Fine Gain multiplier.

S-Fine Gain

Sets the device's Super-Fine Gain value.

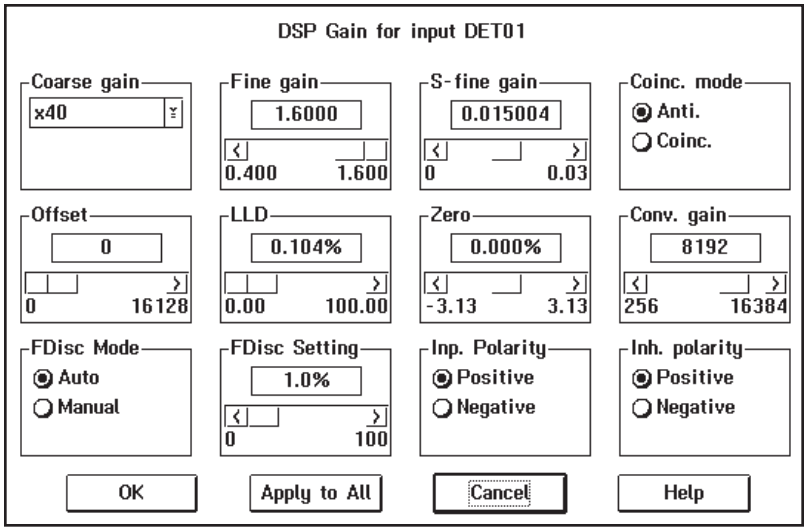


Figure 19 The DSP Gain Settings

The combination of Coarse and Fine Gain sets the overall system gain to match the requirements of the detector and energy application; overall gain is continuously variable from x2.0 to x1536. The Fine Gain factor is dependent on the Super-Fine Gain (SFG) value. With the SFG set to $0.0000e^{-2}$, the Fine Gain covers a range of x0.4 to x1.6. The SFG value adds to the Fine Gain factor and covers a range of $0.0000e^{-2}$ to $3.0000e^{-2}$.

Coinc Mode

Sets the devices gating mode (COINCidence or ANTIcoincidence). In COINCidence mode, a positive GATE pulse; dc level or open input enables the conversion of the event in process (in ANTIcoincidence mode, a positive GATE pulse disables the conversion of the event in process; an open input enables conversion). To enable/disable an event, the GATE pulse must occur during the trapezoid rise time and flat top. The Trapezoid signal timing may be viewed on the MONITOR Output. The GATE pulse duration must be equal to or greater than 50 nanoseconds. This control can only be set via the MID editor.

Offset

Sets the devices digital offset in channels. The digital offset shifts the memory assignment of the device's conversions to the left (e.g. an offset value of 4096 would shift channel 4096 down to correspond to channel zero of the memory).

LLD

Sets the devices Lower Level Discriminator (LLD) as a percentage of the ADC's full scale.

Zero

Sets the device's zero intercept as a percentage of the device's full scale.

Conv. Gain

Sets the device's conversion gain. It can be set from 256 to the maximum number of channels supported by the device. The gain will change by a factor of two. Note that this value is automatically copied down to the DSA-2000's internal Conversion Range parameter.

FDisc Mode

Sets the device's Fast Discriminator threshold mode. AUTO allows the threshold to be optimized automatically above the system noise level; MANUAL allows the threshold to be manually adjusted.

FDisc Setting

Sets the device's Fast Discriminator threshold level (when MANUAL Fdisc Mode is selected). The range is 0 to 100%.

Inp. Polarity

Sets the device's Input signal polarity to either Positive or Negative. The device's input polarity must match the preamplifier's output polarity. This control can only be set via the MID Editor.

Inh. Polarity

Sets the device's Inhibit signal polarity to either Positive or Negative. If you are using a TRP preamplifier, the Inhibit Polarity control matches the polarity of the device's Inhibit (reset) input to the polarity of the preamp's Inhibit output. This control can only be set via the MID Editor.

DSP Filter Settings

The DSP Filter settings screen (Figure 20) for the DSA-2000 contains the following controls.

BLR Mode

Sets the baseline restorer mode. With a setting of AUTO, the baseline restorer is automatically optimized as a function of trapezoid shaping time and count rate. With settings, of SOFT, MEDIUM and HARD, the baseline restorer is set to fixed rates as selected.

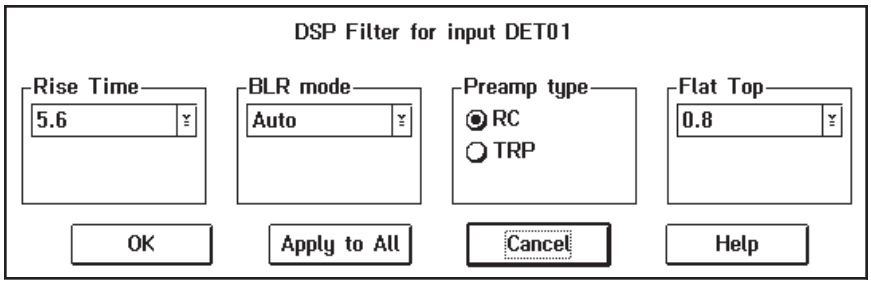


Figure 20 The DSP Filter Settings

Preamp Type

Selects the Preamplifier type as either TRP (Transistor Reset Preamp type) or RC (RC coupled preamp type). RC enables the pole/zero adjust screen in the **MCA | Adjust | Filter Device** screen; TRP disables the pole/zero adjustment. This control can only be set via the MID Editor.

Rise Time

Symmetrically sets the rise time and fall time of the digital filter time response. As with conventional Gaussian shaping, the degree of noise filtering is proportional to the rise time selection. There are 35 rise/fall times, ranging from 0.4 to 28 µs. The rise time can also be set in the Acquisition and Analysis application; for more information please refer to “Rise Time and Flat Top Adjustments” on page 86.

Flat Top

Sets the flat top portion of the digital filter time response. The flat top matches the filter to the detector charge collection characteristics to minimize the effects of ballistic deficit. There are 21 flat top time selections, ranging from 0 to 3 µs. The flat top can also be set using the Auto BDC function in the Acquisition and Analysis application. For more information on using the Auto BDC function, please refer to “Automatic Ballistic Deficit Correction” on page 64.

MCA Settings

If you choose either MCS mode or Both mode, you’ll also have to select the MCS Disc Mode as shown in Figure 21.

Note: This window’s initial focus is on the **Cancel** button; pressing the keyboard’s ENTER key after making changes in this dialog box will cancel the changes. Be sure to click on **OK** to accept the changes.

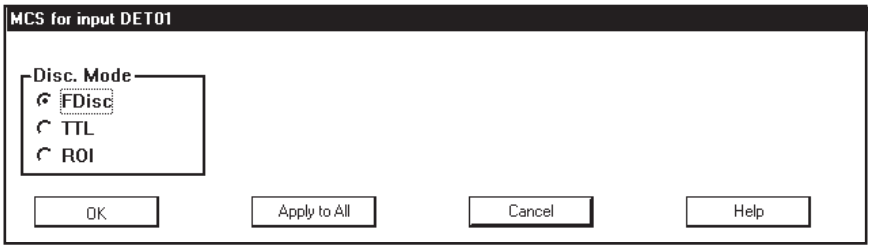


Figure 21 Choosing the MCS Disc Mode

Disc. Mode

The Disc Mode control establishes the MCS mode to be used. Selecting FDisc enables the MCS's "fast discriminator mode": all incoming events processed by the DSP are counted. Selecting TTL enables the MCS's "TTL mode" causes all TTL events (as seen at the MCS IN rear panel connector) to be counted. Selecting ROI enables the "ROI discrimination mode", meaning that all incoming events processed by the DSP that fall within the selected discrimination window are counted.

Input Settings

The **Input** command is used to change the name of the Input and set up the structure of its memory via the Dialog Box shown in Figure 22. These commands are not available in the Acquisition and Analysis application.

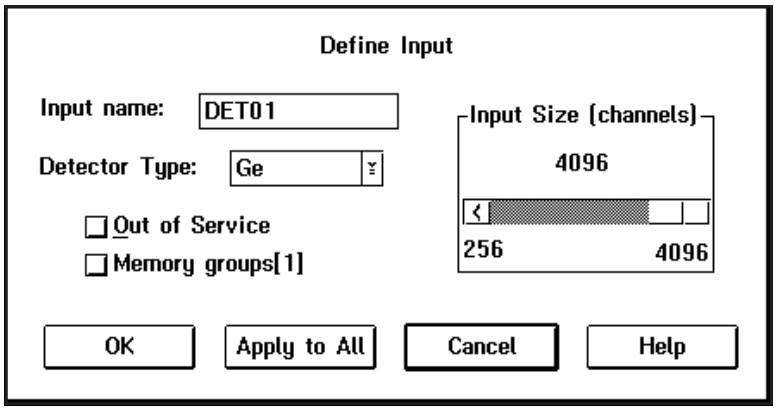


Figure 22 The Define Input Dialog

Note: This window's initial focus is on the **Cancel** button; pressing the keyboard's ENTER key after making changes in this dialog box will cancel the changes. Be sure to click on the **OK** key to accept the changes.

Input Name

The default DETnn name is the name displayed here, allowing you to easily change it to a more meaningful name, such as "H2OSampl", up to a total of eight characters.

Detector Type

Use this drop-down list to select the type of detector to be used with this MCA; this also assigns appropriate default values to the spectrum display and analysis parameters.

Input Size

This parameter defaults to 8K, the number of channels assigned during Device setup for the MCA, on the assumption that you'll be using "Full Memory" for your data acquisition. To use less than the maximum available memory size, use this control to select the size you want to use. For instance, for NaI spectra, you wouldn't want to use more than 1024 channels.

Out of Service

This Check Box allows you to place this Input temporarily "out of service". That is, it will remain as an entry in your MCA Definition File but will not be available for data acquisition. It is meant to be used when the MCA or its front end electronics are temporarily disconnected.

Memory Groups

This check box allows you to define a multi-memory group input; this box is enabled if the input size is defined less than the physical MCA memory size.

Saving the Input Definition

After completing a definition, use the MID Editor's **File | Save** (or Save as) command to save the Definition file.

As a reminder, you'll see an asterisk (*) next to the name of the current definition in the Title Bar when a changed definition has not been saved.

CAUTION If you change an existing Input Definition, saving it will set its calibrations to default and will clear the Acquisition Start time.

The File Descriptor

When a Definition is saved for the first time, the Save As file dialog box is automatically opened. In that dialog box, you'll see a File Descriptor field, which lets you store a 32-character description with your file to make it easier to locate when you want to use it again.

Changing the Summary View

Before going on to see how to edit an existing Input Definition Table, one that you've built previously and saved to disk, there's one more menu to look at. This is the Summary menu, which is shown in Figure 23.

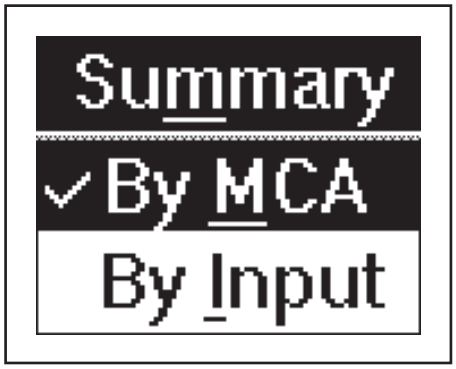


Figure 23 The Summary Menu

The **Summary** menu has two commands: **By MCA** and **By Input**, which change the order in which the information in the Input Definition Table is displayed. By MCA means that the first column of the table will display the MCA type that is being used for each entry. If you choose By Input, the MCA and Input columns will be reversed in the display and the Inputs will be sorted alphabetically.

You can choose either method, but in the case of systems with a large number of inputs, "By Input" is an easier display to understand than "By MCA".

Editing an MCA Definition

To edit an MCA Definition, use the MID Editor's **File | Open** command to select the file and open it in the editor.

Editing a File in the Runtime Configuration Database

If the Definition you want to edit has been loaded into the MCA Runtime Configuration Database, it must first be unloaded before it can be opened in the editor. See "Unloading the Database" on page 38 for instructions.

Viewing the File Details

If you're not sure which file you want to edit, select a file, then click on the **Info** button to see further information about the file, as shown in Figure 24.

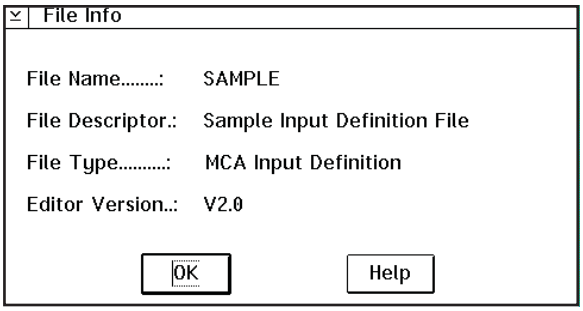


Figure 24 The File Info Display

The key piece of information here is the File Descriptor, which you added when the file was first saved. This should help you decide if the file you selected is the one you want to edit.

Editing the Definition

All of the menus and commands available for defining an MCA are also used for editing a definition. Just select the entry you want to change and apply the commands as before, then **Save** the Definition file.

The New Command

If you want to create a totally new MCA Definition, the **File** menu's **New** command clears the definition table so you can begin a new definition.

Because New is a destructive operation, selecting it will cause the program to ask for a confirmation in one of two ways:

1. If the Definition currently being displayed has not been changed since it was last saved (no asterisk in the Title Bar), you will be asked if you want to erase the current Definition. Click on **OK** to erase it, or **Cancel** to return to the Input Definition Editor.

2. If the Definition currently being displayed has been changed but not saved, you will be given a chance to save it.

The Input Definition Report

The **File** menu's **Report** command always saves to a disk file, but if you click on **Yes** in the dialog box that pops up, you can send the report to a disk file *and* print the report as well. Click on **No** to save it to a disk file without printing the report.

Using MCA Definition Tables

The whole purpose behind building MCA Input Definitions is to let the DSA-2000 know the number and types of MCAs you'll be using with your system. You do this by loading one or more MCA Definition Files into the MCA Runtime Configuration Database.

This database is shared by all of the programs which make up the DSA-2000 software package, and is used by those programs to gain access to the actual MCA hardware in your system. In this section we'll take a look at the procedures used for setting up that database.

Viewing the Current Database

To view the current contents of the database, click on the **Database** menu's **View** command, which will pop up the display shown in Figure 25. If you click on a line in the list, you can use the Device and Settings menus to look at details of that definition. Click on **OK** to close the View window.

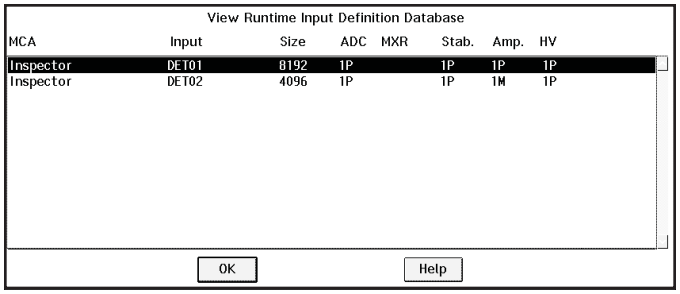


Figure 25 Viewing the Database

Loading and Unloading Definitions

Before you can use an MCA Definition, you'll have to load it into the database, so we'll start with that process. Note that you can't edit a loaded database; you'll first have to unload it as described in "Unloading the Database" on page 38).

The Load/Unload functions will be disabled while any Acquisition and Analysis applications are running and have open datasources. This prevents one user from altering the runtime database while another user is accessing it.

Loading the Database

A new Definition can be loaded into the Database with the **Load to** command, which brings up the Dialog Box in Figure 26, which lets you choose the file to be loaded into the database.

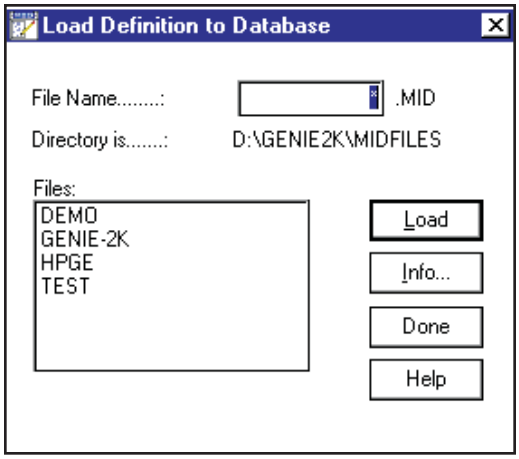


Figure 26 The Load To Dialog

Loading Multiple Definitions

Though you will usually use only one definition at a time, there may be times when you want to load more than one definition. To do this, be sure that the Input name in each of the Definition Files is unique.

If you try to load an Input Definition which contains a duplicate Input name, you'll see an error message telling you that the requested Definition can't be loaded.

Unloading the Database

Though some of the programmable front end controls, such as ADC Gain or Amplifier Gain, are initially set with the MCA Input Definition Editor, many may also be adjusted in the Acquisition and Analysis application while you're collecting data. These adjustments can be stored in the database (with File | Save), and when you Unload the database, are saved in an Input Definition File for future sessions.

The Unload Process

To unload a Database, click on the **Database** menu's **Unload from** command, which will bring up the Dialog Box shown in Figure 27. If several choices are listed, there are multiple definitions in the database.

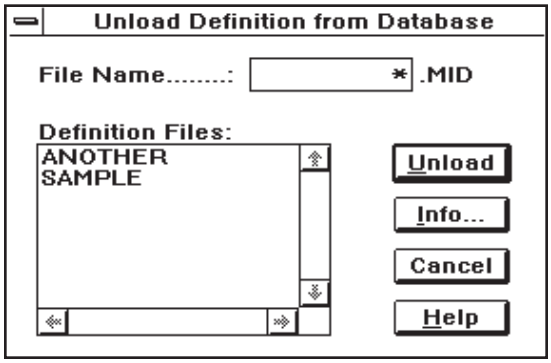


Figure 27 The Unload Dialog

Click on the one you want to unload, then click on the **Unload from** button. Note that this menu item is disabled if the MCA Runtime Configuration Database is currently being used by another application.

Acquisition Window Adjust Screen

The following section describes those parameters for the DSA-2000 that can be accessed from the acquisition windows' Adjust dialog screen. Note that the Adjust screen for a given device may actually be composed of several screens, which are accessed by using the **Next/Prev** pushbuttons. More detail information about specific function can be found in *Basic Spectroscopy Operation* on page 53, *PUR/LTC Operation* on page 67 and *Performance Adjustments* on page 86.

Stabilizer Parameters

The Stabilizer settings screen (Figure 28) for the DSA-2000 contains the following controls.

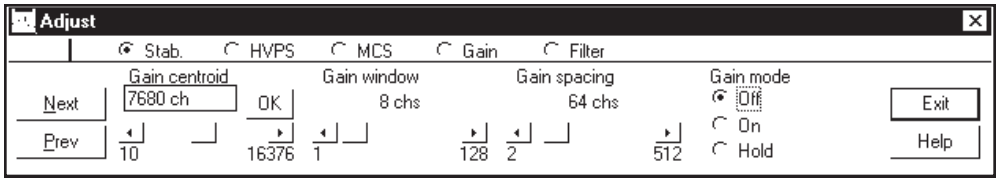


Figure 28 The Adjust Stabilizer Dialog

Gain Centroid

Sets the centroid (in channels) of the reference peak at the high end of the spectrum for gain stabilization.

Gain Window

Sets the width (in channels) of the upper and lower sampling windows on either side of the gain reference peak.

Gain Spacing

Sets the spacing (in channels) between the upper and lower sampling windows. The windows should be placed so that a shift in the reference peak reflects a significant change in count rate through the window. For broad peaks, the spacing should be set so that the windows' edges are not on the flat part of the peak.

Gain Mode

Sets the Gain Stabilization mode to Off, On or Hold.

Off disables gain stabilization and sets the correction adjustment to 0.

On enables gain stabilization, allowing the Stabilizer to compare the incoming data to the gain Centroid and Window settings, then compensate for data below (or above) the Centroid.

Hold disables gain stabilization, but maintains the current correction adjustment at the Stabilizer's output.

Gain Ratio

The Gain ratio value is interpreted by the stabilizer as the ratio to maintain between the two gain windows (ratio = upper window / lower window). For instance, a value of 1 would be appropriate for a pure Gaussian peak.

Zero Centroid

Sets the centroid (in channels) of the reference peak at the low end of the spectrum for zero intercept stabilization.

Zero Window

Sets the width (in channels) of the upper and lower sampling windows on either side of the zero reference peak.

Zero Spacing

Sets the spacing (in channels) between the upper and lower sampling windows. The windows should be placed so that a shift in the reference peak reflects a significant change in count rate through the window. For broad peaks, the spacing should be set so that the windows edges are not on the flat part of the peak.

Zero Mode

Sets the Zero Stabilization mode to Off, On or Hold.

Off disables zero stabilization and sets the correction adjustment to 0.

On enables zero stabilization, allowing the Stabilizer to compare the incoming data to the zero Centroid and Window settings, then compensate for data below (or above) the Centroid.

Hold disables zero stabilization, but maintains the current correction adjustment at the Stabilizer's output.

Zero Ratio

The Zero ratio value is interpreted by the stabilizer as the ratio to maintain between the two zero windows (ratio = upper window / lower window). For instance, a value of 1 would be appropriate for a pure Gaussian peak.

DSP Gain Parameters

The DSP Gain settings screen (Figure 29) for the DSA-2000 contains the following controls.

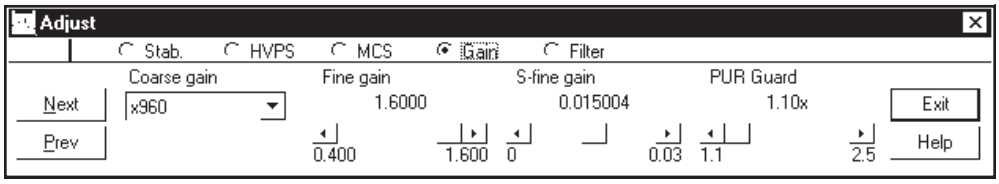


Figure 29 The Adjust DSP Gain Dialog

Coarse Gain

Sets the device's coarse gain. It's best to choose the highest Fine Gain which, combined with the Coarse and Super-Fine Gains, will produce the total desired gain.

Fine Gain

Sets the device's Fine Gain multiplier.

S-Fine Gain

Sets the device's Super-Fine Gain multiplier.

The combination of Coarse and Fine Gain sets the overall system gain to match the requirements of the detector and energy application; overall gain is continuously variable from x2.0 to x1,536. The Fine Gain factor is dependent on the Super Fine Gain (SFG) value. With the SFG set to $0.0000e^{-2}$, the Fine Gain covers a range of x0.4 to x1.6. The SFG value adds to the Fine Gain factor and covers a range of $0.0000e^{-2}$ to $3.0000e^{-2}$.

Offset

Sets the devices digital offset in channels. The digital offset shifts the memory assignment of the device's conversions to the left (e.g. an offset value of 4096 would shift channel 4096 down to correspond to channel zero of the memory).

LLD

Sets the devices Lower Level Discriminator (LLD) as a percentage of the ADC's full scale.

Zero

Sets the device's zero intercept as a percentage of the device's full scale.

Conv. Gain

Sets the device's conversion gain. It can be set from 256 to the maximum number of channels supported by the device. The gain will change by a factor of two. Note that this value is automatically copied down to the DSA-2000's internal Conversion Range parameter.

FDisc Mode

Sets the device's Fast Discriminator threshold mode. AUTO allows the threshold to be optimized automatically above the system noise level; MANUAL allows the threshold to be manually adjusted.

FDisc Setting

Sets the device's Fast Discriminator threshold level (when MANUAL Fdisc Mode is selected). The range is 0 to 100%.

PUR Guard

Sets the device's guard time (GT) multiplier to reject trailing edge pileup in the event of detector/preamp anomalies. The PUR guard sets the pileup reject interval, which is defined by GT x TRisetime + TFlattop.

LT Trim

Allows adjustment of the trapezoid pulse evolution time or dead time to optimize LTC performance. The adjustment range is 0 to 1000; the default value of 250 provides good LTC performance for a wide range of applications.

LTC Mode

Sets the amplifier's Pulse Pileup Rejector and Live Time Corrector. When PUR is On, the pileup rejector and live time corrector (LTC) are enabled. Off disables the pileup rejector and LTC.

Inhibit Mode

Selects inhibit mode. NORMAL instructs the device to gate off while the INHIBIT Input is true. In RESET mode, the inhibit time is automatically extended to account for the system overload recovery time or while external INHIBIT Input is set true.

DSP Filter Parameters

The DSP Filter settings screen (Figure 30) for the DSA-2000 contains the following controls.

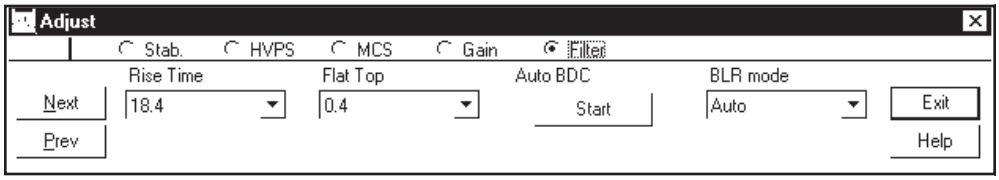


Figure 30 The Adjust DSP Filter Dialog

BLR mode

Sets the baseline restorer mode. With a setting of AUTO, the baseline restorer is automatically optimized as a function of trapezoid shaping time and count rate. With settings, of SOFT, MEDIUM and HARD, the baseline restorer is set to fixed rates as selected.

Rise Time

Symmetrically sets the rise time and fall time of the digital filter time response. As with conventional Gaussian shaping, the degree of noise filtering is proportional to the rise time selection. The rise time can be selected from 35 rise/fall times ranging from 0.4 to 28 µs.

Flat Top

Sets the flat top portion of the digital filter time response. The flat top matches the filter to the detector charge collection characteristics to minimize the effects of ballistic deficit. The flat top time can be selected from 21 flat top selections ranging from 0 to 3 µs.

Pole/Zero

Sets the device's pole/zero setting (0 to 4095). The values 1 to 4095 represent 1.7 ms to 40 µs; a value of zero sets the pole/zero compensation off (infinity).

Auto P/Z (DSA-2000A only)

Available only for the DSA-2000A with the automatic pole/zero option installed. Initiates automatic p/z process at the device.

Auto BDC

Initiates the automatic BDC process (optimizing of the trapezoidal flat top parameters to match the collection time of the detector) at the device.

MCS Parameters

The MCS settings screen (Figure 31) for the DSA-2000 contains the following controls:

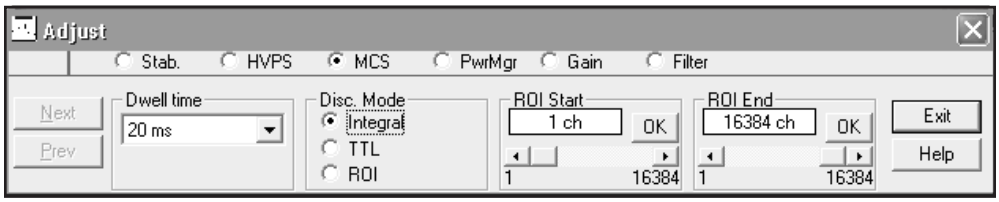


Figure 31 The Adjust MCS Dialog

Dwell Range

Sets the units for dwell time value.

Dwell Value

Sets the dwell time value (in units specified by the Dwell Range control)

Disc. Mode

The Disc Mode control establishes the MCS mode to be used. Selecting FDisc enables the MCS's "fast discriminator mode": all incoming events processed by the DSP are counted. Selecting TTL enables the MCS's "TTL mode" causes all TTL events (as seen at the MCS IN rear panel connector) to be counted. Selecting ROI enables the "ROI discrimination mode", meaning that all incoming events processed by the DSP that fall within the selected discrimination window are counted.

ROI Start

Sets the start channel of the discrimination window used when ROI mode is enabled.

ROI End

Sets the end channel of the discrimination window used when ROI mode is enabled.

Note that the ROI Start/End channels for the MCS input can be selected by setting up the DSA-2000 for "Both inputs" and using the PHA input to select the start/end channels.

High Voltage

The **High Voltage** screen (Figure 32), adjusts the High Voltage Power Supply (HVPS). Some of the controls shown in the figure may not be available on your DSA-2000.

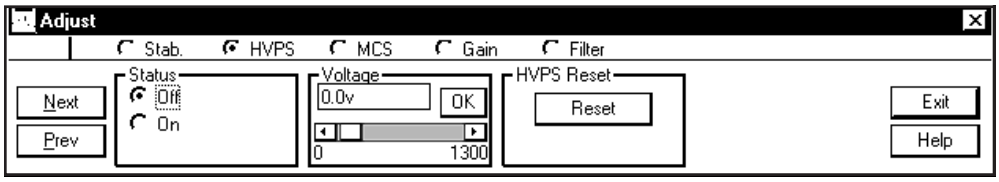


Figure 32 The Adjust HVPS Dialog

Note: This window's initial focus is on the **Cancel** button; pressing the keyboard's ENTER key after making changes in this dialog box will cancel the changes. Be sure to click on the **OK** button to accept the changes.

Status

This control allows you to turn the HVPS on/off.

Voltage

The **Voltage** scroll bar sets the output of the HVPS between the Voltage Limit's minimum and maximum settings.

HVPS Reset

This control resets any HVPS fault condition (for example, inhibit or overload).

Using the DSA-2000 with Genie-VMS

To use the DSA-2000 with Genie-VMS, be sure that the DSA-2000's firmware is at revision 1.08 (12/09/98) or higher. Contact Customer Service for a firmware update if required.

To use a DSA-2000 input you must create a programmable module setup file specific to the MCA configuration. The procedure is the same as that used for an AIM with computer controlled modules. A sample setup file exists in the (VMS) ND_EXAMPLES: directory called DEMO_DSP.CCN.

You must create one setup file for each port on the DSA-2000 that you want to use. The device supports two input ports. Port 1 is for PHA acquisition and port 2 for MCS acquisition.

Configuring the Device Settings

To edit the setup file and specify the device settings, use the Genie-ESP Parameters Editor (PARS/GUI) and to configure the DSA-2000, use the DSP Module, the High Voltage Power Supply Module, and the Miscellaneous Parameters. The parameters in these modules are described in “Defining an MCA”, starting on page 20.

The DSP Module

When you choose the DSP Module option, you’ll see Figure 33, the DSP Module dialog.

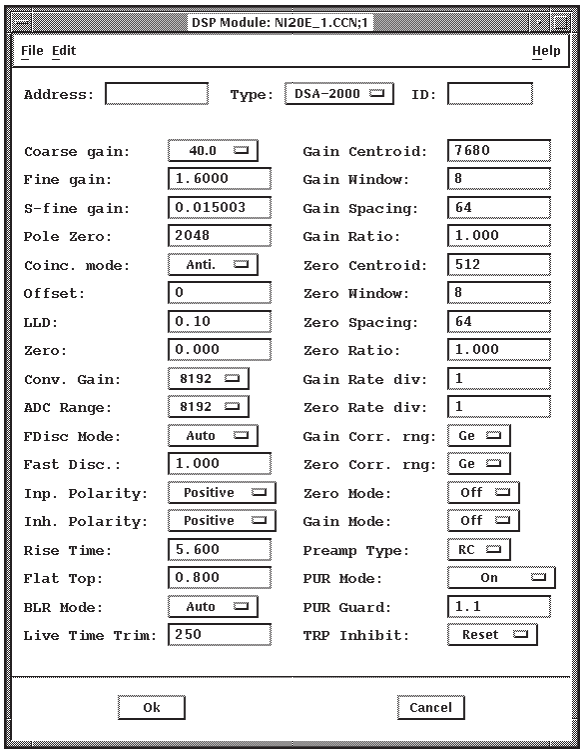


Figure 33 The VMS DSP Module Dialog

The values shown in the figure are typical defaults for a germanium detector, with the exception of the address, and the ID. Leave the address field blank and enter “0” in the ID field; the software will automatically retrieve the serial number of the device when the MCA configuration is created.

The HVPS Settings

Next, use the GUI editor to edit the HVPS parameters shown in Figure 34. Note that the DSA-2000 HVPS range and polarity settings allow only +5000 V, –5000 V, and +1300 V.

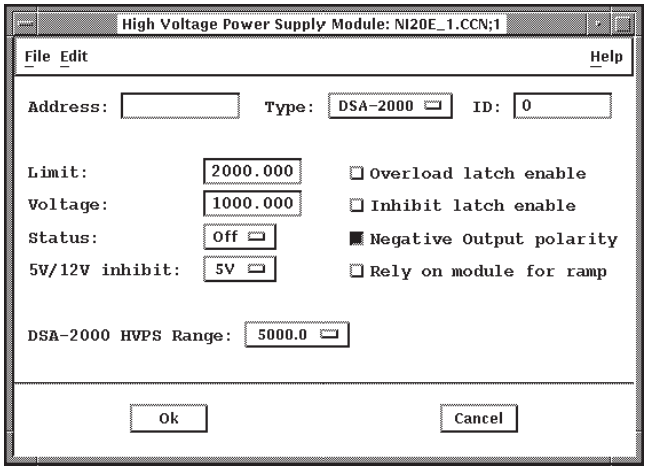


Figure 34 The VMS High Voltage Dialog

CAUTION The HVPS settings are entirely software selectable; there are no internal jumpers for selecting the HVPS range, limit or setting. It is very important that you select the appropriate values for the detector to be used with the DSA-2000. Set these values in the CCN file before creating the MCA configuration in the steps that follow. If in doubt, disconnect the detector’s HVPS cable before creating the MCA configuration for the first time.

The Miscellaneous Parameters

Now set the Miscellaneous Parameters, using the dialog shown in Figure 35.

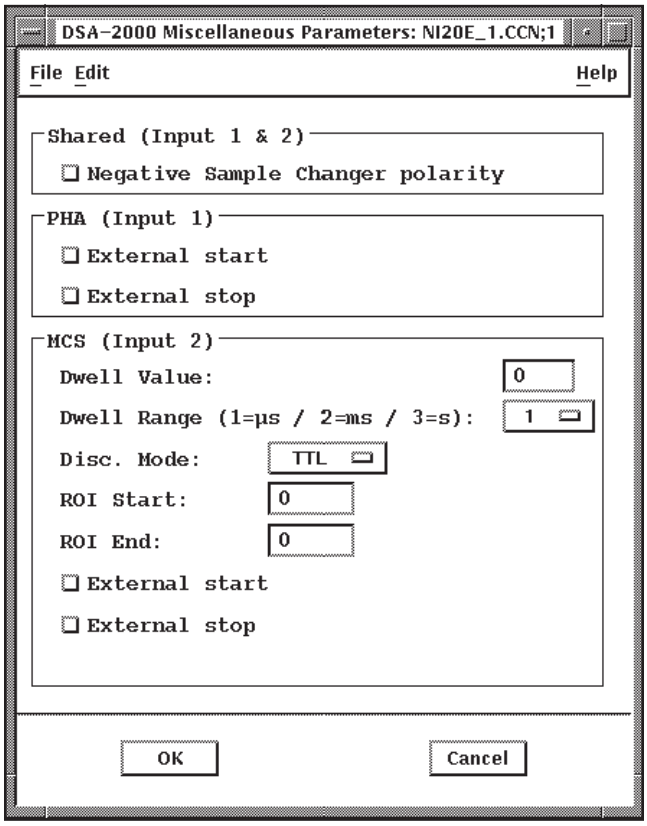


Figure 35 The VMS Miscellaneous Parameters Dialog

Creating the MCA Configuration

Once you have created the CCN file with the appropriate settings, you can create an MCA configuration. For example, the following command will create an MCA configuration DET1 on port one of DSA-2000 NIACB2:

```
$ MCA CREATE DET1 NIACB2:1/CHAN=8K
```

To create an MCA configuration DET2 on port two of DSA-2000 NIACB2:, you might type:

```
$ MCA CREATE DET2 NIACB2:2/CHAN=8K/MODE=MCS
```

5. Using the Monitor Output

The Monitor Output is provided as a visual aid to assist with parameter setup and verify operation of the Model DSA-2000 Digital Spectrum Analyzer. The Monitor Output uses a Digital to Analog Converter (DAC) to convert or reconstruct the sampled digital filtered signal (with trapezoidal weighting function) into the analog time domain for viewing.

The Monitor Output has 12 bits of resolution and an 8 volts dynamic range which reflects full scale for the selected MCA Conversion Gain. It is only intended to drive the input of an oscilloscope for viewing, as it has limited drive capability. Using the Monitor Output to drive accessories other than an oscilloscope, such as traditional ADCs, Mixer/Routers, etc. is not recommended.

In addition to the reconstructed Trapezoid signal, a small amount of digital noise may also be observed mixed in with the signal. This is an artifact of residual noise pickup associated with the monitor output reconstruction DAC and associated circuitry, and is normal. The digital filter data being processed does not contain this noise.

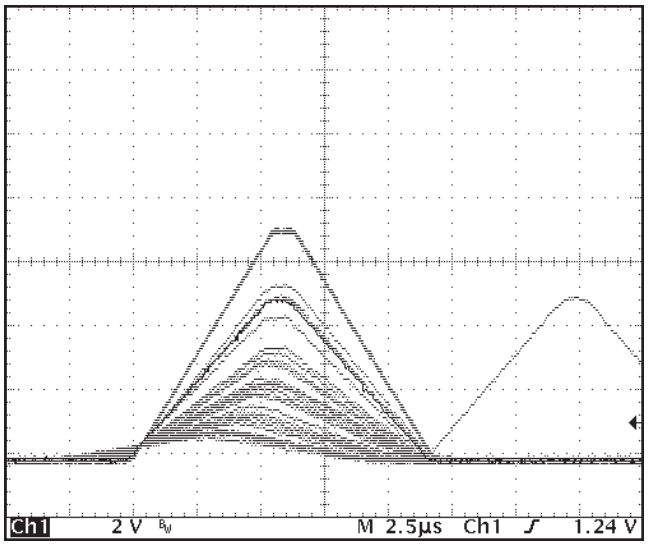
Trapezoid Output

The reconstituted trapezoid waveform provided on the monitor output is similar to the output of a traditional spectroscopy amplifier when verifying operation and setup. Figure 36 shows a typical trapezoidal waveform as viewed on the Monitor Output when using a germanium detector and ^{60}Co source, with the DSA-2000 FILTER set for a Rise Time of 5.6 µs and Flat Top of 0.8 µs.

The maximum trapezoid output level at the Monitor Output is 8 volts. However, because of the extended range of the DSA-2000's digital filter, the digital-to-analog converter which generates the monitor output can be over driven past its 12-bit range. When this happens, the monitor output will limit or clip at 8 volts or sightly above.

Offsets in the digital filter are dependent on gain selection, rise time selection and detector noise. The digital offset can become proportionately large for long rise time settings and may cause the Monitor Output DAC to be driven past its 12-bit range. When this happens, the dynamic range of the Monitor Output may reduce from its nominal 8 volt full scale range.

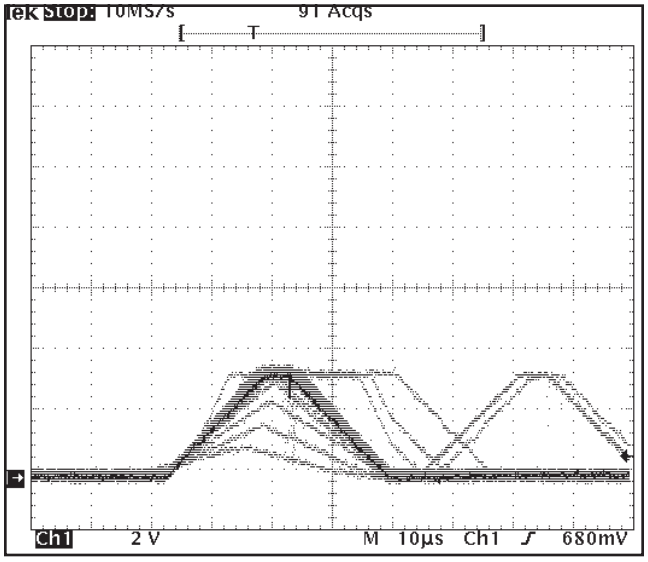
As long as the MCA memory or spectral range is not exceeded, a reduction in the Monitor Output dynamic range will not affect the MCA spectrum, since the dynamic range of the digital filter is significantly larger than that of the Monitor Output.



Scope:
Vert: 2 V/div
Horiz: 2.5 µs/div

Figure 36 A Typical Trapezoidal Monitor Output

Figure 37 shows the type of waveform generated at the Monitor Output when the DSA-2000 is connected to a detector driven by a low energy ^{55}Fe source. The Filter Rise Time and Flat Top are set relatively long, 18.4 µs and 0.4 µs respectively.



Scope:
Vert: 2 V/div
Horiz: 5 µs/div

Figure 37 Output Range Reduced by Detector Noise

This source requires a high system gain to position its peaks in the mid to upper portion of the selected MCA spectral range. For this case, the baseline or DC component of the trapezoid signal is large and signal limiting or clamping begins to occur at slightly over 3 volts. Even though the Monitor Output dynamic range appears to be significantly reduced, the Trapezoid waveform remains useful when verifying setup and optimizing the Pole/Zero.

The reduction of dynamic range is proportional to the gain setting and also to the filter rise time selection, as mentioned earlier. In the event it is troublesome, momentarily reduce the rise time or gain to a lower setting and the effect will be significantly reduced or eliminated. Verify or optimize the setup; when completed, return to the desired rise time and/or gain setting. Again, the MCA spectrum is not affected, due to the large dynamic range of the DSA-2000's digital filter.

Note The optimum Pole/Zero setting is independent of the Filter Rise Time and Flat Top setting. For further information regarding the effect of "wrap around" when setting the Pole/Zero, please refer to "Shaping – Rise Time and Flat Top Adjustments" on page 86.

Using the Monitor Output to Verify System Gain

The DSA-2000 gain settings are calibrated to produce the same system gain (in keV/channel) as a traditional analog system with the same settings. For a given detector, radiation source and MCA setup (conversion gain, conversion range, etc.), the resultant MCA spectral peaks will be located in approximately the same MCA channel location for both the DSA-2000 and the traditional analog system.

The DSA-2000 gain factor can be verified using the Monitor Output. However, keep in mind the Monitor Output signal is reconstructed in the analog time domain and is only a visual aid to assist with setup and verify operation. The Monitor Output is scaled to 8 volts full scale MCA collection as opposed to 10 volts for most traditional analog spectroscopy amplifiers. This scale factor (10/8) must be taken into consideration when verifying the DSA-2000 gain factor.

For example when the DSA-2000 Gain is set as follows:
Coarse Gain: 120
Fine Gain: x0.8337
SF Gain: $0.0000e^{-2}$

- The calculated gain is 120 x 0.8337 = 100.04
- The amplitude of the Monitor Output signal measures 4 volts
- The Input signal measures 0.05 volts.
- The DSA-2000 measured gain (corrected for the 8 volt full scale range) is 4/0.05 x 10/8 = 80 x 1.25 = 100

6. Basic Spectroscopy Operation

This chapter is a quick setup guide, and outlines the operation of the Model DSA-2000 Digital Spectrum Analyzer. More detailed information about specific functions can be found in Chapters 2 through 5, Chapter 7, and the Appendices. Following the procedures below will make you familiar enough with the instrument to be able to use it effectively.

Initialization and Self Diagnostics at Power On

When power is first applied to the Model-2000, it will go through an initialization and self diagnostics process. During this initialization period, indicated by the Power On" LED blinking, the DSA-2000 is running internal diagnostic routines to verify correct operation of the hardware. These routines require 15 to 20 seconds to complete. The front panel hardware is tested next, with the front panel LEDs and bar graph displays turning on sequentially for approximately 2 to 5 seconds. As the bar graph sequently illuminates each segment, it will pause briefly at half scale.

If the diagnostics were successful and communication with the host computer is established, the Power On LED and one of the High Voltage Range LEDs will remain on (unless otherwise programmed by the host computer, the DSA-2000 defaults to the +1.3 kV range). In addition, the Comm Tx and Comm Rx LEDs may flash indicating that communication with the host computer is taking place.

If the DSA-2000 detects a hardware or communication error with the host computer, the Fault LED will remain illuminated. This could result from a fault in the DSA-2000 hardware or a Ethernet communication problem with the network or host computer.

Spectroscopy System Setup

Figure 38 shows a typical gamma spectroscopy system.

Perform the following steps to set up your spectroscopy system:

1. If you are using a detector with a reset preamp, please refer to "Operation with Reset Preamps" on page 93 for specific instructions.

2. Connect the intended Detector/Preamp to the DSA-2000. Preamp power is provided by means of a 9-pin Amphenol connector located on the rear panel of the Model DSA-2000. Connect the Preamp Output signal to the DSA-

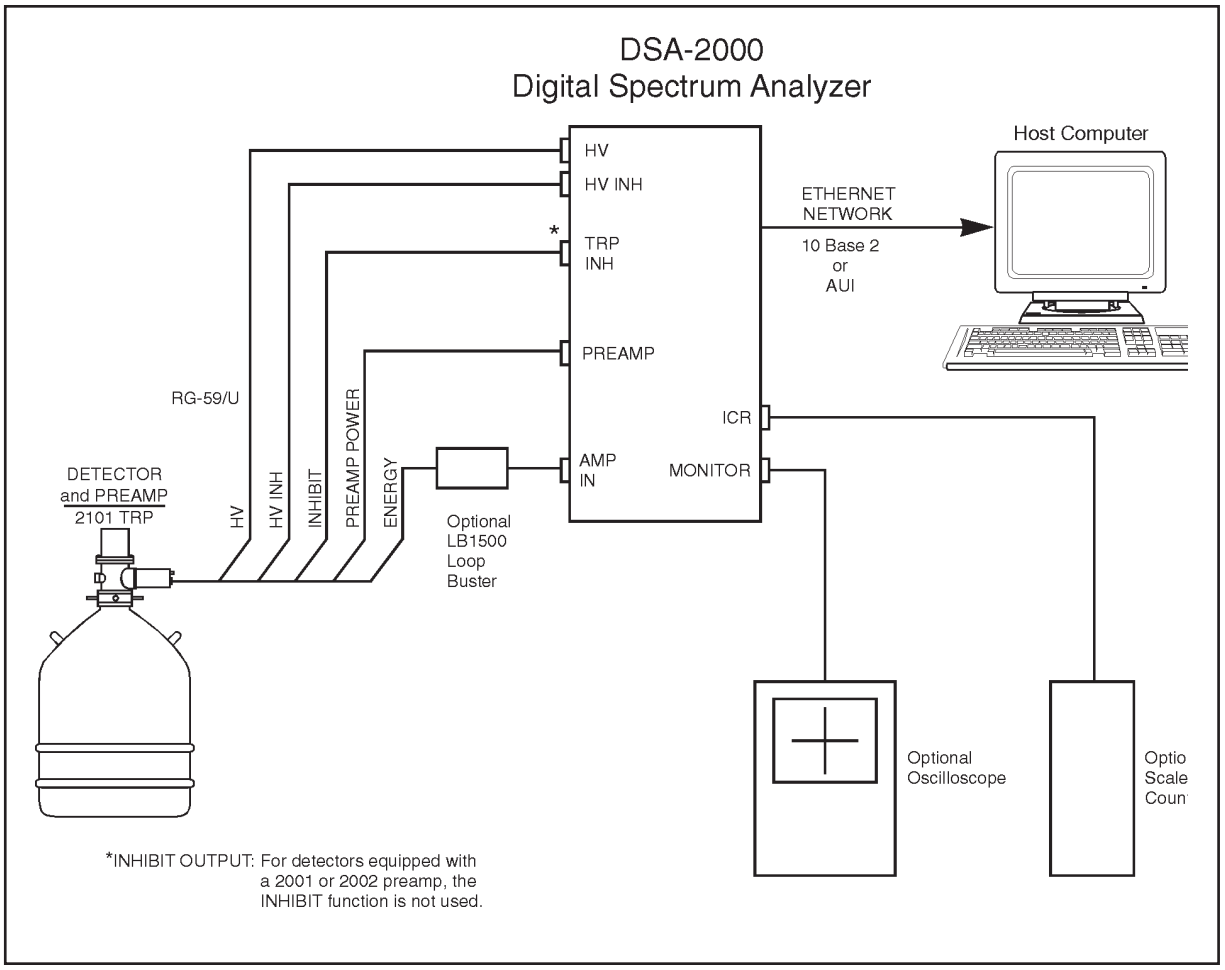


Figure 38 Typical Gamma Spectroscopy System

2000's AMP IN connector. If the detector preamp is a reset type, connect the Inhibit Output signal to the TRP INH connector on the DSA-2000's rear panel.

Note Multiple ground connections to the detector preamp (preamp power, signal BNC cable, HV power supply cable, etc.) can setup ground loops which may be sensitive to EMI noise pickup. These effects can cause resolution degradation, excessive dead time and erratic count rate (ICR) measurement.

If you experience any of these problems, make sure the preamp cables are tightly bundled together and routed away from EMI noise sources such as motors, AC switching equipment, computers, monitors, etc.

If necessary, use the optional LB1500 Loop Buster provided with the DSA-2000 in series with the preamp signal cable. The LB1500 Loop Buster reduces the sensitivity of the DSA-2000 input to ground loop induced noise. Best performance is obtained with the LB1500 installed at the energy or output BNC on the preamp.

3. Connect the Detector/Preamp High Voltage Input to the HV Output SHV connector on the DSA-2000's rear panel. The DSA-2000 provides a high quality ICB Programmable HV Power Supply.

4. Turn on the DSA-2000. At power up, the DSA-2000 will go through an initialization and self-diagnostic process as described in "Initialization and Self-Diagnostics at Power On" on page 53.

5. The setup instructions that follow will allow you to get the DSA-2000 set up and running with a typical detector and to become acquainted with its operation. For the following setup, a detector with preamp gain of 500 mV/MeV and a ^{60}Co radioactive source will produce a 6.5 to 7 volt trapezoid signal at the Monitor Output. The 1332 keV ^{60}Co peak should collect in channel 6500 to 7200 on the MCA when setup for a 8192 memory or spectrum size.

   The parameters are grouped into six device types: MCA, Sample Changer, Stabilizer, High Voltage, Gain and Filter.

   For this quick setup and check of the DSA-2000, many of the parameters may not require adjustment; leave them set to the default values. Parameters marked with an asterisk (*) indicate factory default settings.

   If the setup parameters were previously changed and saved using the MID File Save command, the host computer will down load the last value's saved.

6. MID Editor Settings. Please verify or set the following setup parameters in your Genie Spectroscopy System's MCA Input Definition (MID) Editor. For complete information on editing MID files, refer to the MID Editor chapter in your Genie manual set.

   6a. DSP Filter/Gain Settings

*Preamp Type:	RC
Inp Polarity:	Set Positive or Negative to match the preamp signal polarity of the intended detector.

Inh Polarity: If the detector has an RC type preamp, this function is not applicable and it is not necessary to make selections or changes. If the detector has a reset preamp, set Positive or Negative to match the polarity of the inhibit signal generated by the preamp. The Canberra 2101 TRP and 2008 preamps produce a positive Inhibit signal.

*Coinc mode: Anti

6b. HV Settings

Range: Sets the HV Range to match the high voltage requirements of the intended detector. The choices are +5000, +1300* and –5000.

Voltage Limit: This control limits the maximum voltage for the selected HV range, preventing accidental application of excessive voltage to the detector. Set the slider to the desired limit or maximum for the selected voltage range.

Voltage: Sets the target high voltage value; it is adjustable from 0 to the maximum voltage selected by the Range control. Set the slider to the voltage setting required for the intended detector.

INH Signal: Sets the pull-up voltage of the HV INH connector to +5 V or +12 V. All Canberra detectors and preamps use the +5 V setting.

There are many other parameters that can be adjusted in the MID Editor, but it isn't necessary to adjust them now. They will be adjusted using the MCA/Adjust Screens in the following step. When you make adjustments, be sure to save the MID File.

7. MCA/Adjust Screens. The following parameters can be accessed and set using the Gain and Filter Device Adjust screens. The adjustments can be saved to the datasource's CAM file by using the File | Save command.

7a. Gain Device Adjust Screen

Coarse Gain: x15

Fine Gain: x1.0002

S-Fine Gain: $0.0000e^{-2}$

*FDisc Mode: Auto

*FDisc Setting:	1.0%
*LT TRIM:	250
*LTC Mode:	On
*PUR Guard:	1.1x
*Offset:	0 Ch
*LLD:	0.101%
*Zero:	0.000%
*Conv Gain:	8192
*Inhibit Mode	Reset

7b. Filter Device Adjust Screen

*Rise Time:	5.6 µs
*Flat Top:	0.8 µs
Auto BDC:	Do not Initiate Auto BDC at this time
BLR Mode:	Auto
Pole/Zero:	2048
Auto P/Z	Available only on the DSA-2000A. If equipped, do not initiate Auto P/Z at this time.

Note Please see “Rise Time and Flat Top Adjustments” on page 86 for additional information on setting the Rise Time and Flat Top settings and their relationship to traditional Gaussian shaping times.

7c. Stabilizer Device Adjust Screen

*Gain Mode:	OFF
*Zero Mode:	OFF

Detector Matching

The following section discusses how to adjust and optimize the pole/zero (can be set automatically for Model DSA-2000A) and use the Auto BDC function. Pole/Zero compensation is extremely critical for achieving good performance at high count rates when using detectors with RC preamps. It is equally important for good overload recovery due to high energy and cosmic events. The Pole/Zero adjustment range accommodates RC preamp fall times of 40 µs to 1.7 ms. When a reset type of preamp is used, P/Z compensation is not required and must be set to infinity represented by a value of "0". If you are using a detector with a Reset preamp, such as the Canberra 2101 or 2008, use the MID Editor to change the preamp type from RC to TRP. With TRP selected, the Pole/Zero compensation is automatically set to a value of "0" representing infinity or no compensation. If the RC mode is selected the P/Z SETTING must be set to "0". Please refer to "Operation with Reset Preamps" on page 93 for additional information.

Note Once the Pole/Zero is optimized for the intended detector, the digital filter parameters (Rise Time and Flat Top) can be changed as required without the need to make further Pole/Zero adjustments. However, the Pole/Zero compensation *must* be readjusted if the detector is changed.

The Auto BDC function sets the trapezoid flat top to the correct length insuring that all the detector charge is collected for accurate energy analysis.

Automatic Pole/Zero Matching (DSA-2000A only)

The Automatic Pole/Zero option is installed only on the DSA-2000A. To verify the model number please check the serial number tag located on the rear panel.

The Automatic Pole/Zero (P/Z) feature will give good results for most detector applications and count rates. However, it may be necessary to optimize the P/Z compensation manually at extremely high count rates or for specific applications where the digitally filtered trapezoid signal is prevented from returning monotonically to the baseline. The feedback resistor on some RC preamps may exhibit non-ideal characteristics which produce multiple time constants making the tail pulse fall time non-monotonic. This behavior may become problematic at high count rates causing significant baseline perturbations and resolution degradation. NaI detectors may have multiple time constants due to AC coupled preamps and the scintillator interactions. In these situations it might be possible to minimize performance degradation by fine tuning the pole/zero manually. To adjust the Pole/Zero manually, refer to "Manual Pole/Zero Matching" on page 61.

To initiate the Auto Pole/Zero process, please follow the directions below:

1. Adjust the ^{60}Co radioactive source for an incoming count rate (ICR) between 1 and 20 kHz. The Auto Pole/Zero may fail to converge if the incoming count rate is not within this count rate range. The incoming count rate can be verified by looking at ICR on the **MCA | Adjust | Status Page** of the Acquisition and Analysis window. Select "Update" to update the ICR Status whenever the radioactive source is adjusted. The incoming count rate can also be determined by connecting a scaler to the ICR connector on the DSA's rear panel.

Note Although any radioactive source may be used, the most accurate adjustment is obtained using simple sources such as ^{57}Co, ^{137}Cs or ^{60}Co. The Auto P/Z operates properly with spectral peaks are located within 25% to 100% of the system dynamic range. However best performance is obtained with the system gain adjusted to place the primary peaks within the top 75% to 95% of the system dynamic range. These recommendations also apply when adjusting the Pole/Zero manually on systems without Auto Pole/Zero. Once completed, replace the calibration source with the sample to be analyzed and adjust the system gain as required.

2. In the **MCA | Adjus**t screen, click on the **FILTER** button, then click on the **Next** button until the Adjust screen with the Auto P/Z button appears.

3. Click the AUTO P/Z "Start" button, to start the Auto Pole/Zero. While the pole/zero is converging, "Wait" will be posted in the Adjust screen's Status box.

   The pole/zero value can be viewed on the Filter Device Adjust screen under "Pole/Zero" or on the Status Page. The pole/zero value must be updated each time an Auto P/Z is performed or when the slider bar is changed. To update the pole/zero value momentarily switch the Device Adjust screens by clicking on the Stab button or the Gain button, then back to the Filter Device Adjust screen.

   When a successful auto pole/zero has been done, the new pole/zero value can be verified as indicated in step 3 above. If the pole/zero was unsuccessful, an error message will be posted in the error dialog box.

4. Unsuccessful Pole/Zero and Error Messages

   If the Auto Pole/Zero operations fails to converge when initiated one of the following messages will be displayed in the error dialog box to provide diagnostic information regarding the problem. The error message can be cleared by clicking on Ok in the error dialog box.

a. Pole/zero not possible with TRP

You have attempted to initiate an Auto P/Z operation with the Genie environment and hardware configured for a TRP detector; that is, a detector fitted with a reset type preamp. The Auto P/Z function is disabled when a TRP preamp is selected. If you are using a detector with an RC preamp, please go to the MID Editor and set the Preamp Type to “RC”.

b. Pole/zero failed to converge

This message may result from any of the following reasons:

P/Z Time Out Error – The Auto P/Z has failed to complete within a maximum time of two minutes. The preamp fall time could be outside the 40 µs to 1.7 ms pole/zero adjustment range or the incoming count rate (ICR) is below 1 kHz. The Auto Pole/Zero will not converge properly if the ICR is less than 1 kHz. Additional causes may be excessive noise or abnormal variations of the Trapezoid baseline. This could result from excessive detector microphonics, high voltage arcing in the detector or preamp, secondary preamp signal time constants or a damaged detector. For those cases, P/Z compensation must be performed manually. Please refer to “Manual Pole/Zero Matching” on page 61.

The Incoming Count Rate is Too High – The incoming count rate (ICR) exceeds 20 kHz. The Auto Pole/Zero will not converge properly if the ICR exceeds 20 kHz. For this condition, the error message will be posted very quickly; long before the two minute time out.

5. Pole/Zero Value

The four-digit value, located under the pole/zero slider bar, is a reference number which varies from 0 to 4095 representing the pole/zero adjustment range. The values 1 to 4095 represents a time constant range of 1.7 ms to 40 µs. The value “0” can only be set manually; this setting is for no compensation which represents infinity required for Reset type preamps.

The Pole/Zero value for successive Auto Pole/Zero initiations may vary slightly. This is normal and results from statistical variation associated with the algorithm and system baseline noise.

If Reset Mode was selected, the four digit value will be set to “0”, which is required for proper operation with reset-type preamps.

6. Manual Fine Tuning Using the Pole/Zero Slider Bar

With the RC Pole/Zero Mode selected, the Pole/Zero may be adjusted manually or the Pole/Zero compensation value, resulting from the automatic operation, may be trimmed by adjusting the associated slider bar on the Filter Device Adjust screen. This operation permanently overwrites the Auto value and may be used to fine tune the Pole/Zero setting to optimize performance at high rates. For additional discussion on manual Pole/Zero adjustment, refer to “Manual Pole/Zero Matching” on page 61.

7. Verifying Pole/Zero Accuracy

The precision of the Auto P/Z operation can be verified by observing the reconstructed Trapezoid signal on the Monitor Output. Observe the trailing edge of the Trapezoid signal as it returns to the baseline, it should return with no over or undershoot. Set the oscilloscope vertical range to an appropriate sensitivity. Use a Canberra Schottky Clamp Box, Model 1502 or equivalent to prevent oscilloscope overload.

For additional discussion on Pole/Zero verification and manual adjustment, refer to “Manual Pole/Zero Matching” on page 61.

Manual Pole/Zero Matching

At high count rates, the Pole/Zero (P/Z) matching adjustment is extremely critical for maintaining good resolution and low peak shift. For a precise and optimum setting of the P/Z matching, a scope vertical sensitivity of 50 mV/div should be used.

With correct P/Z, spectral peaks will appear symmetrical; while under compensated P/Z will produce low energy tailing. Over compensated P/Z will produce high energy tailing. An example of each condition is shown in Figure 39.

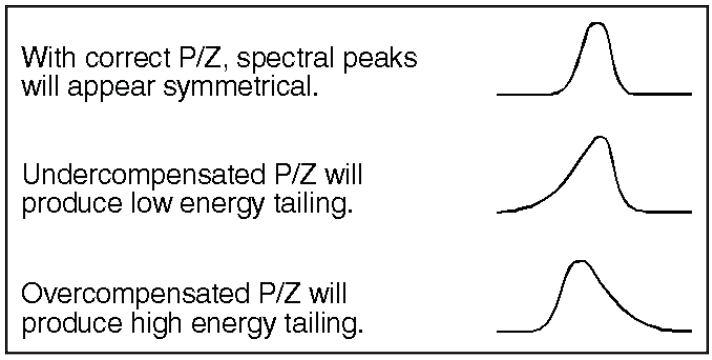


Figure 39 Examples of Pole/Zero Compensation

Higher mV/div scope settings (sensitivity) can also be used, but this will result in a less precise P/Z matching adjustment. Most scopes will overload for a 10 V input signal and will exhibit overload aftereffects when the signal returns to the baseline. Thus the P/Z matching will be incorrectly adjusted resulting in a loss of resolution at high count rates.

To prevent scope overload and increase the P/Z matching accuracy, a clamping circuit such as the Canberra Model LB1502 Schottky Clamp Box should be connected at the scope input.

For additional information and techniques for adjusting pole/zero, refer to “P/Z Matching Using a Square Wave Generator” on page 89.

P/Z Matching Using a Ge Detector and ^{60}Co

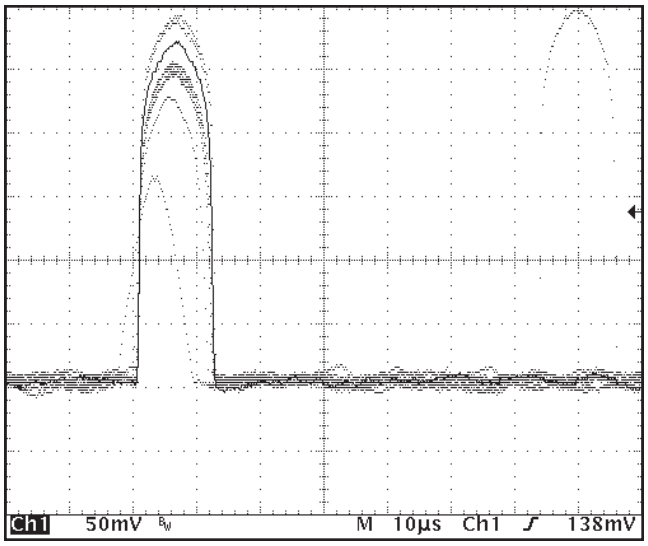
1. Adjust the radiation source count rate to be between 2 kcps and 20 kcps. Observe the trapezoidal waveform on the monitor output.

2. Verify that the preamp type in the filter device MID editor is set to “RC”. Adjust the Pole/Zero slider bar, located in the Filter Device Adjust screen, so that the trailing edge of the trapezoid pulse returns to the baseline with no overshoots or undershoots.

Figure 40 shows the correct setting of the P/Z adjustment, while Figures 41 and 42 show under- and over-compensation for the preamplifier decay time constant. As illustrated for correct P/Z compensation, the monitor output signal should have a clean return to the baseline with no bumps, overshoots or undershoots.

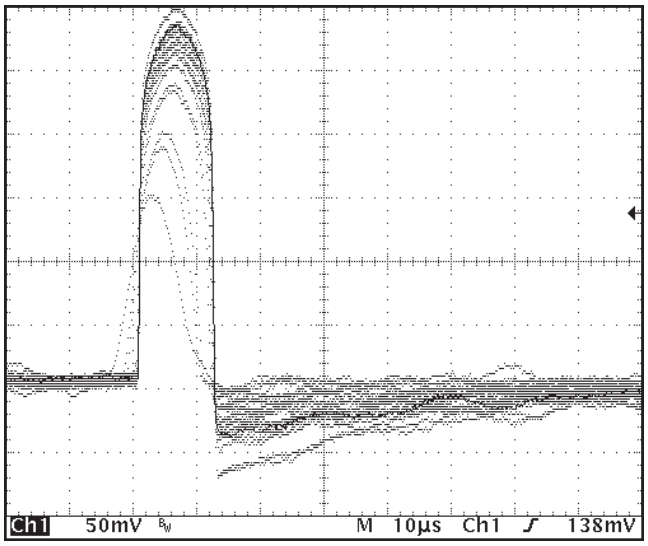
Note Some systems may exhibit small undershoots when the monitor output returns to baseline. These arise primarily from secondary time constants associated with the detector/preamp system. If an undershoot is present and is less than 20 mV, its impact on performance is insignificant. However, if small shaping undershoots are present, they should not be confused with undershoots caused by preamp matching misadjustment, which exhibit a much longer time constant and have a larger performance impact.

At high count rates, P/Z matching misadjustment will affect spectral peak shape and resolution.



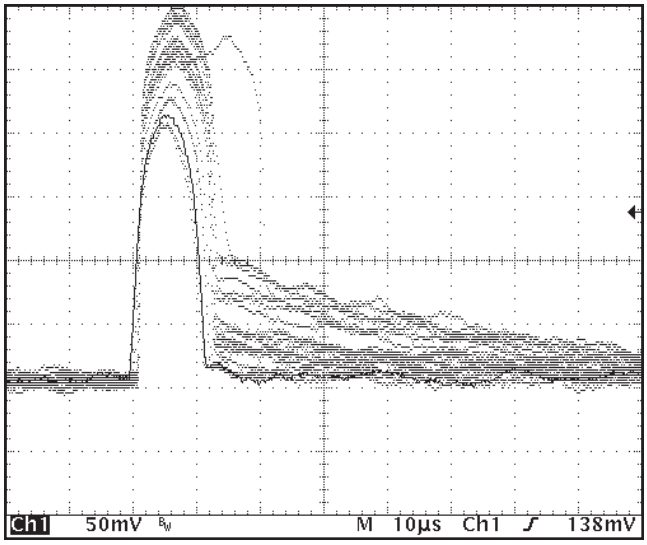
Scope:
Vert: 50 mV/div
Horiz: 10 µs/div
Source: ^{60}Co
1.33 MeV peak at 6 V amplitude
Count rate: 2 kcps
Shaping: 5.6 µs rise time, 0.8 µs flat top

Figure 40 Correct Pole/Zero Compensation



Scope:
Vert: 50 mV/div
Horiz: 10 µs/div
Source: ^{60}Co
1.33 MeV peak at 6 V amplitude
Count rate: 2 kcps
Shaping: 5.6 µs rise time, 0.8 µs flat top

Figure 41 Undercompensated Pole/Zero



Scope:
Vert: 50 mV/div
Horiz: 10 µs/div
Source: ^{60}Co
1.33 MeV peak at 6 V amplitude
Count rate: 2 kcps
Shaping: 5.6 µs rise time, 0.8 µs flat top

Figure 42 Overcompensated Pole/Zero

Automatic Ballistic Deficit Correction

In order to optimize performance with detectors of different sizes and varying charge collection times, the DSA-2000 and DSA-2000A includes Automatic Ballistic Deficit Correction (BDC). Ballistic deficit occurs when the signal from a detector is passed through a filter whose shaping time is too short. When this happens, the filter is unable to completely process all of the charge collected by the associated detector/preamplifier. This can cause a “deficit” in the pulse height value which does not accurately represent the energy of the event. Because the collection time of a detector can vary from one pulse to the next, ballistic deficit may lead to loss of resolution and distortion of the MCA energy peak shape. The effect becomes more pronounced with large detectors and high energies.

Low energy tailing often indicates the presence of ballistic deficit. For traditional analog signal processing, users are forced to manually inspect the peak shape of the MCA energy spectrum and optimize the shaping time selection. For detectors that exhibit ballistic deficit, the shaping time is often increased to improve resolution, but at the expense of throughput. The Trapezoidal shaping function employed in the DSA-2000 allows independent adjustment of the Rise/Fall time and Flat Top. The Rise/Fall time sets the noise filtering characteristics and the Flat Top adds sufficient time for the charge to be collected and integrated. As a result, the ballistic deficit effects can be minimized by adjusting the Flat Top time without burdening the Rise/Fall time. This results in a overall shorter processing time and higher throughput compared to Gaussian shaping and traditional analog signal processing.

Optimizing the Flat Top on the DSA-2000 is automatic and easy; manual adjustment is *not* necessary. Automatic adjustment of the Flat Top time is performed by initiating the Auto BDC (Ballistic Deficit Correction) function. A sophisticated algorithm measures the detector pulses, determines the range of detector rise times, and sets the digital filter trapezoid flat top for full charge integration. After the DSA-2000 has adjusted the flat top, variations in detector rise time will not affect the output.

The instructions presented below assume the DSA-2000 is set up as outlined in "Spectroscopy System Setup" on page 53. The BDC does not change the Rise Time setting; use the 5.6 µs default value or set as desired. For additional information on setting the Rise Time and Flat Top please refer to Appendix B, "Performance Adjustments".

To initiate the Auto BDC process, perform the following steps:

1. Adjust the ^{60}Co radioactive source for an incoming count rate (ICR) between 1 and 20 kHz. The Auto BDC may fail to converge if the incoming count rate is not within this count rate range. The ICR can be verified by viewing the Status Page. Select **MCA | Adjust | Status** from the Acquisition and Analysis window, then "Update" to update the ICR status whenever the radioactive source is adjusted.

Note Although any radioactive source may be used, the most accurate adjustment is obtained using simple sources such as ^{57}Co, ^{137}Cs or ^{60}Co. The Auto BDC operates properly with spectral peaks located within 25% to 100% of the system dynamic range. However, best performance is obtained with the system gain adjusted to place the primary peaks within the top 75% to 95% of the system dynamic range. Once the Auto BDC has completed, replace the calibration source with the sample to be analyzed and adjust the system gain as required.

2. Initiating Auto BDC:

   Note: The Gain and Pole/Zero should be set prior to initiating the Auto BDC function.

   Select the Filter Device Adjust screen (under the MCA | Adjust menu) and press the AUTO BDC "Start" button. The BDC BUSY LED will illuminate for the duration of the process. During this time, normal operation of the DSA-2000 is suspended while detector rise time data is being acquired.

Note Spectral data acquired during the Auto BDC process may be corrupted and should be discarded or cleared when the auto BDC Process has completed.

Upon completing a successful BDC and setting of the Trapezoid Flat Top, the BDC BUSY LED will turn off. Verify the new Flat Top setting. The Filter Device screen must be updated to show the new value, momentarily switch the Device Adjust screens by clicking on the Stab or Gain button, then back to the Filter Device Adjust screen.

3. Unsuccessful BDC and Error Messages

   If the Auto BDC operation fails to complete after initiation, the BDC BUSY LED will turn off and the message "General SAD error" will be posted in the error dialog box. Click on the **Ok** button to clear the message.

   The BDC operation could have failed for one of the following reasons:

   a. **BDC Time Out Error** – The Auto BDC has failed to complete within a maximum time of five minutes. This may result if the detector/preamp signal is not connected or the incoming count rate (ICR) is below 1 kHz. Additional causes may be excessive noise or abnormal variations of the Trapezoid baseline. This could result from excessive detector microphonics, high voltage arching in the detector or preamp, secondary preamp signal time constants or a damaged detector. For this case, the Flat Top may be set manually; select FLAT TOP under the Filter parameter group.

   b. **Incoming Count Rate Too High** – The incoming count rate (ICR) exceeds 20 kHz. The Auto BDC will not operate properly if the ICR exceeds 20 kHz. For this condition, the error message will be posted very quickly, long before the time out occurs.

Acquiring a Spectrum

Please refer to the *Genie-2000 Operations Manual* for specific operating instructions.

Place a low activity ^{60}Co source on the detector. Set the MCA to COLLECT or ACQUIRE. For the DSA-2000 setup performed in "Spectroscopy System Setup" on page 53, the 1332 keV ^{60}Co peak should collect in channel 6500 to 7200 for a detector preamp gain of 500 mV/MeV and 8192 memory or spectrum size.

Adjust the DSA-2000's gain to position the ^{60}Co peaks to the desired MCA spectral location. The Super Fine Gain (SFG) control provides 100 times more resolution than the Fine Gain. Use the SFG when matching the gains of several detectors or when establishing a specific gain calibration (energy per channel).

7. PUR/LTC Operation

The Model DSA-2000 Digital Spectrum Analyzer includes a pileup rejector and live time corrector. The pile up rejector inspects for pulse pileup and allows only non-piled up events to be processed and stored into the spectrum. The result is a reduced number of counts in the pileup region and reduced spectral interference for improved quantitative measurement and analysis.

To compensate for dead times associated with rejected pulses and amplifier processing times, the Model DSA-2000 generates a dead time (DT) signal which extends the collection time by the appropriate amount.

Pileup Rejection With a Live Source

The pileup rejector monitors the signal processing activities of the fast discriminator (fast channel) and digital filtered signal (slow channel) and allows only signals resulting from a single detector event to be processed and stored in the spectrum. The fast discriminator detects the arrival of input events and is capable of discriminating between multiple events separated by less than 500 ns. If the fast discriminator detects two or more events within the processing time of the slow channel, the event is contaminated by pileup and is discarded.

The fast discriminator threshold is automatically adjusted just above the system noise level for accurate operation. However, for the discriminating researcher or special circumstances the threshold can be optimized manually. For instructions on adjusting the threshold manually, see “Manual Fast Discriminator Threshold” on page 92.

The following steps will demonstrate the operation of the Pileup Rejector and its ability to reduce spectral interference.

1. Connect the Model DSA-2000 and set it up as described in “Spectroscopy System Setup” on page 53.

2. For the following demonstration of the Pileup Rejector, a ^{57}Co source will be used. Due to the lower energy of this source, the system gain will need to be increased; set the gain as follows:

   Coarse Gain: x40
   Fine Gain: x1.6000
   SF Gain: 0.0000e^{-2}

Leave the remaining functions as previously setup. Verify that the LTC mode is set on; the function is located on the Gain Device Adjust screen.

Note The pile up rejector (PUR) and Live time corrector (LTC) operate as an integral system. The LTC On/Off function controls both the PUR and the LTC.

3. Pole/Zero Compensation

   The Pole/Zero was previously adjusted and it should not be necessary to do it again. If for some reason readjustment is necessary, please follow the directions in “Detector Matching” on page 58.

4. Adjust the DSA-2000 Gain to locate the 122 keV ^{57}Co peak in channel 3500. This is to allow the Pileup region and sum peaks to be viewed in the upper half of the spectrum.

5. Readjust the ^{57}Co incoming count rate (ICR) for 50 kcps.

6. Set the MCA preset to 60 seconds Live Time.

7. Set the MCA acquire to OFF, clear the memory and set acquire to ON. Accumulate a spectrum with the LTC ON.

8. Save the spectral file or print the spectrum or make note of the background counts and sum peaks for comparison with the LTC set OFF.

9. Set the LTC to OFF, clear the memory and set acquire to ON. Accumulate a spectrum with the LTC OFF.

10. Compare the two spectra, LTC On and LTC Off, overlapping them with the compare function, as seen in Figure 43.

The spectra shown in the comparison are for an ICR of 50 kcps and 4 µs Gaussian Equivalent Processing Time (Rise Time: 5.6 µs and Flat Top: 0.8 µs). Note the reduction in magnitude of both the sum peaks and background counts. Also note the improved resolution of the sum peaks. The background reduction and improved resolution are directly indicative of the Pileup Rejector’s capabilities, since only sum peak pulses which are indeed 100% in coincidence are processed.

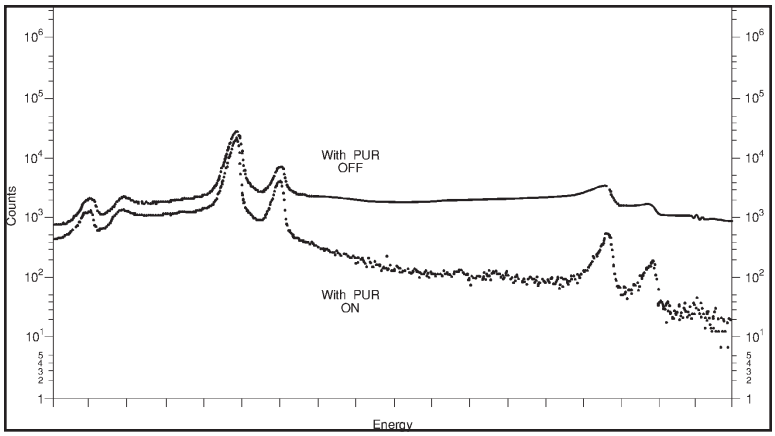


Figure 43 Comparing ^{57}Co Spectra with PUR On and Off

Live Time Correction With a Live Source

To compensate for events rejected due to pile-up and processing time, a system dead time is derived by the live-time correction function. The dead time signal controls the MCA “Live-Time” clock which extends the acquisition time by the appropriate amount.

The accuracy of the Live Time Correction (LTC) deployed on both traditional analog electronic and the DSA-2000 Digital Spectrum Analyzer is dependent on the operation of the Fast Discriminator (fast channel) and the pulse evolution time or dead time of the shaped signal (slow channel). In the case of the DSA-2000, the slow channel is the digital filtered trapezoid signal. Accurate Live Time Correction is obtained when the energy threshold and dynamic range of the fast channel and slow channel are the same. In practice however, the energy threshold of the fast channel is forced to be much higher compared to the slow channel. In order to obtain good pulse pair or timing resolution, the fast channel employs little or no noise filtering. As a result, the signal to noise ratio is much worse, requiring a higher energy/noise threshold.

To optimize the LTC accuracy on traditional systems, the ADC LLD is adjusted or optimized to normalize the energy threshold of the slow and fast channels. However, this has the undesirable effect of affecting the spectral low energy cutoff.

On the DSA-2000, the “LT Trim” function allows minor adjustment of the pulse evolution time or dead time of the digital trapezoid signal to normalize the fast and slow channel energy thresholds without affecting the spectral low energy cutoff threshold.

The LT Trim has an adjustment value of 0 to 1000 and the default value is 250, which gives good Live Time correction performance for most applications. In the steps that follow, Live Time Correction accuracy is measured using the "two source method" which monitors the area of a reference spectral peak when subjected to varying rates of background counts.

Typical LTC performance (reference peak area variation) using the default LT Trim setting is typically less than 3% for dead times of 50%. The discriminating user can improve performance further, for the intended application, by calibrating the system using the "Two Source Method" and optimizing performance using the LT Trim.

The following steps are designed to demonstrate and verify the effectiveness of the Live Time Correction function. The verification/optimization process uses the "Two Source Method" which assumes that source "A" is ^{60}Co and source "B" is ^{137}Cs. The 1173.2 keV peak of ^{60}Co will be used as a reference. The upper peak, at 1332.5 keV, is not a good choice because the sum peak of ^{137}Cs at 2 x 661.6 = 1323.2 keV would interfere with the measurement.

1. Connect and set up the Model DSA-2000 as described in "Spectroscopy System Setup" on page 53.

2. Verify LTC is set ON.

3. Pole/Zero Compensation

   The Pole/Zero was previously adjusted and it should not be necessary to do it again. If for some reason readjustment is necessary, please follow the directions in "Detector Matching" on page 58.

4. Set the MCA's preset to 500 Live seconds.

5. Position the ^{60}Co source near the Ge detector and adjust for an incoming count rate of 2 to 5 kcps. The 1173.2 keV ^{60}Co reference peak should be at approximately 80% of the spectral full scale range. If necessary, adjust the DSA-2000 gain to properly locate the peak.

Note Once in place, the source should not be moved or altered in any way for the remainder of the experiment!

6. Clear the MCA and acquire a spectrum for 500 live seconds. Record the net area of the 1173.2 keV ^{60}Co peak (source "A").

7. To the ^{60}Co source, add approximately 25 kcps of ^{137}Cs to make the total incoming rate 30 kcps.

8. Clear the MCA, Collect a new spectrum for 500 live seconds, and record the net area of source “A”.

9. Compare the net area of the 1173.2 keV ^{60}Co peak acquired in step 6 and compute the percentage change.

10. If improvement is needed, try adjusting the LT TRIM slightly and repeat steps 6 through 9 until an optimum setting is achieved. The LT Trim function is located on the Gain Device Adjust screen. The value can be decremented/incremented over a range of 0 to 1000 using the adjust slide bar (the default setting is 250).

Since the detector-source geometry was maintained and the preset Live Collection time was held constant, the ^{60}Co (1173.2 keV) net area can be used as a standard when comparing the effect of adding background counts Cs^{137} (661 keV).

Note Lowering the LT Trim value will increase the system dead time and counts in the reference peak area at high count rates.

11. Set the LTC ON/OFF switch to Off. Repeat steps 4 through 9. Compare the deviation of source “A’s” spectrum when the LTC is ON and the LTC is OFF.

With the LTC OFF, large changes will be observed in the reference net peak are as a function of count rate. With the LTC set ON, changes in the reference peak net area will be significantly reduced. The Live Time corrector extends the collection time compensating for signal processing time and events rejected due to pileup.

Note Performance may vary and is dependent on factors such as spectrum energy distribution, detector characteristics such as geometry, size, and detector ballistic deficit.

PUR Guard

The PUR Guard Time (GT) function is provided to optimize the performance of the Pileup Rejector. The pile up reject interval is defined as GT x T_R+$T_{Flat\ Top}$ where:

GT = PUR Guard Time selection; 8 selections ranging from 1.1 to 2.5 are provided

T_R = Filter Rise Time selection

$T_{Flat\ Top}$ = Filter Flat Top selection

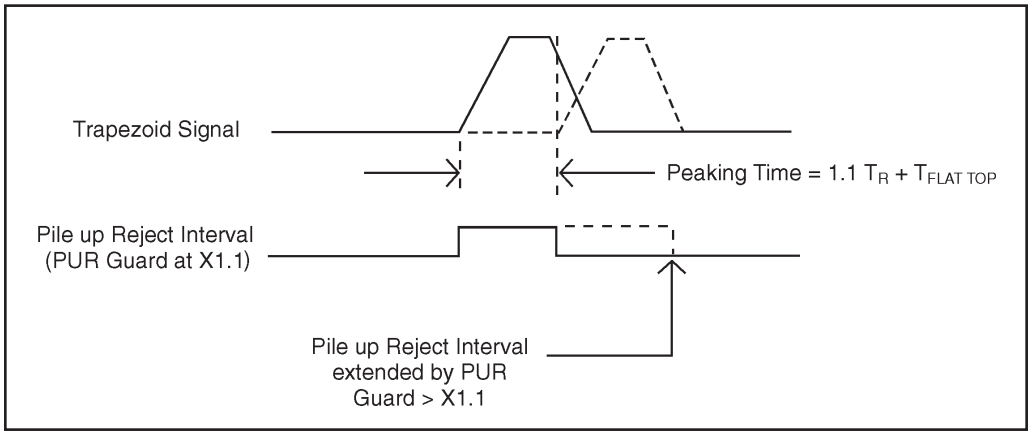


Figure 44 The PUR Reject Interval

With the default (minimum) PUR GT setting (1.1x) the pile up reject interval and the Peaking Time are the same; see Figure 44.

Subsequent events arriving within the PUR reject interval are rejected, events occurring afterwards are accepted. Increasing the Guard Time extends the pile up rejection interval to protect subsequent events from being corrupted by anomalies associated with the tail of the previous event. As expected, throughput is reduced as the Guard time and pile up rejection interval are increased. The maximum Guard Time setting (2.5x) requires the previous event to fully return to the baseline before subsequent events are accepted. The default Guard Time (1.1x) is minimum and provides optimum performance and maximum throughput for most detector applications.

For the example shown above, the second event begins before the first returns to the baseline. This is not normally a problem and the second event should be accepted for maximum throughput. However, if the tail of the first event exhibited detector-induced anomalies, the second event would be corrupted and should not be accepted. To prevent acceptance of this corrupted event, the PUR Guard should be increased as shown.

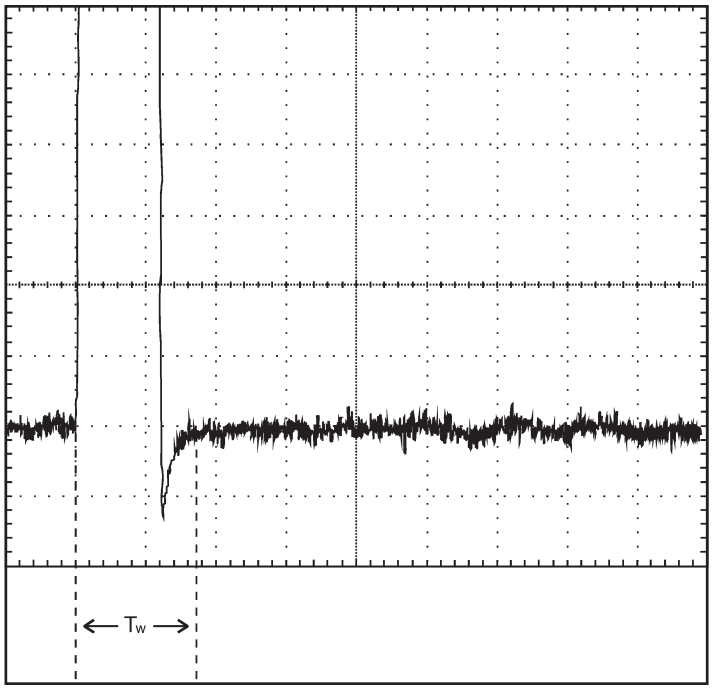


Figure 45 Preamplifier Secondary Time Constant

Some detectors with RC preamps may exhibit secondary time constants which is evidenced by a short lived undershoot or ring on the trailing edge of the shaped signal (see Figure 45).

This behavior is usually due to non-ideal characteristics of the preamp feedback resistor. Events that fall on the tail of an event which exhibits this behavior will become corrupted or distorted when minimal guard time is selected. In this case, the spectral peaks will be distorted with excessive high or low side tailing at high count rates. Events that arrive too close and are corrupted by the tail of the previous pulse can be rejected by increasing the Guard Time. For problematic detectors this will reduce spectral distortion at high count rates, but at the expense of reduced throughput.

PUR Guard Setup

The default PUR Guard Time is 1.1x. This Guard Time is minimum and does not extend the pile up rejection interval beyond the peaking time. For events that exhibit secondary time constants or other anomalies, measure the pulse width from the leading edge to where it returns to the baseline and becomes stable. This is shown as time T_W in Figure 45. The required guard time is determined by dividing T_W by the Peaking Time ($1.1T_R + T_{Flat\ Top}$).

For example:

- The filter rise time is set to 5.6 µs and the flat top is set to 0.8 µs.
- The Peaking Time is: 1.1 x 5.6 µs + 0.8 µs = 7.0 µs. T_w for a stable baseline is 15.0 µs.
- The desired guard time setting is: T_w/Peaking Time = 15.0/7.0 = 2.1

If the calculated guard time falls in between available selections, set the PUR Guard for the next higher setting. The pileup rejection interval will now be extended beyond the peaking time. Subsequent events that occur within the pileup reject interval of 15 µs will be rejected. After this instance, the anomaly associated with the tail of the previous pulse is over and subsequent events can be accepted. As noted earlier, extending the PUR interval by adding Guard Time will degrade throughput. Highest throughput is obtained with the PUR Guard set for minimum; x=1.1.

The PUR Guard adjust function is located on the Gain Device Adjust screen. The value can be decremented/incremented using the adjust slide bar. The adjust range is 1.1x to 2.5x (the default setting is 1.1x).

PUR Guard Adjustment Using a Live Spectrum

As mentioned earlier, detector/preamplifier induced effects on the trailing edge of the shaped signal will cause spectral distortion; low or high side tailing.

At moderate to high count rates, observe the shape of the spectral peaks. They should appear symmetrical. Low or high side tailing may indicate the presence of preamplifier-induced effects corrupting the trailing edge of the shaped signal. This could also be due to a misadjusted pole/zero. Verify the Pole/Zero is correctly optimized (refer to “Detector Matching” on page 58 or Appendix B, “Performance Adjustments”.

If the Pole/Zero is not the problem, set the PUR Guard to 2.5x and acquire a new spectrum. If the symmetry of spectral peaks improves, this affirms that trailing edge pileup effects associated with the shaped signal are responsible. Reduce the PUR Guard time to the next lower setting of 2.3x and re-acquire a spectrum. If the symmetry and FWHM of the spectral peaks remain good, reduce the PUR Guard time again to the next lower setting. Repeat this procedure until spectral distortion begins to reappears, then set the PUR Guard time to the next higher setting.

A. Specifications

Inputs

AMP IN – Accepts positive or negative signals from an associated detector preamplifier; amplitude ±10 V divided by the selected gain, ±12 V maximum; rise time: less than the selected flat top time setting; decay time constant: 40 µs to infinity; Z_{in} varies with Coarse Gain and Polarity settings from 500 to 2 kΩ.

GATE – Accepts a logic pulse or dc level; high amplitude ≥+2.5 V; low amplitude ≤+400 mV, 0 to +7 V maximum; dc coupled; open input allows PHA operation; loading is 1 kΩ to +5 V with Coincidence selected and 1 kΩ to 0 V with Anticoincidence selected; minimum pulse width 50 ns. In COINC (ANTIcoincidence) mode a positive logic pulse or dc level during the rise time and flat top of the trapezoidal waveform will enable (disable) the conversion in process; if the GATE is low during this time the impending conversion will be disabled (enabled). The reconstructed trapezoidal waveform can be seen at the MONITOR output.

TRP INH – Accepts a standard TTL logic signal; functionality is dependent on which Inhibit Mode is selected. NORM selected: resets and inhibits the pileup rejector and extends the Dead Time signal for the duration of the INH signal. RESET preamp selected: inhibits the DSA-2000 during the preamplifier reset cycle, the leading edge of the INH signal resets the pileup rejector and allows the DSA-2000 to automatically disable pulse processing and extend the system dead time for the duration of the resultant overload event. The total inhibit time is the OR of the external INH signal and the DSA-2000's reset disable time, whichever is longer. Positive true or negative true signal polarities, user selectable; minimum pulse width is 1 µs; loading 4.7 kΩ; logic high ≥+3.6 V, logic low ≤+1 V; 0 to +12 V maximum; rear panel BNC connector.

HV INH – Logic low or ground inhibits the HV output; max logic low ≤0.7 V; logic high ≥2.0 V or open circuit enables; loading: 4.7 kΩ pull-up resistor to +5 or +12 V, pull-up voltage is computer selectable.

MCS IN – MCS counts input; HCT compatible; logic low ≤+0.9 V, logic high ≥+3.2 V, minimum pulse width ≥10 ns, maximum rate ≥50 MHz.

PHA S/S – Input starts and stops PHA acquisition, acquisition time determined by the arrival time of two sequential pulses; start and stop are negative edge triggered; TTL compatible; 10 kΩ pull-up resistor to +5 volts, logic low ≤+0.8 V, logic high ≥+2.0 V; minimum pulse width ≥10 ns.

MCS S/S – Input starts and stops MCS acquisition, acquisition time determined by the arrival time of two sequential pulses; start and stop are negative edge triggered; TTL compatible; 10 kΩ pull-up resistor to +5 V, logic low ≤+0.8 V, logic high ≥+2.0 V; minimum pulse width ≥10 ns.

RDY – Sample changer ready input; holds off acquisition until the sample changer mechanism signals that the sample is in the proper position; level-triggered computer-selectable polarity. TTL compatible; 10 kΩ resistor to ground; logic low ≤+0.8 V, logic high ≥+2.0 V.

DIAGNOSTIC – Diagnostic port; RS-232; rear panel 9-pin male, D-connector.

Outputs

MONITOR – Provides viewing of sampled data, reconstructed in time, as a user aid to assist with setup; digitally filtered Trapezoidal/Triangular pulse; amplitude linear to +8 V; 8 V max; Z_{out} ≈50 Ω; short circuit protected; front panel BNC connector.

ICR – ICR (Incoming Count Rate) provides a standard TTL logic signal; frequency corresponds to input count rate; positive true; width ≈150 ns, Z_{out} ≈50 Ω; rear panel BNC connector.

HV – High voltage output; programmable range and polarity; ±5000 V dc with 100 µA output current capability or +1300 V dc with 500 µA output current capability; resolution of 1 part in 4096; rear panel SHV connector isolated from chassis ground by 47 Ω resistor and parallel 33 µH choke.

MSP – Most Significant Pulser: logic signal used to control high amplitude pulse from associated precision dual amplitude pulser; computer selectable rates of 50 Hz, 100 Hz, 500 Hz and 1 kHz; edge triggered, trigger edge dependent on detector's high voltage polarity; HC output through 33 Ω series resistor. Note: detector must be equipped with Canberra precision dual amplitude pulser.

LSP – Least Significant Pulser: HC compatible logic signal used to control low amplitude pulse from associated precision dual amplitude pulser; computer selectable rates of 50 Hz, 100 Hz, 500 Hz and 1 kHz; edge triggered, trigger edge dependent on detector's high voltage polarity; HC output through 33 Ω series resistor. Note: detector must be equipped with Canberra precision dual amplitude pulser.

10 Base 2 – Thin wire Ethernet; rear panel BNC.

AUI – Ethernet AUI; rear panel 15-pin, female D-connector.

ADV – Sample changer advance, logic signal which enables external sample changer movement; polarity selected by computer; pulse width ≥200 ms; TTL compatible; logic low ≤0.4 V, logic high ≥2.4 V.

PREAMP – Provides ±24 V, ±12 V (±3%) and ground for standard preamplifiers; ±24 V at 50 mA max, ±12 V at 100 mA max; rear panel 9-pin D-type connector.

Front Panel Indicators

POWER – Green LED, indicates ac power is *on*.

HV ON – Green LED, indicates HVPS is *on*.

HV FAULT – Yellow LED indicates a high voltage fault (e.g., detector warmup, loss of high voltage).

+5 kV – Green LED indicates HVPS polarity and range is set to +5 kV.

+1.3 kV – Green LED indicates HVPS polarity and range is set to +1.3 kV.

–5 kV – Green LED indicates HVPS polarity and range is set to –5 kV.

VOLTAGE kV – 20-segment horizontal bar graph indicating 0 to 5 kV.

% DEADTIME – 20-segment horizontal bar graph indicating 0 to 100 % deadtime.

PUR ON – Green LED indicates PUR function is on or enabled.

ACQUIRE – Green LED indicates MCA is acquiring.

FAULT – Yellow LED indicates Ethernet communication fault.

COMM TX – Green LED indicates Ethernet transmit activity.

COMM RX – Green LED indicates Ethernet receive activity.

ICR – Green LED indicates incoming count rate activity; also serves as a user aid when setting the Fast Discriminator manually.

BDC BUSY – Green LED indicates Auto BDC is in process.

Rear Panel Connectors

AC LINE – VDE approved IEC 320 line-entry module to accept detachable 3-wire power cord.

AUI – Ethernet AUI Connector; rear panel 15-pin D-connector.

10 Base 2 – Thinwire Ethernet; rear panel BNC.

DIAGNOSTIC – RS-232; rear panel 9-pin male D-connector.

PREAMP – Preamp power connector; rear panel 9-pin female D-connector.

MONITOR – Monitor output connector; rear panel BNC.

ICR – Incoming Count Rate output connector; rear panel BNC.

MSP/LSP – Reserved for control of future precision pulser.

AMP IN – Detector/preamplifier signal input connector; rear panel BNC.

TRP INH – Reset Preamp inhibit input connector; rear panel BNC.

HV INH – Preamp high voltage inhibit input connector; rear panel BNC.

MCS IN – MCS count input connector; rear panel BNC.

HV – High Voltage output connector; rear panel SHV.

PHA S/S – External PHA Start/Stop input connector; rear panel BNC.

MCS S/S – External MCS Start/Stop input connector; rear panel BNC.

GATE – Gate input connector; rear panel BNC.

RDY – Sample Changer Ready input connector; rear panel BNC.

ADV – Sample Changer Advance output connector; rear panel BNC.

Programmable Controls

Gain

Continuously variable from x2.0 to x1536.

COARSE GAIN; x5, x15, x40, x120, x330, x960.

FINE GAIN; Range – x0.4 to x1.6.

SUPER FINE GAIN; Range – 0.0000e–2 to 3.000e–2; the SFG adds to the FINE GAIN Value; resolution is better than 1 part in 16 000.

CONV GAIN – 256, 512, 1024, 2048, 4096, 8192, or 16 384 channels. Represents the full scale resolution of the input signal. Conversion range is set to equal the selected conversion gain.

LLD – Digital Lower Level Discriminator for minimum input acceptance level; adjustment range 0.0% to 100% of the spectrum full scale range.

OFFSET – Offsets the spectrum to the left; subtracts 0 to 16 128 channels in binary multiples of 128 channels.

ZERO ADJUST – Digital Zero Adjustment; ±3.125% of the spectrum full scale range.

INP POLARITY – Selects either POSITIVE or NEGATIVE input polarity.

INH POLARITY – Selects either POSITIVE or NEGATIVE inhibit polarity.

PUR GUARD – Selects guard time multiplier “GT” in increments of 1.1, 1.3, 1.5, 1.7, 1.9, 2.1, 2.3 and 2.5 to reject trailing edge pile-up in the event of detector/preamp anomalies; guard time extends from peak detect time by the amount (GT x T_R+ $T_{FlatTop}$); ”GT=1” selects minimum resolving time for maximum throughput.

FDISC MODE – AUTO: Fast Discriminator (FD) threshold is optimized automatically; MANUAL: Fast Discriminator signal is over a range of 0-100%.

INHIBIT MODE – NORM: the system is gated off while external INHIBIT is set true; RESET: the inhibit time is automatically extended to account for the system overload recovery time or while external INHIBIT is set true.

COINC MODE – In the COINCidence (ANTIcoincidence) mode a positive GATE pulse enables (disables) the conversion of the present input.

FDISC SETTING – Allows adjustment of the fast discriminator threshold level when MANUAL DISC THRES is selected. The adjustment range is 0% to 100%; the front panel ICR LED serves as a user aid when manually setting the Fast Discriminator threshold.

LT TRIM – Allows adjustment of the trapezoid pulse evolution time or dead time to optimize Live Time Correction (LTC) performance. The adjustment range is 0 to 1000; the default value of 250 provides good LTC performance for a wide range of applications.

LTC MODE – ON: Enables pileup rejector and live time corrector (LTC), LTC generates dead time to extend the acquisition time to compensate for events that are piled up and rejected; OFF: Pileup rejector and LTC disabled.

Filter

RISE TIME – 35 rise and fall times ranging from 0.4 µs to 28 µs; step size dependent on rise time range; may be viewed on the MONITOR output.

FLAT TOP – 21 flat top time selections ranging from 0 to 3 µs; increment size dependent on flat top range; may be viewed on the MONITOR output.

BLR MODE – AUTO: The baseline restorer is automatically optimized as a function of the trapezoid shaping time and count rate; HARD, MEDIUM, or SOFT: Sets the baseline restorer to fixed rates.

POLE/ZERO – Displays the current Pole/Zero setting; value ranges from 0 to 4095. 1 to 4095 represents 1.7 ms to 40 µs; a value of zero sets the pole/zero compensation off or to infinity; adjustment enabled when RC preamp type is selected; increment/decrement value using the associated slider bar.

BDC – Computer command to optimize the trapezoidal flat top parameters to match the charge collection time of the detector.

Auto P/Z (DSA-2000A only) – Available only for the DSA-2000A with automatic pole/zero option installed. Computer command initiates the automatic process.

PREAMP TYPE – Selects the pole/zero mode; RC: pole/zero can be adjusted by computer command; range 40 µs to infinity; RESET: Sets pole/zero at infinity for use with pulsed charged restoration (RESET) preamplifiers.

HVPS

RANGE – +5000, +1300, –5000.

VOLTAGE LIMIT – Sets maximum voltage limit; range depends on RANGE selection; +1300 to +5000 V, 0 to +1300 V or 0 to –5000 V.

STATUS – ON, OFF; sets the HVPS ON or OFF.

VOLTAGE – Adjusts the HVPS output over the selected voltage range and limit.

HVPS RESET – Resets the power supply when a fault condition has occurred.

INH SIGNAL – Sets the pull-up voltage of the HV INH connector to +5 V or +12 V. All Canberra detectors and preamps use +5 V.

Stabilizer

GAIN MODE – ON/OFF: enables or disables the Gain Mode; HOLD: disables the stabilizer Gain Mode, but maintains the current Gain correction factor; Centroid (0 to 16 376 channels), Window (1 to 128 channels), Spacing (2 to 512 channels) ratio (0.01 to 100) correction rate (1 to 512); correction range of ±1% of full scale for Ge and ±10% of full scale for NaI detectors.

ZERO – ON/OFF: enables or disables the Zero Mode; HOLD: disables the stabilizer Zero Mode, but maintains the current Zero correction factor; Centroid (0 to 16 376 channels), Window (1 to 128 channels), Spacing (2 to 512 channels) ratio (0.01 to 100), correction rate (1 to 512); correction range is ±1% of full scale.

MCS

Modes

Events are counted for the duration of a programmed amount of sweeps. Each SWEEP incorporates a programmed amount of channels. Each channel represents a DWELL duration.

TTL – TTL pulses counted from MCS IN connector.

Fast Discriminator – Gamma events counted from DSP.

ROI Discrimination – Gamma events counted if they occur within the programmed ROI window.

Programmable Settings

Dwell time – TTL or Fast Discriminator: 2 µs to 2048 s.

Range	Resolution
Microsecond (2 – 2048 µs)	1 µs
Millisecond (2 – 2048 ms)	1 ms
Second (2 – 2048 s)	1 s

ROI Discrimination – 4 µs to 310 µs.

Resolution – 10(RT + FLAT TOP) µs.

Sweep Counter – 65 535 sweeps.

Disc Window – 1 to 32 768 channels.

Sweep Mode – Sweep Counter or Sweep Forever.

MCS Channel Range – 256 to 32 768.

Start Control – External Start via “MCS S/S”.

Stop Control – External Stop via “MCS S/S”/Preset.

Status bit available for sweep finished; interrupt available for sweep count.

Performance

Signal Processing

SPECTRUM BROADENING – The FWHM of ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 100 kcps will typically change less than 6% for 2.8 µs rise/fall time, 0.6 µs flat top and proper P/Z matching. These results may not be reproducible if the associated detector exhibits an inordinate amount of long rise time signals.

INTEGRAL NONLINEARITY – ≤±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY – ≤±1% over the top 99% of the range including the effects from integral nonlinearity.

GAIN DRIFT – ≤50 ppm/°C.

ZERO DRIFT – ≤10 ppm/°C.

OVERLOAD RECOVERY – Recovers to within 1% of full scale output from x1000 overload in 2.5 non-overlapped pulse widths at full gain, at any shaping (processing time), and with pole/zero properly set.

Pileup Rejector/Live Time Corrector

PULSE PAIR RESOLUTION – 500 ns.

FAST DISCRIMINATOR – Threshold set automatically or manually; minimum detectable signal limited by the detector/preamplifier noise characteristics.

DEAD TIME CORRECTION – Extended Live-Time correction, accuracy of reference peak area changes 5% (3% typical) up to 50% system dead time for 4 µs Gaussian equivalent processing time.

Acquisition

DATA MEMORY GROUPS – 1–32K (PHA) channels (single mode only); 32 bits per channel, three day data retention when power is lost. Divisible into halves, quarters, eighths, and sixteenths. 1–32K (MCS) channels; 32 bits per channel, three day data retention when power is lost.

Note: During simultaneous operation PHA/MCS, PHA memory groups reside in lower 32K x 32 of acquisition memory (i.e. PHA at 0–32K, MCS at 32K–64K).

STORAGE MODE – PHA (Port 1), MCS (Port 2).

PRESET MODE – ROI, Live or True Time, Counts per channel.

TIME RESOLUTION – 0.01 s.

PRESET TIME – 1 to >4 $x10^7$ s.

Start-Stop/Sample Changer

Support external PHA or MCS start/stop and sample changer control (RDY and ADVANCE) simultaneously.

Programming of RDY and ADVANCE polarity are supported via computer.

High Voltage Power Supply (HVPS)

LOW RANGE – +5 V to +1300 V at 500 µA programmable to one part in 4096; current limit: 1.1 mA maximum.

HIGH RANGE – +1300 V to +5000 V or –10 V to –5000 V, programmable to one part in 4096; load current 100 µA from 65 V to 5000 V, derated 1.3 µA per volt below 65 V; current Limit: 250 µA.

RIPPLE AND NOISE – ≤5 mV peak to peak at full load for 1.3 kV range, ≤25 mV peak to peak at full load for 5 kV range.

TEMP. COEFFICIENT – ≤±50 ppm/°C after 30 minute warmup.

OUTPUT STABILITY – Long term drift of output voltage is ≤0.01%/h and ≤0.02%/8 h at constant load and ambient temperature after 30 minute warmup.

VOLTAGE ACCURACY – ±10% of setting.

REGULATION – For the 5 kV range, ≤0.02% variation in output voltage over the load range at constant ambient temperature.

OVERLOAD PROTECTION – The high voltage power supply will withstand any overload, including a short circuit, for an indefinite period.

Power

90–259 V ac (47–63 Hz) in four user selectable ranges; 90–113 V, 103–129 V, 193–243 V, or 220–259 V, selected by line entry module voltage selection wheel; 60 watts maximum; Line connector: Line Entry module with integral IEC 320 connector to accept detachable 3-wire line cord; fused with two 5 x 20 mm fuses: 4 A for 90–129 V, 2 A for 193–259 V. On/Off control is provided by a rocker switch.

Physical

Aluminum enclosure with forced air cooling fan. Optional (included) rack mounting kit consisting of rack mount ears.

SIZE – 42.5 cm wide x 8.9 cm high x 40.6 cm deep (16.75 in. wide x 3.5 in. high x 16 in. deep).

WEIGHT – 8.5 kg (18.73 lb).

Environmental

OPERATING TEMPERATURE – 0 to 50 °C.

OPERATING HUMIDITY – Up to 80% non-condensing.

OVERVOLTAGE CATEGORY – II.

Meets the environmental conditions specified by EN 61010, Installation Category I, Pollution Degree 2.

Ordering Information

DSA-2000 – programmable Digital Spectrum Analyzer.

DSA-2000A – programmable Digital Spectrum Analyzer with automatic pole zero option installed.

B. Performance Adjustments

This appendix describes how to make several performance adjustments: adjusting the rise time and the flat top, matching the pole/zero manually, setting the baseline restorer, setting the fast discriminator threshold, and operating the DSA-2000 with reset preamps.

Rise Time and Flat Top Adjustments

The digital filter employed in the DSA-2000 has a Triangular/Trapezoidal weighting or shaping function. The processing time (Shaping) is set by the Rise Time and Flat Top selections and is generally a compromise between optimizing throughput and resolution. Having the ability to independently set the Rise Time and Flat Top allows greater flexibility when optimizing the processing time or shaping for a wide variety of detector applications. The Rise Time sets the noise filtering characteristics of the Digital Filter while the Flat Top allows for the charge collection time of the particular detector. Independent adjustment of the flat top allows the shaping function to be optimized for detectors with long charge collection time, without a large increase in the overall processing time. For small detectors with minimal charge collection time variation or ballistic deficit, the trapezoidal shape reduces to triangular shaping when the Flat Top is set to minimum or zero. The triangular/trapezoidal shaping function is symmetrical. The fall time cannot be set independently, it always equals the Rise Time selection.

Shaping is adjusted by selecting the Rise Time and Flat Top, which determine the Trapezoid pulse shape and optimizes performance for the specific detector, spectral energy range and count rate. As in any signal processing application, a performance tradeoff exists between high resolution and high throughput. For example when using a small Ge detector, 5.6 µs rise time and 0.8 µs flat top settings provide optimum resolution over a wide range of count rates. However, a 2.8 µs rise time and 0.6 µs flat top will degrade low count rate resolution performance slightly, but results in less resolution broadening and peak shift over a much wider count rate range.

For ultra high counting and throughput rates, rise time and flat top settings of less than 1 µs may be used. For this case, optimum resolution is traded off for increased count rate performance. For high resolution detectors, longer rise time settings offer a better signal to noise (S/N) ratio and longer flat top settings reduce the effects of ballistic deficit. However, as the system count rate increases, resolution may degrade more rapidly due to increased processing time and the effects of pulse pile-up.

For most Ge detector applications, digital trapezoidal shaping provides Gaussian equivalent resolution with half the processing time. Faster processing time means the DSA-2000 provides significantly greater throughput than a traditional analog system with its processing or shaping times set for equivalent resolution. When using small Ge detectors which are optimized for high count rate performance, throughputs of 100 kcps can be achieved. To achieve 100 kcps and higher throughput, the highest spectral peak must not exceed 80% of full scale. For more information on count rate performance, refer to Canberra's Application Note "Performance of Digital Signal Processors for Gamma Spectroscopy". Please contact your sales representative to request a copy.

However, the settings which realize reduced processing time, high throughput and equivalent resolution for Ge detectors may be a bit aggressive for some low energy applications. For these applications, which include LEGe, Si(Li) and X-ray detectors, resolution will be equal to or better than that obtained with traditional analog systems when the Rise Time and Flat Top filter parameters are optimized for resolution. For this case, the trapezoidal rise time parameter is increased so that the processing time and throughput are equivalent to Gaussian shaping.

Table B.1 lists the DSA-2000 Rise Time and Flat Top settings which optimize performance for high throughput/good resolution and optional setting for best resolution/lower throughput when using Germanium Coaxial detectors.

Table B.1 Gaussian Shaping vs. Throughput and Resolution

Gaussian Shaping (μs)	Highest Throughput[1] Rise Time / Flat Top	Highest Resolution[2] Rise Time / Flat Top
0.5 μs	0.8 μs / 0.2 μs	1.2 μs / 0.2 μs
1.0 μs	1.2 μs / 0.6 μs	2.8 μs / 0.6 μs
2 μs	2.8 μs / 0.6 μs	5.6 μs / 0.6 μs
4 μs	5.6 μs / 0.8 μs	12 μs / 0.8 μs
6 μs	8.8 μs / 1.2 μs	18.4 μs / 1.2 μs
12 μs	16.8 μs / 2.4μs	28 μs / 2.4 μs

Note 1: Optimized for high throughput, good or equivalent Gaussian shaping resolution.
Note 2: Optimized for highest resolution, equivalent Gaussian shaping processing time/throughput.

Table B.1 lists settings for optimizing throughput or resolution. Of course a setting in between can be chosen to optimize performance for a specific application. The Gaussian Equivalent Shaping Times are suggested as starting values. You may change these values to enhance throughput or resolution as required by your application.

As previously mentioned, the shaping times recommended for highest throughput produce a trapezoidal pulse response which has approximately one-half the processing time when compared with traditional analog Gaussian shaping amplifiers. These settings result in almost twice the throughput compared to traditional analog pulse processing, with little or no resolution degradation in most high energy Ge detector applications.

The shaping times recommended for highest Resolution produce a trapezoidal pulse response with a processing time that is equivalent to traditional analog signal processing. Longer rise time and flat top settings provide better noise filtering and reduced ballistic deficit. However, as the system count rate increases, resolution and throughput may degrade as a result of increased processing time and the effects of pile-up.

The optimum shaping-time constant depends on the detector characteristics (such as size, noise characteristics and collection characteristics), preamplifier and incoming count rate. Settings for typical germanium coaxial detectors have been discussed above. Table B.2 lists DSA-2000 rise time and flat top settings for other common detectors.

Table B.2 Settings for Other Common Detectors

Detector	Rise Time/Flat Top (ms)
Scintillation [NaI(Tl)]	0.8/0.2 or 1.2/0.6
Planar Implanted Passivated Silicon (PIPS) (Silicon Charged Particle)	0.8 / 0.2, 1.2/0.6 or 2.8/0.6
Proportional Counter	0.8/0.2, 1.2/0.6 or 2.8/0.6
Lithium Drifted Silicon [Si(Li)]	8.8/1.2 or 16.8/2.4
Coaxial Germanium	2.8/0.6 or 5.6/0.8
Low Energy Germanium	5.6/0.8, 8.8/1.2 or 16.8/2.4

Refer to the specific Detector Operator's Manual for the recommended shaping time. A good starting point is the Gaussian equivalent processing time selections listed in the table on page 87. The Rise Time and Flat Top setting can be optimized further through experimentation. Collect spectra using rise time and flat top settings above and below the recommended settings, to optimize resolution performance for your particular detector and application.

Flat Top Setting

The DSA-2000 allows independent selection of rise time and flat top. A detector with long charge collection times will require a flat top long enough to process all the charge from the detector (see "Automatic Ballistic Deficit Correction" on page 64). If the flat top is too short, it may result in low side spectral tailing and degraded resolution (However, if these symptoms occur at high rates only, the P/Z setting may be misadjusted. In this case, first verify the correct P/Z setting and readjust if necessary). To set the flat top manually, start with a long value, then collect a spectrum and verify good resolution and peak symmetry. Reduce the flat top and repeat the process. Continue until resolution and peak symmetry begin to degrade, then set the flat top to the next higher value. The optimal (shortest) flat top will allow the best throughput.

The rise time setting can be optimized separately to achieve the best count rate/resolution compromise. However, the optimum flat top for a detector depends somewhat on the rise time selection. Therefore, the best correction for ballistic deficit will be achieved by running the Auto BDC function again or manually checking the flat top setting if the rise time is increased or decreased by a factor of two or more.

Triangular shaping may give enhanced resolution performance for small detectors having little variability in charge collection time. To set the unit for triangular shaping, adjust the rise time to the desired value and set the flat top to zero.

P/Z Matching Using a Square Wave Generator

1. Driving the preamp test input with a square wave will allow a more precise adjustment of the preamp matching.

2. The DSA-2000's GAIN, RISE TIME, FALL TIME and INPUT POLARITY settings should be adjusted for the intended application.

3. Adjust the square wave generator for a frequency of approximately 100 Hz.

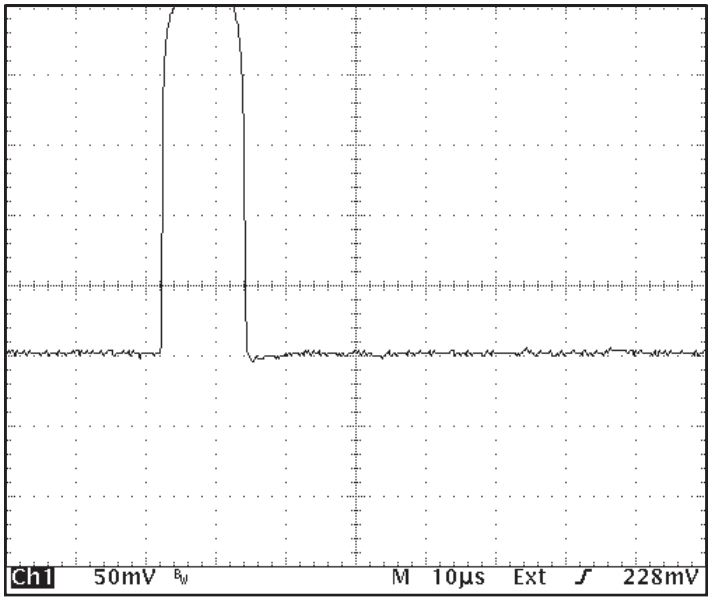
4. Connect the square wave generator's output to the Preamp's TEST INPUT.

5. Remove all radioactive sources from the vicinity of the detector.

6. Set the scope's Channel 1 vertical sensitivity to 2 V/div, and adjust the main time base to 10 µs/div.

7. Observe the Model DSA-2000's Monitor output. If you are using an LB1502 Clamp Box, set the switch in the DIRECT position. Adjust the scope triggering so that the positive trapezoid output is observed, then set the square wave generator's amplitude control (attenuator) for an amplitude of 6 V.

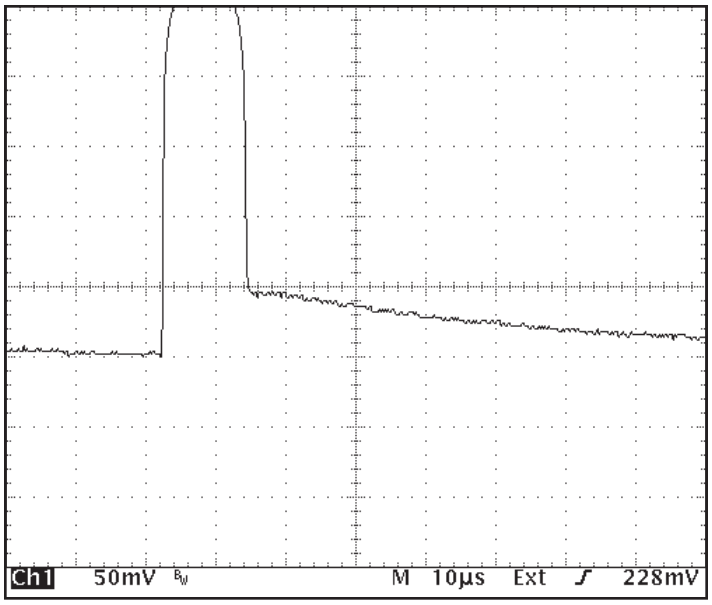
8. Change the scope vertical sensitivity to 50 mV/div. To prevent scope overload, clamp the Monitor output signal by moving the LB1502 Clamp Box switch to the CLAMP position. Adjust the Pole/Zero slider bar for correct pole/zero compensation. Figure 46 shows the correct P/Z setting.



Scope:
Horiz: 20 mV/div
Vert: 10 µs/div

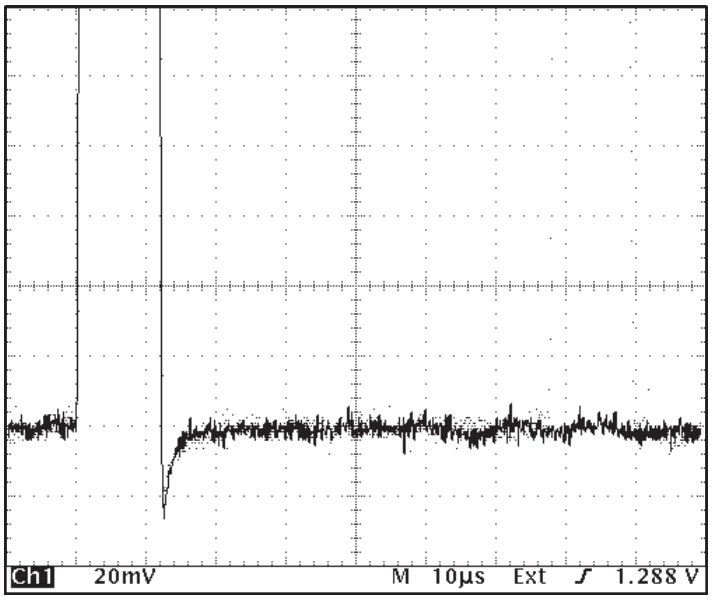
Figure 46 Correct Pole/Zero Compensation

Figures 47 and 48 show over- and under-compensation for the preamplifier decay time constant. As illustrated in Figure 46, the monitor output signal should have a clean return to the baseline with no bumps, overshoots or undershoots.



Scope:
Horiz: 20 mV/div
Vert: 10 µs/div

Figure 47 Overcompensated Pole/Zero



Scope:
Horiz: 20 mV/div
Vert: 10 µs/div

Figure 48 Undercompensated Pole/Zero

Baseline Restorer

The digital baseline restorer in the Model DSA-2000 is flexible and allows adjustment for varying baseline conditions affected by detector type, noise and count rate. The baseline restorer rate is selected using the BLR mode drop down menu in the Filter Device Adjust screen.

With the Baseline set to AUTO, the digital baseline restorer is automatically set for optimum performance throughout the usable input count rate range.

The restorer can also be set to three manual settings: SOFT MEDIUM and HARD. These setting can be used with detectors having exceptionally stable baselines at all rates, or with detectors which at high rates develop unusual noise, requiring a somewhat lower restoration rate than provided by AUTO Rate. The SOFT selection significantly reduces the baseline restorer's restoration rate. This may prove to be advantageous in some low count rate/low energy applications. With the SOFT selected, the restorer's low frequency noise suppression effectiveness is reduced. The ambient low frequency noise and the implementation of noise reduction techniques regarding setup can easily be assessed and tested.

For situations where a higher than normal restoration rate is required, the restorer rate may be set to MEDIUM or HARD, which increases restoration rate proportionately. This can improve performance at extremely high input counting rates or where more control is required to maintain the baseline, such as with some NaI(Tl) scintillation detector systems.

Manual Fast Discriminator Threshold

In some cases, you may want to set the Fast Discriminator threshold manually. For best performance, set the threshold just above the system noise level.

1. Set the Amplifier Gain and shaping as required.

2. Set the FDisc Mode in the Gain Device Adjust screen to "Manual".

3. Remove all excitation sources from the vicinity of the detector.

4. Use the FDisc setting slider bar in the Gain Device Adjust screen to set the fast discriminator threshold just above the system noise as indicated in step 5.

5. The following steps optimize the discriminator sensitivity to insure the threshold is at its lowest setting, just above the noise level:

Adjust the FDisc Setting to 0%. The ICR LED indicator continuously glows green.

Next, increase the FDisc Setting level until the ICR LED indicator is no longer on continuously, but shows low activity by blinking green occasionally. The fast discriminator threshold is properly set.

Note With the Fast Discriminator in the manual mode, the threshold must be re-checked and adjusted if the Detector/Preamplifier is changed or the DSA-2000's GAIN is changed.

Operation with Reset Preamps

The DSA-2000 Digital Spectrum Analyzer is fully compatible with most pulsed reset preamplifiers. Reset preamps use an electronic circuit, as opposed to a feedback resistor, to restore the preamp back to a reference level. As a result, the preamp output is a succession of step functions that staircase or ramp up to an upper limit or threshold that initiates a preamp reset.

Configuring the Preamp Reset Mode

When using a Transistor Reset Preamp (TRP) it may be necessary to disable the Reset Delay feature, if present, on the associated preamplifier. If the Reset Delay feature is left enabled, small phantom peaks may result slightly before or after each of the main spectral peaks.

If you are using a Canberra Model 2101 preamplifier, disable the Reset Delay using these three steps:

1. Remove all signal and power connections from the preamp.

2. Remove the preamp cover and change jumper plug W1 from position A to position B. Jumper plug W1 is located on the main PC board next to RV1.

3. When done, reinstall the preamp cover and reconnect the preamp to the DSA-2000 as before or as indicated in "Spectroscopy System Setup" on page 53 and in Figure 38 on page 54.

For additional information on the Reset Delay feature and jumper plug W1 please refer to the Model 2101 User's Manual.

Pole/Zero Setting for Reset Preamps

Since the Reset Preamp output signal is a step function instead of the classical tail pulse, with exponential decay, Pole/Zero compensation is not required. For this application, the Pole/Zero should be set off or to infinity. On the DSA-2000, this is accomplished by setting the preamp type to RESET. The preamp type can be changed in the Filter Device MID Editor. If RESET is selected, the Pole/Zero is automatically set to a value of zero, corresponding to a fall time of infinity, and no further adjustment is required. If RC is selected, the pole zero value in the Filter Device Adjust screen must be manually set to zero.

Using the Reset Inhibit

During the preamp reset interval, the preamp reset event produces a large signal to the DSA-2000 driving it into severe overload. The DSA-2000 automatically senses preamplifier reset events and gates off pulse processing during the associated overload event. However, to obtain optimum performance, especially at high count rates, it is recommended the preamplifier's Inhibit signal be connected to the Inhibit Input on the DSA-2000. Figure 49 shows Trapezoid Signal, Preamp Output and Inhibit Signals.

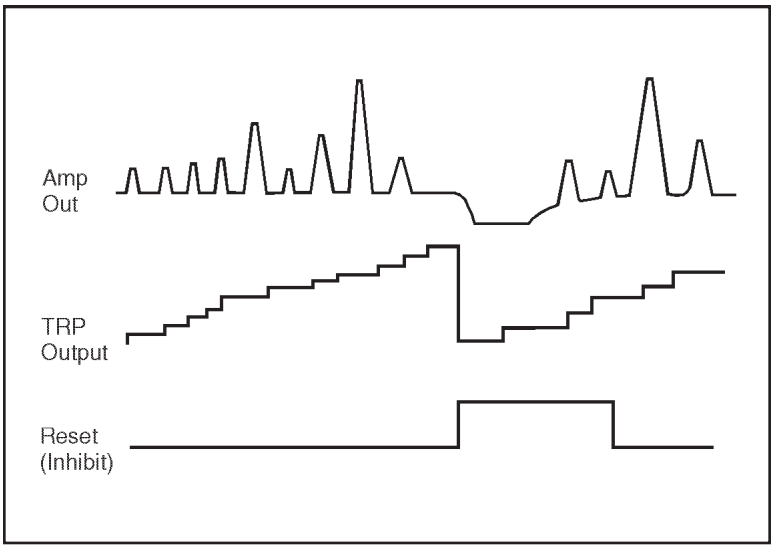


Figure 49 Monitor Output, TRP Output, TRP Inhibit

The DSA-2000 system inhibit is initiated or derived from the preamp inhibit signal. The optimum system inhibit time can be set automatically by the DSA-2000 or adjusted manually. For automatic inhibit, set the Inhibit Mode, Gain Device Adjust screen, to “Reset”. When using the RESET mode of operation, the correct system inhibit time is automatically set. It is not necessary to make critical adjustments of the inhibit signal at the preamp. However, the preamp inhibit signal should be set to its minimum value. Please consult the Detector/Preamp Operator manual for this adjustment.

Note When using the automatic RESET inhibit mode, the system inhibit is the time interval automatically generated by the DSA-2000 “OR” the external inhibit duration which ever lasts longer. For proper operation set the preamp inhibit time to minimum or it can override the optimum inhibit time generated by the DSA-2000.

When setting the inhibit time manually, set the TRP Inhibit to NORMAL. The TRP Inhibit mode is selected in the Gain Device Adjust screen. The inhibit time of the preamp must now be manually adjusted to encompass or extend to the point where the trapezoid signal returns back to the baseline.

Using a “Tee” connector, connect the preamp’s Inhibit signal to the INHIBIT BNC connector located on the rear panel of the DSA-2000. Monitor the preamp’s Inhibit signal and the DSA-2000’s Trapezoid signal, viewed on the Monitor Output, using an oscilloscope. Use a clamp box, such as the Canberra Model LB1502, when viewing the Trapezoid signal to prevent scope overload.

Trigger the Oscilloscope on the leading edge of the preamp Inhibit signal. Adjust the preamp inhibit time so that it returns to zero volts after the negative Trapezoid (negative overload) signal returns to the baseline (see Figure 50). Consult the Detector/Preamp Operator manual for this adjustment.

The DSA-2000’s overload recovery time is approximately 40 µs with the Rise time set to 5.6 µs and Flat Top set to 0.8 µs and using a Canberra Model 2101 preamp and ^{60}Co source.

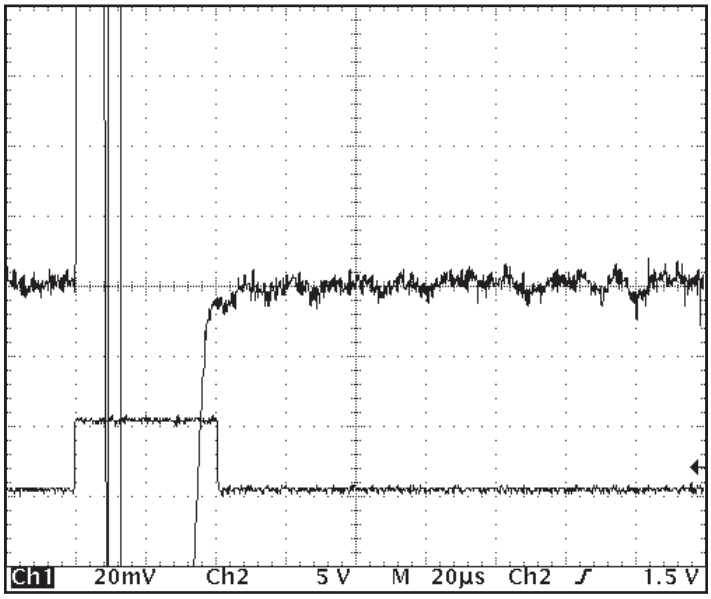


Figure 50 Setting the Reset Preamp Inhibit Pulse Width

C. Voltage Selection

The DSA-2000 ac input power requirement should have been preconfigured at the factory for the standard line power of the destination country. To verify that the setting matches the ac line input power, look through the window on the power entry module's cover. If it becomes necessary to use a different setting, the voltage selection is easy to change. The power entry module voltage selections are: 100 V ac, 120 V ac, 220 V ac and 240 V ac, allowing the DSA-2000 to operate over a voltage range of 90–259 V ac.

To change the DSA-2000 power supply's input voltage, turn the power supply *off* and detach the power cord from the ac main supply.

WARNING Leaving the ac input power connected while working with the power entry module can result in serious injury or death.

Changing the Voltage Selection

1. Open the power entry module's cover, using a small bladed screwdriver or similar tool to pry up the cover's tab, which is just above the voltage selection viewing window. Let the cover open to its resting position.

2. Pull the Selection Wheel straight out of the housing (Figure 51). A small bladed screwdriver or similar tool may be required to pry it out of the housing.

3. Turn the wheel until the desired line voltage is facing you, then push the Selection Wheel back into the module until it clicks into place.

   If the ac voltage from the power mains is not available on the Selection Wheel, select the next higher setting on the card. For example, if the mains voltage is 105, set the Selection Wheel to 120 volts for highest efficiency and lowest temperature rise.

   When changing the voltage selection, it may be necessary to change the fuse as well. Refer to "Fusing" on page 98 for information on fuse selection and installation.

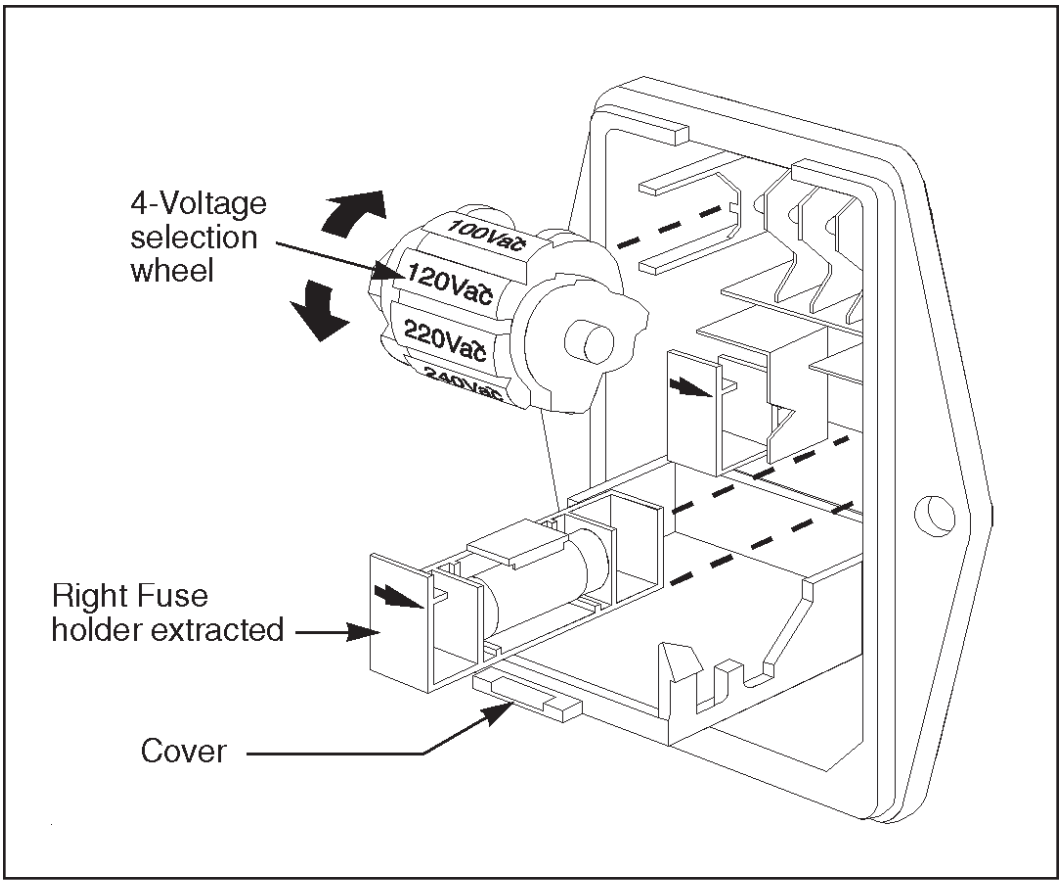


Figure 51 The Line Entry Module

Fusing

1. If not already done, open the Power Entry Module's cover as described in "Changing the Voltage Selection" on page 97.

2. Pull the left and right Fuse Holders from the Power Entry Module. Replace the fuses in each of the holders with fuses of the correct the voltage and current rating. Fuse selection information is listed in the Fuse Types section, below.

3. Reinstall the fuse holders into the Power Entry Module. The arrows should point to the right as indicated on the inside of the Module's cover.

Fuse Types

Note that two metric fuses are required (IEC 127, Type T, sheet 3)

For 90–129 volt ac operation, use two 4 A, 5 mm x 20 mm fast acting fuses.

For 193–259 volt ac operation, use two 2 A, 5 mm x 20 mm slow-blow low-break fuses.

Replacing the Cover

When you have finished changing the Selection Wheel and the fuses, close the module's cover and press on it until it snaps into the locked position.

D. Rack Mount Hardware

A rack mount kit, which includes one set of rack mount ears and hardware, is shipped with the DSA-2000. Using #10 x 3/8 flat head screws, attach the mounting brackets as shown in Figure 52.

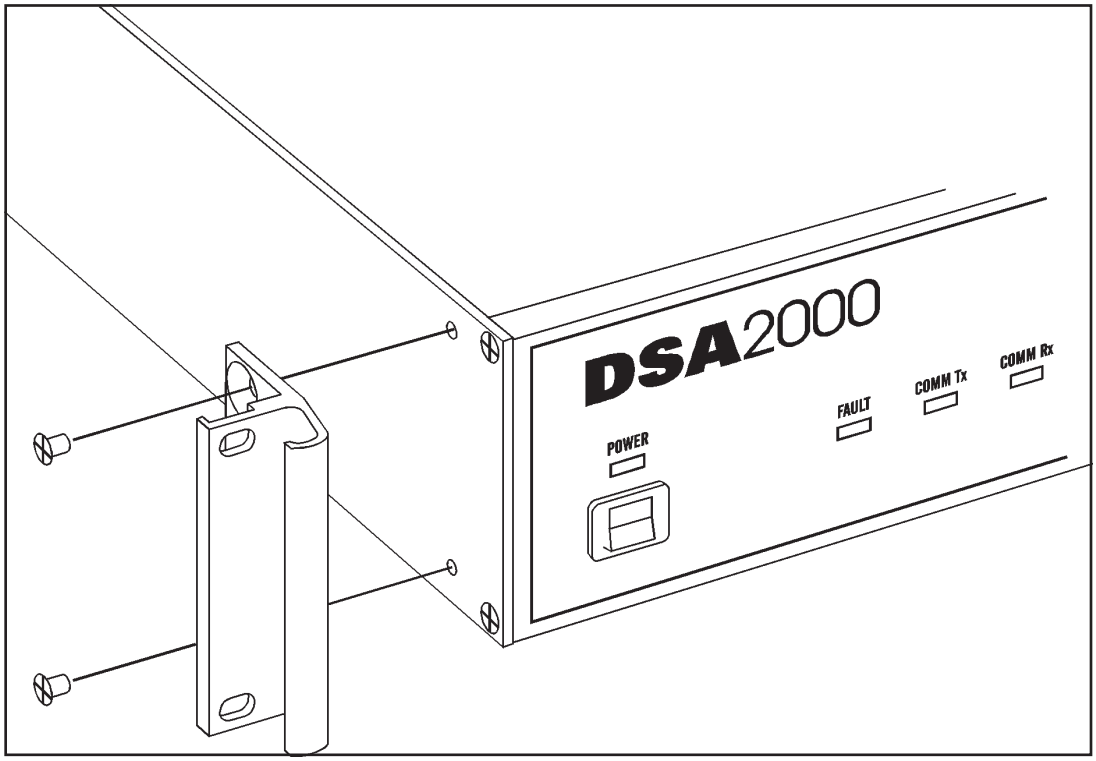


Figure 52 The Rack Mount Hardware

E. Using The Diagnostic Port

DSA-2000 Architecture

The DSA-2000s diagnostic port is a RS-232 bidirectional port used for both to diagnose problems and loading new firmware into the instrument. To load firmware into the instrument, a host computer with appropriate utility software is required. To diagnose problems, a simple VT100-compatible terminal, or host computer equipped with terminal emulator software such as Windows TERMINAL is required.

The DSA-2000s RS-232 diagnostic connector is a 9-pin D-type male connector accessible through the instruments rear-panel. When connecting to host computer or terminal a 1:1 cable is required. No software or hardware handshaking is required. The communication parameters are as follows:

Baud Rate:	9600 baud for normal operation, or 38400 baud when loading firmware. When loading firmware the baud rate is fixed by the DSA2000 and by the download utility at the host computer
Parity:	none
Data bits:	8
Stop bits:	1

The DSA-2000 contains a second RS-232 port which is internal to the instrument. This port is used solely to download the DSP processors main program from a host computer. It has no user interface, thus its operation will be covered in a separate document that will be sent with the program update diskette.

Initialization

Typical initialization output to the terminal is as follows:

```
CI DSA-2000 Loader

RAMTEST...          OK
Boot init...
OK
```

```
CI DSA-2000 Main

Master Program Versions

  Main: V00.95
  Boot: V00.07

Module initialization

Leds init...       OK

SNIC init...       OK

Timers init...     OK

Buffers init...    OK

Adc init...        OK

Acq memory...      OK

DMA Channel...     OK

Ethernet Adrs.00 00 AF 00 AC B1

Ethernet...        OK

  Type...         Thinnet

ICB Comm...        OK

DSP Init...        OK

DSP Versions

  Boot: V01.04

Main: V01.12

Front Panel...     OK

COP Timer...       enabled

SNIC Buffer...     OK

HV Init...         OK

Chngr Init...      OK

[READY - Press Q for Main Menu, Ctrl-D for Diag. Menu]
```

The DSA2000's Initialization Sequence

Each processor in the DSA-2000 contains two distinct programs, a **Program Loader** also referred as the **Bootstrap** (**Boot** for short) and the **Main Program** which is also referred to as the **Application Program**. The Bootstrap is used primarily for loading the Application program into the instrument.

When power is first applied to the instrument, control is immediately passed to the Bootstrap program which performs a basic memory test and critical initialization as required for basic operation.

- Assuming the instrument is working properly, the following text is sent at 9600 baud to the diagnostic terminal:

```
CI DSA-2000 Loader

RAMTEST...OK
Boot init...OK
```

  At this point the Bootstrap enters pause of about 10 to 15 seconds during which it expects communication at 38400 baud from the program- download utility running at the host computer. If no computer is connected and thus proper communication is NOT established, then control is passed to the Main Program which outputs the remaining text at 9600 baud.

- The instrument's CPU program versions are displayed

```
CI DSA-2000 Main
Master Program Versions


    Main: V00.95
    Boot: V00.07
```

- The DSA-2000 initialization

```
Module initialization
Leds init...OK
```

  The instrument's processor performs simple I/O operations to the front-pane logic. OK indicates that Read/Write operations to the front-panel logic were performed within the allowed time. FAIL would typically indicate failure in the front-panel or ICB logic

```
SNIC init...OK
```

  The instrument's processor performs initialization sequence on the SNIC ethernet communication processor. OK indicates the SNIC responded properly to its initialization, including its own internal loopback tests. FAIL would typically indicate failure in the I/O logic or SNIC processor

```
Timers init...OK
```

The instrument's processor performs initialization sequence on the integral timer hardware. OK indicates the timers responded properly to its initialization. FAIL would typically indicate failure within the AIM CPU itself as the timers are integrated within the CPU package

```
Buffers init...OK
```

The instrument's processor performs initialization to essential memory buffers used by the program (Acquisition memory is treated separately). OK indicates no problems encountered. FAIL would typically indicate failure within the memory logic.

```
Adc init...OK
```

The instrument's processor performs initialization ADC acquisition logic for both PHA and MCS. OK indicates no problems encountered. FAIL would typically indicate failure within the acquisition logic

```
Acq memory...OK
```

The instrument's processor performs battery-back retention test to the ADCs battery-backed memory. OK indicates that the memory properly retained its data. INIT indicates that the test failed and the memory contents have been re-initialized. The retention test will fail if the memory's backup power supply depleted below the value necessary for proper retention

```
DMA Channel...OK
```

The instrument's processor performs simple memory transfers via DMA. OK indicates no problems encountered. FAIL would typically indicate failure within the AIM CPU itself as the DMA channels are integrated within the CPU package, or withing the I/O decode logic which is essential in synchronizing DMA transfers.

```
Ethernet Adrs.00 00 AF 00 AC B1
```

The ethernet address for the DSA-2000 is printed here for convenience. This address is programmed into permanent memory at the factory.

```
Ethernet...OK
```

```
    Type...Thinnet
```

The instrument's processor performs automatic ethernet detection test by actually sending a test packet to the network with the ethernet interface set for 10base2 (Thinnet) and 10baseT (AUI). OK indicates that proper echo of the packet has been received, and the Type reflects the interface detected. FAIL indicates that echo has not been received in either mode, and the interface has been defaulted to Thinnet type.

```
ICB Comm...OK
```

The instrument's processor performs extensive read/write operations over the internal ICB bus. OK indicates no problems detected. FAIL indicates failure in the ICB logic, including unplugged or defective interconnection ICB cable. If this test does not succeed then the DSP Init and DSP Version steps will not be performed.

```
DSP Init...OK
```

The instrument's processor directs the DSP processor to perform extensive initialization of the digital signal processing electronics using the DSPs battery-backed parameters. OK indicates the entire initialization sequence was successful. FAIL indicates failure in the ICB logic, front-end electronics, or DSP section.

- The DSP CPU program versions are displayed

```
DSP Versions


    Boot: V01.04
    Main: V01.12

Front Panel...OK
```

The instrument's processor runs through a front-panel initialization sequence by first setting each LED on, then sequencing all segments of the graph LEDs on, then sequencing to off, then turn each LED off. Small delays are added between each operation for viewing results. A longer delay is added when the graph LEDs are at mid-scale.

```
COP Timer...enabled
```

The COP timer is also referred to as the Watchdog timer. Its function is to detect excessive program inactivity, at which time it will issue a hardware reset to restart the instrument. This feature is always enabled.

```
SNIC Buffer...OK
```

The instrument's processor performs write/read/write operation to the SNIC processors local memory. OK indicates the w/r/w verification passed. FAIL indicates interprocessor communication failures. NOTE that this test may indicate FAIL if host commands received by the module over the ethernet connection. If in doubt, disconnect the ethernet cable and repeat the test by cycling power to the instrument (Note that doing so will cause the Ethernet test above to fail).

```
HV Init...OK
```

The instrument's processor performs initialization to the High Voltage hardware. OK indicates no failure. FAIL indicates failure in the high-voltage logic or disconnected signal cable.

```
Chngr Init...OK
```

The instrument's processor performs initialization to the sample change electronics. OK indicates no failure detected. FAIL indicates the S/C logic failed to respond which typically would indicate failure within FPGA logic.

```
[READY - Press Q for Main Menu, Ctrl-D for Diag. Menu]
```

At this point, the instrument is running in its normal mode. Pressing 'Q' will display the Main Menu and pressing 'Ctrl-D' will display the Diagnostic Menu. The Diagnostic Menu should be used only for diagnosing problems because operations within the diagnostic menu will affect the normal operation of the instrument.

Main Menu

```
                DSA2000 MAIN MENU

MODE                                KEYS
Command Monitor On                  CTRL + N
Command Monitor Off                 CTRL + F
Erase Local Terminal                CTRL + E
Ethernet Monitor                    CTRL + L
Diagnostic Monitor                  CTRL + D
```

Command Monitor Mode

The Command Monitor mode displays the Ethernet command being processed and the final status of the command. This mode is entered with the Ctrl+N key combination. The layout for the message is:

Ethernet Type – Message Type – Command Type – Status (only failure will be indicated)

For example:

UI – Packet Message – Return ADC Status
or
UI – Packet Message – Return ADC Status – FAIL

This mode scrolls the messages on the screen as they are received and processed by the instrument. To exit this mode, enter Ctrl+F from the terminal. Exiting from this mode will return you to the main menu.

Erase Local Terminal Command

The Erase Local Terminal command will send the escape sequence to the terminal that will delete all text from the screen. This is only available at the top level of the menu tree and during the Command Monitor mode. It will not be accessible in Ethernet Monitor Mode or Diagnostic Monitor Mode.

Ethernet Monitor Mode

Ethernet Monitor Mode displays the current Ethernet statistics for the module. These statistics indicate the number of receive, transmit, and miscellaneous errors. It also indicates the number of received messages, transmitted messages, and multicast messages processed. A typical Ethernet Error Monitor display is shown in Figure 53.

To update the display, press L. To clear the counters, press Z. Pressing Q will return you to Command Monitor Mode if it is enabled, otherwise it will return you to the Main Menu.

```
                        Ethernet Error Monitor

Receive Errors                          Transmit Errors

CRC                       0             Collision Occurred          0
Frame Alignment           0             Transmit Aborted            0
FIFO Overrun              0             Carrier Sense Lost          0
Missed Packet             0             FIFO Underrun               0
                                        CD Heartbeat                0
                                        Out of Window Collision     0


Valid Traffic                           Miscellaneous Errors

Frames TX                 0             Overwrite                   0
Frames RX                 0             Tally Count Overflow        0
Multicast RX              0



Options
  L - Update Display    Z - Zero all counters     Q - Return to Command Monitor
```

Figure 53 The Ethernet Error Monitor Mode

Diagnostic Menu

```
                        DSA2000 DIAGNOSTICS

————————————————————————Version 7 ————————————————————————————

A - Test SRAM           F - Help            K - Ethernet Mirror Test
B - Test Flash          G - Send ICB        L - Ethernet TDR Test
C - Test Acquisition    H - Receive ICB     M - Test ADC
    SRAM
D - Test Timers         I - Test SNIC       N - Test ICB
E - Show Ethernet       J - Test DMA        Q - Quit Diagnostic Mode
    Address
Diagnostic Option?

————————————————————————————————————————————————————————————
```

Diagnostic Monitor Mode

Diagnostic Monitor mode is a user interactive diagnostics mode which presents a menu of diagnostics tests that can be run on the module. This mode cannot be entered while the module is owned. The reason for this is that some tests are time intensive and would cause communications between a host and the module to fail. Also, the acquisition memory tests perform write/read tests which during an acquisition have the potential to corrupt a spectrum being collected.

The Diagnostic Monitor Mode menu is shown in Figure 54. This screen is divided into two parts, the menu, enclosed by the graphical outline, and the scrolling output region below it which consists of six lines available for output. When running tests multiple times, the output will be displayed at the bottom and will scroll up as space is needed.

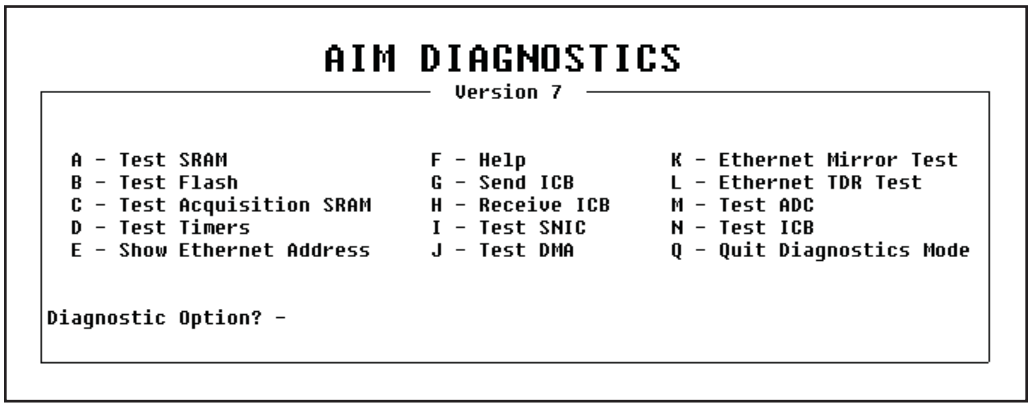


Figure 54 The Diagnostic Monitor Mode Menu

Options A, B, C, D, I, J, K, L, M, and N will ask you to enter the number of times the test is to be run; the value must be in the range 1–999.

A. Test SRAM

This test uses a reserved area of the SRAM to perform read/write tests to ensure its ability to perform these tasks. The test writes a few bytes to the reserved area and then verifies the values read back from the same locations. It should be noted that for the DSA-2000 to enter the main application, SRAM would have to be valid due to the fact that the bootstrap program runs completely out of the SRAM.

B. Test Flash

The flash test verifies the checksums of the parameters sector of the flash to ensure the flash is programmed correctly. The test calculates the checksums on each of the sectors and compares them to those stored in the parameters sector. The test will pass only if all checksums for sectors 0–5 are identical to those stored.

C. Test Acquisition SRAM

This test writes values to specific areas of the acquisition SRAM and then verifies that those values have been written. The previous values at those locations before the test are saved and restored after the test. The test is considered passed if the values written are equivalent to the values read.

D. Test Timers

This test verifies the ability of the timers to count correctly. The test reconfigures Timers 0 and 1 to count at the same rate as Timer 2. Interrupts are disabled during the setup process and when enabled, Timer 2 counts for 10 time ticks or 100 ms. At the end of this count, the contents of Timers 0 and 1 checked for a value greater than or equal to 9. The value of 9 is used in the event that the last timer interrupt for one of the timers is not processed, leaving its count at 9. The test is considered passed if both timer channels have a count of 9 or greater.

E. Show Ethernet Address

This option displays the Ethernet address for the module in the output area of the screen. The address is displayed separated by dashes; for example: 00–00–AF–00–AA–CC. The last two are the ID used by the host when setting up the module.

F. Help

This menu option will give help on any of the menu options. You will be prompted to enter the option for which help is wanted. An incorrect entry will return to the initial option prompt after displaying an error. If a valid entry is made, the help text for that option will be displayed in the output area of the screen.

G. Send ICB

This menu option will enable you to send a one byte value (00–FF hex) over the ICB bus to an address between 00 and FF hex. You will first be prompted for the ICB address. When that value has been entered, you will be prompted to enter the value to send to that address. The function will occur and a status message will appear in the output area of the screen.

H. Receive ICB

The Receive ICB command will prompt you for an address to receive data from the ICB bus. Once entered, the function will be performed and a request for data will be made across the ICB bus. The status of the function will be displayed in the output area of the screen. If the function was successful, the value for the specified address will be displayed. If a timeout error occurs, the appropriate error message will be displayed.

I. Test SNIC

This option will perform a loopback test on the SNIC. This test will perform loopback tests 1 and 2. These are internal tests for the SNIC to ensure the internal integrity of the Ethernet controller. These tests are part of the initial hardware startup tests that are performed when entering the main application.

J. Test DMA

The Test DMA option performs a test to ensure the ability of the microprocessor to perform a DMA transfer properly. Values are put into a buffer which is then transferred, using a DMA write, to the SNIC's ring buffer. The values are then read back into a separate buffer using a DMA read operation, then the two buffers are compared to ensure that the values read back are the same as those written to the ring buffer. The test is passed if the values read back are identical to those written.

K. Ethernet Mirror Test

The Ethernet mirror test requires another module or node that understands 802.2 messages of type TEST. The mirror test composes and transmits a TEST type message over the Ethernet and waits for a response. The responses to 802.2 TEST messages are just a reply to the message with the same data, and the reversal of the destination and source addresses by the receiver. This test requires a test for timeout in the event that no response is received. If no response is received or the response received is not what is expected, the appropriate error message will be displayed, otherwise the pass condition message will be displayed.

L. Ethernet TDR Test

This option performs the 3rd loopback test on the SNIC. The first two are internal tests of the SNIC. This test requires one of the Ethernet ports to be connected to a valid network. The SNIC transmits data out onto the Ethernet network and receives it at the same time. The data received is then compared to that transmitted. The test passes if the data is identical.

M. Test ADC

The test ADC option tests that the status register of the ADC FPGA for a value of 0 for the overflow bits on channels 1 and 2 and a 0 for the acquisition status for both channels, as well. If this is not the case, the test indicates a failure.

N. Test ICB

To test the integrity of the ICB FPGA, the status word is read and a test of the enable remote write bit are made. The test passes if and only if this value is a 0.

Q. Quit Diagnostics Mode

This option will exit from diagnostics mode and return you to the Command Monitor mode.

F. Installation Considerations

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of ROI and EMI on the system. However, care should be taken to maintain full compliance. These considerations include:

- A rack or tabletop enclosure fully closed on all sides with rear door access
- Single point external cable access
- Blank panels to cover open front panel Bin area
- Compliant grounding and safety precautions for any internal power distribution
- The use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance with the specified EU requirements.

Notes

Index

CANBERRA

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES OR REMEDIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, EXEMPLARY, PUNITIVE, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE. REPAIR OR REPLACEMENT OF THE SOFTWARE OR EQUIPMENT DURING THE APPLICABLE WARRANTY PERIOD AT CANBERRA'S COST, OR, IN THE CASE OF DEFECTIVE SERVICES, REPERFORMANCE AT CANBERRA'S COST, IS YOUR SOLE AND EXCLUSIVE REMEDY UNDER THIS WARRANTY.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

Software License

When purchasing our software, you have purchased a license to use the software, not the software itself. Because title to the software remains with us, you may not sell, distribute or otherwise transfer the software. This license allows you to use the software on only one computer at a time. You must get our written permission for any exception to this limited license.

BACKUP COPIES

Our software is protected by United States Copyright Law and by International Copyright Treaties. You have our express permission to make one archival copy of the software for backup protection. You may not copy our software or any part of it for any other purpose.