Reference Manual

Mpression Beryll Board

Revision 1.0

2014 / 2

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Index

1. For Ensuring Safe Use

Be sure to follow the instructions given in this Manual which are intended to prevent harm to the user and others as well as material damage.

1.1 Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

1.2 Cautions

Danger	Make sure to use the AC adapter (included in package) that is specified in this Manual. Using an AC adapter not meeting the specifications described in this Manual will cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances such as microwave ovens, or high-pressure containers. Doing so might cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit that is in use with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Throwing the main unit into fire may cause it to explode. Dispose of the main unit following the laws, regulations, and ordinances governing waste disposal.
	Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit in a temperatures ranging from 5°C to 35°C and a humidity range of 0% to 85%.

Warning (Continued from previous page)	Do not pull the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damaged parts of the power supply cable might cause a short circuit resulting in fire or accidents involving electrical shock.
	Do not unplug the power plug with wet or moist hands. This might cause injuries or equipment malfunctions or failures due to electrical shock.
	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause accidents involving electrical shock or fire due to heat emitted.
	Do not connect many electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Failing to do so may cause the equipment to malfunction or fail, or lead to accidents involving electrical shock or fire due to heat emitted.
	Periodically remove any dust accumulated on the power plug and around the outlet (socket). Do not use a power plug with dust accumulated on it because doing so will lead to insulation failure due to moisture which may lead to fire. Remove any dust on the power plug and around the outlet with dried cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids it may cause the Board to malfunction or lead to accidents involving electrical shock. If you spilled water or other liquid on this Board, immediately stop using the Board, turn off the power, and unplug the power plug. If you have any requests for repairs or technical consultation, please contact the local Macnica company or Mpression inquiry URL.
Caution	Do not place the kit on unstable places such as shaky stands or tilted locations. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures such as in cars in hot weather. Doing so might cause the kit to emit heat, break, ignite, run out of control, warp, or malfunction. Also, some parts of the equipment might emit heat causing burn injuries.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electrical shock.
	Do not place this Board in locations where excessive force is applied to the Board. Failure to do so may cause the PC board to warp, leading to breakage of the PC board, missing parts or malfunctioning parts.

Caution (Continued from previous page)	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of their manuals and to use them correctly. Developer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this Board has been confirmed in separate documents.
	Be sure to turn off the power switch when moving this Board to connect to other devices. Failure to do so may cause this Board to fail or lead to accidents involving electrical shock.
	Do not clean this Board by using a rag containing chemicals such as benzine or thinner. Failure to do so will likely to cause this Board to deteriorate. When using a chemical cloth be sure to comply with any directions or warnings.
	Do not immediately turn on the power if you find that water or moisture had condensed onto the main unit after removing the board from the package. Condensation might occur on this Board when taking it out of the box, if the board is cool yet the room temperature is warm. Do not apply power to the Board while water or moisture has condensed on it because the moisture may cause the Board to break or may shorten the service life of the parts. When you first take this Board out of the box be sure to leave it at room temperature for a while before using it. If condensation or moisture has occurred on this Board, first wait for the moisture to fully evaporate before installing or connecting the Board to other devices.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this kit is customizable, if parts not specified in this Manual as customizable are modified in any way, then the overall product operation cannot be guaranteed. Please consult with developer beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

1.3 Developer Information

The Developer of this product is:
Altima Corp.
1-5-5 Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN
http://www.altima.co.jp

1.4 Inquires

In case you have any inquiries about the use this product, please contact your local Macnica company or make inquiries through the contact form in the following web site:
http://www.m-pression.com/contact

Macnica companies:

• China & HK:	Cytech Technology	http://www.cytech.com/
• ASEAN & India:	Cytech Global	http://www.cytechglobal.com/
• Taiwan:	Galaxy Far East Corp.	http://www.gfec.com.tw/
• North America:	Macnica Americas	http://www.macnica-na.com/
• Brazil:	Macnica DHW	http://www.macnicadhw.com.br/en/
• Japan:	Altima	http://www.altima.co.jp
	Elsena	http://www.elsena.co.jp

2. Important Information

READ FIRST:

- ***READ*** this Reference Manual before using this product.
- ***KEEP*** the Reference Manual handy for future reference.
- ***Do not attempt*** to use the product until you fully understand its mechanism.

Purpose of the Product:

- This product is the Beryll Board; its purpose is to support the evaluation of a system that uses the Cyclone® V GX FPGA, manufactured by Altera® Corporation. It provides support for system development in both software and hardware.

For Users of This Product:

- This product can only be used by operators who have carefully read the user's manual and understand how to use it. Use of this product requires a basic knowledge of electric circuits, logic circuits, and FPGAs.

Precautions to be taken when using This Product:

- This product is an evaluation supporting board for use in your program development and evaluation stages. When mass-producing a program you have finished developing, be sure to decide at your own responsibility whether it can be put to practical use by performing integration test, evaluation, or some other experiment.
- In no event shall Altima Corp. be liable for any consequence arising from the use of this product.
- Altima Corp. cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this reference manual and on the product are therefore not all-inclusive. The user is therefore responsible for the safe use of the product at the user's own responsibility.
- This product is to be used for evaluation of a program, and the evaluation stage. You cannot install the Beryll Board in your product and cannot use the Beryll Board for mass-production.
- The operation of any specific USB memories or SD cards cannot be guaranteed.
- Connection with the apparatus of any specific LAN interfaces cannot be guaranteed.
- This product does not guarantee device functionality.
- Remodeling by the customer is not guaranteed.
- This product is a lead-free mounting product.
- Generally, the brand names carried in this reference manual each constitute a maker's trademark or registered trademark.

Improvement Policy:

- Altima Corp. pursues a policy of continuous improvement in design, performance, and safety of the product. Altima Corp. reserves the right to change, wholly or partially, specifications, design, reference manual, and other documentation at any time without notice.

Warranty:

- Altima Corp offers exchange of this product free of charge only in a set range of cases of initial trouble for this product, and within 30 days from when the customer received delivery of the Board.

Altima Corp. cannot exchange products in cases where breakdown is caused for the following reasons:
(1) Misuse, abuse of the product or use under abnormal conditions
(2) Remodeling and repair
(3) A fire, earthquake, fall or other accidents

Figures:

- Some figures in this reference manual may differ from your system as purchased.

3. Unboxing

Package Components

This product consists of the Board and the parts listed in the table below. Please make sure all components listed below are included as soon as you get the Board.

<table>
<tr><td colspan="2">Customer letter</td></tr>
<tr><td colspan="2">The Beryll Board</td></tr>
<tr><td colspan="2">USB Standard-A to Mini-B plug cable</td></tr>
<tr><td colspan="2">AC adaptor (Output 12 V/3.8 A)</td></tr>
<tr><td>Reference Manual</td><td rowspan="3">Download these files from the web site given in the customer letter.</td></tr>
<tr><td>The Beryll Board circuit diagram</td></tr>
<tr><td>FPGA sample design</td></tr>
</table>

4. The Beryll Board: Hardware Overview

4.1 Overview

The Beryll Board is an FPGA development board that uses Cyclone V GX FPGA, which is a low-cost FPGA manufactured by Altera Corporation. This development board has the following features:

- Users can develop and test user logic flexibly using Cyclone V GX FPGA.
- Users can expand their own system by preparing a daughter card connector (HSMC) manufactured by Altera Corporation.
- With a built-in On-Board USB-Blaster™ circuit, users can download the FPGA configuration circuit by connecting a USB cable.
- Users can use the hard memory controller (HMC), which has been installed in Cyclone V FPGA and later versions, together with DDR3 memory from Micron Technology to carry out evaluations.

4.2 Key Components

Table 1 shows the product specifications of the Beryll Board.

Table 1 Beryll Board Product Specifications

Product Function	Part or Specification
FPGA	5CGXFC4C6F27C
Power Supply	DC 12 V 3.8 A
Dimensions	140.00 mm x 155.00 mm
HSMC	ASP-122953-01
Printed Circuit Board	FR4 10-layer
Configuration ROM	EPCS128SI16N
SRAM	IDT71V416S10PHG8 (512 KByte)
DDR-SDRAM	DDR3-800 256 MBytes (128 MByte x 2) MT41J64MJT
Flash ROM	JS28F256M29EWLA (32 MByte)
USB 2.0 (Mini-B)	CY7C68013A-56LTXC
Audio	UDA1345TS
Ethernet	DP83865DVH
Clock (for FPGA)	27 MHz x 1, 33 MHz x 1, 50 MHz x 1, 125 MHz x 1
JTAG Connector	DIP 10-pin Header, 2.54-mm pitch × 1
Status LED	12 pcs (12V_POWER, HSMC PSNTn, nSTATUS, nCONFIG, CONF_DONE, INIT_DONE, Blaster, ACT,LK10,LK100,LK1000,DUPLEX)
FPGA Reconfiguration Push SW	1 (SYS_RESET)
General-purpose LED	8
General-purpose Push SW	4
General-purpose Dip SW	1 (SW0-SW3)
General-purpose 7 Segment LED	2
Character LCD Connector	1 (3.3-V) * A character LCD is optional.
Power SW	1
RS-232C	DB9 Female Connector

(Note) Although the character LCD connector comes with the Beryll Board, the LCD display is optional. An LCD display should be prepared by the user.

4.3 Block Diagram

Figure 1. shows the block diagram of the Beryll Board. Because the Beryll Board is an evaluation board using the properties of Cyclone V GX FPGA, all of the functions are integrated in Cyclone V GX FPGA.

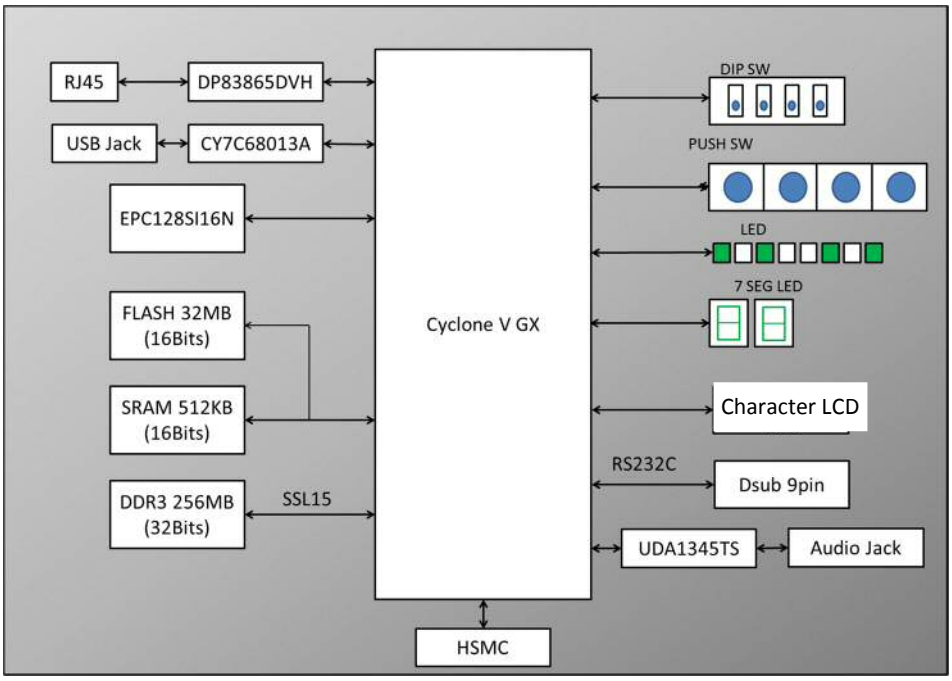


Figure 1 Beryll Board Block Diagram

4.4 Board Specifications

This section describes the layout of switches, connectors, and components on the Beryll Board.

4.4.1 Beryll Switch/Connector Layout

Figure 2 shows the layout of switches and connectors used on the Beryll Board.

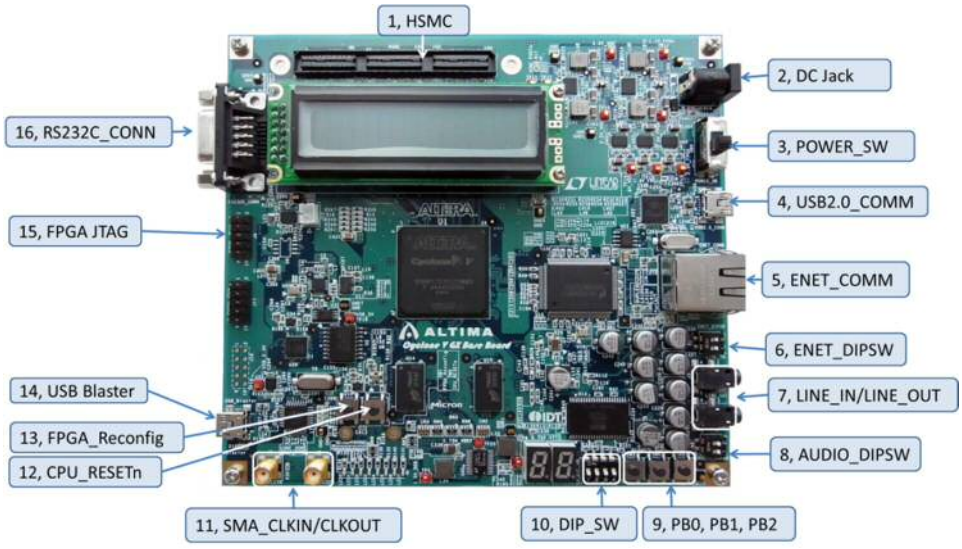


Figure 2 Beryll Switch/Connector layout

1 HSMC
2 DC Jack
3 Power supply switch
4 USB2.0 Mini-B connector
5 Ethernet connector RJ45
6 Ethernet DIP switch
7 Audio line input/output
8 Audio DIP switch
9 General-purpose push switches
10 General-purpose DIP switch
11 SMA_CLKIN/SMA_CLKOUT connectors
12 Reset push switch
13 FPGA reconfiguration push switch
14 USB-blaster switch
15 JTAG connector for FPGA (unimplemented)
16 RS232C connector

4.4.2 Beryll Component Layout

Figure 3 shows the layout of major Beryll components.

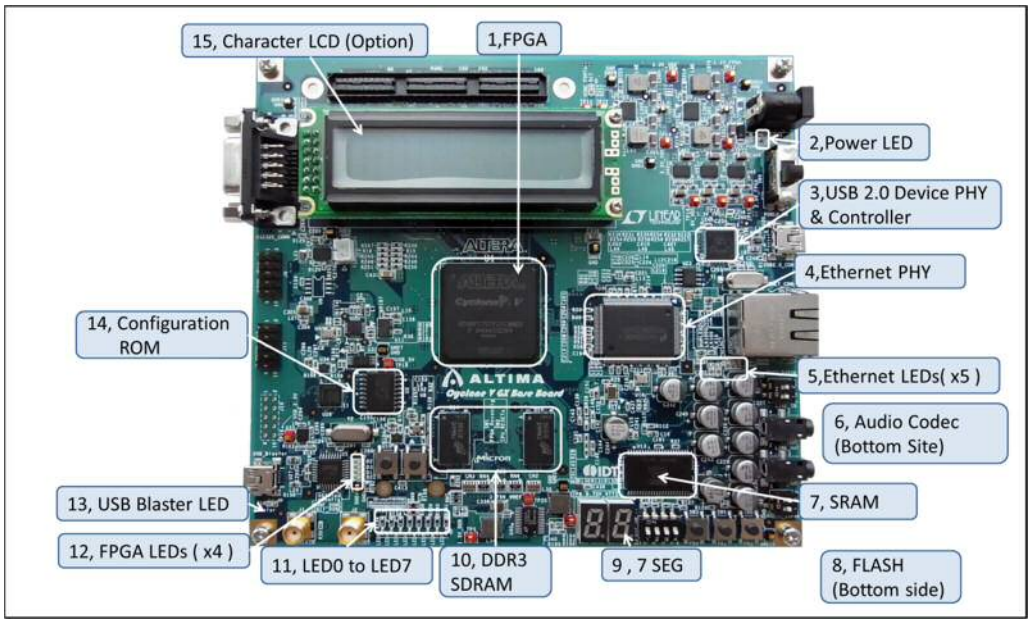


Figure 3 Beryll Component layout

1 Cyclone V GX FPGA
2 Power LED
3 USB2.0 Device PHY and controller
4 Ethernet PHY
5 Ethernet LED × 5
(ACT/ LK10/ LK100/ LK1000/ DUPLEX)
6 Audio Codec
7 SRAM
8 FLASH
9 7 Segment LED
10 DDR3 SDRAM
11 User LED
12 FPGA status LED × 4
(nSTATUS/ nCONFIG/ CONF_DONE/ INIT_DONE)
13 USB_BLASTER LED
14 Configuration ROM
15 Character LCD (Option)

4.4.3 Beryll Switch/LED Layout and Specifications

Figure 4 shows the locations of switches and LEDs on the Beryll Board.

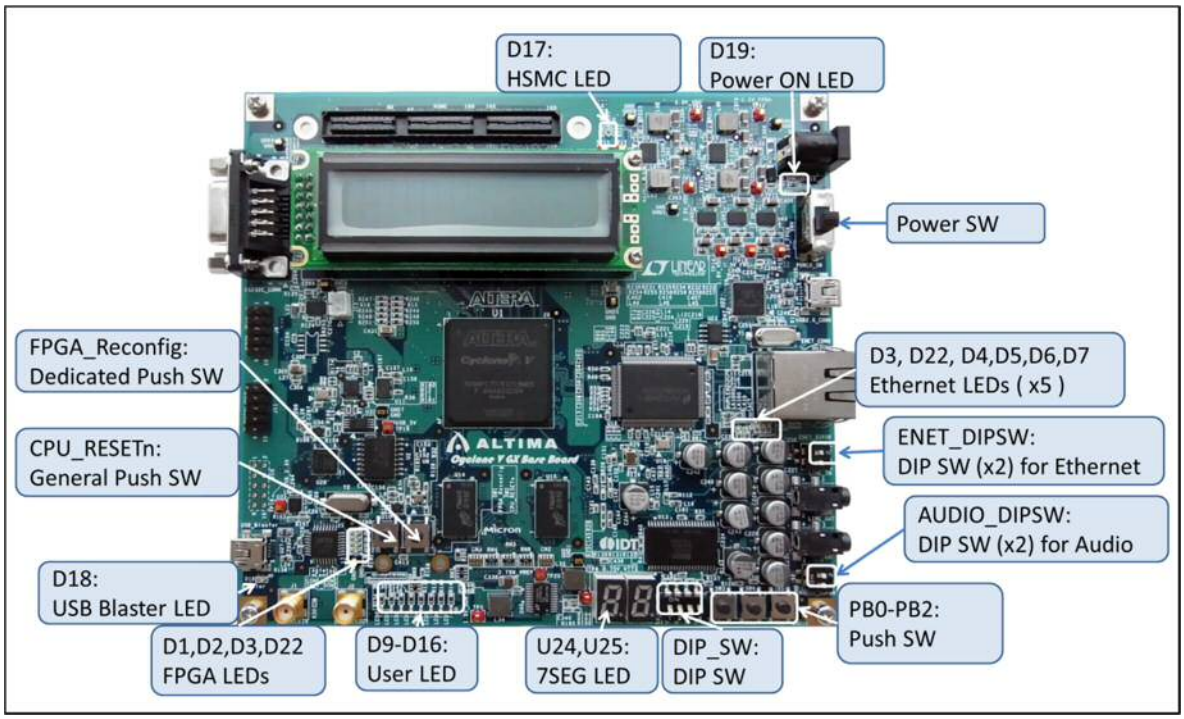


Figure 4 Positions of the Switches and LEDs

Table 2 shows the functions of the LEDs.

Table 2 LED function specifications

Component Location	Function
D1	LED for checking FPGA CONF_DONE
D2	LED for checking FPGA nSTATUS
D3	LED for checking FPGA nCONFIG
D4	ACT: LED for checking communication
D5	LK10: LED for checking link in 10-Mbps communication
D6	LK100: LED for checking link in 100-Mbps communication
D7	LK1000: LED for checking link in 1-Gbps communication
D8	DUPLEX: LED for checking full-duplex communication
D9-D16	General-purpose LED × 8
D17	LED for implementation of the HSMC daughter board
D18	LED for checking the USB-Blaster cable
D19	+12V Power Supply LED
D22	LED for checking FPGA INIT_DONE
U24, U25	General-purpose 7 Segment LED × 2

Table 3 shows the functions of the switches

Table 3 shows the functions of the switches.

Component Location	Default	Function
POWER_SW	Slide Down	Slide Down: Power OFF, Slide Up: Power O
ENET_DIPSW	Both OPEN	CRS/RGMII_SEL0 Open : RGMII - 3COM Short : RGMII - HP COL/CLK_MAC_FREQ Open : 125MHz output Short : 25MHz output
AUDIO_DIPSW	Both OPEN	AUDIO_MP2 Open : StaticPin Low or FPGA Control Short : StaticPin and Mid Voltage AUDIO_MP4 Open : StaticPin High or FPGA Control
DIP_SW	None	Audio Setting DIP SWs (×4)
PU_RESETn, PB0, PB1, PI	None	General-purpose Push SW
FPGA_Reconfig	None	FPGA Reconfiguration Push SW

5. The Beryll Board Components

This chapter describes the FPGA and various components installed on the periphery of the FPGA on the Beryll Board.

5.1 Featured Device: Cyclone V GX FPGA

The Beryll Board carries 28-nm low-cost FPGA Cyclone V GX manufactured by Altera Corporation. Table 4 shows the specifications of the Cyclone V GX FPGA.

Table 4 Cyclone V GX FPGA Specifications

Device	Core Fabric						Internal Connection			Hardware IP	
	Number of LEs	Number of Memory blocks	Block memory (Kb)	MLAB (Kb)	Number of DSP blocks	Number of PLLs	Number of transceivers	Number of GPIO pins	Number of LVDS pairs	Number of PCIe blocks	Number of memory controllers
5CGXC4	50K	250	2,500	295	70	6	6	336	90	2	2

5.2 FPGA and EPCS Configuration ROM Programming

To carry out programming to the FPGA and EPCS ROM, connect the Mini USB Cable that comes with the Beryll Board to USB-Blaster (U27) and write the program in the configuration file. Therefore, users do not need to prepare programming hardware, such as a USB-Blaster cable from Altera, separately.

5.2.1 Preface

Use the Quartus® II Programmer to perform programming (writing the programming file into the configuration file) for the device. When being used for the first time, it is necessary to install the drivers for each piece of programming hardware.

5.2.2 How to Perform Programming for the FPGA

This section introduces the basic operations for programming.

A. Starting Programmer

Connect the programming hardware, and then select the Tools Menu in Quartus II and then "Programmer", or click the  button.

B. Selecting a programming mode

From the Mode pull-down list, select a method for writing the programming file into the device. Select JTAG for the Beryll Board.

C. Setting the programming hardware

a. Click the Hardware Setup button

b. Select the Hardware Settings tab in the Hardware Setup window.

c. From the Current selected hardware pull-down list, select the programming hardware to be used (Move on to step ④).

   If there is no programming hardware to use in the pull-down list, click the Add Hardware button.

d. Select USB-Blaster from Hardware type in the Add Hardware dialog box and click the OK button.

e. Select USB-Blaster from Currently selected hardware in the Hardware Setup window and click the Close button.

D. Programming

a. Click the 

button to select a programming file (*.SOF) to write into the device.

b. To write data into the device, check the Program/Configure box as a programming option.

c. Click the 

button to start programming.

Reference information

* POF file (*.pof): Programming file for the MAX® CPLD series and configuration device
* SOF file (*.sof): Programming file for FPGA of Stratix® FPGA, Arria® FPGA, and Cyclone FPGA
* JIC file (*.jic): Programming file for configuration device

Reference information

◆ Program/Configure

Writes programming data (performs programming) into the device.

◆ Verify

Compares the contents of the programming data registered in Programmer with the contents written in the device to verify the programming data.

◆ Blank-Check

Confirms that the device is completely empty (that the contents in the device have been completely deleted).

◆ Examine

Loads programming data which has been written in the MAX CPLD devices or configuration device. The data which has been loaded can be saved as a programming file.

* Data that has been written when the Security Bit option (see the next item) was enabled cannot be loaded correctly.
* Executing Examine will not delete the data in the device.
* Data that has been loaded cannot be restored to the design file.

- Security Bit

  Prevents the data that has been written into the device from being checked or the data which has been loaded by Examine from being copied when re-programmed. (This option is supported only for MAX® 7000 and MAX® 3000.)

- Erase

  Deletes data stored in the MAX CPLD device or configuration device.

- ISP CLAMP

  Uses the IPS file (*.ips) to set the I/O pin status in programming. (This option is supported only for MAX® 7000B and MAX® II.)

5.3 Programming to the EPCS Configuration device

5.3.1 Preface

With the JTAG Indirect Configuration (JIC) file for the FPGA device, you can perform programming of the EPCS device which does not support the JTAG interface through the JTAG chain.

5.3.2 Outline of JIC

When the EPCS device is used as a configuration device for the Cyclone V device, the data transfer method supports the active serial configuration mode (AS mode). To perform configuration in AS mode, a 10-pin header used to perform programming in AS mode is required in the EPCS device. On the other hand, to configure data for the FPGA through the JTAG port or to perform debugging using SignalTap® II, another 10-pin header for JTAG is also needed.

However, the JIC function is used, the serial flash loader design in the FPGA works as a bridge, and so programming for the EPCS device can be performed through the JTAG port. For this reason, the 10-pin header for the AS mode is no longer needed, which allows users to reduce both the board area and the cost.

5.3.3 Programming method for EPCS configuration ROM

Programming through the serial flash loader is performed using a JIC file, instead of using a traditional SOF file or POF file. To perform programming, create a JIC file from the SOF file, a configuration file for FPGA.

The flow of this operation is as follows:

Step 1: Compiling the design (creating a programming file)

Step 2: Creating a JIC file

Step 3: Programming

Step 1: Compiling the design

Compile the design in order to create a configuration file (.sof) which will be the basis for the JIC file.

– Select the Processing menu and then Start Compilation, or click the  button.

Step 2: Creating a JIC file

Create a *.jic file which will be the programming file for JIC from the SOF file which has been generated after compilation.

1) Select the File menu and then Convert Programming Files.
2) In Output Programming File, set a file format to create, configuration device, and output file name.
   - Select JTAG Indirect Configuration File (.jic) as a Programming file type.
   - In Configuration device, set the type of the configuration device for which programming will be performed.
   - Select EPCS128 for the Beryll Board.
   - Specify a generation path of the output file and an output file name for File name.
     1. In Input files to convert, select a type of FPGA for which the serial flash loader design is used.
   - Select the Flash Loader line and click the Add Device button.
   - In the Select Device dialog box, select Cyclone V GX for Device family and select Device name, and click the OK button.
     2. Specify a configuration file (.sof) that will be the basis for the JIC file.
   - Select the SOF Data line and click the Add File button.
   - Select as SOF file to convert and click the Open button.
     3. To compress a programming file, select an SOF to be compressed and click the Properties button. In the SOF File Properties dialog box, check the Compression option box and click the OK button.
     4. Click the Generate button.

   A message reading “Generated <jic file name> successfully” is displayed and creation of the JIC file is complete.

Step 3 : Programming

Programming of the JIC file you have created to the EPCS device is performed in JTAG mode.

1) Start Programmer.

   Select the Tools menu and then Programmer, or click the  button.
2) Select hardware (download cable) to be used and select JTAG for Mode.
3) Click the 

button and select a JIC file.
4) Check the Program/Configure option box on the JIC file line.
5) Click the 

button to start programming.

   The serial flash loader in the FPGA device becomes enabled first, and then EPCS programming is executed through the serial flash loader. When the programming is completed successfully, the Progress gauge (in the upper right of the Programmer window) reaches 100%

and a message informing you of the successful completion of programming is shown in the Message dialog box.

You have now completed programming of the EPCS device by JTAG Indirect Configuration.

5.4 Connector Pin Assignment

Figure 5 shows the locations of connectors and the pin assignment of each connector.

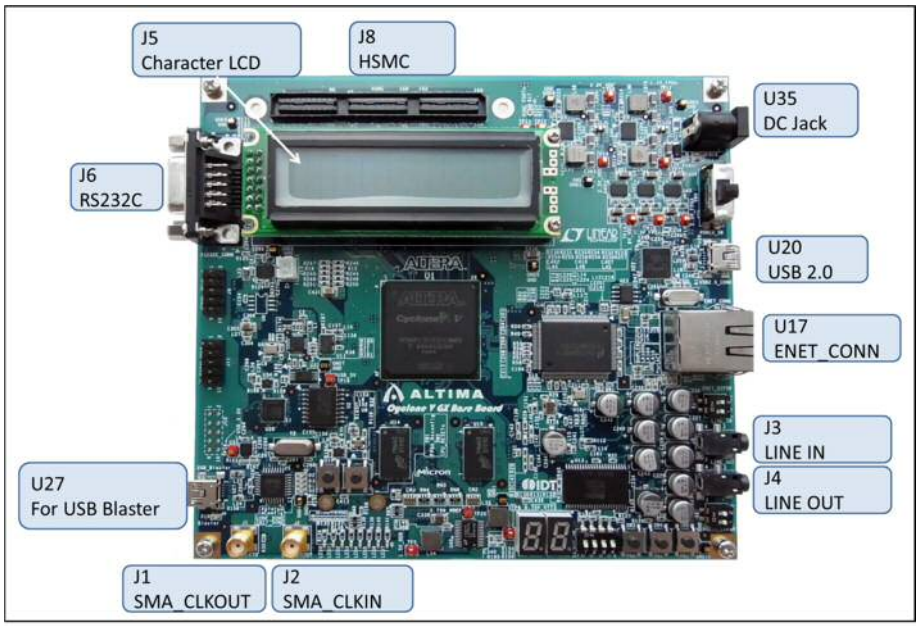
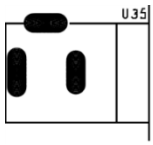


Figure 5. Beryll Connector Assignment

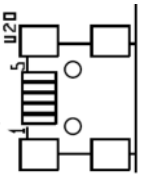
01. U35 (DC jack)

Pin	Signal Name	Pin	Signal Name
1	12V	2	NC
3	GND		



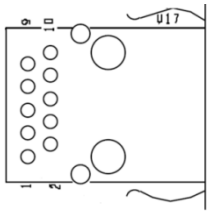
02. U20 (USB 2.0_CONN)

Pin	Signal Name	Pin	Signal Name
1	V_BUS	2	D +
3	D-	4	ID
5	G		



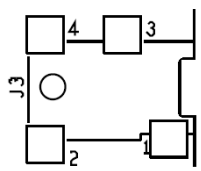
03. U17 (ENET_CONN)

Pin	Signal Name	Pin	Signal Name
1	TD0_P	2	TD0_N
3	TD1_P	4	TD1_N
5	TD2_P	6	TD2_N
7	TD3_P	8	TD3_N
9	VCC	10	GND
11	GND_TAB	12	GND_TAB



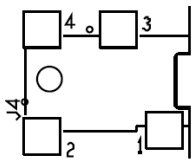
04. J3 (Audio Line In)

Pin	Signal Name	Pin	Signal Name
1	GND	2	L
3	R	4	NCl



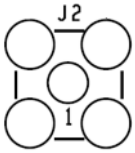
05. J4 (Audio Line Out)

Pin	Signal Name	Pin	Signal Name
1	GND	2	L
3	R	4	NCl



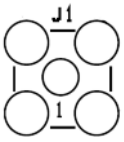
06. J2 (SMA CLKIN)

Pin	Signal Name	Pin	Signal Name
1	SMA_CLK_IN	2	NC
3	NC	4	NC
5	NC		



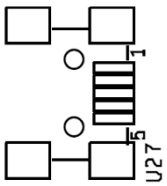
07. J1 (SMA CLKOUT)

Pin	Signal Name	Pin	Signal Name
1	SMA_CLK_OUT	2	NC
3	NC	4	NC
5	NC		



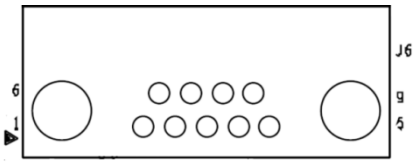
08. U27 (USB-Blaster)

Pin	Signal Name	Pin	Signal Name
1	V_BUS	2	D+
3	D-	4	ID
5	G		



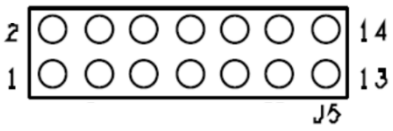
9. J6 (RS232C DSub9 Pin Female Connector)

Pin	Signal Name	Pin	Signal Name
1	NC	2	UART_TXD
3	UART_RXD	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC		

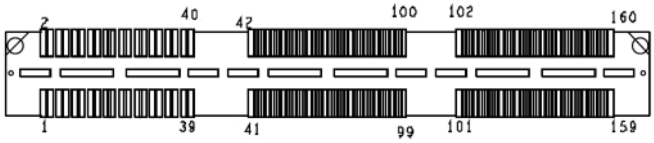


10. J5 (Character LCD)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	NC	4	LCD_RS
5	LCD_RW	6	LCD_E
7	LCD_DATA0	8	LCD_DATA1
9	LCD_DATA2	10	LCD_DATA3
11	LCD_DATA4	12	LCD_DATA5
13	LCD_DATA6	14	LCD_DATA7



11. J8 (HSMC Connector)



Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1		2		81		82	
3		4		83	HSMC_2_DATAOUT6_P	84	HSMC_2_DATAIN6_P
5		6		85	HSMC_2_DATAOUT6_N	86	HSMC_2_DATAIN6_N
7		8		87		88	
9		10		89	HSMC_2_DATAOUT7_P	90	HSMC_2_DATAIN7_P
11		12		91	HSMC_2_DATAOUT7_N	92	HSMC_2_DATAIN7_N
13		14		93		94	
15		16		95	HSMC_2_CLKOUT_P	96	HSMC_2_CLKIN_P
17	GX_TXD3_P	18	GX_RXD3_P	97	HSMC_2_CLKOUT_N	98	HSMC_2_CLKIN_N
19	GX_TXD3_N	20	GX_RXD3_N	99		100	
21	GX_TXD2_P	22	GX_RXD2_P	101	HSMC_3_DATAOUT0_P	102	HSMC_3_DATAIN0_P
23	GX_TXD2_N	24	GX_RXD2_N	103	HSMC_3_DATAOUT0_N	104	HSMC_3_DATAIN0_N
25	GX_TXD1_P	26	GX_RXD1_P	105		106	
27	GX_TXD1_N	28	GX_RXD1_N	107	HSMC_3_DATAOUT1_P	108	HSMC_3_DATAIN1_P
29	GX_TXD0_P	30	GX_RXD0_P	109	HSMC_3_DATAOUT1_N	110	HSMC_3_DATAIN1_N
31	GX_TXD0_N	32	GX_RXD0_N	111		112	
33	HSMC_1_DATA0	34	HSMC_1_DATA1	113	HSMC_3_DATAOUT2_P	114	HSMC_3_DATAIN2_P
35	HSMC_1_DATA2	36	HSMC_1_DATA4	115	HSMC_3_DATAOUT2_N	116	HSMC_3_DATAIN2_N
37	HSMC_1_DATA4	38	HSMC_1_DATA5	117		118	
39	HSMC_1_CLKOUT	40	HSMC_1_CLKIN	119	HSMC_3_DATAOUT3_P	120	HSMC_3_DATAIN3_P
41	HSMC_DATA0	42	HSMC_DATA1	121	HSMC_3_DATAOUT3_N	122	HSMC_3_DATAIN3_N
43	HSMC_DATA2	44	HSMC_DATA3	123		124	
45		46		125	HSMC_3_DATAOUT4_P	126	HSMC_3_DATAIN4_P
47	HSMC_2_DATAOUT0_P	48	HSMC_2_DATAIN0_P	127	HSMC_3_DATAOUT4_N	128	HSMC_3_DATAIN4_N
49	HSMC_2_DATAOUT0_N	50	HSMC_2_DATAIN0_N	129		130	
51		52		131	HSMC_3_DATAOUT5_P	132	HSMC_3_DATAIN5_P
53	HSMC_2_DATAOUT1_P	54	HSMC_2_DATAIN1_P	133	HSMC_3_DATAOUT5_N	134	HSMC_3_DATAIN5_N
55	HSMC_2_DATAOUT1_N	56	HSMC_2_DATAIN1_N	135		136	
57		58		137	HSMC_3_DATAOUT6_P	138	HSMC_3_DATAIN6_P
59	HSMC_2_DATAOUT2_P	60	HSMC_2_DATAIN2_P	139	HSMC_3_DATAOUT6_N	140	HSMC_3_DATAIN6_N
61	HSMC_2_DATAOUT2_N	62	HSMC_2_DATAIN2_N	141		142	
63		64		143	HSMC_3_DATAOUT7_P	144	HSMC_3_DATAIN7_P
65	HSMC_2_DATAOUT3_P	66	HSMC_2_DATAIN3_P	145	HSMC_3_DATAOUT7_N	146	HSMC_3_DATAIN7_N
67	HSMC_2_DATAOUT3_N	68	HSMC_2_DATAIN3_N	147		148	
69		70		149	HSMC_3_DATAOUT8_P	150	HSMC_3_DATAIN7_P
71	HSMC_2_DATAOUT4_P	72	HSMC_2_DATAIN4_P	151	HSMC_3_DATAOUT8_N	152	HSMC_3_DATAIN7_N
73	HSMC_2_DATAOUT4_N	74	HSMC_2_DATAIN4_N	153		154	
75		76		155	HSMC_3_CLKOUT_P	156	HSMC_3_CLKIN_P
77	HSMC_2_DATAOUT5_P	78	HSMC_2_DATAIN5_P	157	HSMC_3_CLKOUT_N	158	HSMC_3_CLKIN_N
79	HSMC_2_DATAOUT5_N	80	HSMC_2_DATAIN5_N	159		160	

5.5 Serial Port

The Beryll Board has an asynchronous serial port. An LTC2803 FPGA transceiver and a 9-pin D SUB connector from Linear Technology's LTC2803 are used for RS232C interface. For pin information on the FPGA, LTC2803, and D SUB connector, see Figure 6 and the pin list shown below. When purchasing a serial cable, choose a straight type. For details of Linear Technology's LTC2803, visit the following URL:

http://www.linear.com/product/LTC2803

Note: The URL above is subject to change without notice.

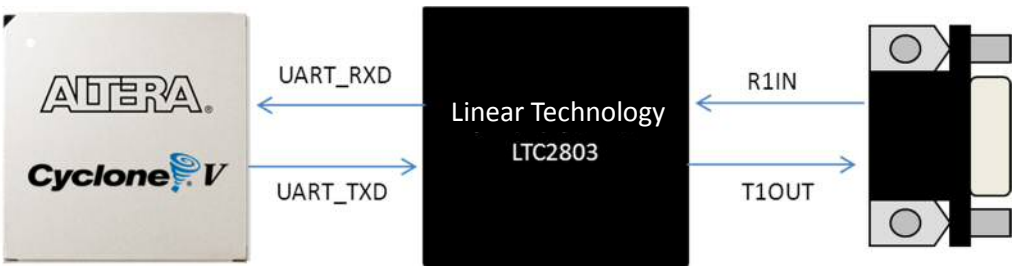


Figure 6 Connections of the FPGA, LTC2803, and DB9 Connector

Table 5. RS232C pin list

Schematic Signal Name	Detail of Signal	FPGA Pin Number	LTC2803 Pin Number (on FPGA side)	LTC2803 Pin Number (on D SUB side)	D SUB Pin Number
UART_TXD	Transmitter	Bank 8A_K6	14	3	2
UART_RXD	Receiver	Bank 8A_L7	16	1	3

5.6 DDR3 SDRAM

The Beryll Board has two MT41J64M16JT (16 bits, 128 MBytes) manufactured by Micron Technology, Inc and they are connected to the hard memory controller (HMC) of the FPGA. Users can evaluate the hard memory controller of Cyclone V GX FPGA by using the attached reference design. For pin information of the Cyclone V GX FPGA and DDR3 memory, see Figure 7.

The data sheet for Micron's MT41J64M16JT can be obtained from the following URL:

http://www.micron.com/parts/dram/ddr3-sdram/mt41j64m16jt-15e

Note: The URL above is subject to change without notice.

Note: The DDR3 memory installed on the Beryll Board may be replaced by an equivalent product that satisfies conditions for realizing DDR3 800 Mbps

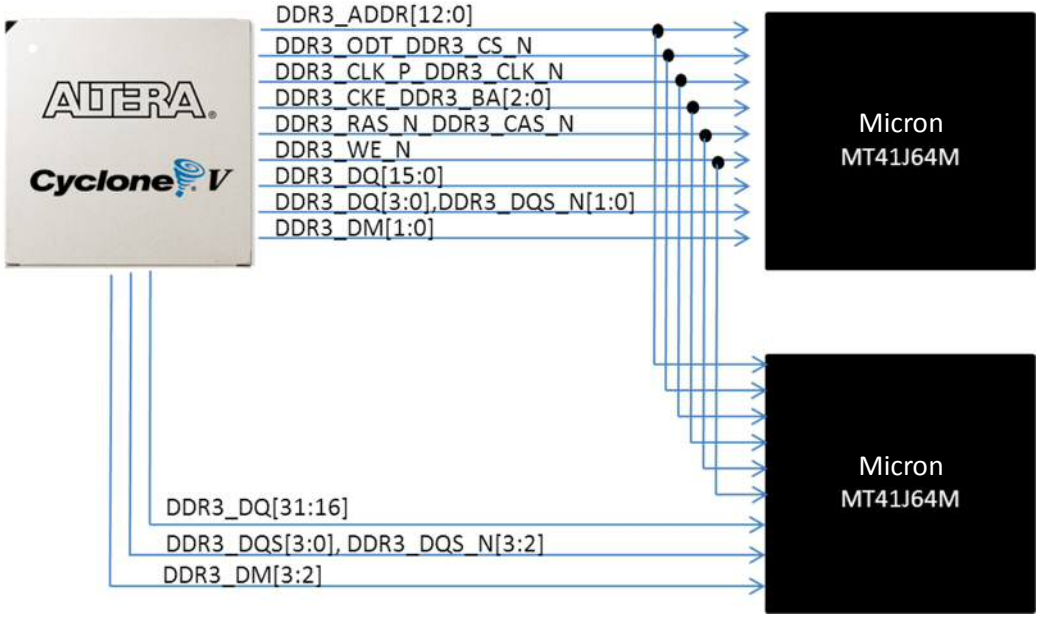


Figure 7 Connections of the FPGA and DDR3 Memory

Table 6 Pin Information of the FPGA and DDR3 Memory

Signal Name	FPGA Pin Number	DDR#0 Pin Number	DDR#1 Pin Number	Signal Name	FPGA Pin Number	DDR#0 Pin Number	DDR#1 Pin Number
DDR3_ADDR0	AE6	N3	N3	DDR3_DQ8	AC15	D7	
DDR3_ADDR1	AF6	P7	P7	DDR3_DQ9	AB15	C3	
DDR3_ADDR2	AF7	P3	P3	DDR3_DQ10	AC14	C8	
DDR3_ADDR3	AF8	N2	N2	DDR3_DQ11	AF13	C2	
DDR3_ADDR4	U10	P8	P8	DDR3_DQ12	AB16	A7	
DDR3_ADDR5	U11	P2	P2	DDR3_DQ13	AA16	A2	
DDR3_ADDR6	AE9	R8	R8	DDR3_DQ14	AE14	B8	
DDR3_ADDR7	AF9	R2	R2	DDR3_DQ15	AF18	A3	
DDR3_ADDR8	AB12	T8	T8	DDR3_DQ16	AD16		F3
DDR3_ADDR9	AB11	R3	R3	DDR3_DQ17	AD17		F7
DDR3_ADDR10	AC9	I7	I7	DDR3_DQ18	AC18		F2
DDR3_ADDR11	AC8	R7	R7	DDR3_DQ19	AF19		F8
DDR3_ADDR12	AB10	N7	N7	DDR3_DQ20	AC17		H3
DDR3_BA0	V10	M2	M2	DDR3_DQ21	AB17		H8
DDR3_BA1	AD8	N8	N8	DDR3_DQ22	AF21		G2
DDR3_BA2	AE8	M3	M3	DDR3_DQ23	AE21		H7
DDR3_DM0	AF11	E7		DDR3_DQ24	AE15		D7
DDR3_DM1	AE18	D3		DDR3_DQ25	AE16		C3
DDR3_DM2	AE20	E7		DDR3_DQ26	AC20		C8
DDR3_DM3	AA14		D3	DDR3_DQ27	AD21		C2
DDR3_CS_N	R11	L2	L2	DDR3_DQ28	AF16		A7
DDR3_CAS_N	W10	K3	K3	DDR3_DQ29	AF17		A2
DDR3_RAS_N	Y10	J3	J3	DDR3_DQ30	AD23		B8
DDR3_WE_N	T9	L3	L3	DDR3_DQ31	AF23		A3
DDR3_RESET_N	AE19	T2	T2	DDR3_DQS_P1		C7	
DDR3_ODT	AD13	K1	K1	DDR3_DQS_N1		B7	
DDR3_DQ0	AA14	F3		DDR3_DQS_P0		F3	
DDR3_DQ1	Y14	F7		DDR3_DQS_N0		G3	
DDR3_DQ2	AD11	F2		DDR3_DQS_P3			C7
DDR3_DQ3	AD12	F8		DDR3_DQS_N3			B7
DDR3_DQ4	Y13	H3		DDR3_DQS_P0			F3
DDR3_DQ5	W12	H8		DDR3_DQS_N0			G3
DDR3_DQ6	AD10	G2		DDR3_CLK_P		J7	J7
DDR3_DQ7	AF12	H7		DDR3_CLK_N		K7	K7
				DDR3_CKE		K9	K9

5.7 FLASH/SRAM

The Beryll Board has JS28F256M29EWL (16-bit width, 256 Mbits) Flash ROM manufactured by Micron Technology, Inc and IDT71V416S10PHG8 (16-bit width, 4 Mbits) SRAM manufactured by Integrated Device Technology® (IDT). The address and data bus are shared by the Flash ROM and SRAM. You can use the Flash ROM for booting the Nios® II software and use the SRAM as a cache ROM for Nios II when you use a Nios II processor for Cyclone V GX FPGA. These devices can also be used as general-purpose Flash ROM and SRAM respectively. For pin information of the Flash ROM and SRAM, see Figure 8.

The data sheet for the Flash ROM can be obtained from the following URL:

http://www.micron.com/parts/nor-flash/parallel-nor-flash/js28f256m29ewla?pc={9A9BFAD5-DEE0-49F7-ACE8-ED039D2582D6}

Note: The URL above is subject to change without notice.

The data sheet for the SRAM can be obtained from the following URL:

http://ja.idt.com/products/memory-logic/srams/asynchronous-srams/71v416-33v-256k-x-16-asynchronous-static-ram-center-pwr-gnd-pinout

Note: The URL above is subject to change without notice.

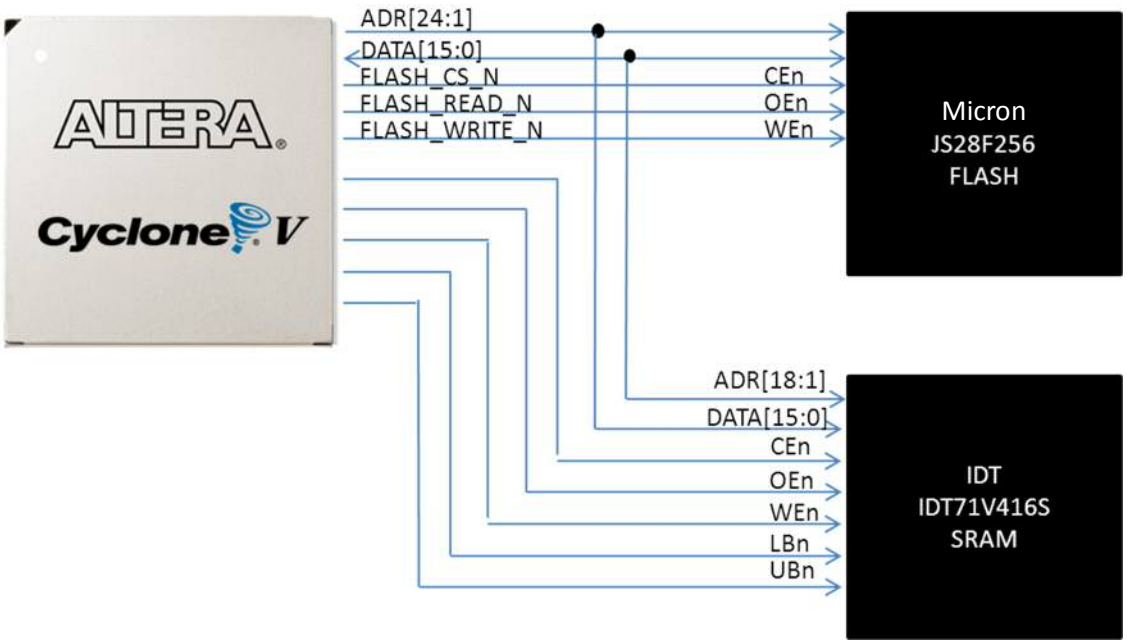


Figure 8 Pin Information of the FPGA and FLASH/SRAM

Table 7 Pin Information of the FPGA and FLASH/SRAM

Signal Name	FPGA Pin Number	FLASH Pin Number	SRAM Pin Number	Signal Name	FPGA Pin Number	FLASH Pin Number	SRAM Pin Number
FLASH_ADDRESS1	AD26	A0	A0	FLASH_DATAO	V24	DQ0	DQ0
FLASH_ADDRESS2	AF26	A1	A1	FLASH_DATA1	V23	DQ1	DQ1
FLASH_ADDRESS3	AE25	A2	A2	FLASH_DATA2	W26	DQ2	DQ2
FLASH_ADDRESS4	AF24	A3	A3	FLASH_DATA3	W25	DQ3	DQ3
FLASH_ADDRESS5	AE23	A4	A4	FLASH_DATA4	AA26	DQ4	DQ4
FLASH_ADDRESS6	AB22	A5	A5	FLASH_DATA5	AA24	DQ5	DQ5
FLASH_ADDRESS7	AD22	A6	A6	FLASH_DATA6	AB26	DQ6	DQ6
FLASH_ADDRESS8	AF22	A7	A7	FLASH_DATA7	AB25	DQ7	DQ7
FLASH_ADDRESS9	AA21	A8	A8	FLASH_DATA8	AC25	DQ8	DQ8
FLASH_ADDRESS10	Y20	A9	A9	FLASH_DATA9	AD25	DQ9	DQ9
FLASH_ADDRESS11	AD20	A10	A10	FLASH_DATA10	Y24	DQ10	DQ10
FLASH_ADDRESS12	V19	A11	A11	FLASH_DATA11	Y23	DQ11	DQ11
FLASH_ADDRESS13	Y19	A12	A12	FLASH_DATA12	AA23	DQ12	DQ12
FLASH_ADDRESS14	AB19	A13	A13	FLASH_DATA13	AA22	DQ13	DQ13
FLASH_ADDRESS15	AC19	A14	A14	FLASH_DATA14	AC23	DQ14	DQ14
FLASH_ADDRESS16	AD18	A15	A15	FLASH_DATA15	AC22	DQ15/A-1	DQ15
FLASH_ADDRESS17	AA18	A16	A16	FLASH_CS_N	U22	CE_N	
FLASH_ADDRESS18	Y18	A17	A17	FLASH_READ_N	V22	OE_N	
FLASH_ADDRESS19	W18	A18		FLASH_WRITE_N	W21	WE_N	
FLASH_ADDRESS20	V18	A19		SRAM_CS_N	V20		CS_N
FLASH_ADDRESS21	V17	A20		SRAM_OE_N	U15		OE_N
FLASH_ADDRESS22	U17	A21		SRAM_WRITE_N	T17		WE_N
FLASH_ADDRESS23	Y16	A22		SRAM_BE0_N	U20		BLE_N
FLASH_ADDRESS24	U16	A23		SRAM_BE1_N	T19		BLH_N

5.8 USB 2.0

The Beryll Board has EZ-USB® CY7C68013A-56LTXC manufactured by Cypress Semiconductor Corporation for USB2.0 interface. This device works as a controller for USB2.0 interface, in which a USB controller with a USB2.0 transceiver and 8051 microprocessor, and 16-KB RAM are integrated. The Cyclone V GX FPGA installed on the Beryll Board receives signals at the GPIF level from

Cypress Semiconductor's EZ-USB. For pin information of the FPGA and CY7C68013, see Figure 9 and the pin assignment list shown below. The data sheet for Cypress Semiconductor's EZ-USB can be obtained from the following URL:

http://www.cypress.com/?mpn=CY7C68013A-56LTXC

Note: The URL above is subject to change without notice.

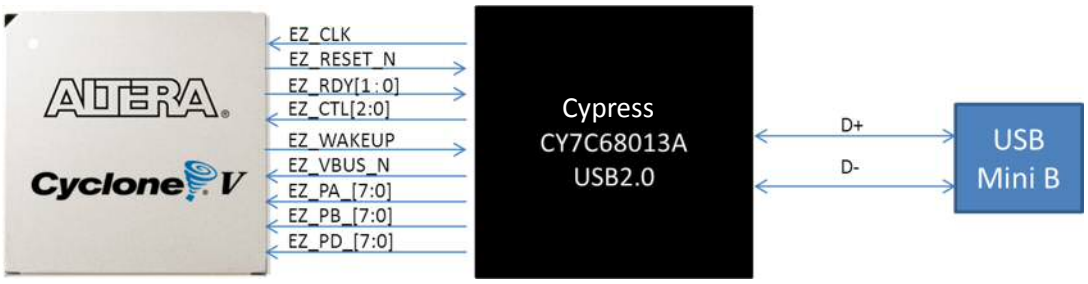


Figure 9 Connections of the FPGA and EZ-USB

Table 8. Pin Information of the FPGA and EZ-USB

Signal Name	FPGA Pin Number	USB Pin Number	Signal Name	FPGA Pin Number	USB Pin Number
EZ_PA0	G25	33	EZ_PD0	B26	45
EZ_PA1	G24	34	EZ_PD1	B25	46
EZ_PA2	G22	35	EZ_PD2	C25	47
EZ_PA3	H25	36	EZ_PD3	D26	48
EZ_PA4	H24	37	EZ_PD4	D25	49
EZ_PA5	H23	38	EZ_PD5	D22	50
EZ_PA6	H22	39	EZ_PD6	E26	51
EZ_PA7	J23	40	EZ_PD7	E25	52
EZ_PB0	E24	18	EZ_RDY0	J25	1
EZ_PB1	E23	19	EZ_RDY1	J26	2
EZ_PB2	E21	20	EZ_CLK	K25	13
EZ_PB3	F24	21	EZ_WAKEUP	K26	44
EZ_PB4	F23	22	EZ_RESET_N	L23	32
EZ_PB5	F22	23	EZ_CTL0	K24	29
EZ_PB6	F21	24	EZ_CTL1	K23	30
EZ_PB7	G26	25	EZ_CTL2	L24	31

5.9 10/100/1000 Ethernet

The Beryll Board has DP83865DVH manufactured by Texas Instruments, Inc for Ethernet interface. Texas Instruments' DP83865DVH is an ultra-low-power-consumption transceiver for Ethernet interface using a 1.8-V, 0.18-µ process. For pin information of the FPGA and DP83865DVH, see Figure 10 and the pin assignment list shown below.

The data sheet for this LSI can be obtained from the following URL:
http://www.ti.com/product/dp83865

Note: The URL above is subject to change without notice.

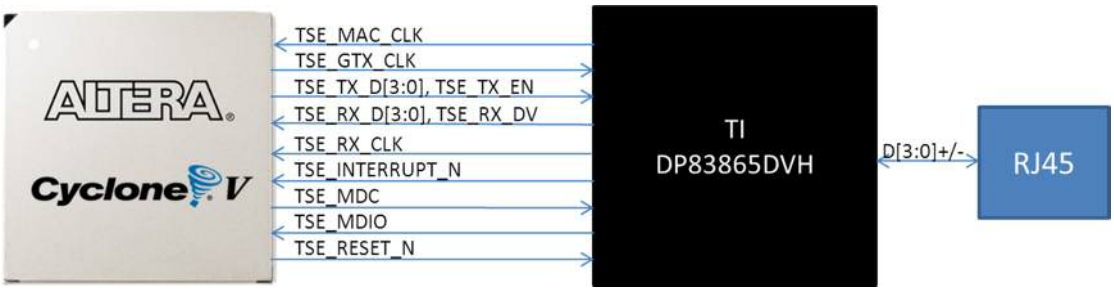


Figure 10. Connection of the FPGA and DP83865DVH

Table 9. Pin Assignment list of the FPGA and DP83865DVH

Signal Name	FPGA Pin Number	DP83865 Pin Number
TSE_MAC_CLK	N20	85
TSE_RESET_N	P21	33
TSE_RX_CLK	R20	44
TSE_RX_DV	R25	41
TSE_RX_D0	R26	56
TSE_RX_D1	P26	55
TSE_RX_D2	P23	52
TSE_RX_D3	N25	51
TSE_GTX_CLK	F26	79
TSE_TX_EN	N23	62
TSE_TX_D0	N24	76
TSE_TX_D1	M26	75
TSE_TX_D2	M25	72
TSE_TX_D3	M24	71
TSE_MDIO	R23	80
TSE_MDC	P22	81
TSE_INTERRUPT_N	P20	3

5.10 24-bit Audio Codec

The Beryll Board has UDA1345TS manufactured by NXP Semiconductors N.V. for 24-bit CODEC for audio interface. For pin information of the FPGA and UDA1345TS, see Figure 11 and the pin assignment list shown below.

The data sheet for this device can be obtained from the following URL:

http://www.nxp.com/documents/data_sheet/UDA1345TS.pdf

Note: The URL above is subject to change without notice.

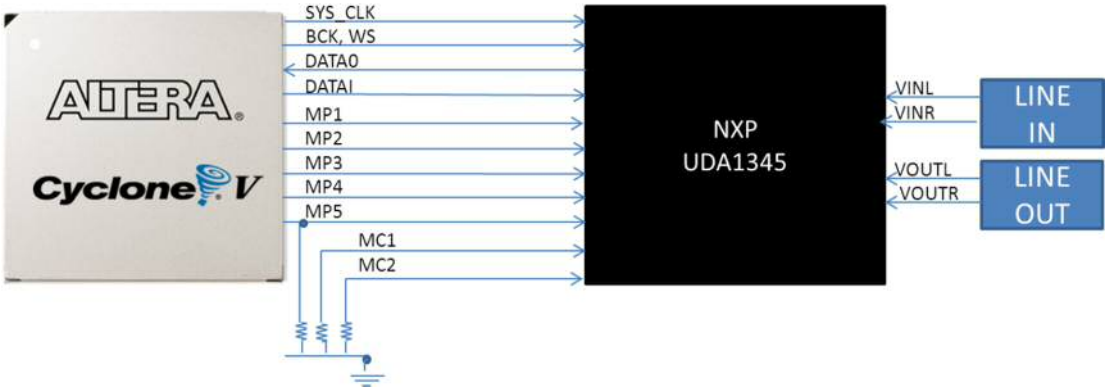


Figure 11 Connection of the FPGA and UDA1345

Table 10. Pin assignment list of the FPGA and UDA1345

Signal Name	FPGA Pin Number	Audio Pin Number
AUDIO_SYSCLK	Y25	12
AUDIO_BCK	Y26	16
AUDIO_DI	T26	18
AUDIO_WS	U25	17
AUDIO_DO	U26	19
AUDIO_MC	T22	8/21
AUDIO_MP1	T24	9
AUDIO_MP2	U24	13
AUDIO_MP3	V25	14
AUDIO_MP4	R24	15
AUDIO_MP5	T23	20

5.11 User Interfaces

The Beryll Board provides various input interfaces that can be set uniquely by the user. Those user interfaces include eight LEDs, two 7-SEGs, four push buttons, one DIP switch, one character LCD, and one UART. For details of the specifications of each pin, see the pin list shown below.

Table 11. Pin Assignment list of the Input Interfaces

Signal Name	FPGA Pin Number	Function	Signal Name	FPGA Pin Number	Function
LED_N0	H19	LED8~0	DIPSW0	P12	User DIP SW
LED_N1	G20		DIPSW1	T12	
LED_N2	H20		DIPSW2	U9	
LED_N3	J20		DIPSW3	V9	
LED_N4	J21		LCD_DATA0	H7	Character LCD
LED_N5	K21		LCD_DATA1	H8	
LED_N6	M22		LCD_DATA2	H9	
LED_N7	M21		LCD_DATA3	G6	
SEVEN_SEG0	AD7	SEVEN SEG 0	LCD_DATA4	G7	
SEVEN_SEG1	AD6		LCD_DATA5	F6	
SEVEN_SEG2	AB6		LCD_DATA6	F7	
SEVEN_SEG3	AA7		LCD_DATA7	E6	
SEVEN_SEG4	AA6		LCD_E	J8	
SEVEN_SEG5	Y9		LCD_RS	J7	
SEVEN_SEG6	Y8		LCD_RW	K9	
SEVEN_SEG7	W8		PUSHSW_N0	AB24	User Push Button
SEVEN_SEG8	V8	SEVEN SEG 1	PUSHSW_N1	W20	
SEVEN_SEG9	U7		PUSHSW_N2	AC13	
SEVEN_SEG10	T8		PUSHSW_N3	V12	
SEVEN_SEG11	T7		UART RXD	L7	UART
SEVEN_SEG12	R10		UART TXD	K6	
SEVEN_SEG13	R9				
SEVEN_SEG14	R8				
SEVEN_SEG15	P8				

5.12 Clock Circuitry

This section describes the board's clock inputs and outputs.

5.12.1 On-board clock source

The Beryll Board includes clock sources for Cyclone V GX FPGA with a frequency of 27-MHz, 33MHz, 50-MHz, and 125-MHz.
Figure 12 shows the default frequencies of all external clocks going to the Beryll Board.

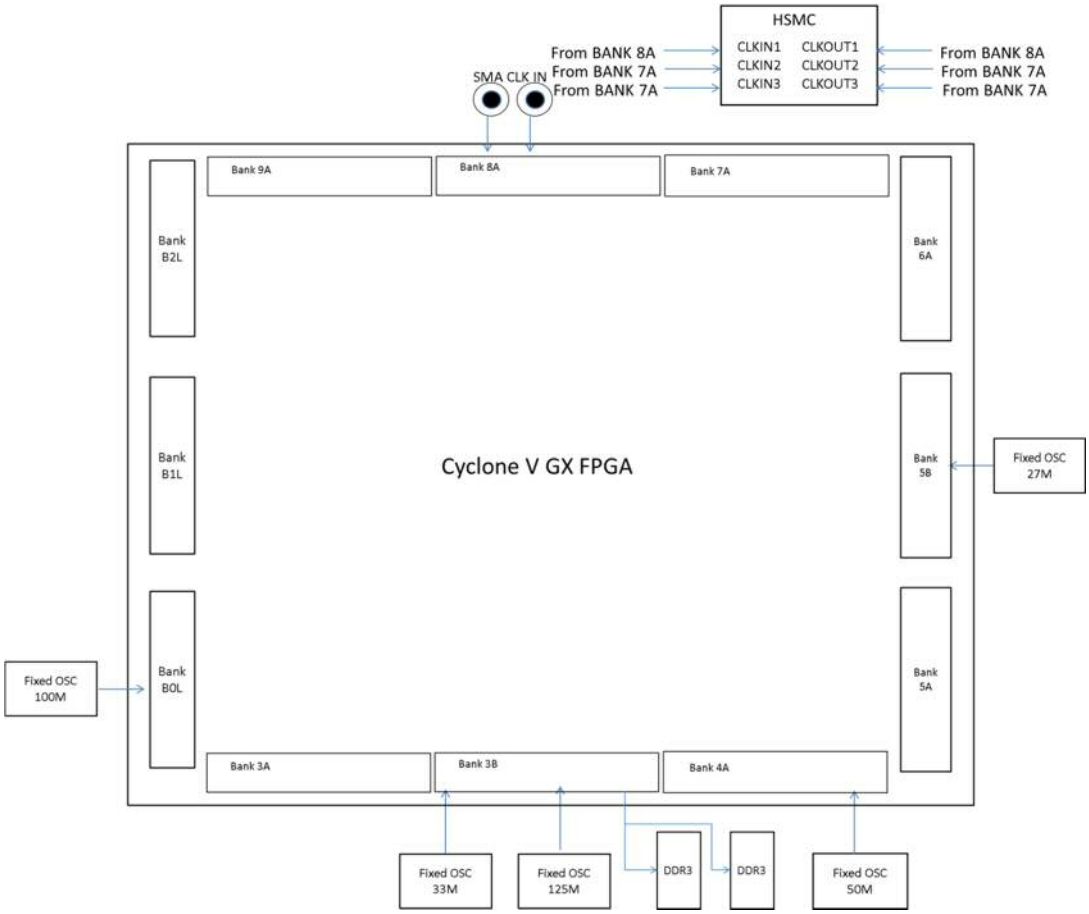


Figure 12. Beryll Board Clocks

Table 12 lists the clock sources, the relevant I/O standard, and voltages required for the Beryll Board.

Table 12. On-board clock sources

Source	Schematic Signal Name	Frequency	I/O Standard	Cyclone V Pin Number	Description
U7	CLK27M	27 MHz	3.3V	T21	User
U8	CLK33M	33 MHz	1.8V	T13	User
U10	CLK50M	50 MHz	1.8	U12	User
U11	CLK125M	125 MHz	1.8V	P11	User
U3	DIFF0_P	100 MHz	LVDS	V6	Transceiver reference
	DIFF0_N	100 MHz	LVDS	W6	Transceiver reference
U18	TSE_MAC_CLK	25 MHz	3.3V	N20	Ethernet PHY
	TSE_RX_CLK	25 MHz	3.3V	R20	Ethernet PHY
U22	EZ_CLK	48 MHz	3.3V	K25	USB2.0 PHY & controller

5.12.2 Off-board Inputs/Outputs

The Beryll Board has input and output clocks which can be driven onto the board. Table 13 lists the clock inputs for the Beryll Board.

Table 13. Off-board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Cyclone V Pin Number	Description
HSMC	HSMC_1_CLKIN	2.5V	L8	Single-ended input from the installed HSMC cable or board.
HSMC	HSMC_2_CLKIN_P	LVDS/ 2.5V	H12	LVDS input from the installed HSMC cable or board. Can also support 2x 2.5V inputs.
	HSMC_2_CLKIN_N	LVDS/ 2.5V	G11	
HSMC	HSMC_3_CLKIN_P	LVDS/ 2.5V	G15	LVDS input from the installed HSMC cable or board. Can also support 2x 2.5V inputs.
	HSMC_3_CLKIN_N	LVDS/ 2.5V	G14	
SMA	SMA_CLKIN	2.5V	N9	User

Table 14 lists the clock outputs for the Beryll Board.

Table 14. Off-board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Cyclone V Pin Number	Description
HSMC	HSMC_1_CLKOUT	2.5V	A7	FPGA 2.5V output(or GPIO)
HSMC	HSMC_2_CLKOUT_P	LVDS/ 2.5V	B15	LVDS output. Can also support 2x 2.5V outputs.
	HSMC_2_CLKOUT_N	LVDS/ 2.5V	C15	
HSMC	HSMC_3_CLKOUT_P	LVDS/ 2.5V	A23	LVDS output. Can also support 2x 2.5V outputs.
	HSMC_3_CLKOUT_N	LVDS/ 2.5V	A22	
SMA	SMA_CLKOUT	2.5V	M9	User

5.13 Power Tree

The Beryll Board uses a power supply device manufactured by Linear Technology.
Figure 12 shows the tree diagram of the power supply for the Beryll Board.

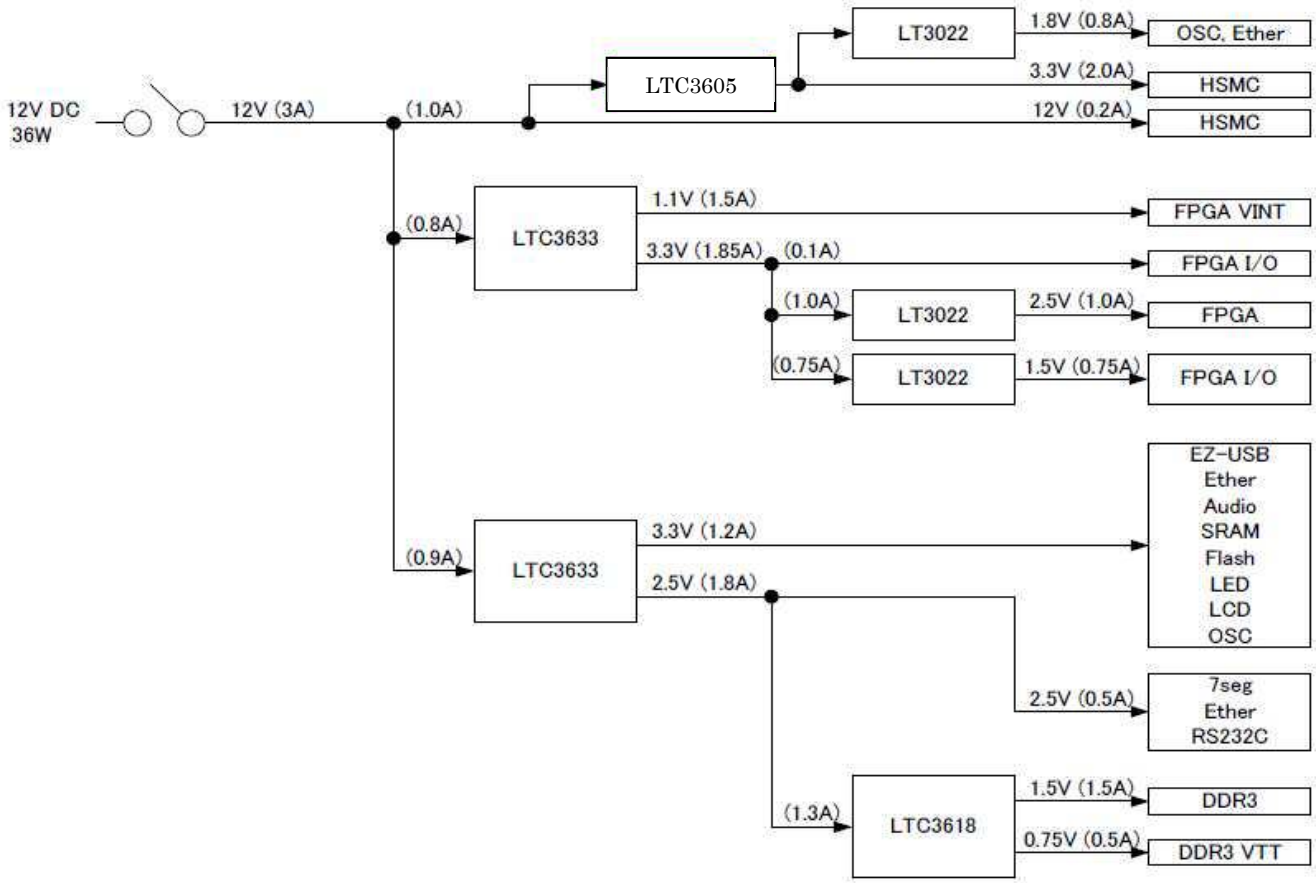


Figure 12. Beryll Power Tree

6. Operating Precautions

6.1 Mode Selection for Unused Pins

This section describes how to handle the pins which are not used on the hardware design (unused pins).
When using the Beryll Board, the unused pins must be set to the tri-stated mode.
Follow the steps below to make the necessary setting for the unused pins in Quartus® II.

1. Select the Assignments menu and then Device.

2. Click the [Device & Pin Options] button.
   The Device & Pin Options window appears.

3. Select the Unused Pins tab.

4. From the Reserve all unused pins item, select As input tri-stated.

5. Click the [OK] button.

6. Click the [OK] button to close the Device & Pin Options window.

7. Document Revision History

Date	Revision	Changes
February, 2014	1	• Document created
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