EE 2310 Experiment #3: Flip-Flop or Latch Circuits

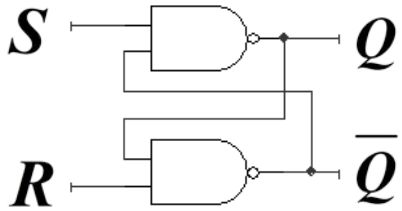
1. **Introduction:** This lab introduces the bistable multivibrator, or flip-flop (FF). Bistable circuits, or FF's, can remember two internal states. More complex circuits made from FF's are called sequential logic. Both simple FF's and more complex FF circuits will be studied, including the storage register, the shift register and the binary counter.

2. **Goal of this exercise:** Observe a simple FF in operation, operate D and J-K flip-flops and registers, a serial-to-parallel shift register and a simple binary counter. Construct simple flip-flops on the prototype board.

3. **Equipment List:** The following are required for this experimental procedure:
   - **IDL-800 Digital Lab and IDL-800 User Manual (as required)**
   - **SN 74LS00 Quad NAND, 74LS04 Hex Inverter, SN 74LS74 Dual D FF, SN 74LS107 Dual J-K FF, SN 74LS163 binary counter, 74LS195 serial-to-parallel shift register (all in digital logic kit)**
   - **Breadboard wire connection kit**

4. **Pre-Work:** Study class notes on bistable circuits, especially the R-S, clocked R-S, and D FF's, in Tokheim. Also study the class notes on sequential logic.
5. **Experimental Procedure:**

   - **Building an R-S FF:**
     - **Plug an 74LS00 NAND chip into the prototype board and connect power. There are 4 equal NAND circuits on the chip; any two may be used to make the circuit below:**

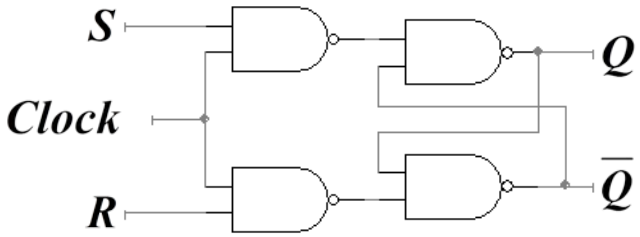


     - **Connect the two NAND gates as shown (refer to the 74LS00 pin-outs on the data sheet).**
     - **Connect the two pulse switches to the open NAND gate inputs (those that are not connected to the opposite outputs). Make sure both inputs (switch positions) are 1, since the R-S FF is activated by negative logic (S and R go "low" to set and reset). Connect the NAND gate outputs to LED inputs. Note that either output may be initially designated as Q.**
     - **Turn on the power. The FF may be activated in an arbitrary state, so that either one of the LEDs may be illuminated. Activate the S and R inputs and watch the FF set and reset..**
     - **Turn both pulse switches to 0 and the LEDs should both go on. This is the "forbidden (unstable) state" for the R-S FF. Note that when you release the switches, the resulting state of the FF is not predictable. Try this several times. Disconnect the circuit.**
   - **D Flip-Flop:**
     - **Plug in the 74LS74 D-type flip-flop and connect power. As this is a two-circuit package, referring to the 74LS74 diagram, choose one of the two D FFs and connect input switches to the D and Preset inputs. Since the preset is negative-true logic input, make sure the switch is set to 1. Connect the pulse switches (the negative-true outputs) to Clock and Clear, and the Q and Q-NOT outputs to LED's.**
     - **Turn on power. The D FF may power up in either state, so toggle Clear to initialize the circuit. After you do so, the Q LED should be off, and the Q-NOT LED on. Toggle the Preset**

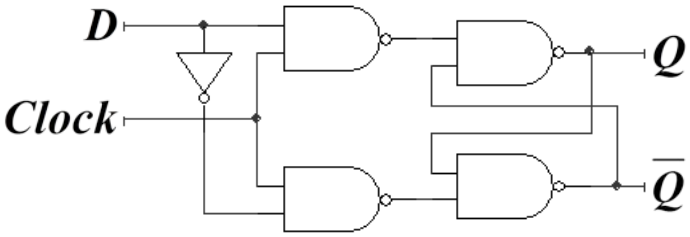
switch (low and back) and notice that the FF "sets" (Q →1) and its LED lights. The Preset switch allows an initial "on" state if necessary. Toggle Clear to reset the FF.

- **Toggle Clock with the D input switch set at 0. Notice that the FF does not change state. Now set D input to 1, and re-toggle Clock. Note that the D FF "sets."**
- **Now reset the D FF, setting D = 0 and re-pulsing Clock. Try these various inputs (Clock with D, Preset, Clear) and observe the circuit operation several times. Note that simultaneous switching of Clear and Preset results in Q and Q-NOT going to 1 (both LEDs will light). This is again the "forbidden state." Turn off the power and disconnect the circuit.**

- **J-K FF:**
  - **Plug in the 74LS107 J-K-type flip-flop and connect power. Since this is a two-circuit chip, refer to the 74LS107 pin-out diagram and select one J-K FF. Connect switch inputs to the J and K input, and pulse switches (negative-true outputs) to Clock and Clear. Q and Q-NOT should be connected to LED's.**
  - **Turn on the power. The FF will power up in an arbitrary state, so toggle the Clear to initialize the circuit. After you do so, the Q should be off, and the Q-NOT should be on.**
  - **Alternately set J and K to 0-0, 0-1, 1-1, and 1-0. Notice from the LED's how the JK FF changes state according to the truth table for that of a J-K FF.**
  - **Experiment with the J-K FF and note how it prevents a forbidden state.**
  - **Turn off power and disconnect the circuit.**
- **Construction of Clocked R-S and D FF's:**
  - **A simple clocked R-S FF (see below) may be made from a NAND gate.**



  - **Plug in the 74LS00 NAND chip and 74LS04 inverter chip (used later) and connect power. Connect the four NAND gates as shown (choice of gate is arbitrary). Connect slide switches to the S and R inputs as shown. Connect the normally-low output of a pulse switch to the "Clock" input. Connect the output of the two downstream NANDs to two LEDs.**
  - **Turn on power. The FF can come up in an arbitrary state. If it is set, with the R switch in the high (1) position, toggle clock. The FF should reset (Q=0, Q-NOT=1. Switch the S input to 1 and R to 0, and toggle clock. The FF should set (Q LED on, Q-NOT LED off).**
  - **Exercise the R-S FF and get used to its operation. Note that R=S=1 causes an arbitrary condition to the RS FF when clock is pulsed.**
  - **Turn off power, disconnect the R input and connect it to the output of a 74LS04 Inverter. Connect the input of the inverter to the S input (Which now becomes the "D" input of a D FF—see below).**

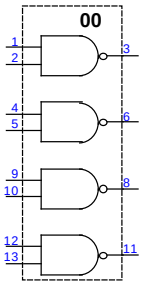


  - **Set the D input first to 1, then to 0, and continue to alternate the input, pulsing Clock after each change. Note that when the clock is pulsed, Q tracks D. Note that there is no forbidden input.**
  - **When you have become familiar with circuit operation, dismantle it and continue.**

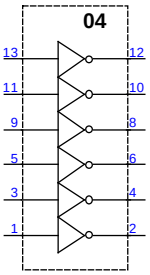
- **4-Bit Serial-to-Parallel Shift Register:**
  - **Plug the 74LS195 serial-to-parallel shift register into the prototype board and connect power. Note: for all the following instructions on connections of circuits in parts 1)-4), please refer to the appropriate chip diagram on the last page of these instructions. Connect parallel output pins Q_A-Q_D to LED indicators. Connect the serial-in input pins J and K (pins 2 & 3) to data switches, making sure that they are set to 0, and the clock input to the clock generator output. Connect the clear input to one of the negative-true pulse-switch outputs.**
  - **Turn on power. Press clear and make sure that all 4 LED's are dark. Set the clock frequency to 1 Hz and the clock amplitude to about ½ max. (indicator on the clock level knob pointing about straight up). The shift register should be operational at this point, but since the data switch is set to 0, all LED's will remain dark. Set the switch to 1. You should immediately see serial bits passing from the lowest stage (A) to the highest (D) each time the clock pulses. After four clock cycles the output data bits should all be 1. Return the data switch to 0 and the shift register will be filled serially with 0's again. A little rapid switching of the data switch at this point can alternate 1 and 0 bits being shifted into the register. You can also attach the data input to a pulse switch and control alternate 1's and 0's more easily.**
  - **When you are familiar with shift register operation, turn off the power and disconnect.**
- **Binary Counter:**
  - **Plug in the 74LS163 binary counter and connect power. Connect clock input to the clock pulse output (still set to 1 Hz), and the clear input to the true-negative pulse switch output. As we inputting data in series, do not connect the A-B-C-D data inputs. Connect LED's to Q_A-Q_D outputs (Q_A is least significant bit or LSB). Turn on power and again set the clock amplitude to about ½ max. Clear the counter and watch the LED outputs. Verify that the counter counts the clock pulses sequentially, from 1 to 15, and then reset to 0 automatically on the 16^{th} pulse. Note that clearing the clock during the middle of a cycle merely starts the counter at 0 again and counting resumes.**
  - **Experiment until familiar with counter operation, then turn off power and disconnect.**

6. **Equipment Disassembly:** The experimental procedure is complete. Please replace wires and parts in their containers and return to the parts cabinet. Make sure that your work area is clean, and have your TA check the area and sign your data sheet.
7. **Laboratory Report:** Follow the laboratory report standard form. In your write-up, discuss the operation of the circuits, and include the following items:
   - **Discuss your experience in the laboratory and any problems with the procedure.**
   - **Show the circuit hook-up for the three FF circuits that you made out of NAND gates. Include these in your report. Make sure to include the pin numbers of each gate used. You do NOT have to show the package outline, just the pin numbers of the gates.**
   - **Consider a 4-bit parallel-in, serial-out shift register. Using D FF's, design the register and show a timing diagram of the loading and shifting out of data. Assume the FF's are master-slave, in order to assure separation of stages, and also that each D FF has a separate "Preset" input, so that a bit may be initially set in parallel, before the serial shifting is begun.**

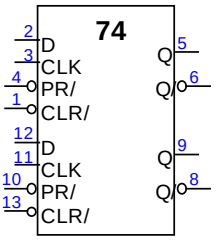
Digital Logic Chip Pin-Out Diagrams



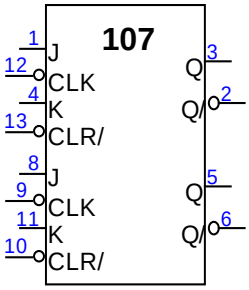
SN 74LS00
Quad 2-input
NAND gate



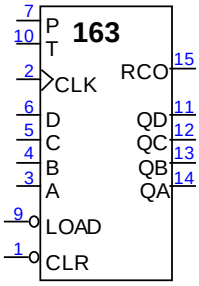
SN 74LS04
Hex Inverter



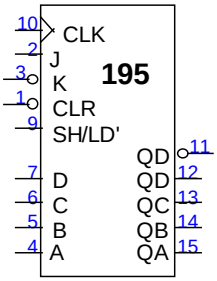
SN 74LS74
Dual D FF



SN 74LS107
Dual JK FF

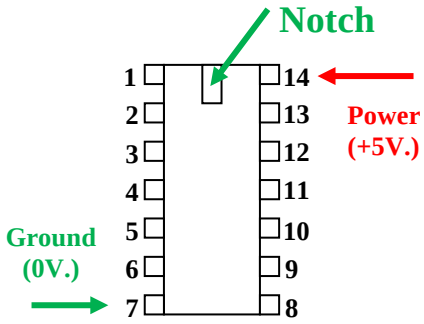


SN 74LS163
Counter



SN 74LS195
Quad Latch

Power Pin-Outs



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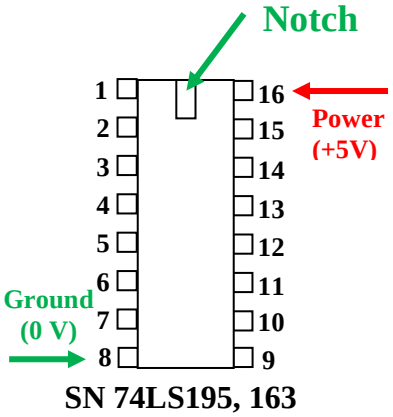

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